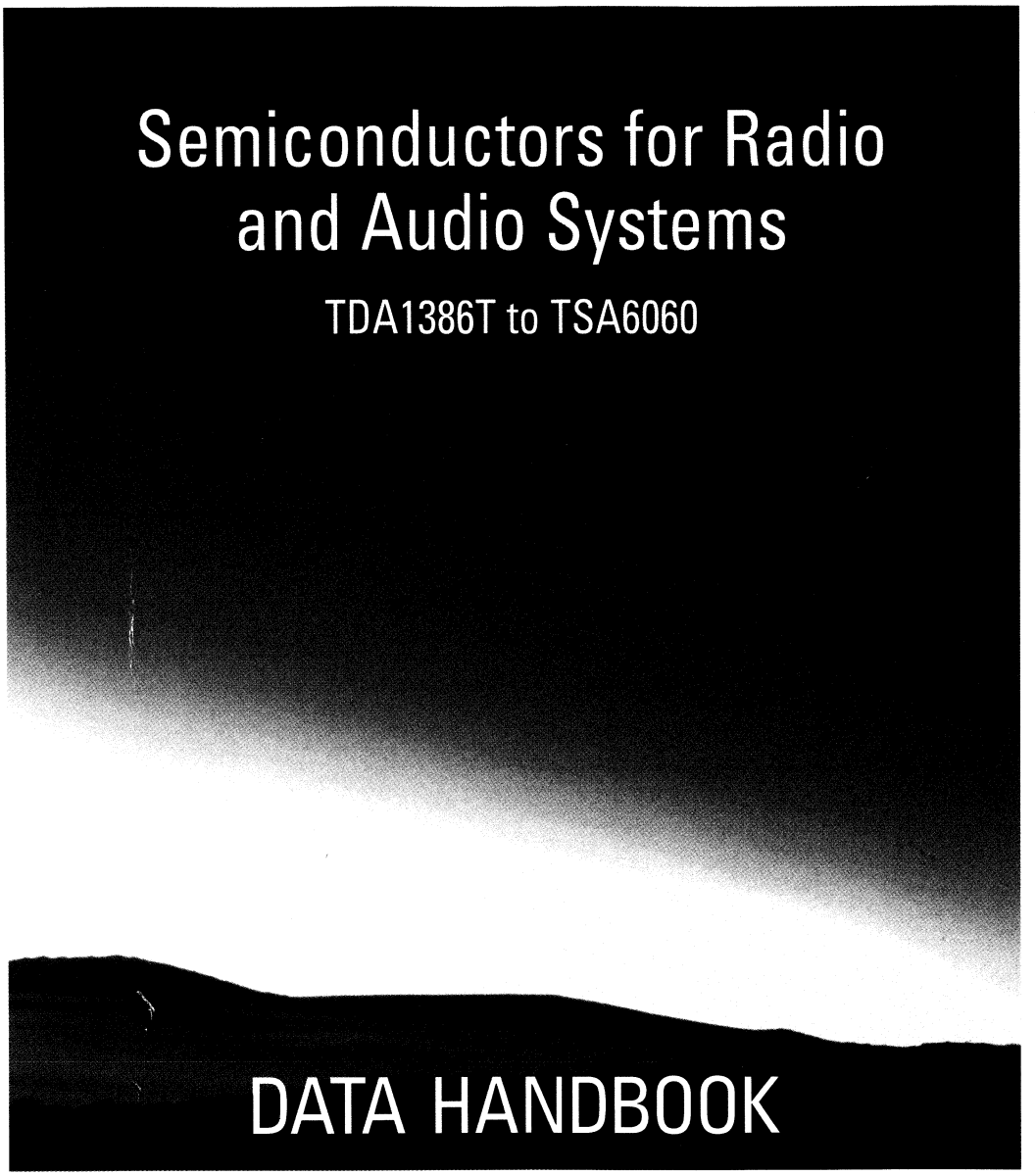
Semiconductors for Radio and Audio Systems

TDA1386T to TSA6060



DATA HANDBOOK

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Our quality system focuses on the continuing high quality of our components and the best possible service for our customers. We have a three-sided quality strategy: we apply a system of total quality control and assurance; we operate customer-oriented dynamic improvement programmes; and we promote a partnering relationship with our customers and suppliers.

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Semiconductors for Radio and Audio Systems

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DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

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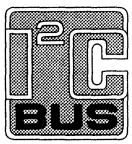
PURCHASE OF PHILIPS I²C COMPONENTS



Purchase of Philips I²C components conveys a license under the Philips' I²C patent to use the components in the I²C system provided the system conforms to the I²C specification defined by Philips. This specification can be ordered using the code 9398 393 40011.

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Semiconductors for Radio and Audio Systems

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Combination AM/FM, IF, PLL, MPX and NC circuits

SEMICONDUCTORS

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MOSFETs for AM/FM tuning

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DEVICE DATA

Noise shaping filter DAC TDA1386T

FEATURES

General

- Double-speed mode
- Digital volume control
- Soft mute function
- 12 dB attenuation
- Low power dissipation
- Digital de-emphasis.

Easy application

- Voltage output
- Only 1st-order analog post-filtering required
- Operational amplifiers and digital filter integrated
- $256f_s$ system clock (f_{sys})
- I^2S-bus or 16, 18 or 20 bits LSB fixed serial input format
- Single rail supply.

High performance

- Superior signal-to-noise ratio
- Wide dynamic range
- No zero crossing distortion
- Inherently monotonic
- Continuous calibration digital-to-analog conversion combined with noise shaping technique.

GENERAL DESCRIPTION

The TDA1386T is a dual CMOS digital-to-analog converter with up-sampling filter and noise shaper. The combination of oversampling up to $4f_s$, noise shaping and continuous calibration conversion ensures that only simple 1st order analog post filtering is required.

The TDA1386T supports the I^2S-bus data input mode with word lengths of up to 20 bits and the LSB fixed serial data input format with word lengths of 16, 18 or 20 bits. Two cascaded IIR filters increase the sampling rate 4 times.

The DACs are of the continuous calibration type and incorporate a special data coding. This ensures a high signal-to-noise ratio, wide dynamic range and immunity to process variation and component ageing.

Two on-board operational amplifiers convert the digital-to-analog current to an output voltage.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA1386T	SO24	plastic small outline package; 24 leads; body width 7.5 mm.	SOT137-1

QUICK REFERENCE DATA

All power supply pins V_{DD} and GND must be connected to the same external supply unit.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX	UNIT
Supply						
V_{DDD}	digital supply voltage		4.5	5.0	5.5	V
V_{DDA}	analog supply voltage		4.5	5.0	5.5	V
V_{DDO}	operational amplifier supply voltage		4.5	5.0	5.5	V
I_{DDD}	digital supply current	V_{DDD} = 5 V; at code 00000H	–	5	8	mA
I_{DDA}	analog supply current	V_{DDA} = 5 V; at code 00000H	–	3	5	mA
I_{DDO}	operational amplifier supply current	V_{DDO} = 5 V; at code 00000H	–	2	4	mA
Analog signals						
$V_{FS(rms)}$	full-scale output voltage (RMS value)	$V_{DDD} = V_{DDA} = V_{DDO}$ = 5 V; R_{OL} > 5 kΩ	0.935	1.1	1.265	V
R_L	output load resistance		5	–	–	kΩ
DAC performance						
(THD + N)/S	total harmonic distortion plus noise-to-signal ratio	at 0 dB signal level; f_i = 1 kHz	–	–70	–	dB
			–	0.032	–	%
		at –60 dB signal level; f_i = 1 kHz	–	–42	–32	dB
			–	0.8	2.5	%
S/N_{ds}	signal-to-noise ratio at digital silence	no signal; A-weighted	–	–108	–96	dB
BR	input bit rate at data input	f_s = 44.1 kHz; normal speed	–	–	2.822	bits
		f_s = 44.1 kHz; double speed	–	–	5.645	bits
f_{sys}	clock frequency		6.4	–	18.432	MHz
T_{amb}	operating ambient temperature		–40	–	+85	°C

BLOCK DIAGRAM

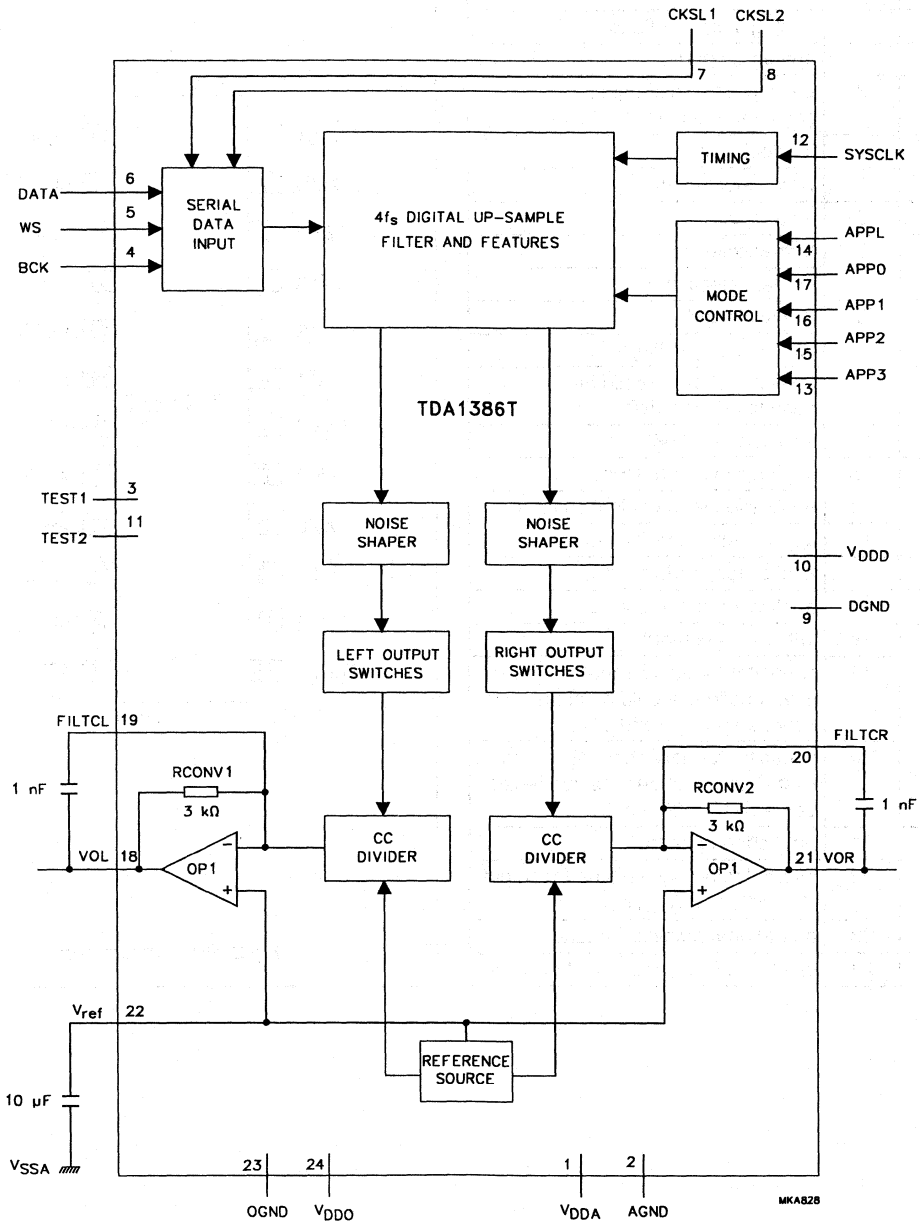


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
V_{DDA}	1	analog supply voltage
AGND	2	analog ground
TEST1	3	test input 1; pin should be connected to DGND
BCK	4	bit clock input
WS	5	word select input
DATA	6	data input
CKSL1	7	format selection 1
CKSL2	8	format selection 2
DGND	9	digital ground
V_{DDD}	10	digital supply voltage
TEST2	11	test input 2; pin should be connected to DGND
SYSCLK	12	system clock $256f_s$
APP3	13	application mode 3 input
APPL	14	application mode selection input
APP2	15	application mode 2 input
APP1	16	application mode 1 input
APP0	17	application mode 0 input
VOL	18	left channel output
FILTCL	19	capacitor for left channel 1st-order filter function, should be connected between pins 19 and 18
FILTCR	20	capacitor for right channel 1st-order filter function, should be connected between pins 20 and 21
VOR	21	right channel output
V_{ref}	22	internal reference voltage for output channels ($0.5V_{DDO}$ typ.)
OGND	23	operational amplifier ground
V_{DDO}	24	operational amplifier supply voltage

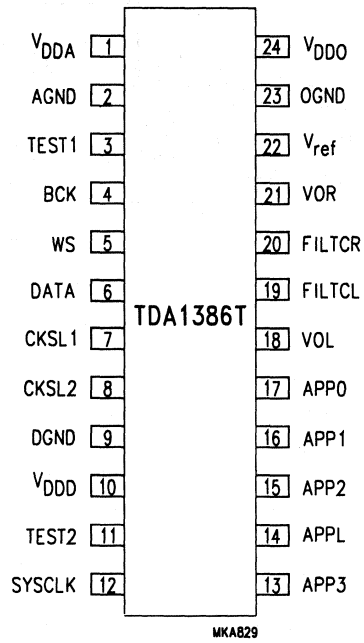


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The TDA1386T CMOS DAC incorporates an up-sampling filter, a noise shaper, continuous calibrated current sources and operational amplifiers.

System clock and data input format

The TDA1386T accommodates slave mode only consequently, in all applications, the system devices must provide the $256f_s$ system clock.

The TDA1386T supports the following data input modes:

- I^2S-bus with data word length of up to 20 bits.
- LSB fixed serial format with data word length of 16, 18 or 20 bits. As this format idles on the MSB it is necessary to know how many bits are being transmitted.

The data input formats are illustrated in Fig.7. Left and right data-channel words are time multiplexed.

Table 1 Data input format and system clock.

CKSL1	CKSL2	DATA INPUT FORMAT	SYSTEM CLOCK	
			NORMAL SPEED	DOUBLE SPEED
0	0	I^2S-bus	$256f_s$	$128f_s$
0	1	LSB fixed 16 bits	$256f_s$	$128f_s$
1	0	LSB fixed 18 bits	$256f_s$	$128f_s$
1	1	LSB fixed 20 bits	$256f_s$	$128f_s$

Device operation

When the APPL pin is held HIGH and APP3 is held LOW, pins APP0, APP1 and APP2 form a microcontroller interface. When the APPL pin is held LOW, pins APP0, APP1, APP2 and APP3 form pseudo-static application pins (TDA1305T pin compatible).

PSEUDO-STATIC APPLICATION MODE (APPL = LOGIC 0)

In this mode, the device operation is controlled by pseudo-static application pins (APP0: attenuation mode control; APP1: double-speed mode control; APP2: mute mode control and APP3: de-emphasis mode control).

In the pseudo-static application mode the TDA1386T is pin compatible with the TDA1305T slave mode. The correspondence between TDA1386T pin number, TDA1386T pin name, TDA1305T pin name and a description of the effects is given in Table 2.

Table 2 Pseudo-static application mode.

PIN NAME	PIN NUMBER	TDA1305T FUNCTION	LOGIC VALUE	DESCRIPTION
APP0	17	ATSB	0	12 dB attenuation (from full scale) activated (only if MUSB = 1)
			1	full scale (only if MUSB = 1)
APP1	16	DSMB	0	double-speed mode
			1	normal-speed mode
APP2	15	MUSB	0	samples decrease to mute level
			1	level in accordance with ATSB
APP3	13	DEEM1	0	de-emphasis OFF (44.1 kHz)
			1	de-emphasis ON (44.1 kHz)

MICROCONTROLLER APPLICATION MODE (APPL = LOGIC 1, APP3 = LOGIC 0)

In this mode, the device operation is controlled by a set of flags in an 8-bit mode control register. The 8-bit mode control register is written by a microprocessor interface (pin APPL = 1, APP0 = Data, APP1 = Clock, APP2 = RAB and APP3 = 0).

The correspondence between serial to parallel conversion, mode control flags and a summary of the effect of the control flags is given in Table 3. Figures 3 and 4 illustrate the mode set timing.

MICROCONTROLLER WRITE OPERATION SEQUENCE

- APP2 is held LOW by the microcontroller.
- Microprocessor data is clocked into the internal shift register on the LOW-to-HIGH transition at pin APP1.
- Data D(7 to 0) is latched into the appropriate control register on the LOW-to-HIGH transition of pin APP2 (with APP1 HIGH).
- If more data is clocked into the TDA1386T before the LOW-to-HIGH transition on pin APP2 then only the last 8 bits are used.
- If less data is clocked into the TDA1386T unpredictable operation will result.
- If the LOW-to-HIGH transition of pin APP2 occurs with APP1 LOW, the command will be disregarded.

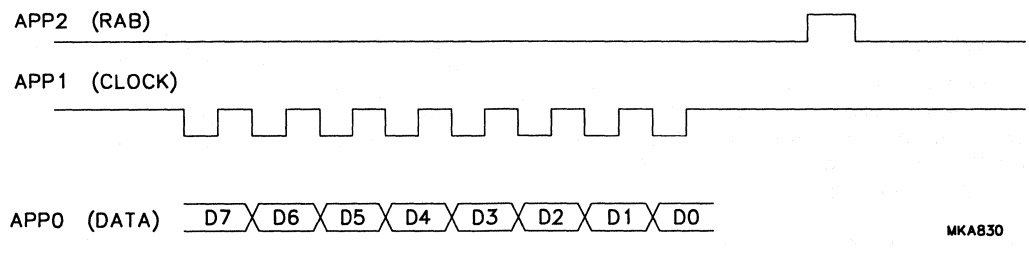


Fig.3 Microcontroller timing.

MICROCONTROLLER WRITE OPERATION SEQUENCE; REPEAT MODE

The same command can be repeated several times (e.g. for fade function) by applying APP2 pulses as shown in Fig.4. It should be noted that APP1 must stay HIGH between APP2 pulses. A minimum pause of 22 ms is necessary between any two step-up or step-down commands.

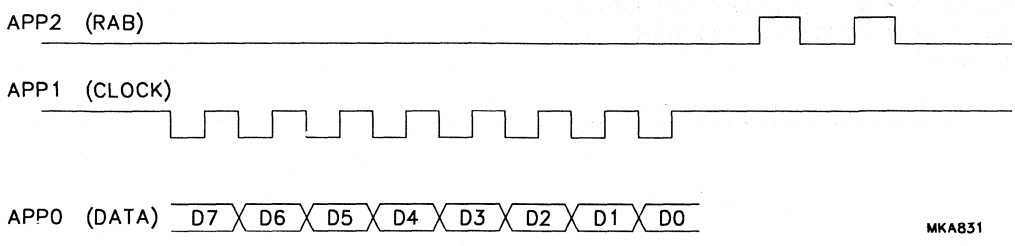


Fig.4 Microcontroller timing; repeat mode.

Table 3 Microcontroller mode control register.

BIT POSITION	FUNCTION	DESCRIPTION	ACTIVE LEVEL
D7	ATSB	12 dB attenuation (from full scale)	LOW
D6	DSMB	double speed	LOW
D5	MUSB	mute	LOW
D4	DEEM	de-emphasis	HIGH
D3	FS	full scale	HIGH
D2	INCR	increment	HIGH
D1	DECR	decrement	HIGH
D0	–	reserved	–

Volume control

A digital level control is incorporated on the TDA1386T which performs the function of soft mute and attenuation (pseudo-static application mode) or soft mute, attenuation, fade, increment and decrement (microcontroller application mode). The volume control of both channels can be varied in small step changes, determined by the value of the internal fade counter according to:

Audio level = counter × maximum level/120.

Where the counter is a 7-bit binary number between 0 and 120. The time taken for mute to vary from 120 to 0 is $120/f_s$. For example, when f_s = 44.1 kHz, the time taken is approximately 3 ms.

VOLUME CONTROL IN PSEUDO-STATIC APPLICATION MODE

In the pseudo-static application mode (APPL = logic 0) the digital audio output level is controlled by APP0 (attenuation) and APP2 (mute) so only the final volume levels full scale, 12 dB (attenuate) and mute (–infin dB) can be selected. The mute function has priority over the attenuation function. Accordingly, if MUSB is LOW, the state of ATSB has no effect. An example of volume control in this application mode is illustrated in Fig.5.

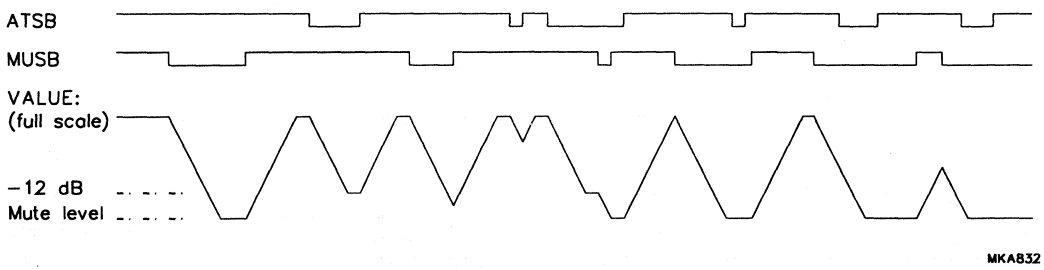


Fig.5 Volume control; pseudo-static application mode.

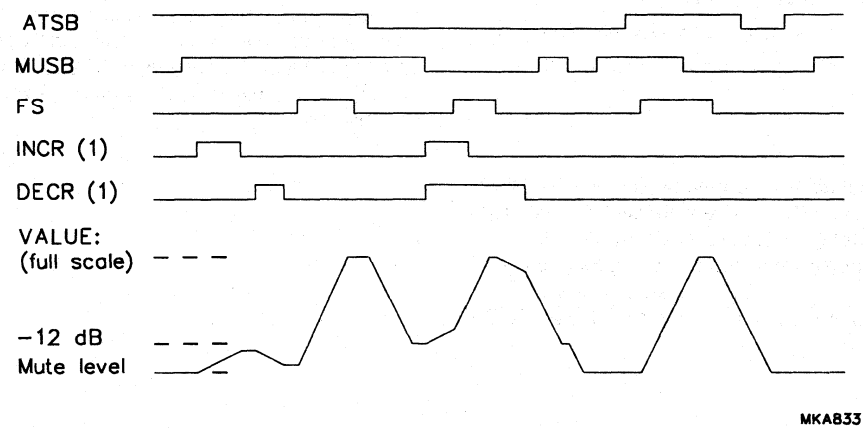
VOLUME CONTROL IN MICROCONTROLLER APPLICATION MODE

In the microcontroller application mode (APPL = logic 1, APP3 = logic 0) the audio output level is controlled by volume control bits ATSB, MUSB, FS, INCR and DECR.

Mute is activated by sending the MUSB command to the mode control register via the microcontroller interface. The audio output level will be reduced to zero in a maximum 120 steps (depending on the current position of the fade counter) and taking a maximum of 3 ms. Mute, attenuation and full scale are synchronized to prevent operation in the middle of a word.

- The counter is preset to 120 by the full scale command.
- The counter is preset to 30 by the attenuate command when its value is more then 30. If the value of the counter is less than 30 dB the ATSB command has no effect.
- The counter is preset to 0 by the mute command MUSB.
- Attenuation (−12 dB) is activated by sending the ATSB command to the fade control register (D7).
- Attenuation and mute are cancelled by sending the full scale command to the fade control register (D3).

To control the fade counter in a continuous way, the INCREMENT and DECREMENT commands are available (fade control registers D1 and D2). They will increment and decrement the counter by 1 for each register write operation. When issuing more than 1 step-up or step-down command in sequence, the write repeat mode may be used (see microprocessor application mode). An example of volume control in this application mode is illustrated in Fig.6.



(1) INCR and DECR in repeat mode.

Fig.6 Volume control; microcontroller application mode.

There are two recommended application situations within the microcontroller mode:

- The customer wants to use the microcontroller interface without the volume setting facility. In this event the operation is as follows:
  - Mute ON; by sending the MUSB command
  - Mute OFF; by sending the FS command
  - Attenuation ON; by sending the ATSB command
  - Attenuation OFF; by sending the FS command.

  It is possible to switch from 'Attenuation ON' to 'Mute ON' but not vice-versa.
- Incorporating the volume control feature operates as follows:
  - Mute ON; by sending the MUSB command the microcontroller has to store the previous volume setting
  - Mute OFF; by sending succeeding INCR commands until the previous volume is reached
  - Attenuation ON; by sending succeeding DECR commands until a relative downstep of −12 dB is reached. The microcontroller has to store the previous volume
  - Attenuation OFF; by sending the succeeding INCR commands until the previous volume is reached
  - Volume UP; by sending successive INCR commands
  - Volume DOWN; by sending successive DECR commands.

De-emphasis

A digital de-emphasis is implemented in the TDA1386T. By selecting the DEEM bit at register D4 (microcontroller application mode) or activating the APP0 pin (pseudo-static application mode), de-emphasis can be applied by means of an IIR filter. De-emphasis is synchronized to prevent operation in the middle of a word.

Double-speed mode

The double-speed mode is controlled by the DSMB bit at register D6 (microcontroller application mode) or by activating the APP1 pin (pseudo static application mode). When the control bit is active LOW the device operates in the double-speed mode.

Oversampling filter and noise shaper

The digital filter is a four times oversampling filter. It consists of two sections which each increase the sample rate by 2. The noise-shaper operates on $4f_s$ and reduces the in-band noise density.

DAC and operational amplifiers

In this noise shaping DAC a special data code and bidirectional current sources are used in order to achieve true low-noise performance. The special data code guarantees that only small values of current flow to the output during small signal passages while larger positive or negative values are generated using the bidirectional current sources. The noise shaping DAC uses the continuous calibration conversion technique. The DAC currents are repeatedly generated from one single reference current.

The operational amplifiers and the internal conversion resistors R_{CONV1} and R_{CONV2} convert the DAC current to an output voltage available at VOL and VOR. Connecting an external capacitor between FILTCL and VOL, FILTCR and VOR respectively provides the required first-order post filtering.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX	UNIT
V_{DDD}	digital supply voltage	note 1	–	7.0	V
V_{DDA}	analog supply voltage	note 1	–	7.0	V
V_{DDO}	operational amplifiers supply voltage	note 1	–	7.0	V
T_{xtal}	maximum crystal temperature		–	+150	°C
T_{stg}	storage temperature		–65	+125	°C
T_{amb}	operating ambient temperature		–40	+85	°C
V_{es}	electrostatic handling	note 2	–2000	+2000	V
		note 3	–200	+200	V

Notes

1. All V_{DD} and GND connections must be made to the same power supply.
2. Equivalent to discharging a 100 pF capacitor via a 1.5 kΩ series resistor.
3. Equivalent to discharging a 200 pF capacitor via a 2.5 µH series inductor.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air	69	K/W

QUALITY SPECIFICATION

In accordance with *"UZW-BO/FQ-0601"*. The numbers of the quality specification can be found in the *"Quality Reference Handbook"*. The handbook can be ordered using the code 9398 510 34011.

DC CHARACTERISTICS

$V_{DDD} = V_{DDA} = V_{DDO} = 5$ V; $T_{amb} = 5$ °C; all voltages referenced to ground (pins 2, 9 and 23); unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX	UNIT
V_{DDD}	digital supply voltage (pin 10)	note 1	4.5	5.0	5.5	V
V_{DDA}	analog supply voltage (pin 1)	note 1	4.5	5.0	5.5	V
V_{DDO}	operational amplifier supply voltage (pin 24)	note 1	4.5	5.0	5.5	V
I_{DDD}	digital supply current	f_{sys} = 11.28 MHz	–	5	8	mA
I_{DDA}	analog supply current	at digital silence	–	3	6	mA
I_{DDO}	operational amplifier supply current	no operational amplifier load resistor	–	2	4	mA
P_{tot}	total power dissipation	f_{sys} = 11.28 MHz; digital silence; no operational amplifier load resistor	–	50	90	mW
V_{IH}	HIGH level digital input voltage (pins 3 to 8 and 11 to 17)		$0.7V_{DDD}$	–	V_{DDD} + 0.5	V
V_{IL}	LOW level digital input voltage (pins 3 to 8 and 11 to 17)		–0.5	–	$0.3V_{DDD}$	V
R_{pd}	internal pull-down resistor to V_{SSD} (pins 3 and 11)		17	–	134	kΩ
$\|I_{LI}\|$	input leakage current		–	–	10	μA
C_I	input capacitance		–	–	10	pF
V_{ref}	reference voltage (pin 22)	with respect to OGND	$0.45V_{DDO}$	$0.5V_{DDO}$	$0.55V_{DDO}$	V
R_{CONV}	current-to-voltage conversion resistor		2.4	3.0	3.6	kΩ
$V_{FS(rms)}$	full scale output voltage (RMS value)	R_L > 5 kΩ; note 2	0.935	1.1	1.265	V
R_L	output load resistance		5	–	–	kΩ

Notes

1. All power supply pins (V_{DD} and GND) must be connected to the same external power supply unit.
2. R_L is the AC impedance of the external circuitry connected to the audio outputs of the application circuit.

AC CHARACTERISTICS (ANALOG)

$V_{DDD} = V_{DDA} = V_{DDO} = 5$ V; $T_{amb} = 25$ °C; all voltages referenced to ground (pins 2, 9 and 23); unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX	UNIT
DACs						
SVRR	supply voltage ripple rejection pins 9 and 16	f_{ripple} = 1 kHz; $V_{ripple(p-p)}$ = 100 mV; C22 = 10 µF	–	40	–	dB
$\Delta V_{o(DAC)}$	unbalance between the 2 DAC voltage outputs (pins 18 and 21)	maximum volume	–	–	0.5	dB
α_{DAC}	crosstalk between the 2 DAC voltage outputs (pins 18 and 21)	one output digital silence the other maximum volume	–	–110	–85	dB
(THD + N)/S	total harmonic distortion plus noise as a function of signal	at 0 dB signal; f_i = 1 kHz	–	–70	–	dB
			–	0.032	–	%
		at –60 dB signal; f_i = 1 kHz	–	–42	–32	dB
			–	0.8	2.5	%
S/N_{ds}	signal-to-noise ratio at digital silence,	f_i = 20 Hz to 17 kHz; A-weighted; no signal	–	–108	–96	dB
Operational amplifiers						
G_v	open-loop voltage gain		–	85	–	dB
PSRR	power supply rejection ratio	f_{ripple} = 3 kHz; $V_{ripple(p-p)}$ = 100 mV; A-weighted	–	90	–	dB
(THD + N)/S	total harmonic distortion plus noise as a function of signal	$R_L > 5$ kΩ; V_o = 2.8 V (p-p); f_i = 1 kHz	–	–100	–	dB
f_{ug}	unity gain frequency	open loop	–	4.5	–	MHz
Z_o	AC output impedance	$R_L > 5$ kΩ	–	1.5	150	Ω

AC CHARACTERISTICS (DIGITAL)

$V_{DDD} = V_{DDA} = V_{DDO} = 4.5$ to 5.5 V; $T_{amb} = -40$ to +85 °C; all voltages referenced to ground (pins 2, 9 and 23); unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX	UNIT
t_W	clock cycle	$f_{sys} = 256f_s$; normal speed	81.3	88.6	156	ns
		$f_{sys} = 128f_s$; double speed	81.3	88.6	156	ns
t_{CWL}	f_{sys} LOW-level pulse width		22	–	–	ns
t_{CWH}	f_{sys} HIGH-level pulse width		22	–	–	ns
Serial input data timing (see Fig.8)						
f_s	word selection input audio sample frequency	normal speed	25	44.1	48	kHz
		double speed	50	88.2	96	kHz
f_{BCK}	clock input frequency (data input rate)	$f_{sys} = 256f_s$; normal speed	–	–	$64f_s$	kHz
		$f_{sys} = 128f_s$; double speed; note 1	–	–	$48f_s$	kHz
t_r	rise time		–	–	20	ns
t_f	fall time		–	–	20	ns
t_{HB}	bit clock HIGH time		55	–	–	ns
t_{LB}	bit clock LOW time		55	–	–	ns
$t_{SU;DAT}$	data set-up time		20	–	–	ns
$t_{HD;DAT}$	data hold time		10	–	–	ns
$t_{SU;WS}$	word select set-up time		20	–	–	ns
$t_{HD;WS}$	word select hold time		10	–	–	ns
Microcontroller interface timing (see Fig.9)						
t_L	input LOW time		2	–	–	µs
t_H	Input HIGH time		2	–	–	µs
$t_{SU;DC}$	set-up time DATA to CLOCK		1	–	–	µs
$t_{HD;CD}$	hold time CLOCK to DATA		1	–	–	µs
$t_{SU;CR}$	set-up time CLOCK to RAB		1	–	–	µs

Note

1. A clock frequency of up to $96f_s$ is possible in the event that a rising edge of BCK occurs while SYSCLK is LOW.

TEST AND APPLICATION INFORMATION

Filter characteristics

Table 4 Digital filter specification, f_s = 44.1 kHz.

BAND	ATTENUATION
0 to 19 kHz	< 0.001 dB
19 to 20 kHz	< 0.03 dB
24 kHz	> 25 dB
25 to 35 kHz	> 40 dB
35 to 64 kHz	> 50 B
64 to 68 kHz	> 31 dB
68 kHz	> 35 dB
69 to 88 kHz	> 40 dB

Table 5 Digital filter phase distortion, f_s = 44.1 kHz.

BAND	PHASE DISTORTION
0 to 16 kHz	<±1 deg

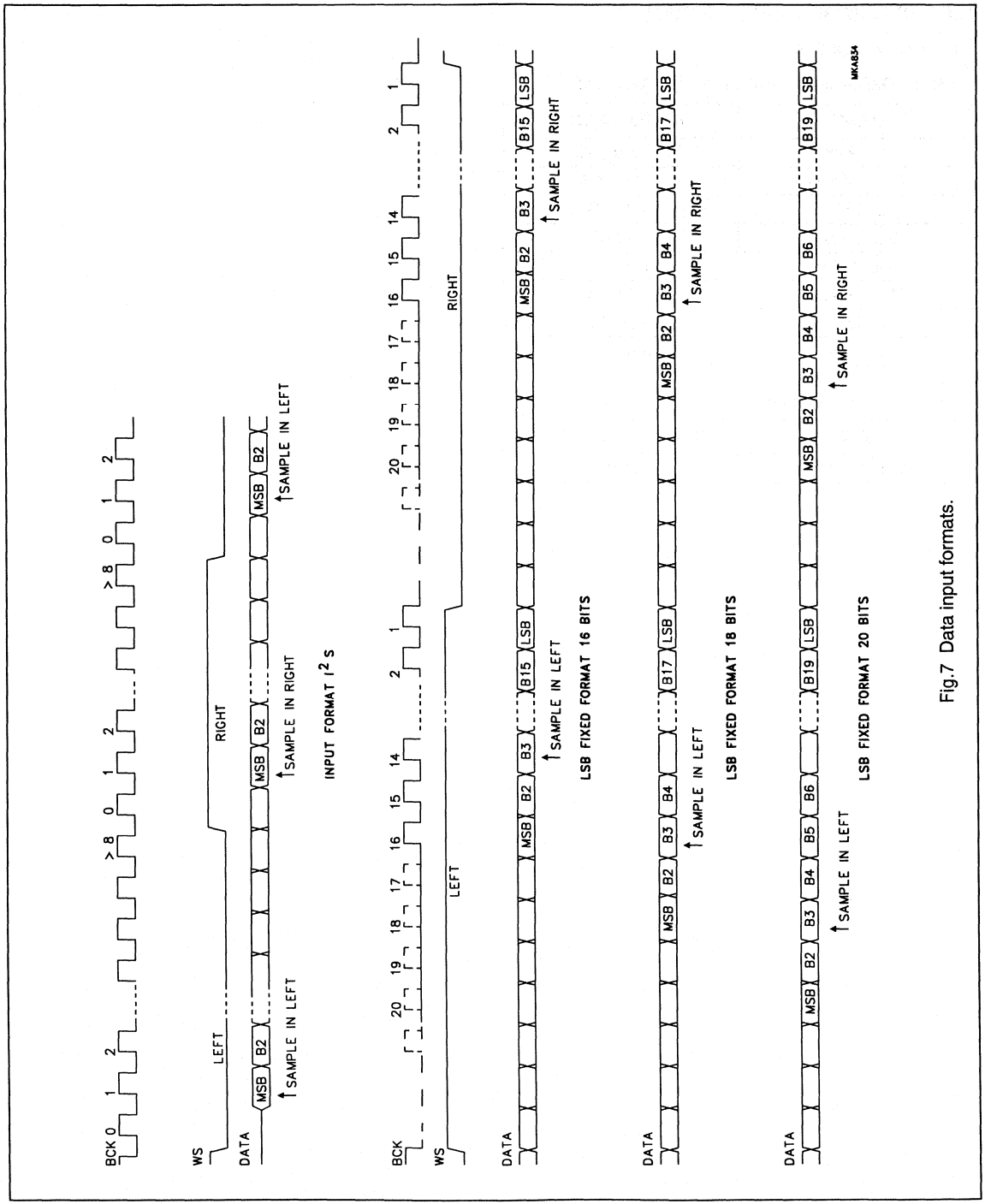


Fig.7 Data input formats.

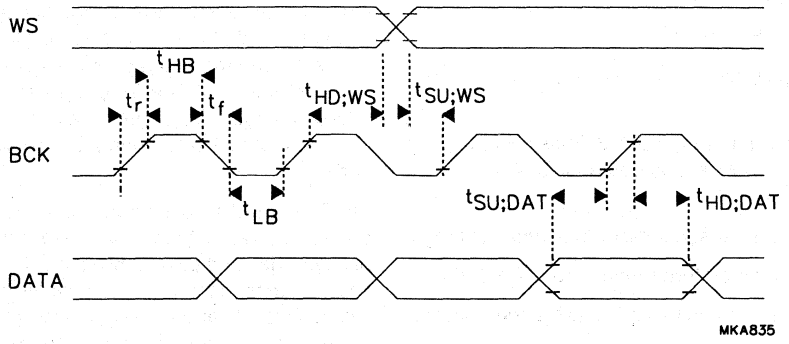


Fig.8 Timing of input signals.

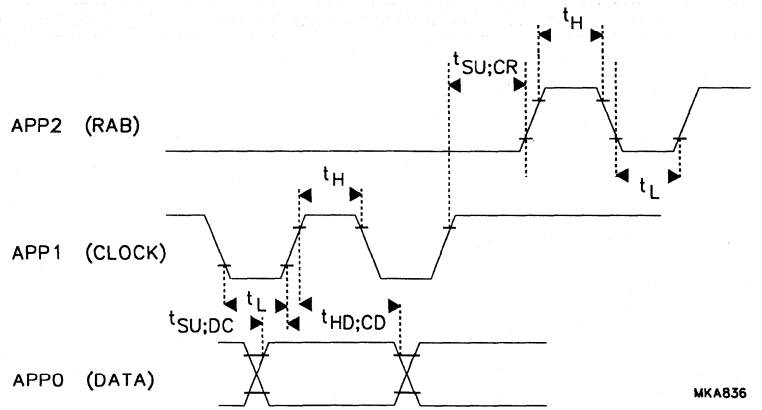


Fig.9 Microcontroller timing.

Stereo Continuous Calibration DAC (CC-DAC)

TDA1387T

FEATURES

- Low power consumption
- Low total harmonic distortion
- Wide dynamic range (16-bit resolution)
- Continuous Calibration (CC) concept
- Single 3 to 5.5 V supply rail
- Output and bias current are proportional to the supply voltage
- Fast settling time enables 2, 4 and 8 times oversampling (serial input) or double-speed operation at 4 times oversampling
- Internal bias current ensures maximum dynamic range
- Wide operating temperature range (–40 to + 85 °C)
- I^2S-bus input format (time multiplex, two's complement, TTL)
- No zero-crossing distortion
- Large DC output voltage compliance
- Contained in small outline package.

APPLICATIONS

- Portable digital audio equipment.

GENERAL DESCRIPTION

The TDA1387T is a member of a generation of digital-to-analog converters which incorporates the innovative technique of Continuous Calibration. The largest bit currents are repeatedly generated from one single reference current. This duplication is based upon an internal charge storage principle and has an accuracy which is insensitive to ageing, temperature and process variations.

The TDA1387T is fabricated in a 1.0 μm CMOS process and features an extremely low power dissipation, small package size and easy application. The intrinsic high coarse current accuracy combined with the implemented symmetrical offset decoding method preclude zero-crossing distortion and ensure high quality audio reproduction. The CC-DAC is eminently suitable for use in portable digital audio equipment.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA1387T	SO8	plastic small outline package; 8 leads; body width 3.9 mm.	SOT96-1

Stereo Continuous Calibration DAC (CC-DAC)

TDA1387T

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage		3.0	5.0	5.5	V
I_{DD}	supply current	V_{DD} = 5 V at code 0000H	–	5.5	6.5	mA
I_{FS}	full scale output current	V_{DD} = 5 V	0.86	1.0	1.14	mA
		V_{DD} = 3 V	–	0.6	–	mA
(THD + N)/S	total harmonic distortion plus noise-to-signal ratio	at 0 dB signal level	–	–88	–78	dB
		at 0 dB signal level	–	0.004	0.012	%
		at –60 dB signal level	–	–33	–24	dB
		at –60 dB signal level	–	2.2	6	%
		at –60 dB; A-weighted	–	–35	–	dB
		at –60 dB; A-weighted	–	1.7	–	%
S/N	signal-to-noise ratio at bipolar zero	A-weighted at code 0000H	86	98	–	dB
t_{cs}	current settling time to ±1 LSB		–	0.2	–	µs
BR	input bit rate (pin 3)		–	–	18.4	Mbits/s
f_{clk}	clock frequency		–	–	18.4	MHz
TC_{FS}	full scale temperature coefficient at pins 6 and 8		–	$\pm 400 \times 10^{-6}$	–	
T_{amb}	operating ambient temperature		–40	–	+85	°C
P_{tot}	total power dissipation	V_{DD} = 5 V at code 0000H	–	27.5	36	mW
		V_{DD} = 3 V at code 0000H	–	10	–	mW

BLOCK DIAGRAM

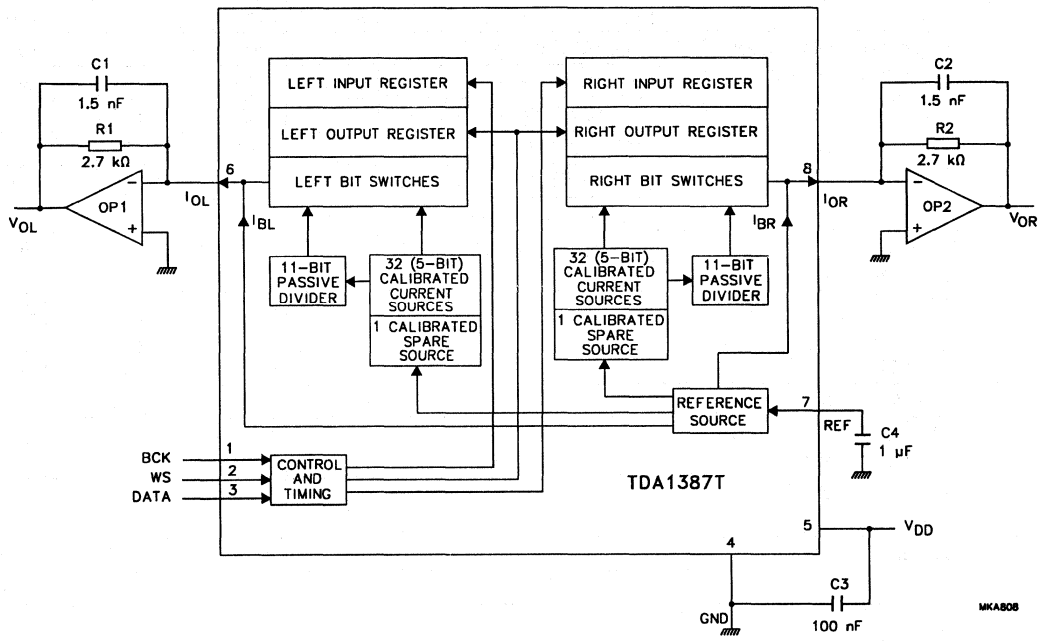


Fig.1 Block diagram.

Stereo Continuous Calibration DAC (CC-DAC)

TDA1387T

PINNING

SYMBOL	PIN	DESCRIPTION
BCK	1	bit clock input
WS	2	word selection input
DATA	3	data input
GND	4	ground
V_{DD}	5	supply voltage input
I_{OL}	6	left channel output
REF	7	reference decoupling
I_{OR}	8	right channel output

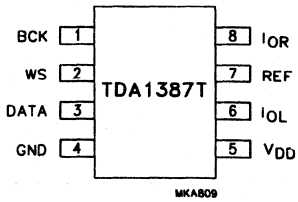


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The basic operation of the continuous calibration DAC is illustrated in Fig.3 which shows the calibration and operation cycle. During calibration of the MOS current source (Fig.3a) transistor M1 is connected as a diode by applying a reference current. The voltage V_{gs} on the intrinsic gate-source capacitance C_{gs} of M1 is then determined by the transistor characteristics. After the drain current has been calibrated to the reference value I_{ref}, the switch S1 is opened and S2 is switched to the other position (Fig.3b). The gate-to-source voltage V_{gs} of M1 is not changed because the charge on C_{gs} is preserved. Therefore, the drain current of M1 will still be equal to I_{ref} and this exact duplication of I_{ref} is now available at the OUT terminal.

In the TDA1387T, 32 current sources and one spare current source are continuously calibrated (see Fig.1). The spare current source is included to allow continuous converter operation. The output of one calibrated source is connected to an 11-bit binary current divider which consists of 2048 transistors. A symmetrical offset decoding principle is incorporated and arranges the bit switching such that the zero-crossing is performed by switching only the LSB currents.

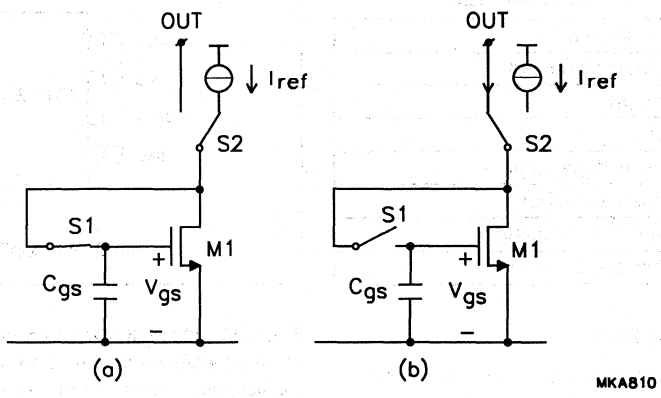
The TDA1387T (CC-DAC) accepts serial input data format of 16-bit word length. Left and right data words are time multiplexed. The input data format is shown in Figs 4 and 5.

With a HIGH level on the WS input, data is placed in the right input register, with a LOW level on the WS input, data is placed in the left input register. The data in the input registers are simultaneously latched to the output registers which control the bit switches. An internal bias current I_{bias} is added to the full scale output current I_{FS} in order to achieve maximum dynamic range at the outputs of OP1 and OP2.

The signal current I_{FS} and the bias current I_{bias} are both proportional to the supply voltage V_{DD}, and have a fixed mutual relation A_{bias} (where $A_{bias} = I_{bias}/I_{FS}$).

It is preferred that the non-inverting input of operational amplifiers OP1 and OP2 is tied to ground to achieve a maximum dynamic range over the supply voltage range.

A decoupling capacitor C4 is recommended for enhancing the supply voltage ripple rejection of the DAC. It has no significant effect on the noise performance.



(a) Calibration.
(b) Operation.

Fig.3 Calibration principle.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage		–	6.0	V
$T_{xtal(max)}$	maximum crystal temperature		–	+150	°C
T_{stg}	storage temperature		–55	+150	°C
T_{amb}	operating ambient temperature		–40	+85	°C
V_{es}	electrostatic handling	note 1	–2000	+2000	V
		note 2	–200	+200	V

Notes

1. Human body model: C = 100 pF; R = 1.5 kΩ; 3 zaps positive and 3 zaps negative.
2. Machine model: C = 200 pF; L = 0.5 µH; R = 10 Ω; 3 zaps positive and 3 zaps negative.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air	210	K/W

CHARACTERISTICS

V_{DD} = 5 V; T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD}	supply voltage		3.0	5.0	5.5	V
I_{DD}	supply current	at code 0000H	–	5.5	6.5	mA
SVRR	supply voltage ripple rejection	note 1	–	30	–	dB
Digital inputs; WS, BCK and DATA						
$\|I_{LI}\|$	LOW level input leakage current	V_i = 0 V	–	–	10	µA
$\|I_{HI}\|$	HIGH level input leakage current	V_i = 5 V	–	–	10	µA
f_{BCK}	clock frequency		–	–	18.4	MHz
BR	data bit rate		–	–	18.4	Mbits/s
f_{WS}	word select input frequency		–	–	384	kHz
Timing						
t_r	rise time		–	–	12	ns
t_f	fall time		–	–	12	ns
T_{cy}	bit clock cycle time		54	–	–	ns
t_{HB}	bit clock HIGH time		15	–	–	ns
t_{LB}	bit clock LOW time		15	–	–	ns
$t_{su;DA}$	data set-up time		12	–	–	ns
$t_{h;DA}$	data hold time		2	–	–	ns
$t_{h;WS}$	word select hold time		2	–	–	ns
$t_{su;WS}$	word select set-up time		12	–	–	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Analog outputs; I_{OL} and I_{OR}						
RES	output resolution		–	–	16	bits
V_{DCC}	DC output voltage compliance		0	–	3.5	V
$I_{o(p-p)}$	AC output signal current (peak-to-peak value)	note 2	0.86	1.0	1.14	mA
TC_{FS}	full-scale temperature coefficient		–	$\pm 400 \times 10^{-6}$	–	
I_{bias}	output bias current	note 2	0.93	1.08	1.23	mA
V_{ref}	output reference voltage	note 2	–	$\frac{1}{6}V_{DD}$	–	V
R_{ref}	output resistance at pin 7		7.6	11.4	14.8	kΩ
(TDH + N)/S	total harmonic distortion plus noise-to-signal ratio	at 0 dB signal level; note 3	–	–88	–78	dB
		at 0 dB signal level; note 3	–	0.004	0.01	%
		at –60 dB signal level; note 3	–	–33	–24	dB
		at –60 dB signal level; note 3	–	2.2	6	%
		at –60 dB; A-weighted; note 3	–	–35	–	dB
		at –60 dB; A-weighted; note 3	–	1.8	–	%
		f_i = 20 Hz to 20 kHz; at 0 dB signal level; note 3	–	–84	–70	dB
		f_i = 20 Hz to 20 kHz; at 0 dB signal level; note 3	–	0.006	0.03	%
t_{cs}	current settling time to ±1 LSB		–	0.2	–	µs
α_{cs}	channel separation		86	95	–	dB
$\lvert\Delta I_O\rvert$	unbalance between outputs	note 3	–	0.2	0.3	dB
$\lvert t_d \rvert$	delay time between outputs		–	±0.2	–	µs
S/N	signal-to-noise ratio at bipolar zero	A-weighted at code 0000H	86	98	–	dB

Notes

1. V_{ripple} = 1% of the supply voltage; f_{ripple} = 100 Hz.
2. Values are proportional to V_{DD}.
3. Measured with 1 kHz sine wave generated at a sampling rate of 192 kHz.

QUALITY SPECIFICATION

In accordance with *"UZW-BO/FQ-0601"*. The numbers of the quality specification can be found in the *"Quality Reference Handbook"*. The handbook can be ordered using the code 9398 510 63011.

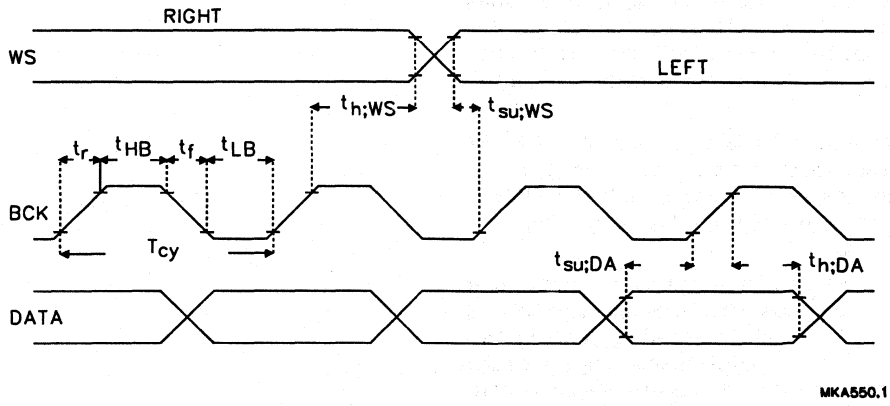


Fig.4 Input signal timing (I^2S-bus).

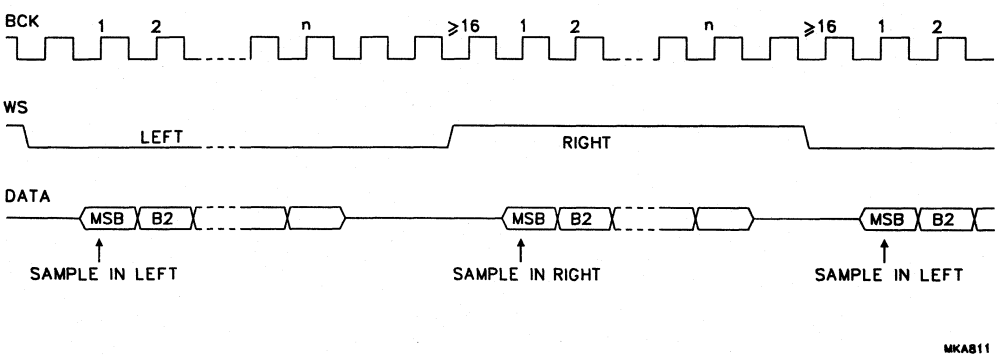


Fig.5 Input signal format (I^2S-bus).

APPLICATION INFORMATION

The TDA1387T offers great ease in designing-in to printed-circuit board due to its small size and low pin count. The TDA1387T being a mixed-signal IC in CMOS, some attention needs to be paid to layout and topology of the application PCB. The following basic rules will yield the desired performance. The most important considerations are:

1. Supply: care should be taken to supply the TDA1387T with a clean, noiseless supply voltage, for a good noise performance of the analog parts of the DAC. Supply purity can easily be achieved by using an RC-filtered supply.
2. Grounding: preferably a ground plane should be used, in order to have a low-impedance return available at any point in the layout. It is advantageous to make a partitioning of the ground plane according to the nature of the expected return currents (digital input returns separate from supply returns separate from the analog section).
3. Topology: the capacitor decoupling high-frequency supply interference from V_{DD} to GND should be placed as close as is physically possible to the IC body, ensuring a low-inductance path to ground. The digital input conductors may be shielded by ground leads running alongside. The placement of a passive ground plane underside the entire IC surface gives 'free' additional decoupling from the IC body to ground as well as providing a shield between the digital input pins and the analog output pins.

24 W BTL OR 2 × 12 W STEREO CAR RADIO POWER AMPLIFIER

GENERAL DESCRIPTION

The TDA1510AQ is a class-B integrated output amplifier encapsulated in a 13-lead single in-line (SIL) plastic power package. Developed primarily for car radio application, the device can also be used to drive low impedance loads (down to 1,6 Ω). With a supply voltage (V_P) of 14,4 V, an output power of 24 W can be delivered into a 4 Ω Bridge Tied Load (BTL), or when used as a stereo amplifier, 2 x 12 W into 2 Ω or 2 x 7 W into 4 Ω.

Features

- Flexibility — stereo as well as mono BTL
- Low offset voltage at the output (important for BTL)
- Load dump protection
- A.C. short-circuit-safe to ground
- Low number, small sized external components
- Internal limiting of bandwidth for high frequencies
- High output power
- Large useable gain variation
- Good ripple rejection
- Thermal protection
- Low stand-by current possibility
- High reliability

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage range:						
operating		V_P	6,0	14,4	18,0	V
non-operating		V_P	–	–	28,0	V
non-operating, load dump protection		V_P	–	–	45,0	V
Repetitive peak output current		I_{ORM}	–	–	4,0	A
Total quiescent current		I_{tot}	–	75	120	mA
Stand-by current		I_{sb}	–	–	2	mA
Switch-on current		I_{so}	0,15	0,35	0,80	mA
Input impedance	pins 1, 2, 12 and 13	$\lvert Z_I \rvert$	1	–	–	MΩ
Storage temperature range		T_{stg}	–65	–	+ 150	°C
Crystal temperature		T_c	–	–	150	°C

PACKAGE OUTLINE

TDA1510AQ: 13-lead SIL-bent-to-DIL; plastic power (SOT141C).

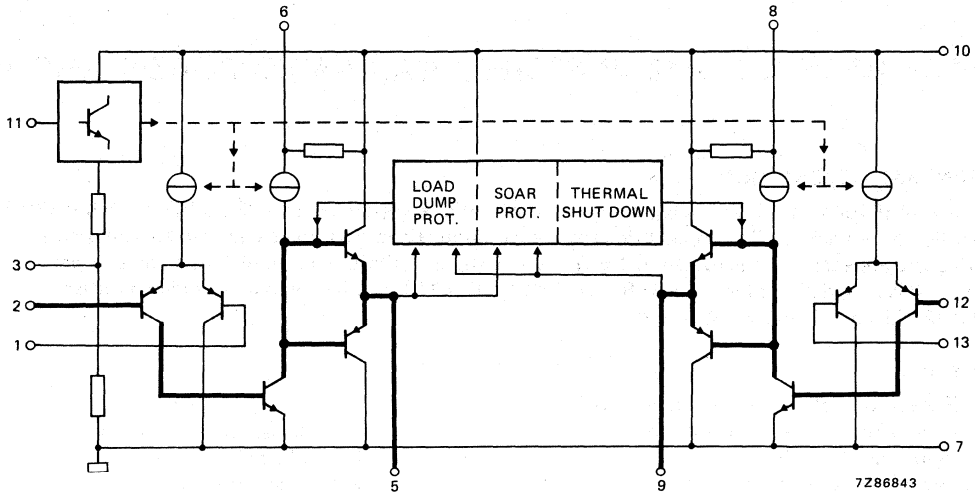


Fig. 1 Functional diagram; heavy lines indicate signal paths.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage:					
operating	pin 10	V_P	–	18	V
non-operating		V_P	–	28	V
non-operating, load dump protection	during 50 ms	V_P	–	45	V
Peak output current		I_{OM}	–	6	A
Total power dissipation	see Fig. 2	P_{tot}			
Storage temperature range		T_{stg}	–65	+ 150	°C
Crystal temperature		T_c	–	+ 150	°C

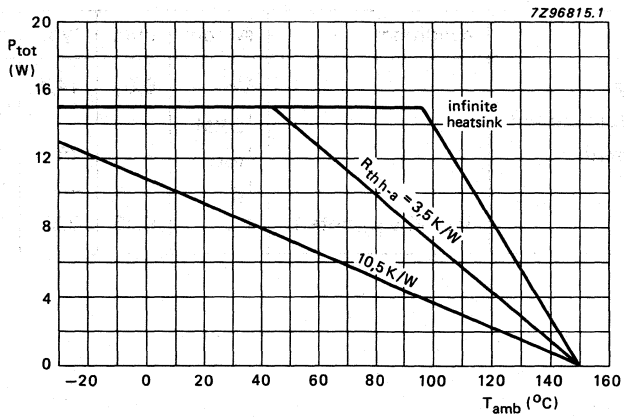


Fig. 2 Power derating curves.

HEATSINK DESIGN EXAMPLE

The derating of the encapsulation requires the following external heatsink (for sine-wave drive):

$(R_{th\ j\text{-}mb}) = 3{,}5$ K/W

24 W BTL (4 Ω) or 2 x 12 W stereo (2 Ω); maximum sine-wave dissipation = 12 W;
$T_{amb} = 65\ ^{o}C$ (maximum):

$$R_{th\ h\text{-}a} = \frac{150 - 65}{12} - 3{,}5 = 3{,}5\ \text{K/W}$$

2 x 7 W stereo (4 Ω); maximum sine-wave dissipation = 6 W;
$T_{amb} = 65\ ^{o}C$ (maximum):

$$R_{th\ h\text{-}a} = \frac{150 - 65}{6} - 3{,}5 = 10{,}5\ \text{K/W}$$

D.C. CHARACTERISTICS

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage range		V_P	6,0	14,4	18,0	V
Repetitive peak output current		I_{ORM}	–	–	4,0	A
Total quiescent current		I_{tot}	–	75	120	mA
Stand-by current		I_{sb}	–	–	2	mA
Switch-on current	$V_{11} \leqslant V_{10}$; note 1	I_{so}	0,15	0,35	0,80	mA

A.C. CHARACTERISTICS

T_{amb} = 25 °C; V_P = 14,4 V; f = 1 kHz; unless otherwise specified

parameter	parameter	symbol	min.	typ.	max.	unit
Bridge Tied Load application (BTL)						
Output power with bootstrap	note 6; R_L = 4 Ω					
	V_P = 13,2 V					
	d_{tot} = 0,5%	P_o	–	15,0	–	W
	d_{tot} = 10%	P_o	–	20,0	–	W
	V_P = 14,4 V					
	d_{tot} = 0,5%	P_o	15,5	18,0	–	W
	d_{tot} = 10%	P_o	20,0	24,0	–	W
Open loop voltage gain		G_o	–	75	–	dB
Closed loop voltage gain	note 2	G_c	39,5	40,0	40,5	dB
Frequency response	at –3 dB; note 3	f_r	–	20 to > 20 k	–	Hz
Input impedance	note 4	$\|Z_i\|$	1	–	–	MΩ
Noise output voltage (r.m.s. value)	f = 20 Hz to 20 kHz					
	R_S = 0 Ω	$V_{n\ (rms)}$	–	0,2	–	mV
	R_S = 10 kΩ	$V_{n\ (rms)}$	–	0,35	0,8	mV
	R_S = 10 kΩ; according to IEC 179 curve A	$V_{n\ (rms)}$	–	0,25	–	mV
Supply voltage ripple rejection	f = 100 Hz; note 5	SVRR	42	50	–	dB
D.C. output offset voltage between channels		$\|\Delta V_{5\text{-}9}\|$	–	2	50	mV
Power bandwidth	–1 dB; d_{tot} = 0,5%	B	–	30 to > 40 k	–	Hz

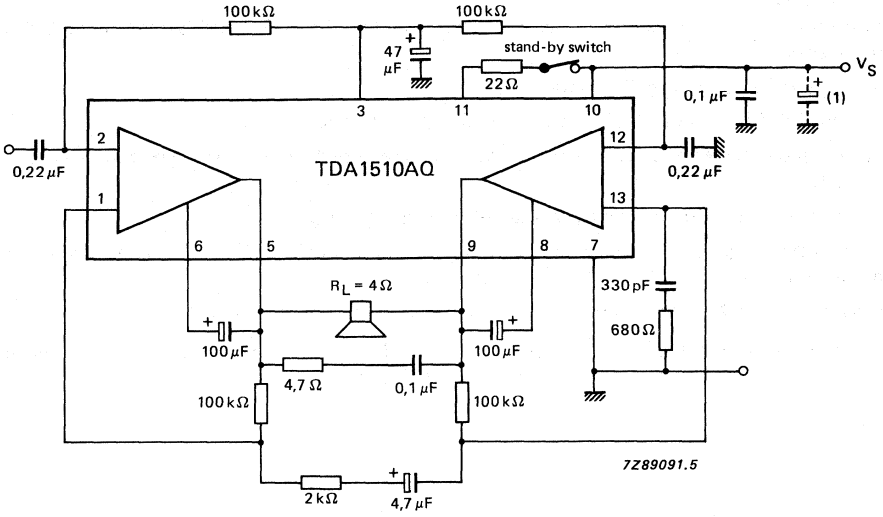
A.C. CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Stereo application						
Output power; with bootstrap	note 6; $R_L = 4\ \Omega$					
	$V_P = 13{,}2$ V					
	$d_{tot} = 0{,}5\%$	P_o	–	4,5	–	W
	$d_{tot} = 10\%$	P_o	–	6,0	–	W
	$V_P = 14{,}4$ V					
	$d_{tot} = 0{,}5\%$	P_o	4,5	5,5	–	W
	$d_{tot} = 10\%$	P_o	6,0	7,0	–	W
	$R_L = 2\ \Omega$					
	$V_P = 13{,}2$ V					
	$d_{tot} = 0{,}5\%$	P_o	–	7,5	–	W
	$d_{tot} = 10\%$	P_o	–	10,0	–	W
	$V_P = 14{,}4$ V					
	$d_{tot} = 0{,}5\%$	P_o	7,75	9,0	–	W
	$d_{tot} = 10\%$	P_o	10,0	12,0	–	W
Output power; without bootstrap	notes 6, 8 and 9 $R_L = 4\ \Omega$ $V_P = 14{,}4$ V					
	$d_{tot} = 10\%$	P_o	–	6	–	W
Frequency response	notes 3 and 6					
	−3 dB	f_r	–	40 to > 20 k	–	Hz
Supply voltage ripple rejection	note 5					
	f = 1 kHz	SVRR	–	50	–	dB
Channel separation	$R_S = 10\ k\Omega$;					
	f = 1 kHz	α	40	50	–	dB
Closed loop voltage gain	note 7	G_c	39,5	40,0	40,5	dB
Noise output voltage (r.m.s. value)	f = 20 Hz to 20 kHz;					
	$R_S = 0\ \Omega$	$V_{n(rms)}$	–	0,15	–	mV
	$R_S = 10\ k\Omega$	$V_{n(rms)}$	–	0,25	–	mV
	$R_S = 10\ k\Omega$; according to IEC179 curve A	$V_{n(rms)}$	–	0,2	–	mV

Notes to the characteristics

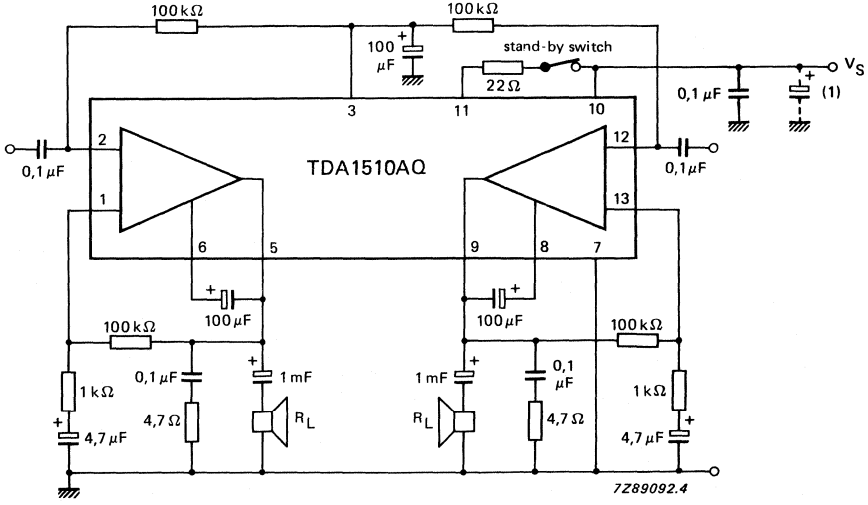
1. If $V_{11} > V_{10}$ then I_{11} must be < 10 mA.
2. Closed loop voltage gain can be chosen between 32 and 56 dB (BTL), and is determined by external components.
3. Frequency response externally fixed.
4. The input impedance in the test circuit (Fig. 3) is typ. 100 kΩ.
5. Supply voltage ripple rejection measured with a source impedance of 0 Ω (maximum ripple amplitude 2 V).
6. Output power is measured directly at the output pins of the IC.
7. Closed loop voltage gain can be chosen between 26 and 50 dB (stereo), and is determined by external components.
8. A resistor of 56 kΩ between pins 3 and 7 is required for symmetrical clipping.
9. Without bootstrap the 100 μF capacitor between pins 5 and 6 and the 100 μF capacitor between pins 8 and 9 can be omitted. Pins 6 and 8 connected to pin 10.

APPLICATION INFORMATION



(1) belongs to power supply

Fig. 3 Test and application circuit; Bridge Tied Load (BTL).



(1) belongs to power supply

Fig. 4 Test and application circuit; stereo mode.

50 W HIGH- PERFORMANCE HI-FI AMPLIFIER

GENERAL DESCRIPTION

The TDA1514A integrated circuit is a hi-fi power amplifier for use as a building block in radio, tv and other audio applications. The high performance of the IC meets the requirements of digital sources (e.g. Compact Disc equipment).
The circuit is totally protected, the two output transistors both having thermal and SOAR protection (see Fig.3). The circuit also has a mute function that can be arranged for a period after power-on with a delay time fixed by external components.
The device is intended for symmetrical power supplies but an asymmetrical supply may also be used.

Features

- High output power
- Low harmonic distortion
- Low intermodulation distortion
- Low offset voltage
- Good ripple rejection
- Mute/stand-by facilities
- Thermal protection
- Protected against electrostatic discharge
- No switch-on or switch-off clicks
- Very low thermal resistance
- Safe Operating Area (SOAR) protection

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage range (pin 6 to pin 4)		V_P	± 10	–	± 30	V
Total quiescent current	V_P = ± 27.5 V	I_{tot}	–	56	–	mA
Output power	THD = –60 dB; V_P = ± 27.5 V; R_L = 8 Ω	P_o	–	40	–	W
	V_P = ± 23 V; R_L = 4 Ω	P_o	–	48	–	W
Closed loop voltage gain	determined externally	G_c	–	30	–	dB
Input resistance	determined externally	R_i	–	20	–	kΩ
Signal plus noise-to-noise ratio	P_o = 50 mW	(S+N)/N	–	83	–	dB
Supply voltage ripple rejection	f = 100 Hz	SVRR	–	64	–	dB

PACKAGE OUTLINE

9-lead SIL, plastic power (SOT131R).

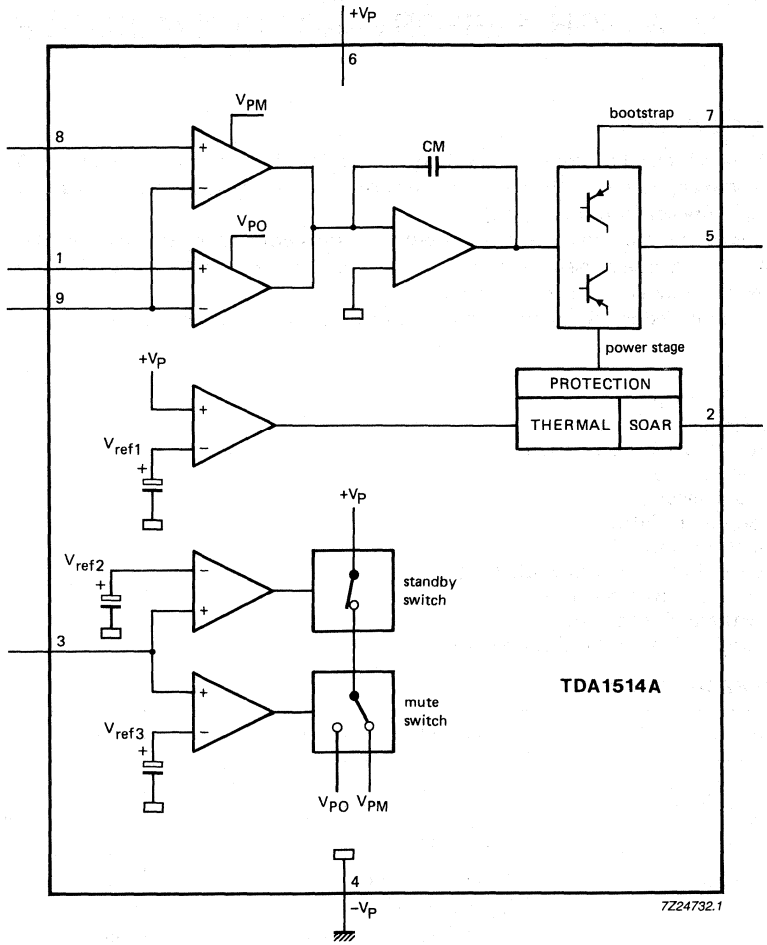


Fig.1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum Rating System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage (pin 6 to pin 4)	V_P	–	±30	V
Bootstrap voltage (pin 7 to pin 4)	V_{bstr}	–	70	V
Output current (repetitive peak)	I_o	–	8	A
Operating ambient temperature range	T_{amb}	see Fig.2		
Storage temperature range	T_{stg}	−55	+150	°C
Power dissipation		see Fig.2		
Thermal shut-down protection time	t_{pr}	–	1	hour
Mute voltage (pin 3 to pin 4)	V_m	–	7.25	V

THERMAL RESISTANCE

From junction to mounting base $R_{th\ j\text{-}mb}$ 1 K/W

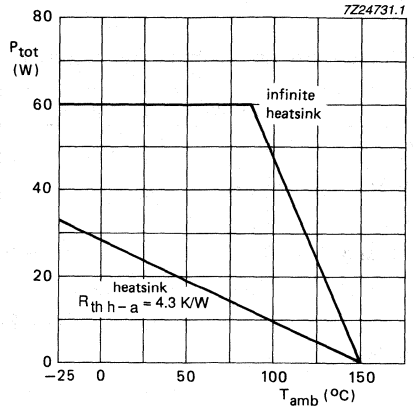


Fig.2 Power derating curve.

The theoretical maximum power dissipation for P_o = 40 W with a stabilized power supply is:

$$\frac{V_P^2}{2\pi^2 R_L} = 19\ \text{W; where } V_P = \pm 27.5\ \text{V; } R_L = 8\ \Omega$$

Considering, for example, a maximum ambient temperature of 50 °C and a maximum junction temperature of 150 °C the total thermal resistance is:

$$R_{th\ j\text{-}a} = \frac{150 - 50}{19} = 5.3\ \text{K/W}$$

Since the thermal resistance of the SOT131A encapsulation is $R_{th\ j\text{-}mb} < 1$ K/W, the thermal resistance required of the heatsink is $R_{th\ h\text{-}a} < 4.3$ K/W.

SAFE OPERATING AREA (SOAR) PROTECTION

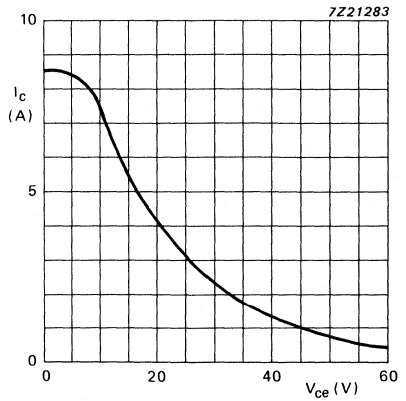


Fig.3 SOAR protection curve.

CHARACTERISTICS

V_P = ± 27.5 V; R_L = 8 Ω; f = 1 kHz; T_{amb} = 25 °C; test circuit as Fig.4; unless otherwise specified.

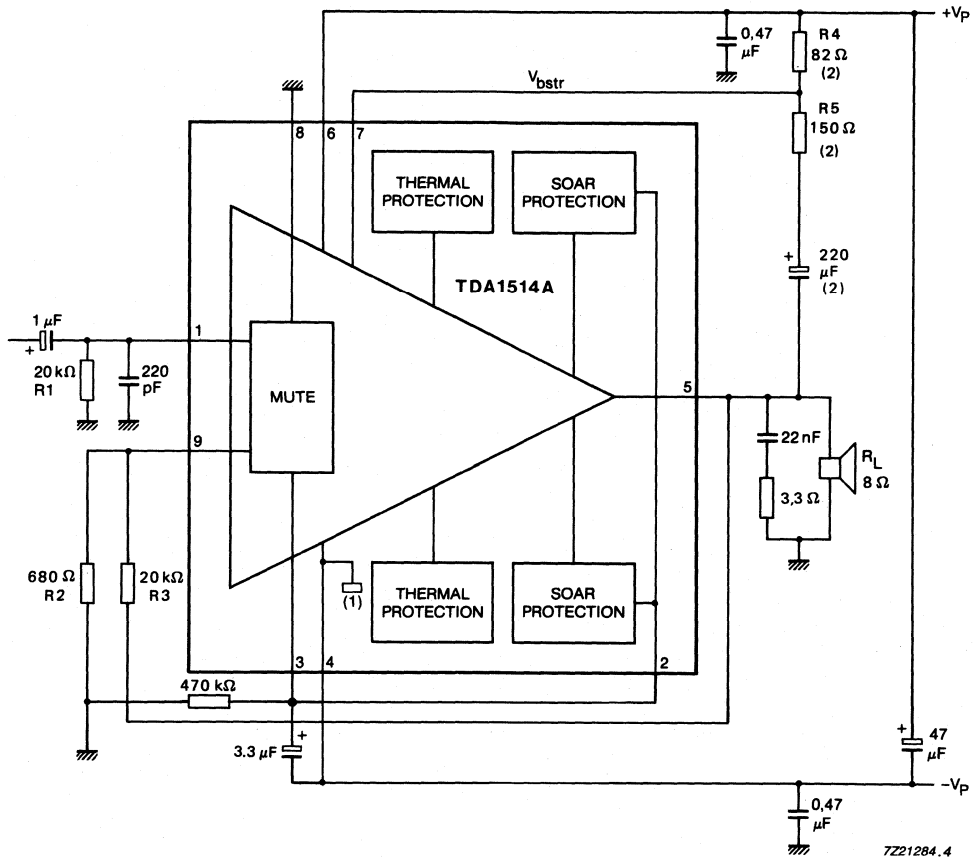
parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage range (pin 6 to pin 4)		V_P	± 10	–	± 30	V
Maximum output current (peak value)		$I_{OM\,max}$	6.4	–	–	A
Operating state						
Voltage (pins 3 to 4)		V_{3-4}	6	–	7.25	V
Total quiescent current	$R_L = \infty$	I_{tot}	30	56	90	mA
Output power	THD = –60 dB	P_o	37	40	–	W
	THD = –20 dB	P_o	–	51	–	W
Output power	V_P = ± 23 V; THD = –60 dB					
	R_L = 8 Ω	P_o	–	28	–	W
	R_L = 4 Ω	P_o	–	48	–	W
Total harmonic distortion	P_o = 32 W	THD	–	–90	–80	dB
Intermodulation distortion	P_o = 32 W note 1	d_{im}	–	–86	–	dB
Power bandwidth	(–3 dB); THD = –60 dB	B	–	20 to 25 000		Hz
Slew rate		dV/dt	–	14	–	V/μs
Closed loop voltage gain	note 2	G_c	–	30	–	dB
Open loop voltage gain		G_o	–	89	–	dB
Input impedance	note 3	$\|Z_i\|$	1	–	–	MΩ
Signal-to-noise ratio	note 4 P_o = 50 mW	S/N	80	83	–	dB
Output offset voltage		V_o	–	7	200	mV
Input bias current		I_I	–	0.1	1.0	μA
Output impedance		$\|Z_o\|$	–	–	0.1	Ω
Supply voltage ripple rejection	note 5	SVRR	58	64	–	dB
Quiescent current into pin 2	note 6	I_2	–	0.1	–	μA

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Mute state						
Voltage on pin 3		V_{3-4}	2	–	4.5	V
Offset voltage		V_o	–	30	200	V
Output voltage	$V_{i(rms)}$ = 1 V f = 1 kHz	V_o	–	450	–	μV
Ripple rejection	note 5	RR	–	60	–	dB
Standby state						
Voltage on pin 3		V_{3-4}	0	–	0.9	V
Total quiescent current		I_{tot}	–	18	25	mA
Ripple rejection	notes 5 and 7	RR	–	60	–	dB
Supply voltage to obtain standby state		$\pm V_P$	5.0	–	7.0	V

Notes to the characteristics

1. Measured with two superimposed signals of 50 Hz and 7 kHz with an amplitude relationship of 4 : 1.
2. The closed loop gain is determined by external resistors (Fig.4, R2 and R3) and is variable between 20 and 46 dB.
3. The input impedance in the test circuit (Fig.4) is determined by the bias resistor R1.
4. The noise output voltage is measured in a bandwidth of 20 Hz to 20 kHz with a source resistance of 2 kΩ.
5. f = 100 Hz; R_S = 2 kΩ; ripple voltage = 500 $mV_{(eff)}$ on positive and negative supply.
6. The quiescent current into pin 2 has an impact on the mute time.
7. Without bootstrap.



(1) Mounting base connected to $-V_P$.

(2) When used without a bootstrap these components are disconnected and pin 6 is connected to pin 7 thus decreasing the output power by approximately 4 W.

(3) When $R_L = 4\ \Omega$: R4 = 47 Ω and R5 = 82 Ω.

Fig.4 Application and test circuit.

24 W BTL OR 2 x 12 W STEREO CAR RADIO POWER AMPLIFIER

The TDA1515BQ is a monolithic integrated class-B output amplifier in a 13-lead single in-line (SIL) plastic power package. The device is primarily developed for car radio applications, and also to drive low-impedance loads (down to 1,6 Ω). At a supply voltage V_P = 14,4 V, an output power of 24 W can be delivered into a 4 Ω BTL (Bridge Tied Load), or, when used as stereo amplifier, it delivers 2 x 12 W into 2 Ω or 2 x 7 W into 4 Ω.

Special features are:

- flexibility in use – mono BTL as well as stereo
- high output power
- low offset voltage at the output (important for BTL)
- large usable gain variation
- very good ripple rejection
- internal limited bandwidth for high frequencies
- low stand-by current possibility (typ. 1 μA), to simplify required switches; TTL drive possible
- low number and small sized external components
- high reliability

The following currently required protections are incorporated in the circuit. These protections also have positive influence on reliability in the applications.

- load dump protection
- **a.c. and d.c. short-circuit safe to ground up to V_P = 18 V**
- thermal protection
- speaker protection in bridge configuration
- SOAR protection
- outputs short-circuit safe to ground in BTL
- reverse polarity safe

QUICK REFERENCE DATA

Supply voltage range (operating)	V_P		6 to 18	V
Supply voltage (non-operating)	V_P	max.	28	V
Supply voltage (non-operating; load dump protection)	V_P	max.	45	V
Repetitive peak output current	I_{ORM}	max.	4	A
Total quiescent current	I_{tot}	typ.	75	mA
Stand-by current	I_{sb}	typ.	1	μA
Switch-on current	I_{so}	<	100	μA
Input impedance	$\|Z_i\|$	>	1	MΩ
Bridge tied load application (BTL)	V_P	= 14,4	13,2	V
Output power at R_L = 4 Ω (with bootstrap)				
d_{tot} = 0,5%	P_o	typ. 18	15	W
d_{tot} = 10%	P_o	typ. 24	20	W
Supply voltage ripple rejection; R_S = 0 Ω; f = 100 Hz	RR	typ. 50	50	dB
D.C. output offset voltage between the outputs	$\|\Delta V_{5-9}\|$	< 50	50	mV
Stereo application				
Output power at d_{tot} = 10% (with bootstrap)				
R_L = 4 Ω	P_o	typ. 7	6	W
R_L = 2 Ω	P_o	typ. 12	10	W
Output power at **d_{tot} = 0,5%** (with bootstrap)				
R_L = 4 Ω	P_o	typ. 5,5	4,5	W
R_L = 2 Ω	P_o	typ. 9	7,5	W
Channel separation	α	> 40	40	dB
Noise output voltage; R_S = 10 kΩ; according to IEC curve-A	V_n	typ. 0,2	0,2	mV

PACKAGE OUTLINE 13-lead SIL-bent-to-DIL; plastic power (SOT141C).

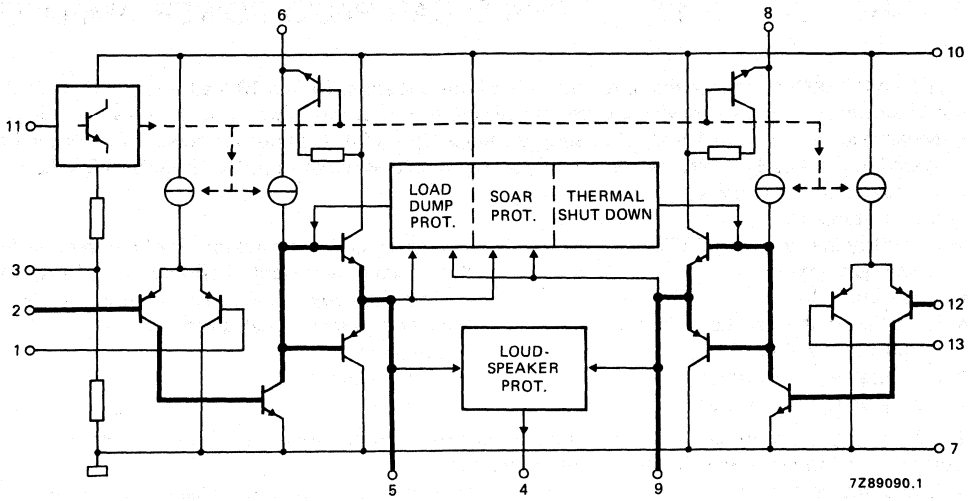


Fig. 1 Internal block diagram; the heavy lines indicate the signal paths.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage; operating (pin 10)	V_P	max.	18 V
Supply voltage; non-operating	V_P	max.	28 V
Supply voltage; during 50 ms (load dump protection)	V_P	max.	45 V
Peak output current	I_{OM}	max.	6 A
Total power dissipation	see derating curve Fig. 2		
Storage temperature range	T_{stg}	−55 to + 150	°C
Crystal temperature	T_c	max.	150 °C
A.C. and d.c. short-circuit safe voltage		max.	18 V
Reverse polarity		max.	10 V

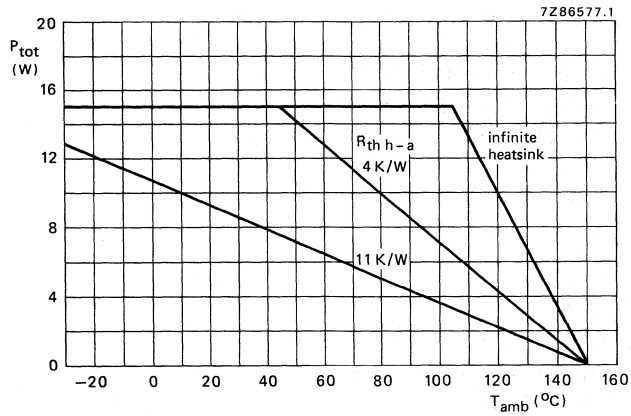


Fig. 2 Power derating curves.

HEATSINK DESIGN EXAMPLE

The derating of 3 K/W of the encapsulation requires the following external heatsink (for sine-wave drive):

24 W BTL (4 Ω) or 2 x 12 W stereo (2 Ω)
maximum sine-wave dissipation: 12 W
T_{amb} = 65 °C maximum

$$R_{th\ h-a} = \frac{150-65}{12} - 3 = 4\ \text{K/W}.$$

2 x 7 W stereo (4 Ω)
maximum sine-wave dissipation: 6 W
T_{amb} = 65 °C maximum

$$R_{th\ h-a} = \frac{150-65}{6} - 3 = 11\ \text{K/W}.$$

D.C. CHARACTERISTICS

Supply voltage range (pin 10)	V_P		6 to 18 V
Repetitive peak output current	I_{ORM}	<	4 A
Total quiescent current	I_{tot}	typ.	75 mA
Switching level 11 : OFF	V_{11}	<	1,8 V
ON	V_{11}	>	3 V
Impedance between pins 10 and 6; 10 and 8 (stand-by position $V_{11} < 1,8$ V)	$\|Z_{OFF}\|$	>	100 kΩ
Stand-by current at V_{11} = 0 to 0,8 V	I_{sb}	typ. <	1 μA 100 μA
Switch-on current (pin 11) at $V_{11} \leqslant V_{10}$ (note 1)	I_{so}	typ. <	10 μA 100 μA

A.C. CHARACTERISTICS

T_{amb} = 25 °C; V_P = 14,4 V; f = 1 kHz; unless otherwise specified

Bridge tied load application (BTL); see Fig. 3

Output power at R_L = 4 Ω (with bootstrap)			
V_P = 14,4 V; **d_{tot} = 0,5%**	P_o	> typ.	15,5 W 18 W
V_P = 14,4 V; d_{tot} = 10%	P_o	> typ.	20 W 24 W
V_P = 13,2 V; **d_{tot} = 0,5%**	P_o	typ.	15 W
V_P = 13,2 V; d_{tot} = 10%	P_o	typ.	20 W
Open loop voltage gain	G_o	typ.	75 dB
Closed loop voltage gain (note 2)	G_c	typ.	40 (± 0,5) dB
Output power without bootstrap (note 9)			
V_P = 14,4 V; d_{tot} = 10 %	P_o	typ.	15 W
V_P = 14,4 V; d_{tot} = 0,5 %	P_o	typ.	12 W
V_P = 13,2 V; d_{tot} = 10 %	P_o	typ.	12 W
V_P = 13,2 V; d_{tot} = 0,5 %	P_o	typ.	9 W
Frequency response at −3 dB (note 3)	B		20 Hz to min. 20 kHz
Input impedance (note 4)	$\|Z_i\|$	>	1 MΩ
Noise input voltage (r.m.s. value) at f = 20 Hz to 20 kHz			
R_S = 0 Ω	$V_{n(rms)}$	typ.	0,2 mV
R_S = 10 kΩ	$V_{n(rms)}$	typ. <	0,35 mV 0,8 mV
R_S = 10 kΩ; according to IEC 179 curve A	V_n	typ.	0,25 mV
Supply voltage ripple rejection (note 5)			
f = 100 Hz	RR	> typ.	42 dB 50 dB
D.C. output offset voltage between the outputs	$\|\Delta V_{5\text{-}9}\|$	<	50 mV
		typ.	2 mV
Loudspeaker protection (all conditions) maximum d.c. voltage (across the load)	$\|\Delta V_{5\text{-}9}\|$	<	1 V
Power bandwidth; −1 dB; **d_{tot} = 0,5%**	B		30 Hz to 40 kHz

Stereo application; see Fig. 4

Output power at d_{tot} = 10%; with bootstrap (note 6)			
V_P = 14,4 V; R_L = 4 Ω	P_o	>	6 W
		typ.	7 W
V_P = 14,4 V; R_L = 2 Ω	P_o	>	10 W
		typ.	12 W
V_P = 13,2 V; R_L = 4 Ω	P_o	typ.	6 W
V_P = 13,2 V; R_L = 2 Ω	P_o	typ.	10 W
Output power at d_{tot} = 0,5%; with bootstrap (note 6)			
V_P = 14,4 V; R_L = 4 Ω	P_o	typ.	5,5 W
V_P = 14,4 V; R_L = 2 Ω	P_o	typ.	9 W
V_P = 13,2 V; R_L = 4 Ω	P_o	typ.	4,5 W
V_P = 13,2 V; R_L = 2 Ω	P_o	typ.	7,5 W
Output power at d_{tot} = 10%; without bootstrap			
V_P = 14,4 V; R_L = 4 Ω (notes 6, 8 and 9)	P_o	typ.	6 W
Frequency response at −3 dB (note 3)	B	40 Hz to min.	20 kHz
Supply voltage ripple rejection (note 5)	RR	typ.	50 dB
Channel separation; R_S = 10 kΩ; f = 1 kHz	α	>	40 dB
		typ.	50 dB
Closed loop voltage gain (note 7)	G_c	typ.	40 dB
Noise output voltage (r.m.s. value) at f = 20 Hz to 20 kHz			
R_S = 0 Ω	$V_{n(rms)}$	typ.	0,15 mV
R_S = 10 kΩ	$V_{n(rms)}$	typ.	0,25 mV
R_S = 10 kΩ; according to IEC 179 curve A	V_n	typ.	0,2 mV

Notes

1. The internal circuit impedance at pin 11 is > 5 kΩ if $V_{11} > V_{10}$.
2. Closed loop voltage gain can be chosen between 32 and 56 dB (BTL), and is determined by external components. For further gain reduction see Application Report.
3. Frequency response externally fixed.
4. The input impedance in the test circuit (Fig. 3) is typ. 100 kΩ.
5. Supply voltage ripple rejection measured with a source impedance of 0 Ω (maximum ripple amplitude: 2 V).
6. Output power is measured directly at the output pins of the IC.
7. Closed loop voltage gain can be chosen between 26 and 50 dB (stereo), and is determined by external components.
8. A resistor of 56 kΩ between pins 3 and 7 to reach symmetrical clipping.
9. Without bootstrap the 100 μF capacitor between pins 5 and 6 (8 and 9) can be omitted. Pins 6, 8 and 10 have to be interconnected.

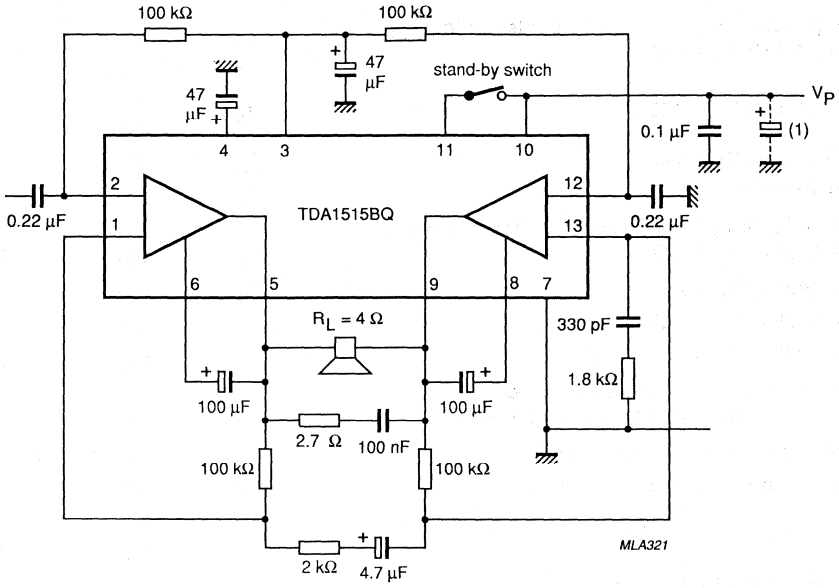


Fig. 3 Test/application circuit bridge tied load (BTL).

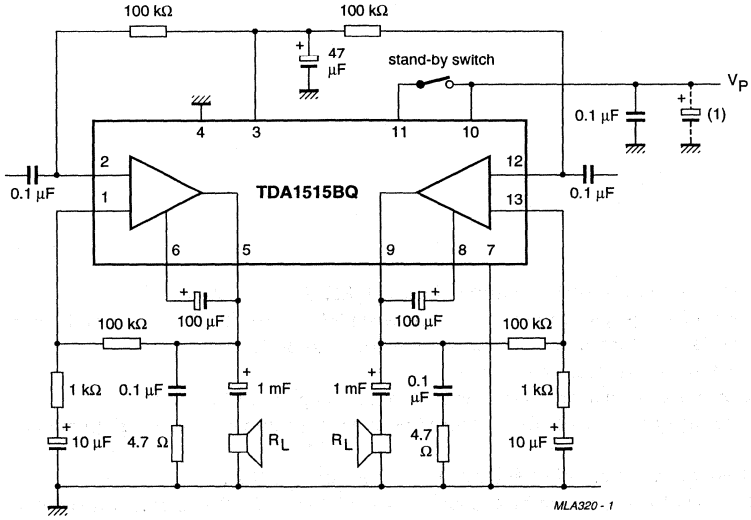


Fig. 4 Test/application circuit stereo.

1. Belongs to power supply.

24 W BTL OR 2 X 12 WATT STEREO CAR RADIO POWER AMPLIFIER

GENERAL DESCRIPTION

The TDA1516BQ is an integrated class-B output amplifier in a 13-lead single-in-line (SIL) plastic power package. The device is primarily developed for car radio applications.

FEATURES

- Requires very few external components
- Flexibility in use — stereo as well as mono BTL
- High output power (without bootstrap)
- Low offset voltage at output (important for BTL)
- Fixed gain
- Good ripple rejection
- Mute/stand-by switch
- Load dump protection
- A.C. and d.c. short-circuit-safe to ground and V_P
- Thermally protected
- Reverse polarity safe
- Capability to handle high energy on outputs (V_P = 0 V)
- No switch-on/switch-off plop
- Flexible leads
- Low thermal resistance
- Identical inputs (inverting and non-inverting)
- Compatible with TDA1518Q (except gain)

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage range						
operating		V_P	6,0	14,4	18,0	V
non-operating		V_P	–	–	30,0	V
load dump protected		V_P	–	–	45,0	V
Repetitive peak output current		I_{ORM}	–	–	4	A
Total quiescent current		I_{tot}	–	30	–	mA
Stand-by current		I_{sb}	–	0,1	100	μA
Switch-on current		I_{sw}	–	–	40	μA
Input impedance						
BTL		$\|Z_I\|$	25	–	–	kΩ
stereo		$\|Z_I\|$	50	–	–	kΩ
Stereo application						
Output power	THD = 10%; 4 Ω	P_o	–	6	–	W
	THD = 10%; 2 Ω	P_o	–	11	–	W
Channel separation		α	40	–	–	dB
Noise output voltage		$V_{no(rms)}$	–	50	–	μV
BTL application						
Output power	THD = 10%; 4 Ω	P_o	–	22	–	W
Supply voltage ripple rejection	R_S = 0 Ω; f = 100 Hz to 10 kHz	RR	48	–	–	dB
D.C. output offset voltage		$\|\Delta V_O\|$	–	–	100	mV

PACKAGE OUTLINE

13-lead SIL-bent-to-DIL; plastic power (SOT141).

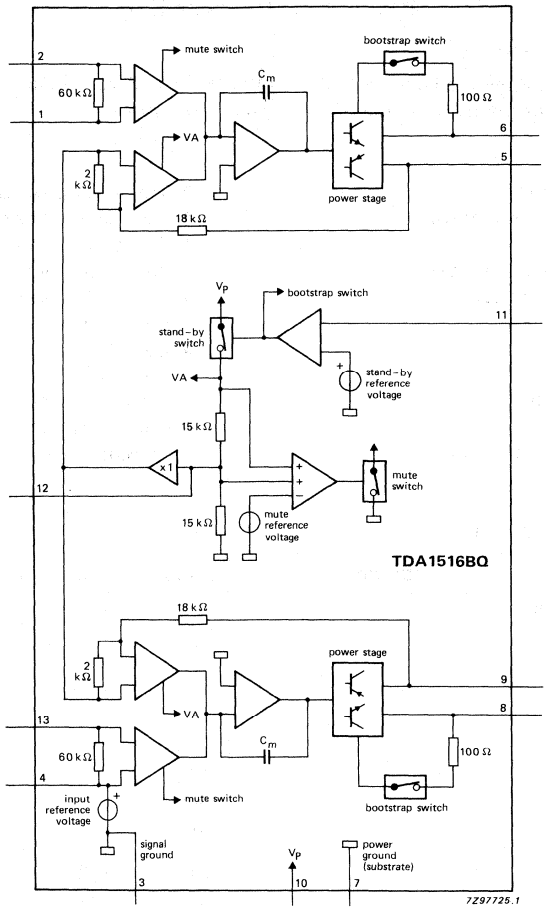


Fig. 1 Block diagram.

PINNING

1	−INV1	non-inverting input 1
2	INV	inverting input
3	GND1	ground (signal)
4	V_{ref}	reference voltage
5	OUT1	output 1
6	BS1	bootstrap 1
7	GND2	ground (substrate)
8	BS2	bootstrap 2
9	OUT2	output 2
10	V_P	supply voltage
11	M/SS	mute/stand-by switch
12	RR	supply voltage ripple rejection
13	−INV2	non-inverting input 2

FUNCTIONAL DESCRIPTION

The TDA1516BQ contains two identical amplifiers with differential input stages. This device can be used for stereo or bridge applications. The gain of each amplifier is fixed at 20 dB. A special feature of this device is the mute/stand-by switch which has the following features:

- low stand-by current ($< 100\ \mu A$)
- low mute/stand-by switching current (low cost supply switch)
- mute condition

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage					
operating		V_P	–	18	V
non-operating		V_P	–	30	V
load dump protected	during 50 ms; $t_r \geqslant 2{,}5$ ms	V_P	–	45	V
A.C. and d.c. short-circuit-safe voltage		V_{PSC}	–	18	V
Reverse polarity		V_{PR}	–	6	V
Energy handling capability at outputs	V_P = 0 V		–	200	mJ
Non-repetitive peak output current		I_{OSM}	–	6	A
Repetitive peak output current		I_{ORM}	–	4	A
Total power dissipation	see Fig. 2	P_{tot}	–	25	W
Crystal temperature		T_c	–	150	°C
Storage temperature range		T_{stg}	−55	+ 150	°C

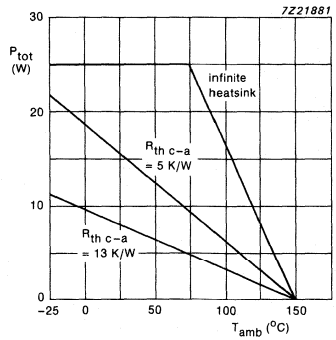


Fig. 2 Power derating curve.

D.C. CHARACTERISTICS (note 1)

V_P = 14,4 V; T_{amb} = 25 °C; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage range	note 2	V_P	6,0	14,4	18,0	V
Quiescent current		I_P	–	40	80	mA
D.C. output voltage at approximately Vp/2	note 3	V_O	–	6,8	–	V
D.C. output offset voltage		$\lvert\Delta V_{5\text{-}9}\rvert$	–	–	100	mV
Mute/stand-by switch						
Switch-on voltage level		V_{ON}	8,5	–	–	V
Mute condition		V_{mute}	3,0	–	6,4	V
Output signal in mute position	V_I = 1 V (max.); f = 20 Hz to 15 kHz	V_O	–	*	2	mV
D.C. output offset voltage		$\lvert\Delta V_{5\text{-}9}\rvert$	–	–	100	mV
Stand-by condition		V_{sb}	0	–	2	V
D.C. current in stand-by condition		I_{sb}	–	–	100	μA
Switch-on current		I_{sw}	–	12	40	μA

* Value to be fixed.

A.C. CHARACTERISTICS

V_P = 14,4 V; R_L = 4 Ω; f = 1 kHz; T_{amb} = 25 °C; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Stereo application	note 1					
Output power	note 4;					
	THD = 0,5%	P_o	4	5	–	W
	THD = 10%	P_o	5,5	6,0	–	W
	notes 4 and 5;					
	THD = 10%	P_o	6	7	–	W
Output power at	note 4;					
R_L = 2 Ω	THD = 0,5%	P_o	7.5	8,5	–	W
	THD = 10%	P_o	10	11	–	W
	notes 4 and 5;					
	THD = 10%	P_o	10,5	12,0	–	W
Low frequency roll-off	note 6;					
	−3 dB	f_L	–	45	–	Hz
High frequency roll-off	−1 dB	f_H	20	–	–	kHz
Closed loop voltage gain		G_v	19	20	21	dB
Supply voltage ripple rejection:	note 7					
ON		RR	48	–	–	dB
mute		RR	48	–	–	dB
stand-by		RR	80	–	–	dB
Input impedance		$\|Z_I\|$	50	60	75	kΩ
Noise output voltage:	note 8;					
ON	R_S = 0 Ω	$V_{no(rms)}$	–	50	–	μV
ON	R_S = 10 kΩ	$V_{no(rms)}$	–	70	100	μV
mute	note 9	$V_{no(rms)}$	–	50	–	μV
Channel separation	R_S = 10 kΩ	α	40	–	–	dB
Channel balance		G_v	–	–	1	dB

A.C. CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
BTL application	note 10					
Output power	THD =0,5%	P_o	15,5	17,0	–	W
	THD = 10%	P_o	20	22	–	W
	note 5; THD = 10%	P_o	21	24	–	W
Output power at V_P = 13,2 V	THD = 0,5%	P_o	–	13,5	–	W
	THD = 10%	P_o	–	17	–	W
	note 5; THD = 10%	P_o	–	19	–	W
Power bandwidth	THD = 0,5%; P_o = 15 W	B_w	–	20 to 15 000	–	Hz
Low frequency roll-off	note 6; –3 dB	f_L	–	25	–	Hz
High frequency roll-off	–1 dB	f_H	20	–	–	kHz
Closed loop voltage gain		G_v	25	26	27	dB
Supply voltage ripple rejection:	note 7					
ON		RR	48	–	–	dB
mute		RR	48	–	–	dB
stand-by		RR	80	–	–	dB
Input impedance		$\|Z_I\|$	25	30	38	kΩ
Noise output voltage	note 8;					
ON	R_S = 0 Ω	$V_{no(rms)}$	–	70	–	μV
ON	R_S = 10 kΩ	$V_{no(rms)}$	–	100	200	μV
mute	note 9	$V_{no(rms)}$	–	60	–	μV

Notes to the characteristics

1. All characteristics, for stereo application are measured using the circuit shown in Fig. 3.
2. The circuit is d.c. adjusted at V_P = 6 V to 18 V and a.c. operating at V_P = 8,5 to 18 V.
3. At 18 V $<$ V_P $<$ 30 V the d.c. output voltage $\leqslant V_P/2$.
4. Output power is measured directly at the output pins of the IC.
5. With bootstrap and a 100 kΩ resistor from pin 12 to the positive supply voltage (V_P), value of bootstrap capacitor is 47 μF.
6. Frequency response externally fixed.
7. Ripple rejection measured at the output with a source impedance of 0 Ω (maximum ripple amplitude of 2 V) and a frequency between 1 kHz and 10 kHz.
8. Noise voltage measured in a bandwidth of 20 Hz to 20 kHz.
9. Noise output voltage independent of R_S (V_I = 0 V).
10. All characteristics, for BTL application are measured using the circuit shown in Fig. 4.

APPLICATION INFORMATION

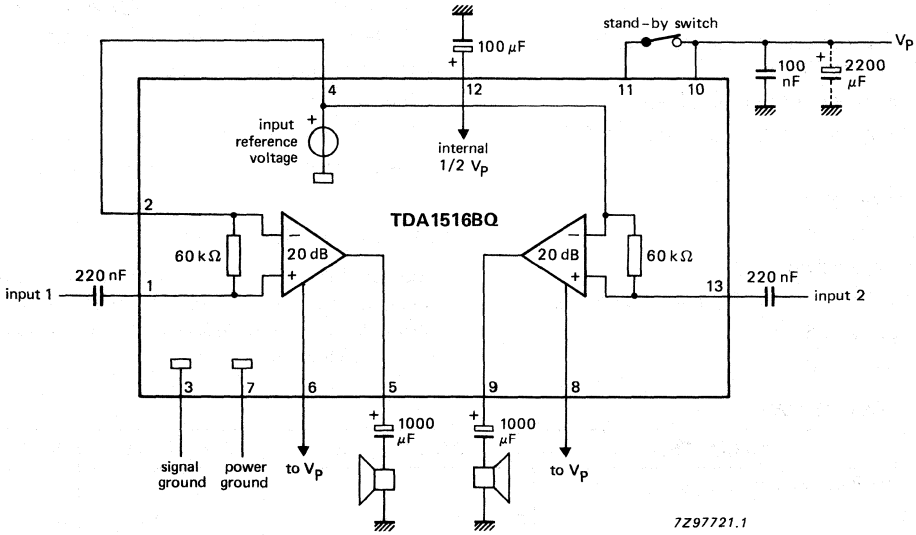


Fig. 3 Stereo application circuit diagram.

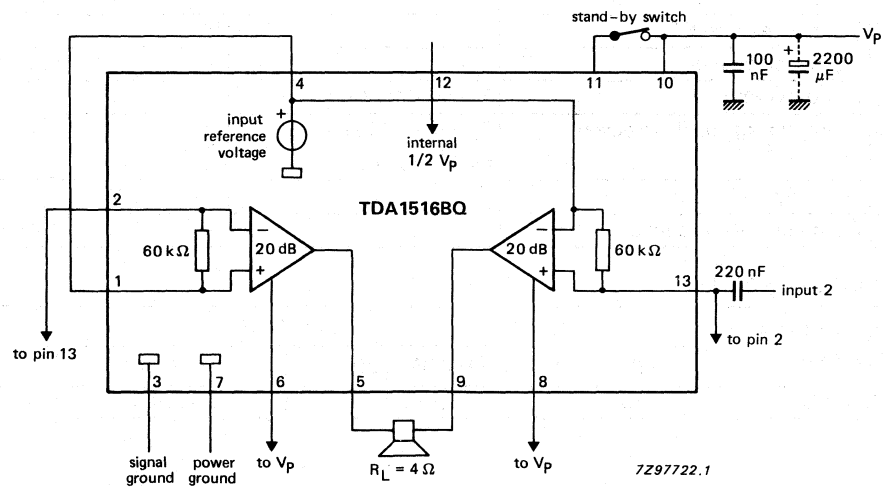


Fig. 4 BTL application circuit diagram (without bootstrapping).

24 W BTL car radio power amplifier TDA1516CQ

FEATURES

- Requires very few external components for Bridge-Tied-Load (BTL)
- High output power (without bootstrap)
- Low offset voltage at output (important for BTL)
- Fixed gain
- Good ripple rejection
- Mute/stand-by switch
- Load dump protection
- AC and DC short-circuit-safe to ground and V_P
- Thermally protected
- Reverse polarity safe
- Capability to handle high energy on outputs (V_P = 0)
- Protected against electrostatic discharge
- No switch-on/switch-off plop
- Flexible leads
- Low thermal resistance
- Identical inputs (inverting and non-inverting).

GENERAL DESCRIPTION

The TDA1516CQ is a monolithic integrated class-B output amplifier in a 13-lead single-in-line (SIL) plastic power package. The device is primarily developed for car radio applications.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	positive supply voltage range					
		operating	6.0	14.4	18	V
		non-operating	–	–	30	V
		load dump	–	–	45	V
I_{ORM}	repetitive peak output current		–	–	4	A
I_P	total quiescent current		–	40	80	mA
I_{sb}	stand-by current		–	0.1	100	µA
I_{sw}	switch-on current		–	–	60	µA
$\|Z_i\|$	input impedance BTL		25	–	–	kΩ
T_{XTAL}	crystal temperature		–	–	+150	°C
P_O	output power	THD = 10%; 4 Ω	–	22	–	W
SVRR	supply voltage ripple rejection	R_S = 0; f = 100 Hz	45	–	–	dB
		f = 1 to 10 kHz	48	–	–	dB
V_{no}	noise output voltage		–	70	–	µV
$\|\Delta V_{os}\|$	DC output offset voltage		–	–	100	mV

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA1516CQ	13	DIL	plastic	SOT141

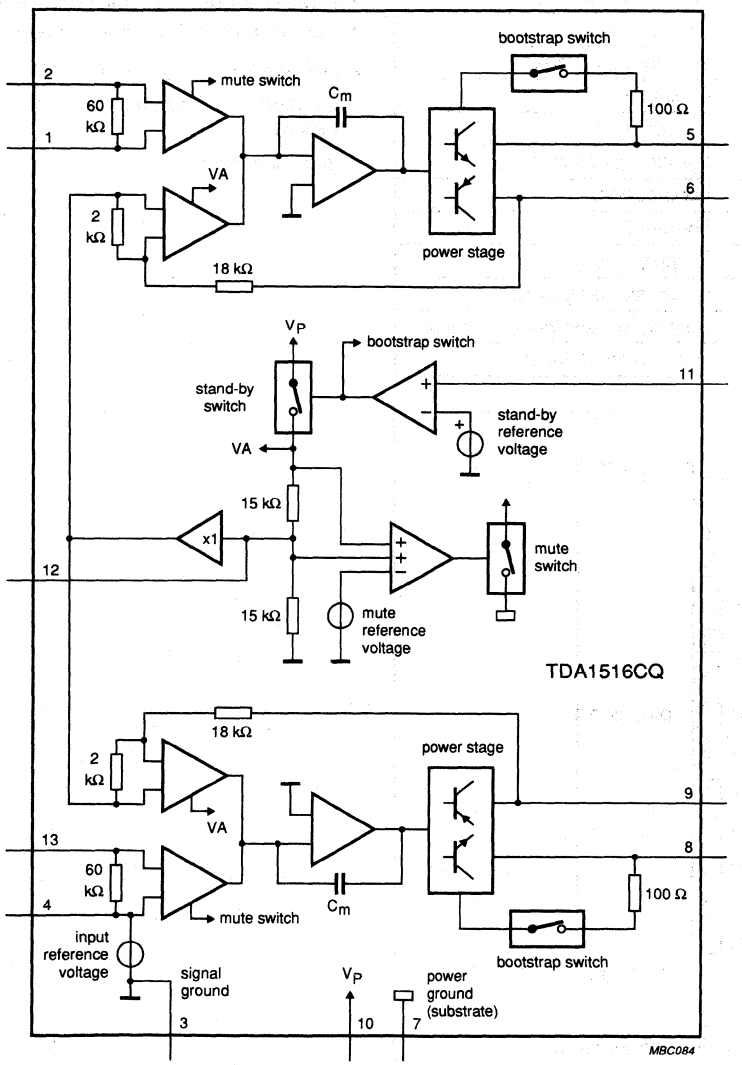


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
–INV1	1	non-inverting input 1
INV	2	inverting input
GND1	3	ground (signal)
V_{ref}	4	reference voltage
OUT1	5	output 1
BS1	6	bootstrap 1
GND2	7	ground (substrate)
BS2	8	bootstrap 2
OUT2	9	output 2
V_P	10	supply voltage
M/SB	11	mute/stand-by switch
RR	12	supply voltage ripple rejection
–INV2	13	non-inverting input 2

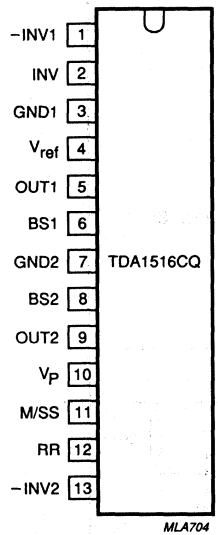


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The TDA1516CQ contains two identical amplifiers with differential input stages. It can be used for bridge applications. The gain of each amplifier is fixed at 20 dB. A special feature of this device is the mute/stand-by switch, which has the following features:

- low stand-by current (< 100 μA)
- low mute/stand-by switching current (low cost supply switch)
- mute condition.

LIMITING VALUES

In accordance with the Absolute maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_P	supply voltage				
		operating	–	18	V
		non-operating	–	30	V
		load dump protected; during 50 ms; rise time ≥ 2.5 ms	–	45	V
V_{PSC}	AC and DC short-circuit safe voltage		–	18	V
V_{PR}	reverse polarity		–	6	V
	energy handling capability at outputs	$V_P = 0$	–	200	mJ
I_{OSM}	non-repetitive peak output current		–	6	A
I_{ORM}	repetitive peak output current		–	4	A
P_{tot}	total power dissipation	$T_{case} < 75$ °C; (see Fig.3)	–	25	W
T_{stg}	storage temperature range		–55	+150	°C
T_{vj}	virtual junction temperature		–	+150	°C

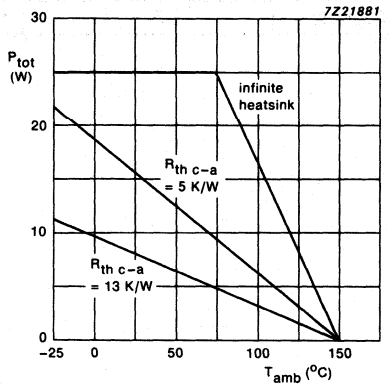


Fig.3 Power derating curve.

DC CHARACTERISTICS

V_P = 14.4 V; T_{amb} = 25 °C; unless otherwise specified. See note 1.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_P	positive supply voltage range	note 2	6.0	14.4	18	V
I_P	quiescent current		–	40	80	mA
V_O	DC output voltage	note 3	–	6.8	–	V
$\lvert\Delta V_{os}\rvert$	DC output offset voltage (pins 5 and 9)		–	–	100	mV
Mute/stand-by switch						
V_{sw}	switch-on voltage level		8.5	–	–	V
MUTE CONDITION						
V_{mute}	mute voltage		3.3	–	6.4	V
V_O	output signal in mute position	V_I = 1 V (max); f = 20 Hz to 10 kHz	–	–	2	mV
$\lvert\Delta V_{os}\rvert$	DC output offset voltage (pins 5 and 9)		–	–	100	mV
STAND-BY CONDITION						
V_{sb}	stand-by voltage		0	–	2	V
I_{sb}	DC standby current	$V_{11} \leq 0.5$ V	–	–	100	µA
		$0.5 < V_{11} \leq 2$ V	–	–	500	µA
I_{sw}	switch-on current	$V_{11} \leq V_{10}$; note 4	–	25	60	µA
I_P	supply current	short-circuit to GND; note 5	–	5.5	–	mA

AC CHARACTERISTICS

V_P = 14.4 V; R_L = 4 Ω; f = 1 kHz; T_{amb} = 25 °C; unless otherwise specified. See note 1.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
P_O	output power	THD = 0.5%	15	17	–	W
		THD = 10%	20	22	–	W
		THD = 10%; note 6	21	24	–	W
		V_P = 13.2 V; THD = 0.5%	–	13.5	–	W
		V_P = 13.2 V; THD = 10%	–	17	–	W
		V_P = 13.2 V; THD = 10%; note 6	–	19	–	W
THD	total harmonic distortion	P_O = 1 W	–	0.05	–	%
B	power bandwidth	THD = 0.5%; P_O = −1 dB with respect to 15 W	–	20 to 15 000	–	Hz
f_{low}	low frequency roll-off	−3 dB; note 7	–	25	–	Hz
f_{high}	high frequency roll-off	−1 dB	20	–	–	kHz
G_v	closed loop voltage gain		25	26	27	dB
SVRR	supply voltage ripple rejection					
		ON; notes 8 and 9	45	–	–	dB
		ON; notes 8 and 10	48	–	–	dB
		MUTE; notes 8 to 10	48	–	–	dB
		stand-by; notes 8 to 10	80	–	–	dB
$\|Z_I\|$	input impedance		25	30	38	kΩ
V_{no}	noise output voltage					
		ON; R_S = 0; note 11	–	70	–	μV
		R_S = 10 kΩ; note 12	–	100	200	μV
		MUTE; note 12	–	60	–	μV

Notes to the characteristics

1. All characteristics are measured using the circuit shown in Fig.4
2. The circuit is DC adjusted at V_P = 6 to 18 V and AC operating at V_P = 8.5 to 18 V
3. At 18 V < V_P < 30 V, the DC output voltage ≤ $V_P/2$
4. If $V_{11} > V_{10}$, then I_{11} must be ≤ 10 mA
5. Conditions: V_{11} = 0; short-circuit output to GND; switch V_{11} to mute or on condition (rise time V_{11} > 10 μs)
6. With bootstrap and a resistor of 100 kΩ from $V_P/2$ to the positive supply voltage (V_P). (Bootstrap capacitor of 47 μF)
7. Frequency response externally fixed
8. Ripple rejection measured at the output with a source-impedance of 0 Ω (max. ripple amplitude of 2 V)
9. Frequency = 100 Hz
10. Frequency = 1 to 10 kHz
11. Noise voltage measured in a bandwidth of 20 Hz to 20 kHz
12. Noise output voltage independent of R_S (V_{in} = 0)

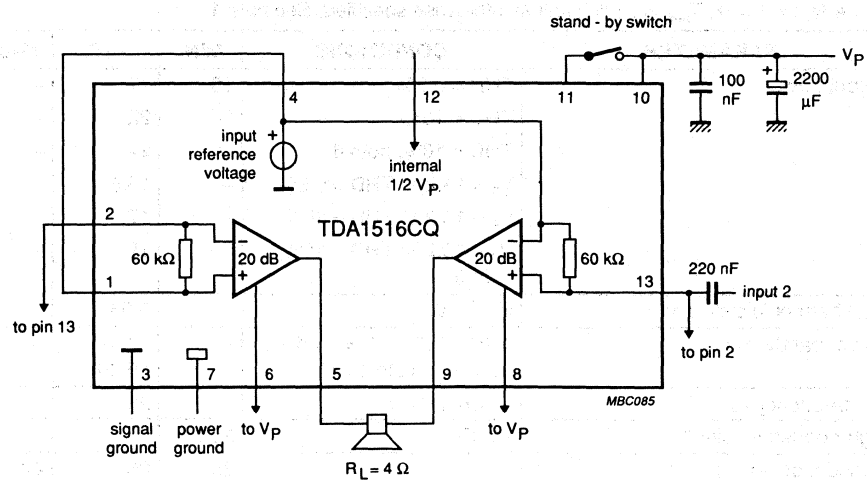


Fig.4 Application diagram.

2 × 6 WATT STEREO CAR RADIO POWER AMPLIFIER

GENERAL DESCRIPTION

The TDA1517 is an integrated class-B dual output amplifier in a 9-lead single-in-line (SIL) plastic medium power package. The device is primarily developed for car radio applications.

Features

- Requires very few external components
- High output power
- Fixed gain
- Good ripple rejection
- Mute/stand-by switch
- Load dump protection
- AC and DC short-circuit-safe to ground and V_P
- Thermally protected
- Reverse polarity safe
- Capability to handle high energy on outputs (V_P = 0 V)
- No switch-on/switch-off plop
- Protected against electrostatic discharge
- Compatible with TDA1519 (except gain)

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage range						
operating		V_P	6,0	14,4	18,0	V
non-operating		V_P	–	–	30,0	V
load dump protected		V_P	–	–	45,0	V
Repetitive peak output current		I_{ORM}	–	–	2,5	A
Total quiescent current		I_{tot}	–	40	80	mA
Stand-by current		I_{sb}	–	0,1	100	μA
Switch-on current		I_{sw}	–	–	40	μA
Input impedance		$\|Z_I\|$	50	–	–	kΩ
Output power	THD = 0,5%; 4 Ω	P_o	–	5	–	W
	THD = 10%; 4 Ω	P_o	–	6	–	W
Channel separation		α	40	–	–	dB
Noise output voltage		$V_{no(rms)}$	–	50	–	μV
Supply voltage ripple rejection	f = 100 Hz to 100 kHz	SVRR	48	–	–	dB
Crystal temperature		T_c	–	–	150	°C

PACKAGE OUTLINE

9-lead SIL-bent-to-DIL; plastic (SOT110B).

PINNING

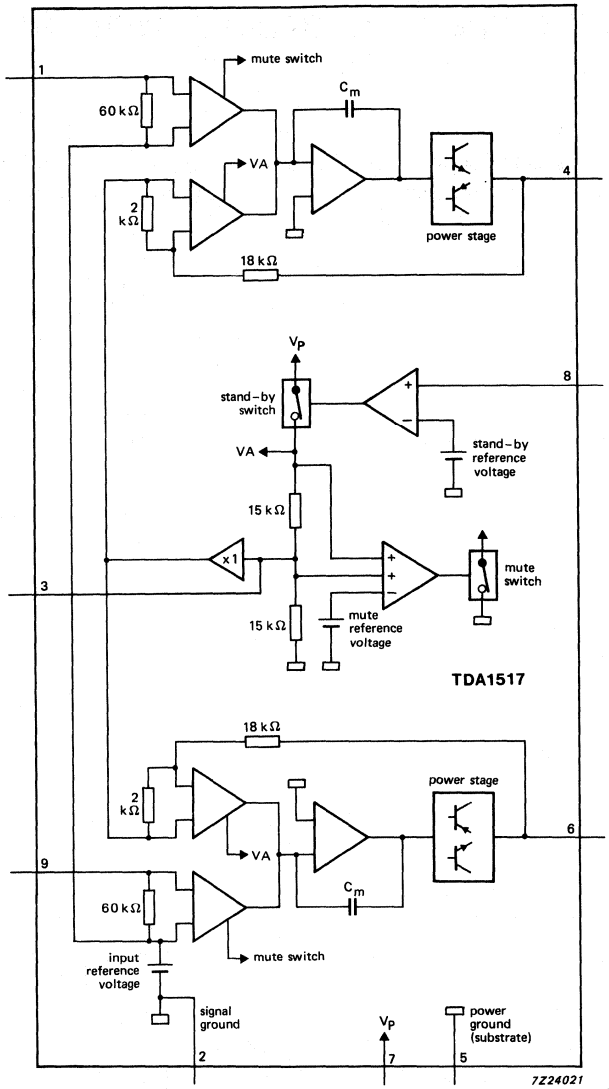


Fig. 1 Block diagram.

1	−INV1	non-inverting input 1
2	GND1	ground (signal)
3	SVRR	supply voltage ripple rejection
4	OUT1	output 1
5	GND2	ground (substrate)
6	OUT2	output 2
7	V_P	supply voltage
8	M/SS	mute/stand-by switch
9	−INV2	non-interting input 2

FUNCTIONAL DESCRIPTION

The TDA1517 contains two identical amplifiers with differential input stages. The gain of each amplifier is fixed at 20 dB. A special feature of this device is the mute/stand-by switch which has the following features:

- low stand-by current ($< 100\ \mu A$)
- low mute/stand-by switching current (low cost supply switch)
- mute condition

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage					
operating		V_P	–	18	V
non-operating		V_P	–	30	V
load dump protected	during 50 ms; $t_r \geqslant 2{,}5$ ms	V_P	–	45	V
AC and DC short-circuit-safe voltage		V_{PSC}	–	18	V
Reverse polarity		V_{PR}	–	6	V
Energy handling capability at outputs	$V_P = 0$ V		–	200	mJ
Non-repetitive peak output current		I_{OSM}	–	4	A
Repetitive peak output current		I_{ORM}	–	2,5	A
Total power dissipation	see Fig. 2	P_{tot}	–	15	W
Crystal temperature		T_c	–	150	°C
Storage temperature range		T_{stg}	−55	+150	°C

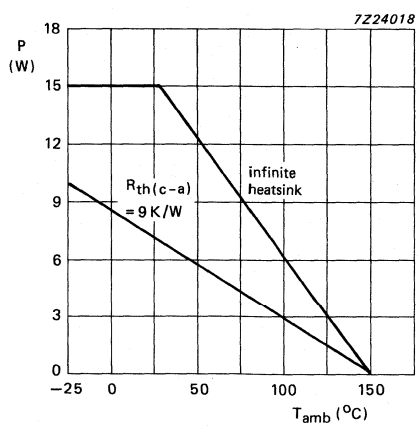


Fig. 2 Power derating curve.

DC CHARACTERISTICS (note 1)

V_P = 14,4 V; T_{amb} = 25 °C; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage range	note 2	V_P	6,0	14,4	18,0	V
Quiescent current		I_P	–	40	80	mA
DC output voltage	note 3	V_O	–	6,95	–	V
Mute/stand-by switch	see Fig. 3					
Switch-on voltage level		V_{ON}	8,5	–	–	V
Mute condition		V_{mute}	3,3	–	6,4	V
Output signal in mute position	V_I = 1 V (max); f = 20 Hz to 15 kHz	V_O	–	–	2	mV
Stand-by condition		V_{sb}	0	–	2	V
DC current in stand-by condition		I_{sb}	–	–	100	μA
Switch-on current		I_{sw}	–	12	40	μA

AC CHARACTERISTICS (note 1)

V_P = 14,4 V; R_L = 4 Ω; f = 1 kHz; T_{amb} = 25 °C; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Output power	note 4;					
	THD = 0,5%	P_o	4	5	–	W
	THD = 10%	P_o	5,5	6,0	–	W
Total harmonic distortion	P_o = 1 W	THD	–	0,1	–	%
Low frequency roll-off	note 5; –3 dB	f_L	–	45	–	Hz
High frequency roll-off	–1 dB	f_H	20	–	–	kHz
Closed loop voltage gain		G_v	19	20	21	dB
Supply voltage ripple rejection:	note 6					
ON		SVRR	48	–	–	dB
mute		SVRR	48	–	–	dB
stand-by		SVRR	80	–	–	dB
Input impedance		$\|Z_i\|$	50	60	75	kΩ
Noise output voltage:	note 7;					
ON	R_S = 0 Ω	$V_{no(rms)}$	–	50	–	μV
ON	R_S = 10 kΩ	$V_{no(rms)}$	–	70	100	μV
mute	note 8	$V_{no(rms)}$	–	50	–	μV
Channel separation	R_S = 10 kΩ	α	40	–	–	dB
Channel balance		$\|\Delta G_v\|$	–	0,1	1	dB

Notes to the characteristics

1. All characteristics are measured using the circuit shown in Fig. 4.
2. The circuit is DC adjusted at V_P = 6 V to 18 V and AC operating at V_P = 8,5 V to 18 V.
3. At 18 V $< V_P <$ 30 V the DC output voltage $\leqslant V_P/2$.
4. Output power is measured directly at the output pins of the IC.
5. Frequency response externally fixed.
6. Ripple rejection measured at the output with a source impedance of 0 Ω (maximum ripple amplitude of 2 V) and a frequency between 100 Hz and 10 kHz.
7. Noise voltage measured in a bandwidth of 20 Hz to 20 kHz.
8. Noise output voltage independent of R_S (V_I = 0 V).

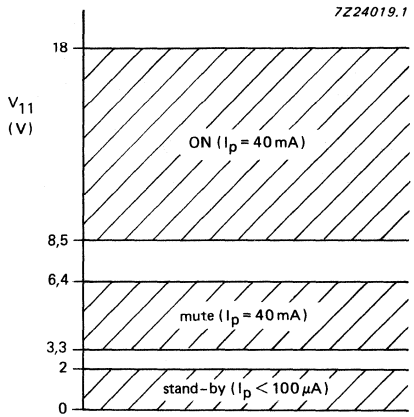


Fig. 3 Stand-by, mute and ON conditions.

APPLICATION INFORMATION

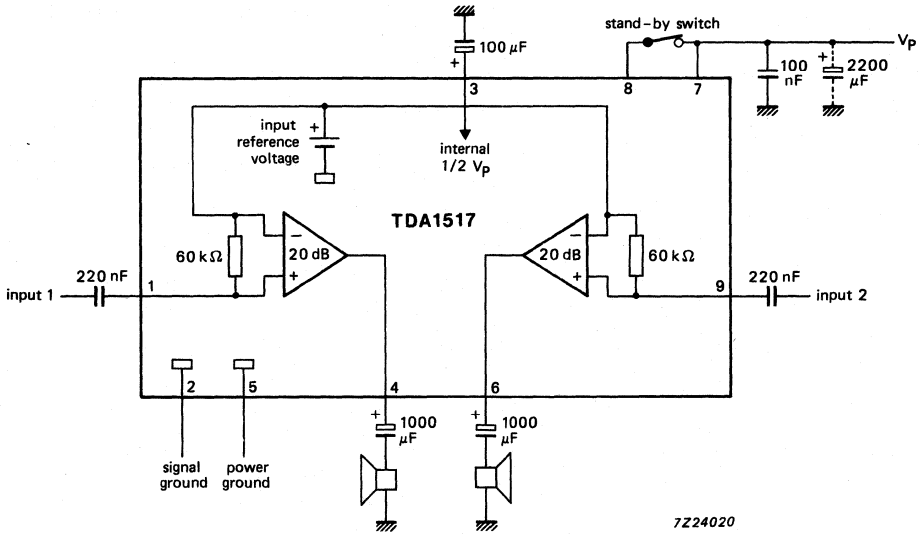


Fig. 4 Application circuit diagram.

24 W BTL OR 2 X 12 WATT STEREO CAR RADIO POWER AMPLIFIER

GENERAL DESCRIPTION

The TDA1518BQ is an integrated class-B output amplifier in a 13-lead single-in-line (SIL) plastic power package. The device is primarily developed for car radio applications.

FEATURES

- Requires very few external components
- Flexibility in use – stereo as well as mono BTL
- High output power (without bootstrap)
- Low offset voltage at output (important for BTL)
- Fixed gain
- Good ripple rejection
- Mute/stand-by switch
- Load dump protection
- A.C. and d.c. short-circuit-safe to ground and V_P
- Thermally protected
- Reverse polarity safe
- Capability to handle high energy on outputs (V_P = 0 V)
- No switch-on/switch-off plop
- Flexible leads
- Low thermal resistance
- Identical inputs (inverting and non-inverting)
- Compatible with TDA1516BQ (except gain)

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage range						
operating		V_P	6,0	14,4	18,0	V
non-operating		V_P	–	–	30,0	V
load dump		V_P	–	–	45,0	V
Repetitive peak output current		I_{ORM}	–	–	4	A
Total quiescent current		I_{tot}	–	30	–	mA
Stand-by current		I_{sb}	–	0,1	100	μA
Switch-on current		I_{sw}	–	–	40	μA
Input impedance						
BTL		$\|Z_I\|$	25	–	–	kΩ
stereo		$\|Z_I\|$	50	–	–	kΩ
Stereo application						
Output power	THD = 10%; 4 Ω	P_o	–	6	–	W
	THD = 10%; 2 Ω	P_o	–	11	–	W
Channel separation		α	40	–	–	dB
Noise output voltage		$V_{no(rms)}$	–	150	–	μV
BTL application						
Output power	THD = 10%; 4 Ω	P_o	–	22	–	W
Supply voltage ripple rejection	R_S = 0 Ω; f = 100 Hz to 10 kHz	RR	48	–	–	dB
D.C. output offset voltage		$\|\Delta V_O\|$	–	–	250	mV

PACKAGE OUTLINE

13-lead SIL-bent-to-DIL; plastic power (SOT141C).

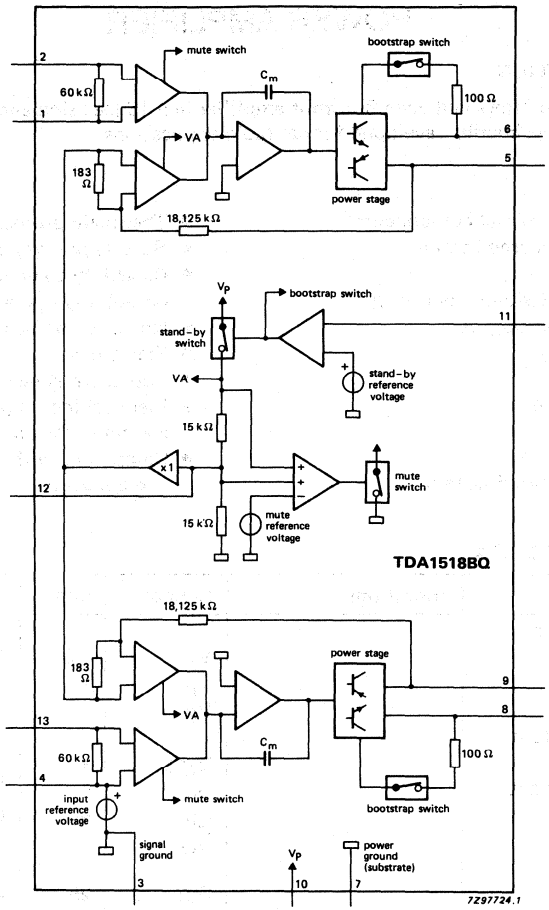


Fig. 1 Block diagram.

PINNING

1	−INV1	non-inverting input 1
2	INV	inverting input
3	GND1	ground (signal)
4	V_{ref}	reference voltage
5	OUT1	output 1
6	BS1	bootstrap 1
7	GND2	ground (substrate)
8	BS2	bootstrap 2
9	OUT2	output 2
10	V_P	supply voltage
11	M/SS	mute/stand-by switch
12	RR	supply voltage ripple rejection
13	−INV2	non-inverting input 2

FUNCTIONAL DESCRIPTION

The TDA1518BQ contains two identical amplifiers with differential input stages. This device can be used for stereo or bridge applications. The gain of each amplifier is fixed at 40 dB. A special feature of this device is the mute/stand-by switch which has the following features:

- low stand-by current ($< 100\ \mu A$)
- low mute/stand-by switching current (low cost supply switch)
- mute condition

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage					
operating		V_P	–	18	V
non-operating		V_P	–	30	V
load dump	during 50 ms; $t_r \geqslant 2{,}5$ ms	V_P	–	45	V
A.C. and d.c. short-circuit-safe voltage		V_{PSC}	–	18	V
Reverse polarity		V_{PR}	–	6	V
Energy handling capability at outputs	$V_P = 0$ V		–	200	mJ
Non-repetitive peak output current		I_{OSM}	–	6	A
Repetitive peak output current		I_{ORM}	–	4	A
Total power dissipation	see Fig. 2	P_{tot}	–	25	W
Crystal temperature		T_c	–	150	°C
Storage temperature range		T_{stg}	–55	+ 150	°C

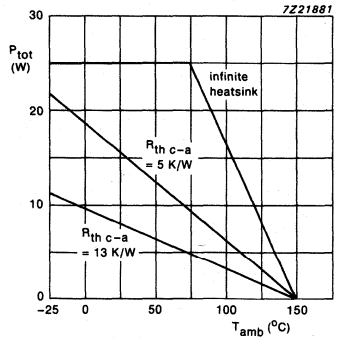


Fig. 2 Power derating curve.

D.C. CHARACTERISTICS (note 1)

V_P = 14.4 V; T_{amb} = 25 °C; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage range	note 2	V_P	6,0	14,4	18,0	V
Quiescent current		I_P	–	30	*	mA
D.C. output voltage at approximately $V_P/2$	note 3	V_O	–	6,8	–	V
D.C. output offset voltage		$\lvert\Delta V_{5\text{-}9}\rvert$	–	–	200	mV
Mute/stand-by switch						
Switch-on voltage level		V_{ON}	8,5	–	–	V
Mute condition		V_{mute}	3,0	–	6,4	V
Output signal in mute position	V_I = 1 V (max.); f = 20 Hz to 15 kHz	V_O	–	*	20	mV
D.C. output offset voltage		$\lvert\Delta V_{5\text{-}9}\rvert$	–	–	250	mV
Stand-by condition		V_{sb}	0	–	2	V
D.C. current in stand-by condition		I_{sb}	–	–	100	μA
Switch-on current		I_{sw}	–	12	40	μA

* Value to be fixed.

A.C. CHARACTERISTICS

V_P = 14,4 V; R_L = 4 Ω; f = 1 kHz; T_{amb} = 25 °C; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Stereo application	note 1					
Output power	note 4;					
	THD = 0,5%	P_o	4	5	–	W
	THD = 10%	P_o	5,5	6,0	–	W
	notes 4 and 5;					
	THD = 10%	P_o	6	7	–	W
Output power at	note 4;					
R_L = 2 Ω	THD = 0,5%	P_o	7,75	8,5	–	W
	THD = 10%	P_o	10	11	–	W
	notes 4 and 5;					
	THD = 10%	P_o	10,5	12,0	–	W
Low frequency roll-off	note 6;					
	−3 dB	f_L	–	45	–	Hz
High frequency roll-off	−1 dB	f_H	20	–	–	kHz
Closed loop voltage gain		G_v	39	40	41	dB
Supply voltage ripple rejection:	note 7					
ON		RR	48	–	–	dB
mute		RR	48	–	–	dB
stand-by		RR	80	–	–	dB
Input impedance		$\|Z_I\|$	50	60	75	kΩ
Noise output voltage:	note 8;					
ON	R_S = 0 Ω	$V_{no(rms)}$	–	150	–	μV
ON	R_S = 10 kΩ	$V_{no(rms)}$	–	250	500	μV
mute	note 9	$V_{no(rms)}$	–	120	–	μV
Channel separation	R_S = 10 kΩ	α	40	–	–	dB
Channel balance		G_v	–	0.1	1	dB

A.C. CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
BTL application	note 10					
Output power	THD = 0,5%	P_o	15,5	17,0	–	W
	THD = 10%	P_o	20	22	–	W
	note 5; THD = 10%	P_o	21	24	–	W
Output power at V_P = 13,2 V	THD = 0,5%	P_o	–	13.5	–	W
	THD = 10%	P_o	–	17	–	W
	note 5; THD = 10%	P_o	–	19	–	W
Power bandwidth	THD = 0,5%; P_o = 15 W	B_w	–	20 to 15 000	–	Hz
Low frequency roll-off	note 6; –3 dB	f_L	–	45	–	Hz
High frequency roll-off	–1 dB	f_H	20	–	–	kHz
Closed loop voltage gain		G_v	45	46	47	dB
Supply voltage ripple rejection:	note 7					
ON		RR	48	–	–	dB
mute		RR	48	–	–	dB
stand-by		RR	80	–	–	dB
Input impedance		$\|Z_I\|$	25	30	38	kΩ
Noise output voltage:	note 8;					
ON	R_S = 0 Ω	$V_{no(rms)}$	–	200	–	μV
ON	R_S = 10 kΩ	$V_{no(rms)}$	–	350	700	μV
mute	note 9	$V_{no(rms)}$	–	120	–	μV
Switch-on/switch-off behaviour		dV/dt	–	–	*	V/ms

Notes to the characteristics

1. All characteristics, for stereo application are measured using the circuit shown in Fig. 3.
2. The circuit is d.c. adjusted at V_P = 6 V to 18 V and a.c. operating at V_P = 8,1 V to 18 V.
3. At 18 V $<$ V_P $<$ 30 V the d.c. output voltage $\leqslant V_P/2$.
4. Output power is measured directly at the output pins of the IC.
5. With bootstrap and a 100 kΩ resistor from pin 12 to the positive supply voltage (V_P), value of bootstrap capacitor is 47 μF.
6. Frequency response externally fixed.
7. Ripple rejection measured at the output with a source impedance of 0 Ω (maximum ripple amplitude of 2 V) and a frequency between 1 kHz and 10 kHz.
8. Noise voltage measured in a bandwidth of 20 Hz to 20 kHz.
9. Noise output voltage independent of R_S (V_I = 0 V).
10. All characteristics, for BTL application are measured using the circuit shown in Fig. 4.

* Value to be fixed.

APPLICATION INFORMATION

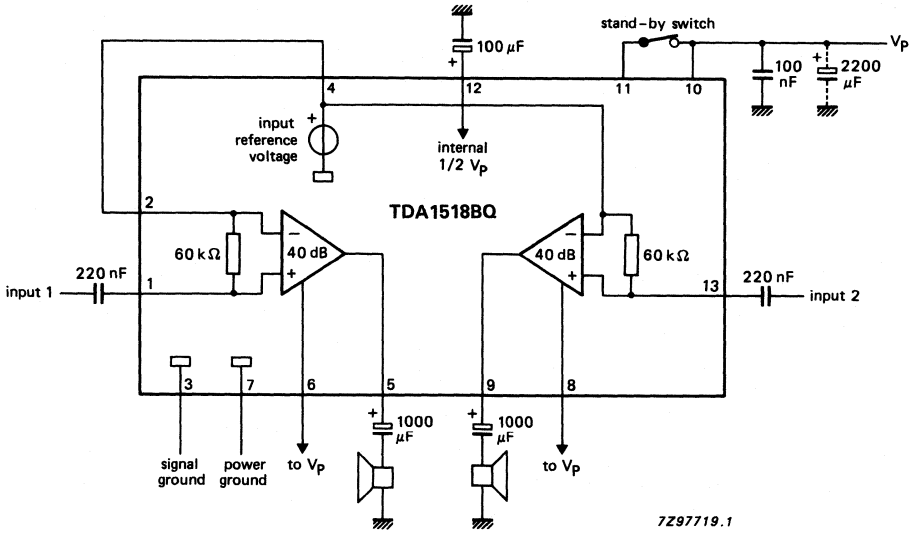


Fig. 3 Stereo application circuit diagram.

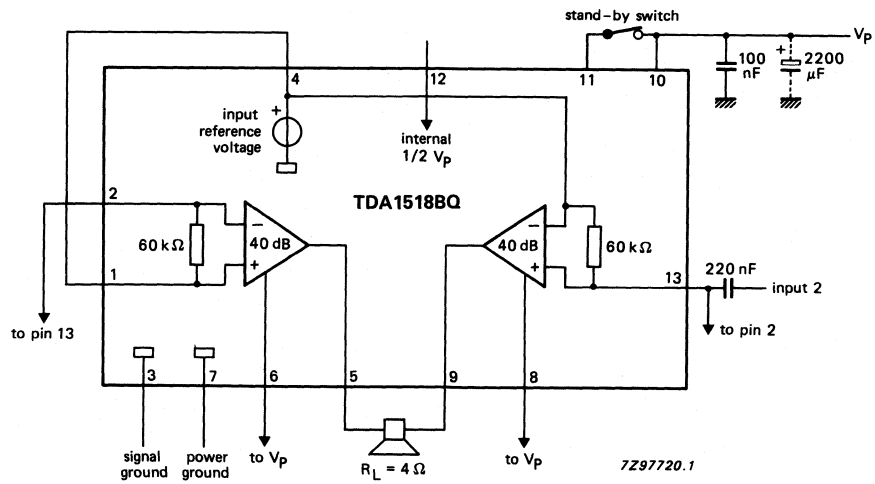


Fig. 4 BTL application circuit diagram (without bootstrapping).

2 × 6 WATT STEREO CAR RADIO POWER AMPLIFIER

GENERAL DESCRIPTION

The TDA1519 is an integrated class-B dual output amplifier in a 9-lead single in-line (SIL) plastic medium power package. The device is primarily developed for car radio applications.

Features

- Requires very few external components
- High output power
- Fixed gain
- Good ripple rejection
- Mute/stand-by switch
- Load dump protection
- AC and DC short-circuit-safe to ground and V_P
- Thermally protected
- Reverse polarity safe
- Capability to handle high energy on outputs (V_P = 0 V)
- No switch-on/switch-off plop
- Protected against electrostatic discharge
- Compatible with TDA1517 (except gain)

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage range						
operating		V_P	6,0	14,4	18,0	V
non-operating		V_P	–	–	30	V
load dump protected		V_P	–	–	45	V
Repetitive peak output current		I_{ORM}	–	–	2,5	A
Total quiescent current		I_{tot}	–	40	80	mA
Stand-by current		I_{sb}	–	0,1	100	μA
Switch-on current		I_{sw}	–	–	40	μA
Input impedance		$\|Z_I\|$	50	–	–	kΩ
Output power	THD = 0,5%; 4 Ω	P_o	–	5	–	W
	THD = 10%; 4 Ω	P_o	–	6	–	W
Channel separation		α	40	–	–	dB
Noise output voltage		$V_{no(rms)}$	–	150	–	μV
Supply voltage ripple rejection	f = 100 Hz	SVRR	40	–	–	dB
	f = 1 kHz to 10 kHz	SVRR	48	–	–	dB
Crystal temperature		T_c	–	–	150	°C

PACKAGE OUTLINE

9-lead SIL-bent-to-DIL; plastic (SOT110B).

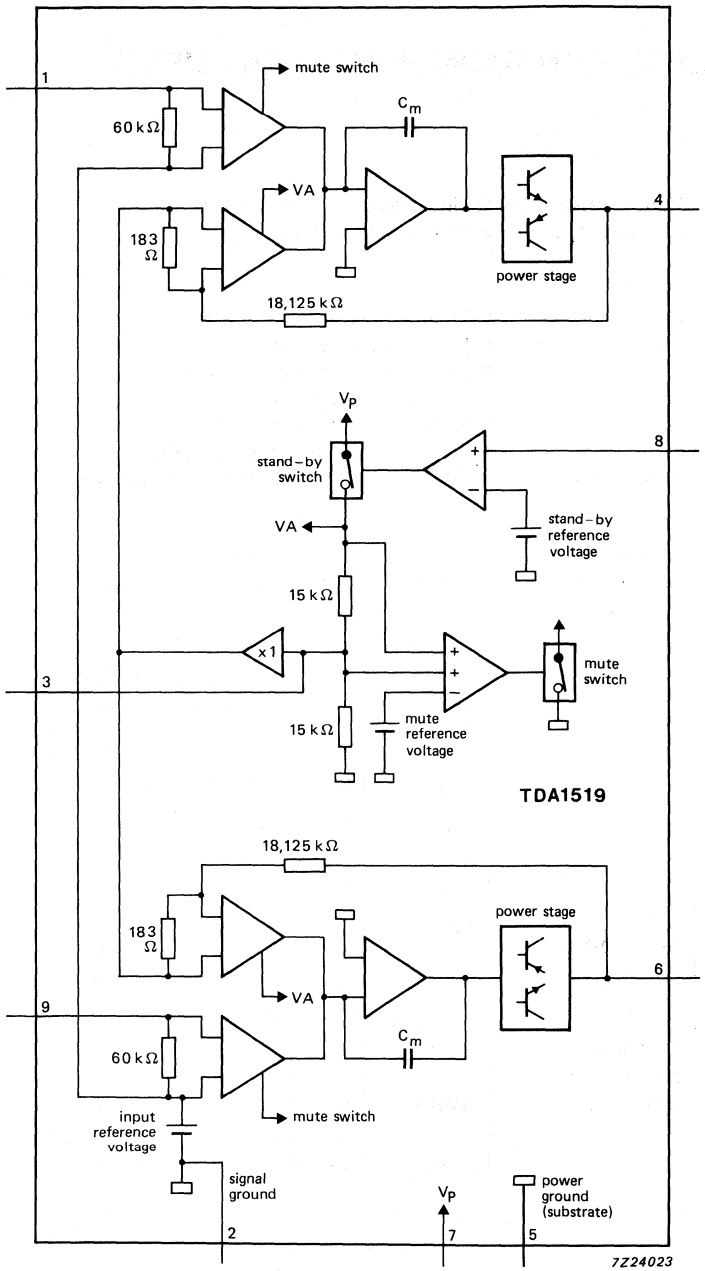


Fig. 1 Block diagram.

PINNING

1	INV1	non-inverting input 1
2	GND1	ground (signal)
3	SVRR	supply voltage ripple rejection
4	OUT1	output 1
5	GND2	ground (substrate)
6	OUT2	output 2
7	V_P	supply voltage
8	M/SS	mute/stand-by switch
9	−INV2	non-inverting input 2

FUNCTIONAL DESCRIPTION

The TDA1519 contains two identical amplifiers with differential input stages. The gain of each amplifier is fixed at 40 dB. A special feature of this device is the mute/stand-by switch which has the following features:

- low stand-by current ($< 100\ \mu A$)
- low mute/stand-by switching current (low cost supply switch)
- mute condition

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage					
operating		V_P	–	18	V
non-operating		V_P	–	30	V
load dump protected	during 50 ms; $t_r \geqslant 2{,}5$ ms	V_P	–	45	V
AC and DC short-circuit-safe voltage		V_{PSC}	–	18	V
Reverse polarity		V_{PR}	–	6	V
Energy handling capability at outputs	$V_P = 0$ V		–	200	mJ
Non-repetitive peak output current		I_{OSM}	–	4	A
Repetitive peak output current		I_{ORM}	–	2,5	A
Total power dissipation	see Fig. 2	P_{tot}	–	15	W
Crystal temperature		T_c	–	150	°C
Storage temperature range		T_{stg}	−55	+ 150	°C

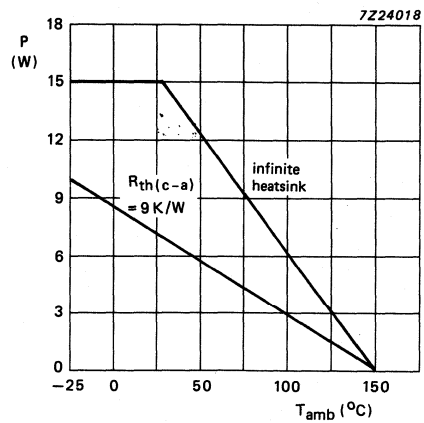


Fig. 2 Power derating curve.

DC CHARACTERISTICS (note 1)

V_P = 14,4 V; T_{amb} = 25 °C; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage range	note 2	V_P	6,0	14,4	18,0	V
Quiescent current		I_P	–	40	80	mA
DC output voltage	note 3	V_O	–	6,95	–	V
Mute/stand-by switch						
Switch-on voltage level	see Fig. 3	V_{ON}	8,5	–	–	V
Mute condition		V_{mute}	3,3	–	6,4	V
Output signal in mute position	V_I = 1 V (max.); f = 20 Hz to 15 kHz	V_O	–	–	20	mV
Stand-by condition		V_{sb}	0	–	2	V
DC current in stand-by condition		I_{sb}	–	–	100	μA
Switch-on current		I_{sw}	–	12	40	μA

AC CHARACTERISTICS (note 1)

V_P = 14,4 V; R_L = 4 Ω; f = 1 kHz; T_{amb} = 25 °C; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Output power	note 4;					
	THD = 0,5%	P_o	4	5	–	W
	THD = 10%	P_o	5,5	6,0	–	W
Total harmonic distortion	P_o = 1 W	THD	–	0,1	–	%
Low frequency roll-off	note 5;					
	–3 dB	f_L	–	45	–	Hz
High frequency roll-off	–1 dB	f_H	20	–	–	kHz
Closed loop voltage gain		G_v	39	40	41	dB
Supply voltage ripple rejection	note 6					
ON	f = 100 Hz	SVRR	40	–	–	dB
ON	f = 10 Hz to 10 kHz	SVRR	48	–	–	dB
mute		SVRR	48	–	–	dB
stand-by		SVRR	80	–	–	dB
Input impedance		$\|Z_i\|$	50	60	75	kΩ
Noise output voltage	note 7;					
ON	R_S = 0 Ω	$V_{no(rms)}$	–	150	–	μV
ON	R_S = 10 kΩ	$V_{no(rms)}$	–	250	500	μV
mute	note 8	$V_{no(rms)}$	–	120	–	μV
Channel separation	R_S = 10 kΩ	α	40	–	–	dB
Channel balance		$\|\Delta G_v\|$	–	0,1	1	dB

Notes to the characteristics

1. All characteristics are measured using the circuit shown in Fig. 4.
2. The circuit is DC adjusted at V_P = 6 V to 18 V and AC operating at V_P = 8,5 V to 18 V.
3. At 18 V < V_P < 30 V the DC output voltage ⩽ $V_P/2$.
4. Output power is measured directly at the output pins of the IC.
5. Frequency response externally fixed.
6. Ripple rejection measured at the output with a source impedance of 0 Ω (maximum ripple amplitude of 2 V) and a frequency between 100 Hz and 10 kHz.
7. Noise voltage measured in a bandwidth of 20 Hz to 20 kHz.
8. Noise output voltage independent of R_S (V_I = 0 V).

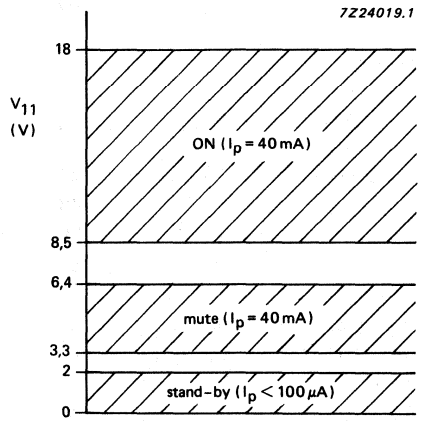


Fig. 3 Stand-by, mute and ON conditions.

APPLICATION INFORMATION

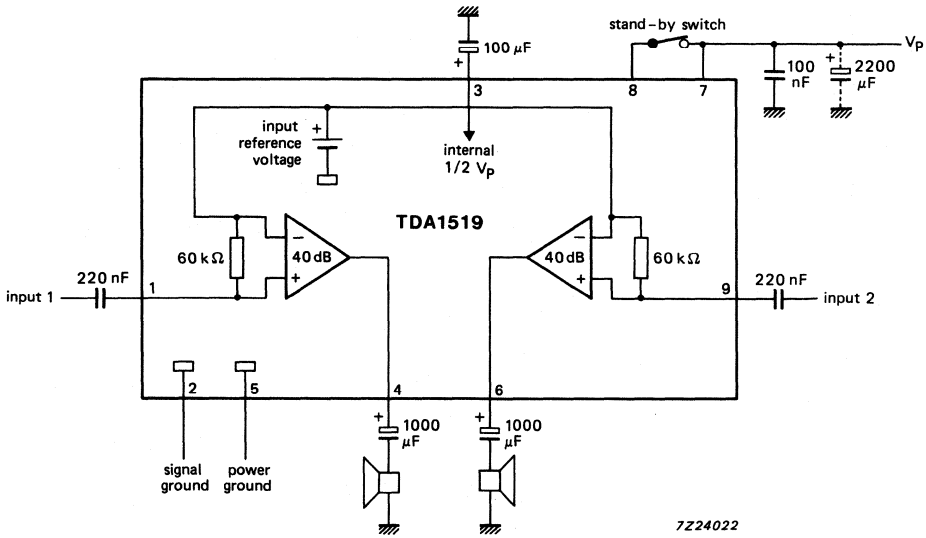


Fig. 4 Application circuit diagram.

22 W BTL OR 2 × 11 WATT STEREO CAR RADIO POWER AMLIFIER

GENERAL DESCRIPTION

The TDA1519A is an integrated class-B dual output amplifier in a 9-lead single in-line (SIL) plastic power package. The device is primarily developed for car radio applications.

Features

- Requires very few external components for Bridge Tied Load (BTL)
- Stereo or BTL application
- High output power
- Low offset voltage at output (important for BTL)
- Fixed gain
- Good ripple rejection
- Mute/stand-by switch
- Load dump protection
- AC and DC short-circuit-safe to ground and V_P
- Thermally protected
- Reverse polarity safe
- Capability to handle high energy on outputs (V_P = 0 V)
- No switch-on/switch-off plop
- Protected against electrostatic discharge
- Low thermal resistance
- Identical inputs (inverting and non-inverting)
- Compatible with TDA1519B (except output power)

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage range						
operating		V_P	6.0	14.4	17.5	V
non-operating		V_P	–	–	30	V
load dump protected		V_P	–	–	45	V
Repetitive peak output current		I_{ORM}	–	–	4	A
Total quiescent current		I_{tot}	–	40	80	mA
Stand-by current		I_{sb}	–	0.1	100	μA
Switch-on current		I_{sw}	–	–	40	μA
Input impedance						
BTL		$\|Z_I\|$	25	–	–	kΩ
stereo		$\|Z_I\|$	50	–	–	kΩ
Stereo application						
Output power	THD = 10%; 4 Ω	P_o	–	6	–	W
	THD = 10%; 2 Ω	P_o	–	11	–	W
Channel separation		α	40	–	–	dB
Noise output voltage		$V_{no(rms)}$	–	150	–	μV
BTL application						
Output power	THD = 10%; 4 Ω	P_o	–	22	–	W
Supply voltage ripple rejection	R_S = 0 Ω					
	f = 100 Hz	RR	34	–	–	dB
	f = 1 kHz to 10 kHz	RR	48	–	–	dB
DC output offset voltage		$\|\Delta V_O\|$	–	–	250	mV
Crystal temperature		T_c	–	–	150	°C

PACKAGE OUTLINES

9-lead SIL; plastic power (SOT131).
9-lead SIL-bent-to-DIL; plastic power (SOT157).

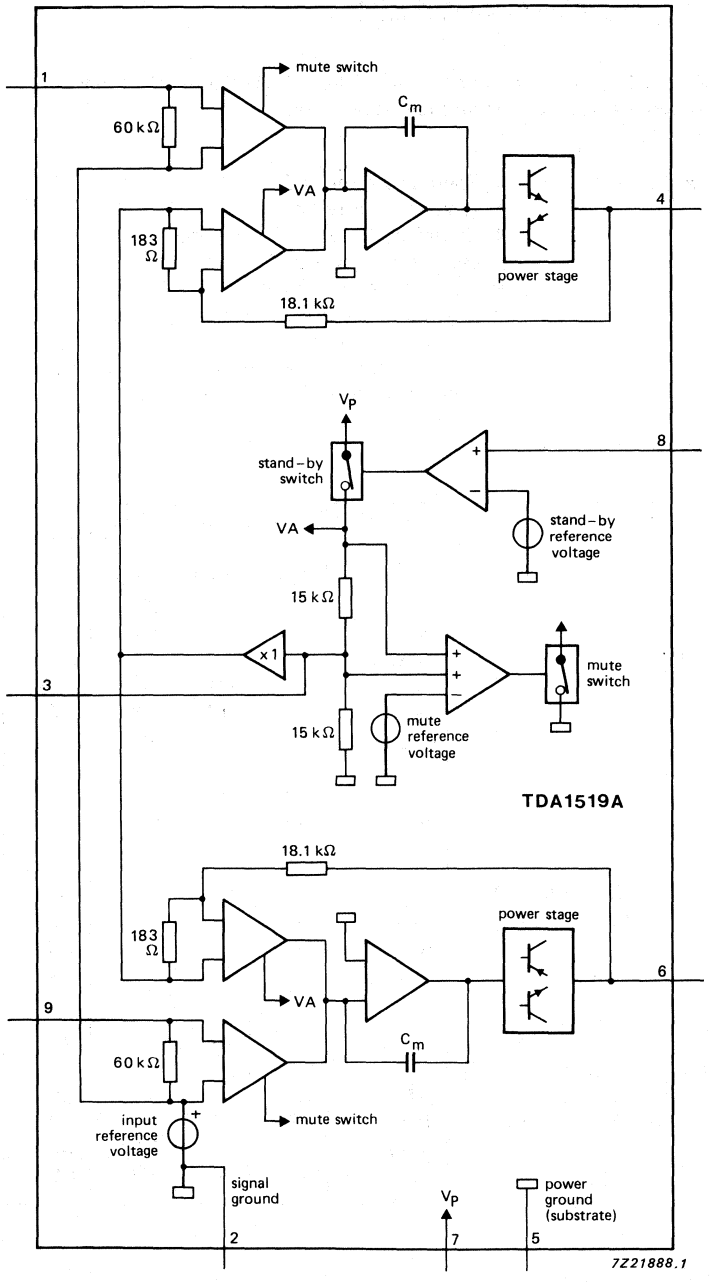


Fig.1 Block diagram.

PINNING

1	NINV	non-inverting input
2	GND1	ground (signal)
3	RR	supply voltage ripple rejection
4	OUT1	output 1
5	GND2	ground (substrate)
6	OUT2	output 2
7	V_P	positive supply voltage
8	M/SS	mute/stand-by switch
9	INV	inverting input

FUNCTIONAL DESCRIPTION

The TDA1519A contains two identical amplifiers with differential input stages. The gain of each amplifier is fixed at 40 dB. A special feature of this device is the mute/stand-by switch which has the following features:

- Low stand-by current ($< 100\ \mu A$)
- Low mute/stand-by switching current (low cost supply switch)
- Mute condition

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage					
operating		V_P	–	17.5	V
non-operating		V_P	–	30	V
load dump protected	during 50 ms; $t_r \geqslant 2.5$ ms	V_P	–	45	V
AC and DC short-circuit-safe voltage		V_{PSC}	–	18	V
Reverse polarity		V_{PR}	–	6	V
Energy handling capability at outputs	$V_P = 0$ V		–	200	mJ
Non-repetitive peak output current		I_{OSM}	–	6	A
Repetitive peak output current		I_{ORM}	–	4	A
Total power dissipation	see Fig.2	P_{tot}	–	25	W
Crystal temperature		T_c	–	150	°C
Storage temperature range		T_{stg}	–55	+150	°C

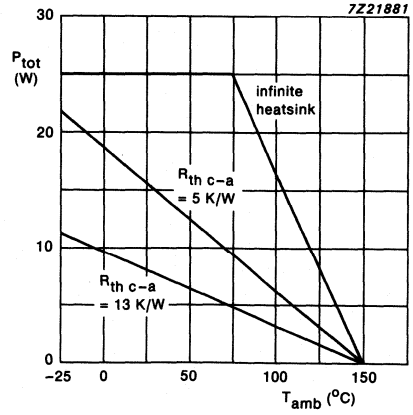


Fig.2 Power derating curve.

DC CHARACTERISTICS

V_P = 14.4 V; T_{amb} = 25 °C; measurements taken using Fig.3; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage range	note 1	V_P	6.0	14.4	17.5	V
Total quiescent current		I_{tot}	–	40	80	mA
DC output voltage	note 2	V_O	–	6.95	–	V
DC output offset voltage		$\lvert\Delta V_{4\text{-}6}\rvert$	–	–	250	mV
Mute/stand-by switch						
Switch-on voltage level		V_{ON}	8.5	–	–	V
Mute condition		V_{mute}	3.3	–	6.4	V
Output signal in mute position	V_I = 1 V (max.); f = 20 Hz to 15 kHz	V_O	–	–	20	mV
DC output offset voltage		$\lvert\Delta V_{4\text{-}6}\rvert$	–	–	250	mV
Stand-by condition		V_{sb}	0	–	2	V
DC current in stand-by condition		I_{sb}	–	–	100	μA
Switch-on current		I_{sw}	–	12	40	μA

AC CHARACTERISTICS

V_P = 14.4 V; R_L = 4 Ω; f = 1 kHz; T_{amb} = 25 °C; measurements taken using Fig.3; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Stereo application						
Output power	note 3					
	THD = 0.5%	P_o	4	5	–	W
	THD = 10%	P_o	5.5	6.0	–	W
Output power at R_L = 2 Ω	note 3					
	THD = 0.5%	P_o	7.5	8.5	–	W
	THD = 10%	P_o	10	11	–	W
Total harmonic distortion	P_o = 1 W	THD	–	0.1	–	%
Low frequency roll-off	note 4					
	−3 dB	f_L	–	45	–	Hz
High frequency roll-off	−1 dB	f_H	20	–	–	kHz
Closed loop voltage gain		G_v	39	40	41	dB
Supply voltage ripple rejection						
ON	notes 5 and 6	RR	40	–	–	dB
ON	notes 5 and 7	RR	45	–	–	dB
mute	notes 5 and 8	RR	45	–	–	dB
stand-by	notes 5 and 8	RR	80	–	–	dB
Input impedance		$\|Z_i\|$	50	60	75	kΩ
Noise output voltage (RMS value)	note 9					
ON	R_S = 0 Ω	$V_{no(rms)}$	–	150	–	μV
ON	R_S = 10 kΩ	$V_{no(rms)}$	–	250	500	μV
mute	note 10	$V_{no(rms)}$	–	120	–	μV
Channel separation	R_S = 10 kΩ	α	40	–	–	dB
Channel unbalance		$\|\Delta G_v\|$	–	0.1	1	dB

AC CHARACTERISTICS

V_P = 14.4 V; R_L = 4 Ω; f = 1 kHz; T_{amb} = 25 °C; measurements taken using Fig.4, unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
BTL application						
Output power	note 3					
	THD = 0.5%	P_o	15	17	–	W
	THD = 10%	P_o	20	22	–	W
Output power at V_P = 13.2 V	note 3					
	THD = 0.5%	P_o	–	13	–	W
	THD = 10%	P_o	–	17.5	–	W
Total harmonic distortion	P_o = 1 W	THD	–	0.1	–	%
Power bandwidth	THD = 0.5%; P_o = −1 dB; w.r.t. 15 W	B_w	–	35 to 15 000	–	Hz
Low frequency roll-off	note 4					
	−1 dB	f_L	–	45	–	Hz
High frequency roll-off	−1 dB	f_H	20	–	–	kHz
Closed loop voltage gain		G_v	45	46	47	dB
Supply voltage ripple rejection						
ON	notes 5 and 6	RR	34	–	–	dB
ON	notes 5 and 7	RR	48	–	–	dB
mute	notes 5 and 8	RR	48	–	–	dB
stand-by	notes 5 and 8	RR	80	–	–	dB
Input impedance		$\|Z_i\|$	25	30	38	kΩ
Noise output voltage (RMS value)	note 9					
ON	R_S = 0 Ω	$V_{no(rms)}$	–	200	–	μV
ON	R_S = 10 kΩ	$V_{no(rms)}$	–	350	700	μV
mute	note 10	$V_{no(rms)}$	–	180	–	μV

Notes to the characteristics

1. The circuit is DC adjusted at $V_P = 6$ V to 17.5 V and AC operating at $V_P = 8.5$ V to 17.5 V.
2. At 17.5 V $< V_P <$ 30 V the DC output voltage $\leqslant V_P/2$.
3. Output power is measured directly at the output pins of the IC.
4. Frequency response externally fixed.
5. Ripple rejection measured at the output with a source impedance of 0 Ω (maximum ripple amplitude of 2 V).
6. Frequency f = 100 Hz.
7. Frequency between 1 kHz and 10 kHz.
8. Frequency between 100 Hz and 10 kHz.
9. Noise voltage measured in a bandwidth of 20 Hz to 20 kHz.
10. Noise output voltage independent of R_S ($V_I = 0$ V).

APPLICATION INFORMATION

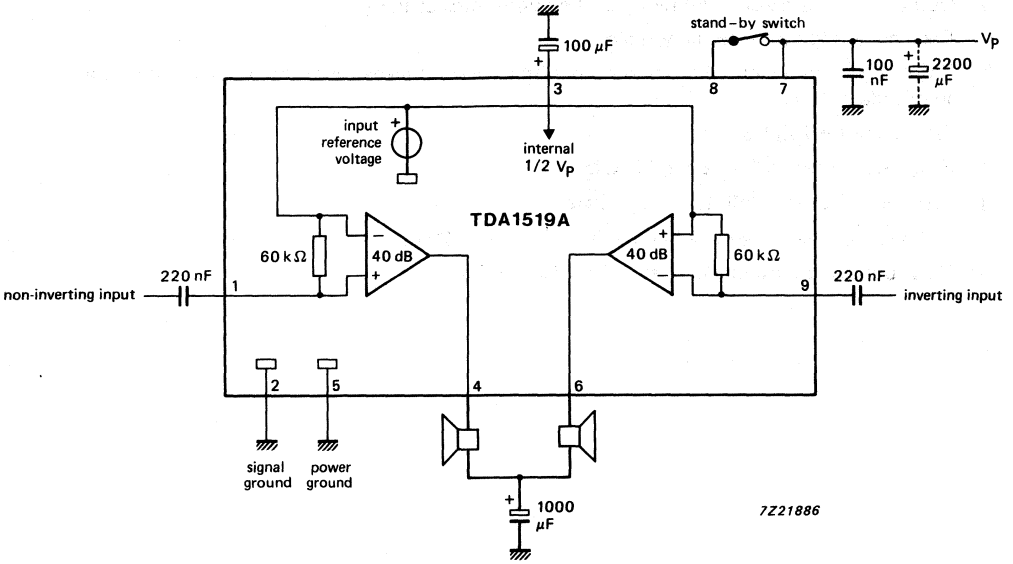


Fig.3 Stereo application circuit diagram.

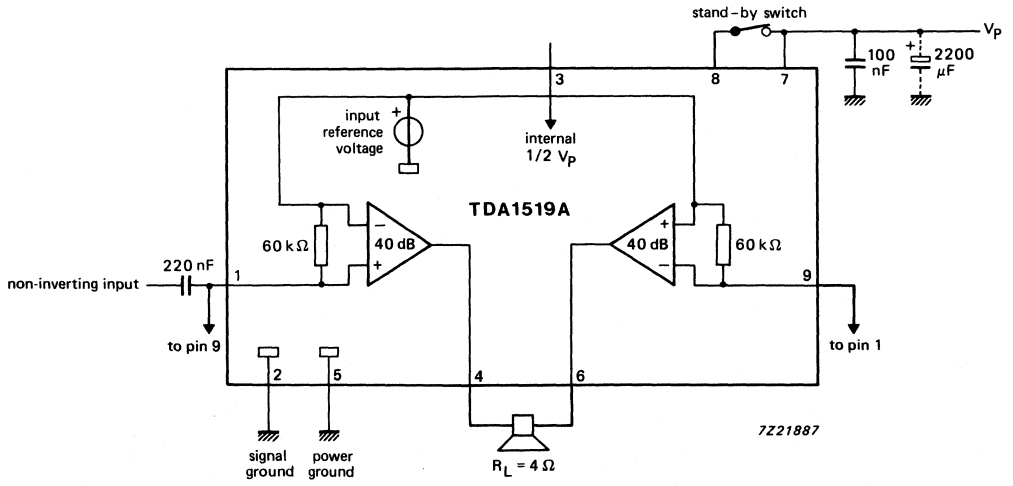


Fig.4 BTL application circuit diagram.

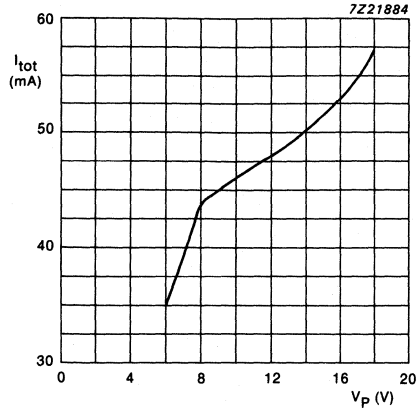


Fig.5 Total quiescent current (I_{tot}) as a function of supply voltage (V_P).

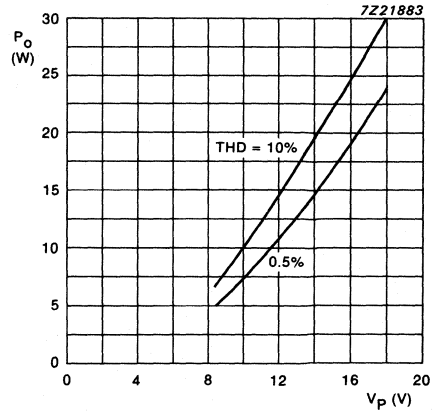


Fig.6 Output power (P_o) as a function of supply voltage (V_P) for BTL application at $R_L = 4\ \Omega$; f = 1 kHz.

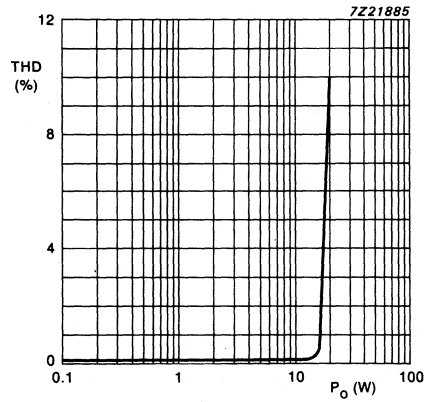


Fig.7 Total harmonic distortion (THD) as a function of output power (P_o) for BTL application at $R_L = 4\ \Omega$; f = 1 kHz.

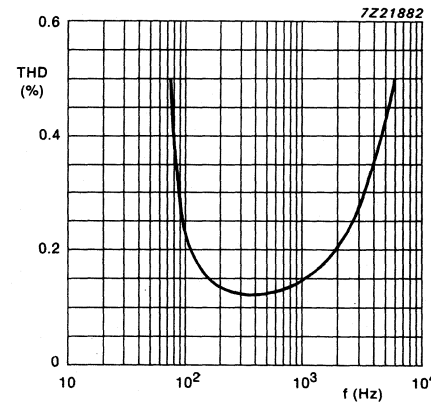


Fig.8 Total harmonic distortion (THD) as a function of operating frequency (f) for BTL application at $R_L = 4\ \Omega$; $P_o = 1$ W.

12 W BTL OR 2 × 6 WATT STEREO CAR RADIO POWER AMPLIFIER

GENERAL DESCRIPTION

The TDA1519B is an integrated class-B dual output amplifier in a 9-lead single in-line (SIL) plastic medium power package. The device is primarily developed for car radio applications.

Features

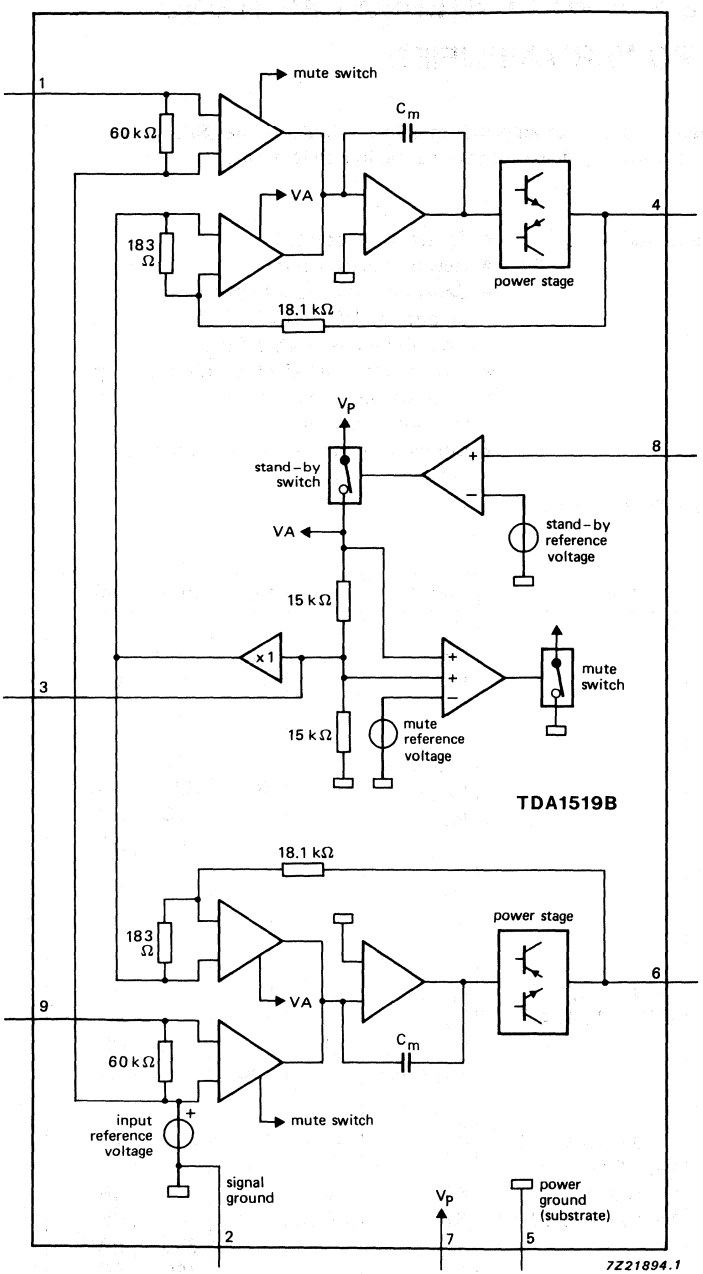
- Requires very few external components for Bridge Tied Load (BTL)
- Stereo or BTL application
- High output power
- Low offset voltage at output (important for BTL)
- Fixed gain
- Good ripple rejection
- Mute/stand-by switch
- Load dump protection
- AC and DC short-circuit-safe to ground and V_P
- Thermally protected
- Reverse polarity safe
- Capability to handle high energy on outputs (V_P = 0 V)
- No switch-on/switch-off plop
- Protected against electrostatic discharge
- Identical inputs (inverting and non-inverting)
- Compatible with TDA1519A (except output power)

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage range						
operating		V_P	6.0	14.4	18.0	V
non-operating		V_P	–	–	30	V
load dump protected		V_P	–	–	45	V
Repetitive peak output current		I_{ORM}	–	–	2.5	A
Total quiescent current		I_{tot}	–	40	80	mA
Stand-by current		I_{sb}	–	0.1	100	μA
Switch-on current		I_{sw}	–	–	40	μA
Input impedance						
BTL		$\|Z_I\|$	25	–	–	kΩ
stereo		$\|Z_I\|$	50	–	–	kΩ
Stereo application						
Output power	THD = 5%; 4 Ω	P_o	–	5	–	W
	THD = 10%; 4 Ω	P_o	–	6	–	W
Channel separation		α	40	–	–	dB
Noise output voltage		$V_{no(rms)}$	–	150	–	μV
BTL application						
Output power	THD = 10%; 8 Ω	P_o	–	12	–	W
Supply voltage ripple rejection	R_S = 0 Ω					
	f = 100 Hz	RR	34	–	–	dB
	f = 1 kHz to 10 kHz	RR	48	–	–	dB
DC output offset voltage		$\|\Delta V_O\|$	–	–	250	mV
Crystal temperature		T_c	–	–	150	°C

PACKAGE OUTLINE

9-lead SIL; plastic (SOT110B).



PINNING

1	NINV	non-inverting input
2	GND1	ground (signal)
3	RR	supply voltage ripple rejection
4	OUT1	output 1
5	GND2	ground (substrate)
6	OUT2	output 2
7	V_P	positive supply voltage
8	M/SS	mute/stand-by switch
9	INV	inverting input

Fig.1 Block diagram.

FUNCTIONAL DESCRIPTION

The TDA1519B contains two identical amplifiers with differential input stages. The gain of each amplifier is fixed at 40 dB. A special feature of this device is the mute/stand-by switch which has the following features:

- Low stand-by current ($< 100\ \mu A$)
- Low mute/stand-by switching current (low cost supply switch)
- Mute condition

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage					
operating		V_P	–	18	V
non-operating		V_P	–	30	V
load dump protected	during 50 ms; $t_r \geqslant 2.5$ ms	V_P	–	45	V
AC and DC short-circuit-safe voltage		V_{PSC}	–	18	V
Reverse polarity		V_{PR}	–	6	V
Energy handling capability at outputs	$V_P = 0$ V		–	200	mJ
Non-repetitive peak output current		I_{OSM}	–	4	A
Repetitive peak output current		I_{ORM}	–	2.5	A
Total power dissipation	see Fig.2	P_{tot}	–	15	W
Crystal temperature		T_c	–	150	°C
Storage temperature range		T_{stg}	−55	+150	°C

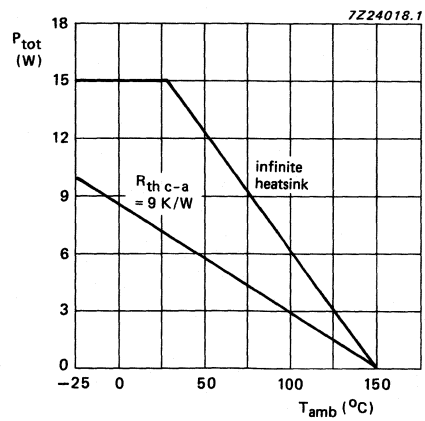


Fig.2 Power derating curve.

DC CHARACTERISTICS

V_P = 14.4 V; T_{amb} = 25 °C; measurements taken using Fig.3; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage range	note 1	V_P	6.0	14.4	18.0	V
Total quiescent current		I_{tot}	–	40	80	mA
DC output voltage	note 2	V_O	–	6.95	–	V
DC output offset voltage		$\lvert\Delta V_{4\text{-}6}\rvert$	–	–	250	mV
Mute/stand-by switch						
Switch-on voltage level		V_{ON}	8.5	–	–	V
Mute condition		V_{mute}	3.3	–	6.4	V
Output signal in mute position	V_I = 1 V (max.); f = 20 Hz to 15 kHz	V_O	–	–	20	mV
DC output offset voltage		$\lvert\Delta V_{4\text{-}6}\rvert$	–	–	250	mV
Stand-by condition		V_{sb}	0	–	2	V
DC current in stand-by condition		I_{sb}	–	–	100	μA
Switch-on current		I_{sw}	–	12	40	μA

AC CHARACTERISTICS

V_P = 14.4 V; R_L = 4 Ω; f = 1 kHz; T_{amb} = 25 °C; measurements taken using Fig.3; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Stereo application						
Output power	note 3					
	THD = 0.5%	P_o	4	5	–	W
	THD = 10!	P_o	5.5	6.0	–	W
Output power at V_P = 13.2 V	note 3					
	THD = 0.5%	P_o	–	3.5	–	W
	THD = 10%	P_o	–	4.8	–	W
Total harmonic distortion	P_o = 1 W	THD	–	0.1	–	%
Low frequency roll-off	note 4					
	−3 dB	f_L	–	45	–	Hz
High frequency roll-off	−1 dB	f_H	20	–	–	kHz
Closed loop voltage gain		G_v	39	40	41	dB
Supply voltage ripple rejection						
ON	notes 5 and 6	RR	40	–	–	dB
ON	notes 5 and 7	RR	45	–	–	dB
mute	notes 5, 6 and 7	RR	45	–	–	dB
stand-by	notes 5, 6 and 7	RR	80	–	–	dB
Input impedance		$\|Z_i\|$	50	60	75	kΩ
Noise output voltage (RMS value)	note 8					
ON	R_S = 0 Ω	$V_{no(rms)}$	–	150	–	μV
ON	R_S = 10 kΩ	$V_{no(rms)}$	–	250	500	μV
mute	note 9	$V_{no(rms)}$	–	120	–	μV
Channel separation	R_S = 10 kΩ	α	40	–	–	dB
Channel unbalance		$\|\Delta G_v\|$	–	0.1	1	dB

AC CHARACTERISTICS

V_P = 14.4 V; R_L = 8 Ω; f = 1 kHz; T_{amb} = 25 °C; measurements taken using Fig.4; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
BTL application						
Output power	note 3					
	THD = 0.5%	P_o	8	10	–	W
	THD = 10%	P_o	11	12	–	W
Output power at V_P = 13.2 V	note 3					
	THD = 0.5%	P_o	–	7.5	–	W
	THD = 10%	P_o	–	10	–	W
Total harmonic distortion	P_o = 1 W	THD	–	0.1	–	%
Power bandwidth	THD = 0.5%; P_o = −1 dB; w.r.t. 15 W	B_w	–	35 to 15 000	–	Hz
Low frequency roll-off	note 4					
	−1 dB	f_L	–	45	–	Hz
High frequency roll-off	−1 dB	f_H	20	–	–	kHz
Closed loop voltage gain		G_v	45	46	47	dB
Supply voltage ripple rejection						
ON	notes 5 and 6	RR	34	–	–	dB
ON	notes 5 and 7	RR	48	–	–	dB
mute	notes 5, 6 and 7	RR	48	–	–	dB
stand-by	notes 5, 6 and 7	RR	80	–	–	dB
Input impedance		$\|Z_i\|$	25	30	38	kΩ
Noise output voltage (RMS value)	note 8					
ON	R_S = 0 Ω	$V_{no(rms)}$	–	200	–	μV
ON	R_S = 10 kΩ	$V_{no(rms)}$	–	350	700	μV
mute	note 9	$V_{no(rms)}$	–	180	–	μV

Notes to the characteristics

1. The circuit is DC adjusted at V_P = 6 V to 18 V and AC operating at V_P = 8.5 V to 18 V.
2. At 18 V < V_P < 30 V the DC output voltage ⩽ $V_P/2$.
3. Output power is measured directly at the output pins of the IC.
4. Frequency response externally fixed.
5. Ripple rejection measured at the output with a source impedance of 0 Ω (maximum ripple amplitude of 2 V).
6. Frequency f = 100 Hz.
7. Frequency between 1 kHz and 10 kHz.
8. Noise voltage measured in a bandwidth of 20 Hz to 20 kHz.
9. Noise output voltage independent of R_S (V_I = 0 V).

APPLICATION INFORMATION

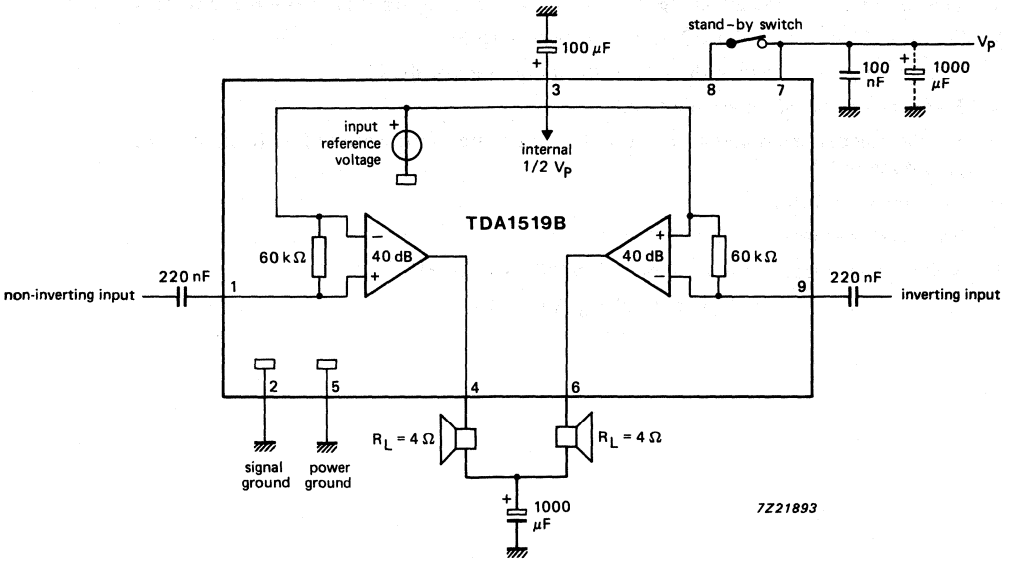


Fig.3 Stereo application circuit diagram.

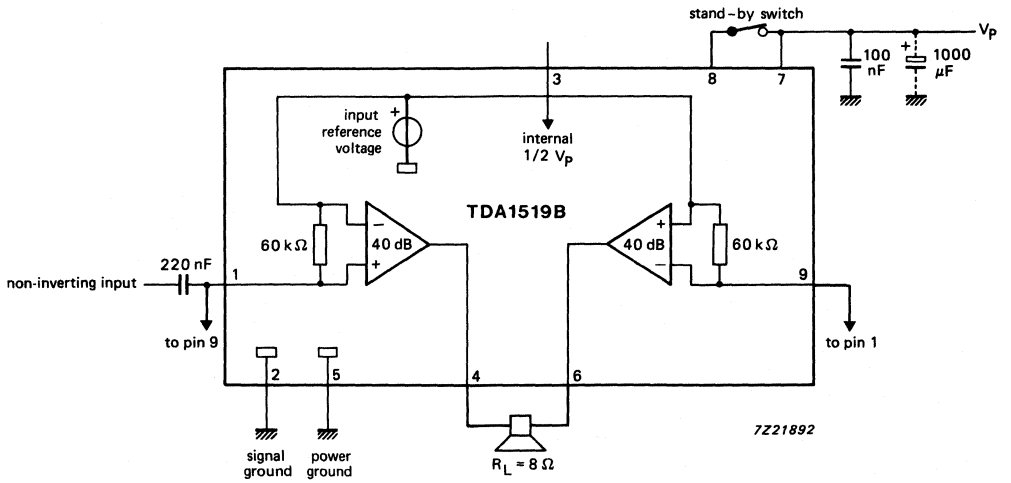


Fig.4 BTL application circuit diagram.

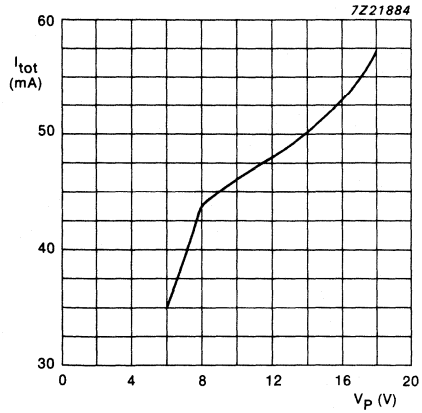


Fig.5 Total quiescent current (I_{tot}) as a function of supply voltage (V_P).

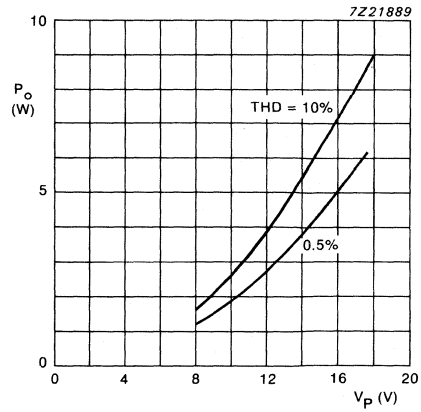


Fig.6 Output power (P_O) as a function of supply voltage (V_P) for stereo application at $R_L = 4\ \Omega$, f = 1 kHz.

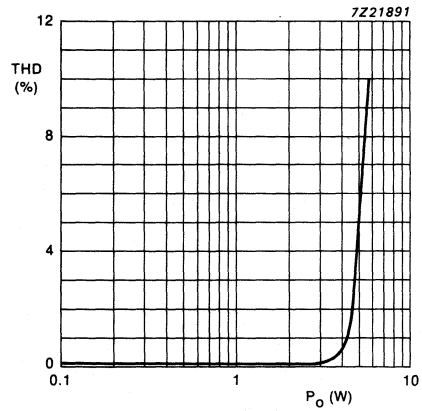


Fig.7 Total harmonic distortion (THD) as a function of output power (P_O) for stereo application at $R_L = 4\ \Omega$, f = 1 kHz.

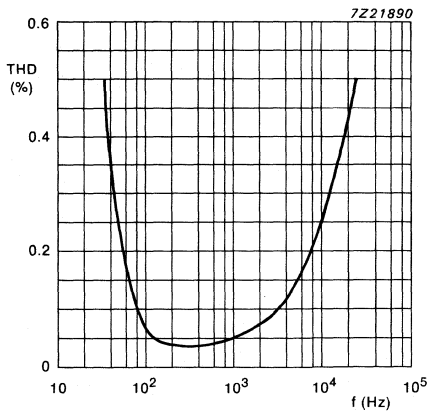


Fig.8 Total harmonic distortion (THD) as a function of operating frequency (f) for stereo application at $R_L = 4\ \Omega$, $P_O = 1$ W.

2 x 12 W HI-FI AUDIO POWER AMPLIFIER

GENERAL DESCRIPTION

The TDA1521/TDA1521Q is a dual hi-fi audio power amplifier encapsulated in a 9-lead plastic power package. The device is especially designed for mains fed applications (e.g. stereo tv sound and stereo radio).

Features

- Requires very few external components
- Input muted during power-on and off (no switch-on or switch-off clicks)
- Low offset voltage between output and ground
- Excellent gain balance between channels
- Hi-fi according to IEC 268 and DIN 45500
- Short-circuit-proof
- Thermally protected

QUICK REFERENCE DATA

Stereo applications			
Supply voltage range	V_P	± 7,5 to ± 21,0	V
Output power at THD = 0,5%, V_P = ± 16 V	P_o	typ. 12	W
Voltage gain	G_v	typ. 30	dB
Gain balance between channels	ΔG_v	typ. 0,2	dB
Ripple rejection	SVRR	typ. 60	dB
Channel separation	α	typ. 70	dB
Noise output voltage	$V_{no(rms)}$	typ. 70	μV

PACKAGE OUTLINES

TDA1521: 9-lead single in-line; plastic power (SOT131).
TDA1521Q: 9-lead SIL-bent-to-DIL; plastic power (SOT157).

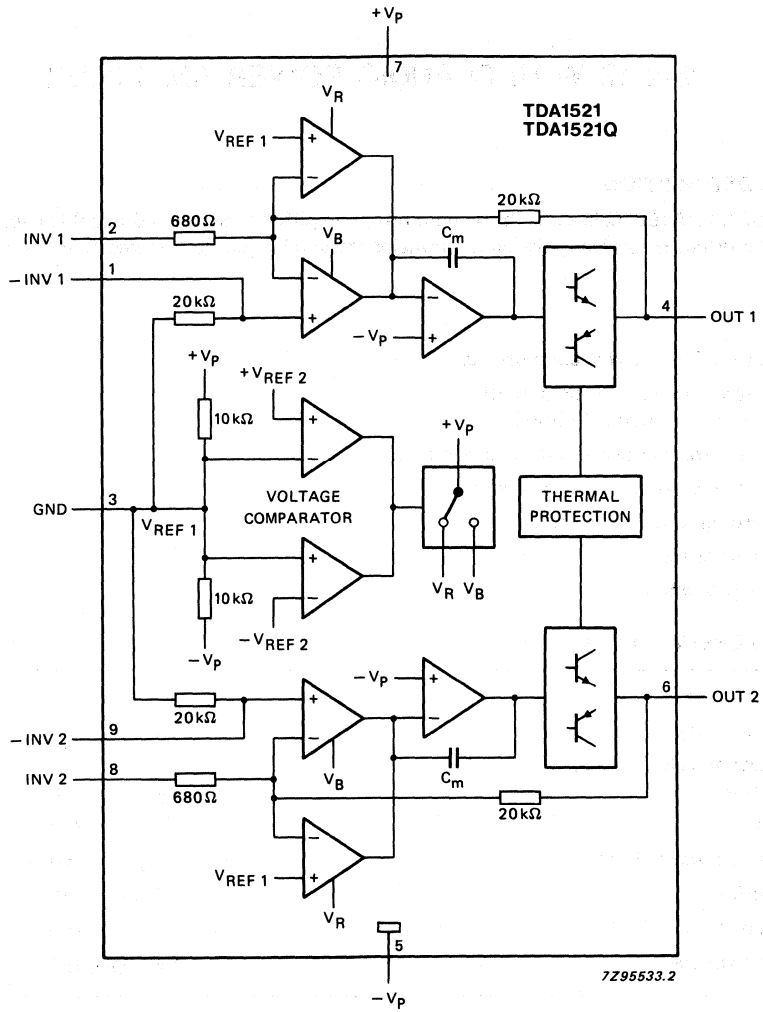


Fig. 1 Block diagram.

PINNING

1	–INV1	non-inverting input 1
2	INV1	inverting input 1
3	GND	ground (symmetrical) / ½ Vp (asymmetrical)
4	OUT1	output 1
5	–Vp	negative supply (symmetrical) / ground (asymmetrical)
6	OUT2	output 2
7	+ Vp	positive supply
8	INV2	inverting input 2
9	–INV2	non-inverting input 2

FUNCTIONAL DESCRIPTION

This hi-fi stereo power amplifier is designed for mains fed applications. The circuit is designed for both symmetrical and asymmetrical power supply systems. An output power of 2 x 12 watts (THD = 0,5%) can be delivered into an 8 Ω load with a symmetrical power supply of ± 16 V.

The gain is fixed internally at 30 dB. Internal gain fixing gives low gain spread and very good balance between the amplifiers (0,2 dB).

A special feature of this device is a mute circuit which suppresses unwanted input signals during switching on and off. Referring to Fig. 13, the 100 μF capacitor creates a time delay when the voltage at pin 3 is lower than an internally fixed reference voltage. During the delay the amplifiers remain in their DC operating mode but are isolated from the non-inverting inputs on pins 1 and 9.

Two thermal protection circuits are provided, one monitors the average junction temperature and the other the instantaneous temperature of the power transistors. Both protection circuits activate at 150 °C allowing safe operation to a maximum junction temperature of 150 °C without added distortion.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage	pin 7	$V_P = V_{7-3}$	–	+21	V
	pin 5	$-V_P = V_{5-3}$	–	−21	V
Non-repetitive peak output current	pins 4 and 6	I_{OSM}	–	4	A
Total power dissipation	see Fig. 2	P_{tot}			
Storage temperature range		T_{stg}	−55	+ 150	°C
Junction temperature		T_j	–	150	°C
Short-circuit time: outputs short-circuited to ground (full signal drive)	see note				
	symmetrical power supply	t_{sc}	–	1	hour
	asymmetrical power supply; $V_P < 32$ V (unloaded); $R_i \geqslant 4\ \Omega$	t_{sc}	–	1	hour

Note

For asymmetrical power supplies (at short circuiting of the load) the maximum supply voltage is limited to V_P = 28 V. If the total internal resistance of the supply (R_i) > 4 Ω, the maximum unloaded supply voltage is increased to 32 V.

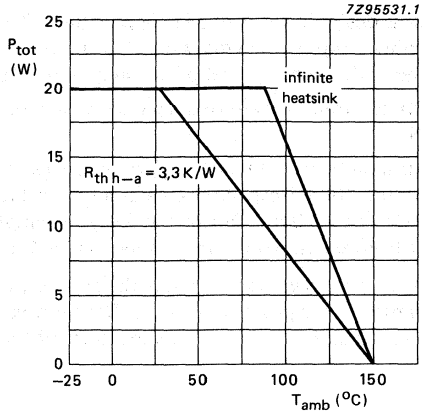


Fig. 2 Power derating curve.

THERMAL RESISTANCE

From junction to case $R_{th\ j\text{-}c}$ = 2,5 K/W

HEATSINK DESIGN EXAMPLE

With derating of 2,5 K/W, the value of heatsink thermal resistance is calculated as follows:

given $R_L = 8\ \Omega$ and $V_P = \pm 16$ V, the measured maximum dissipation is 14,6 W; then, for a maximum ambient temperature of 65 °C, the required thermal resistance of the heatsink is

$$R_{th\ h\text{-}a} = \frac{150 - 65}{14,6} - 2,5 = 3,3\ \text{K/W}$$

Note: The internal metal block (heatsink) has the same potential as pin 5 ($-V_P$)

CHARACTERISTICS

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage range						
operating mode		V_P	± 7,5	± 16,0	± 21,0	V
input mute mode		V_P	± 2,0	–	± 5,8	V
Repetitive peak output current		I_{ORM}	2,2	–	–	A
Operating mode: symmetrical power supply; test circuit as per Fig. 12; V_P = ± 16 V; R_L = 8 Ω; T_{amb} = 25 °C; f = 1 kHz						
Total quiescent current	without R_L	I_{tot}	18	40	70	mA
Output power	THD = 0,5%	P_o	10	12	–	W
	THD = 10%	P_o	12	15	–	W
Total harmonic distortion	P_o = 6 W	THD	–	0,15	0,2	%
Power bandwidth	THD = 0,5% note 1	B		20 to 20k		Hz
Voltage gain		G_v	29	30	31	dB
Gain balance		ΔG_v	–	0,2	1,0	dB
Noise output voltage (r.m.s. value); unweighted (20 Hz to 20 kHz)	R_S = 2 kΩ	$V_{no(rms)}$	–	70	140	μV
Input impedance		$\|Z_i\|$	14	20	26	kΩ
Ripple rejection	note 2	SVRR	40	60	–	dB
Channel separation	R_S = 0 Ω	α	46	70	–	dB
Input bias current		I_{ib}	–	0,3	–	μA
DC output offset voltage	with respect to ground	V_{OFF}	–	30	200	mV
Input mute mode: symmetrical power supply; test circuit as per Fig. 12; V_P = ± 4 V; R_L = 8 Ω; T_{amb} = 25 °C; f = 1 kHz						
Total quiescent current	without R_L	I_{tot}	9	30	40	mA
Output voltage	V_i = 600 mV	V_{out}	–	0,6	1,8	mV
Noise output voltage (r.m.s. value); unweighted (20 Hz to 20 kHz)	R_S = 2 kΩ	$V_{no(rms)}$	–	70	140	μV
Ripple rejection	note 2	SVRR	35	55	–	dB
DC output offset voltage	with respect to ground	V_{OFF}	–	40	200	mV

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Operating mode: asymmetrical power supply; test circuit as per Fig. 13; V_S = 24 V; R_L = 8 Ω; T_{amb} = 25 °C; f = 1 kHz						
Total quiescent current		I_{tot}	18	40	70	mA
Output power	THD = 0,5%	P_o	5	6	–	W
	THD = 10%	P_o	6,5	8	–	W
Total harmonic distortion	P_o = 4 W	THD	–	0,13	0,2	%
Power bandwidth	THD = 0,5% note 1	B		40 to 20k		Hz
Voltage gain		G_v	29	30	31	dB
Gain balance		ΔG_v	–	0,2	1	dB
Noise output voltage (r.m.s. value); unweighted (20 Hz to 20 kHz)	R_S = 2 kΩ	$V_{no(rms)}$	–	70	140	μV
Input impedance		$\|Z_i\|$	14	20	26	kΩ
Ripple rejection		SVRR	35	44	–	dB
Channel separation	R_S = 0 Ω	α	–	45	–	dB

Notes to the characteristics

1. Power bandwidth at $P_{o\ max}$ −3 dB.
2. Ripple rejection at R_S = 0 Ω, f = 100 Hz to 20 kHz;
   ripple voltage = 200 mV (r.m.s. value) applied to positive or negative supply rail.

APPLICATION INFORMATION

Input mute circuit

The input mute circuit operates only during switching on and off of the supply voltage. The circuit compares the ½ supply voltage (at pin 3) with an internally fixed reference voltage (V_{ref}), derived directly from the supply voltage. When the voltage at pin 3 is lower than V_{ref} the non-inverting inputs (pins 1 and 9) are disconnected from the amplifier. The voltage at pin 3 is determined by an internal voltage divider and the external 100 μF capacitor.
During switching on, a time delay is created between the reference voltage and the voltage at pin 3, during which the input terminal is disconnected, (as illustrated in Fig. 3).

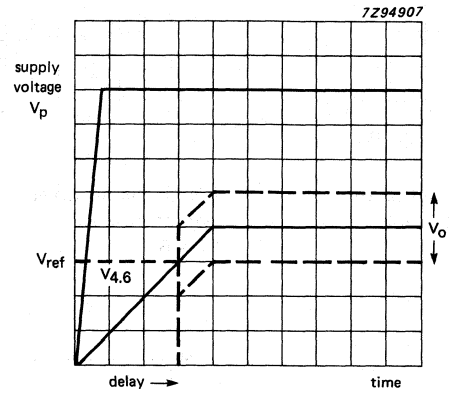


Fig. 3 Input mute circuit; time delay.

APPLICATION INFORMATION (continued)

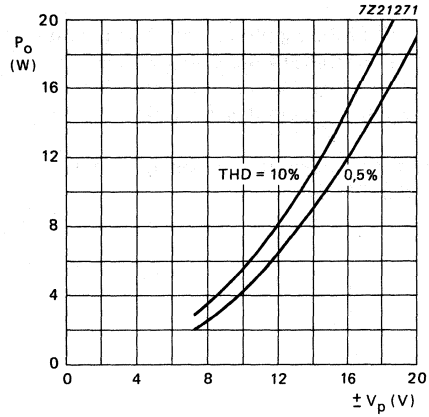


Fig. 4 Output power as a function of supply voltage, symmetrical supply; $R_L = 8\ \Omega$; f = 1 kHz.

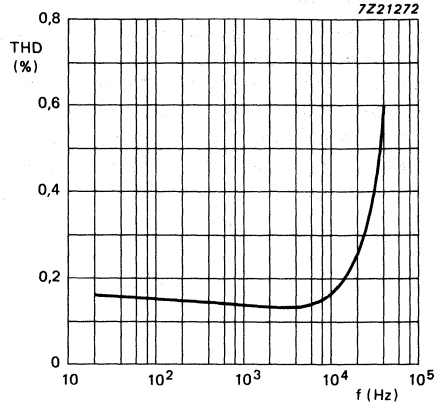


Fig. 5 Distortion as a function of frequency; symmetrical supply; $V_P = \pm 16$ V; $R_L = 8\ \Omega$; $P_o = 6$ W.

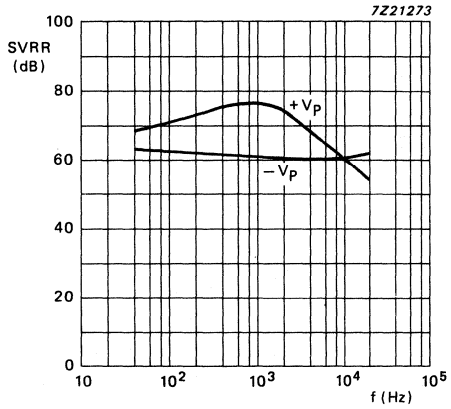


Fig. 6 Supply voltage ripple rejection; symmetrical supply; $V_P = \pm 16$ V; $V_{RR} = 200$ mV.

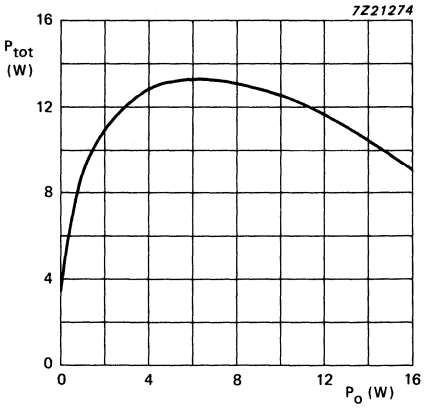


Fig. 7 Power dissipation as a function of output power; symmetrical supply; $V_P = \pm 16$ V; $R_L = 8\ \Omega$; f = 1 kHz.

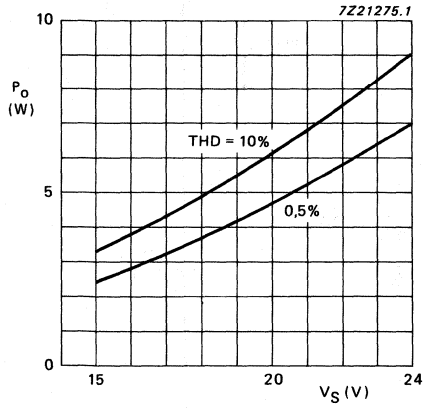


Fig. 8 Output power as a function of supply voltage; asymmetrical supply; $R_L = 8\ \Omega$; f = 1 kHz.

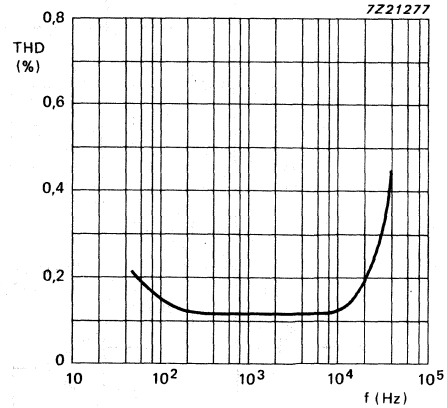


Fig. 9 Distortion as a function of frequency; asymmetrical supply; $V_S = 24$ V; $R_L = 8\ \Omega$; $P_o = 4$ W.

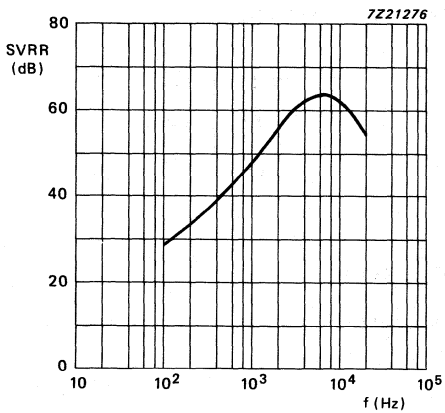


Fig. 10 Supply voltage ripple rejection; asymmetrical supply; $V_S = 24$ V; $V_{RR} = 200$ mV.

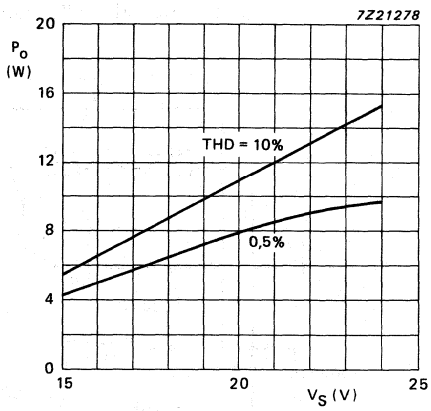
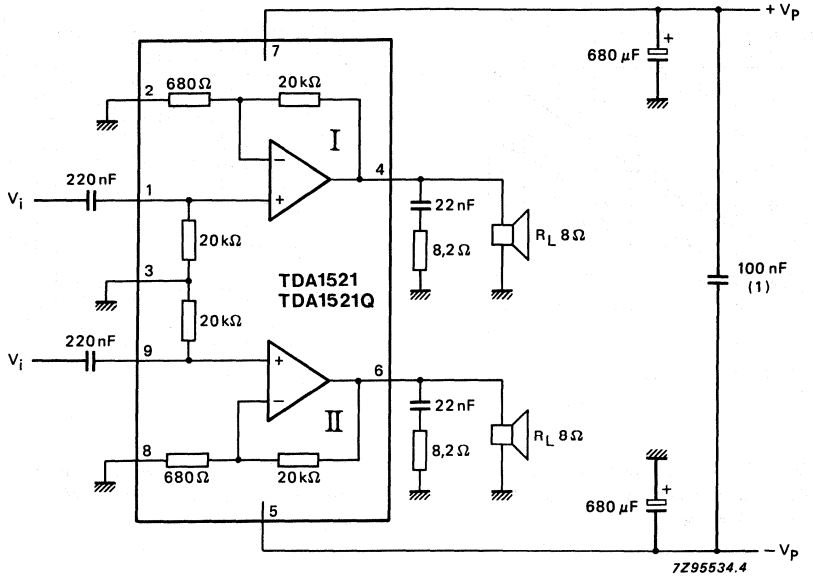
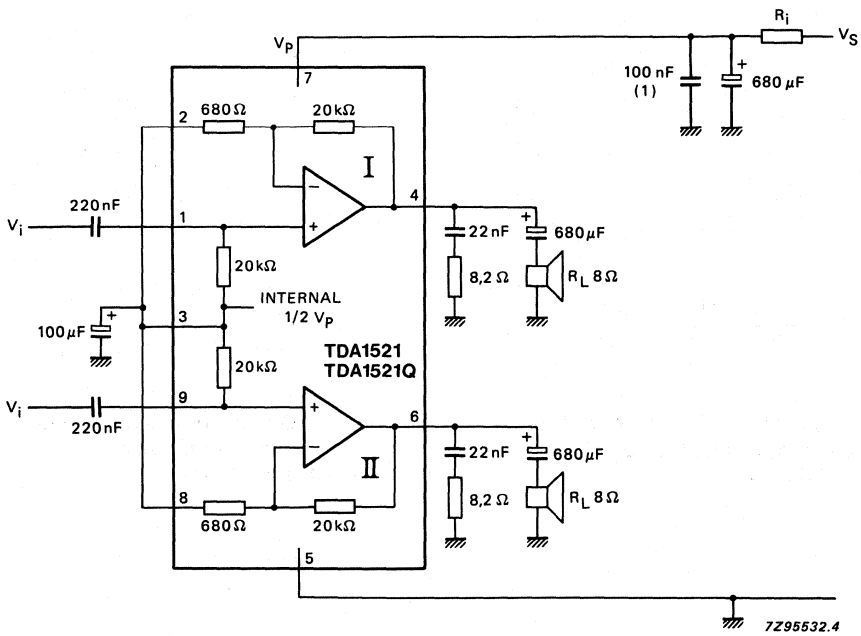


Fig. 11 Output power as a function of supply voltage; asymmetrical supply; $R_L = 4\ \Omega$; f = 1 kHz.



1 To be connected as close as possible to the IC

Fig. 12 Test and application circuit; symmetrical power supply.



1 To be connected as close as possible to the IC

Fig. 13 Test and application circuit; asymmetrical power supply.

2 x 6 W HI-FI AUDIO POWER AMPLIFIER

GENERAL DESCRIPTION

The TDA1521A is a dual hi-fi audio power amplifier encapsulated in a 9-lead plastic power package. The device is especially designed for mains fed applications (e.g. stereo tv sound and stereo radio).

Features

- Requires very few external components
- Input muted during power-on and off (no switch-on or switch-off clicks)
- Low offset voltage between output and ground
- Excellent gain balance between channels
- Hi-fi according to IEC 268 and DIN 45500
- Short-circuit-proof
- Thermally protected

QUICK REFERENCE DATA

Stereo applications				
Supply voltage range	V_P		± 7,5 to ± 21,0	V
Output power at THD = 0,5%, V_P = ± 12 V	P_O	typ.	6	W
Voltage gain	G_V	typ.	30	dB
Gain balance between channels	ΔG_V	typ.	0,2	dB
Ripple rejection	SVRR	typ.	60	dB
Channel separation	α	typ.	70	dB
Noise output voltage	$V_{no(rms)}$	typ.	70	μV

PACKAGE OUTLINE

TDA1521A: 9-lead single in-line; plastic power (SOT 110B).

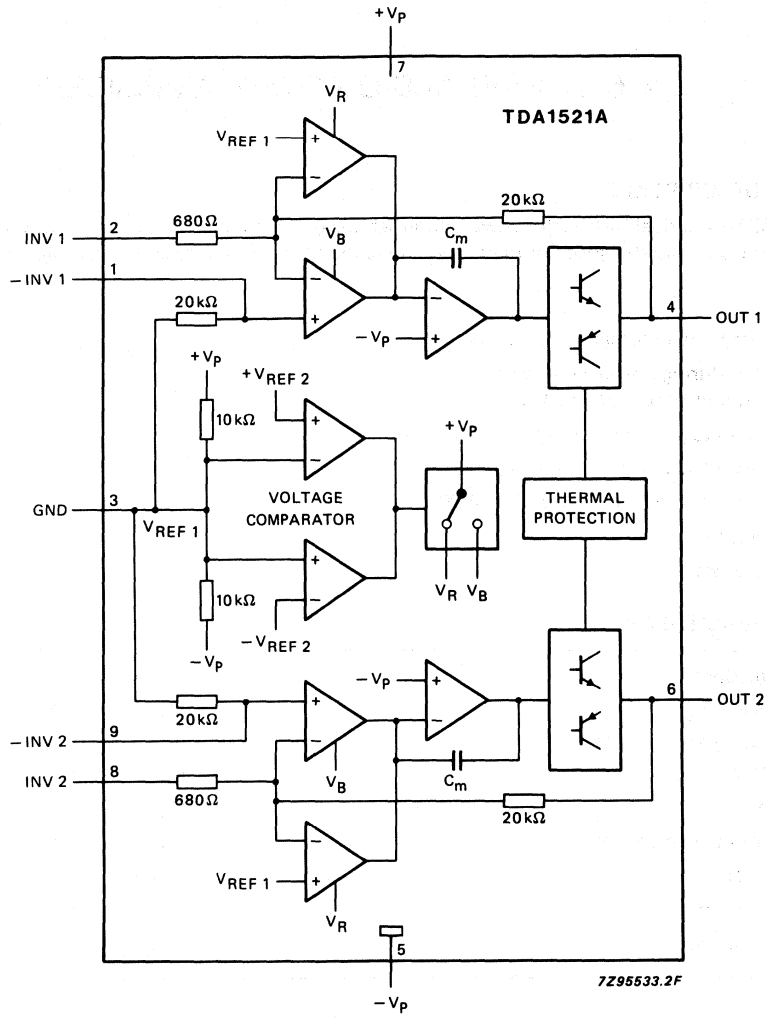


Fig. 1 Block diagram.

PINNING

1	–INV1	non-inverting input 1
2	INV1	inverting input 1
3	GND	ground (symmetrical) / ½ VP (asymmetrical)
4	OUT1	output 1
5	–VP	negative supply (symmetrical) / ground (asymmetrical)
6	OUT2	output 2
7	+ VP	positive supply
8	INV2	inverting input 2
9	–INV2	non-inverting input 2

FUNCTIONAL DESCRIPTION

This hi-fi stereo power amplifier is designed for mains fed applications. The circuit is designed for both symmetrical and asymmetrical power supply systems. An output power of 2 x 6 watts (THD = 0,5%) can be delivered into an 8 Ω load with a symmetrical power supply of ± 12 V.

The gain is fixed internally at 30 dB. Internal gain fixing gives low gain spread and very good balance between the amplifiers (0,2 dB).

A special feature of this device is a mute circuit which suppresses unwanted input signals during switching on and off. Referring to Fig. 12, the 100 μF capacitor creates a time delay when the voltage at pin 3 is lower than an internally fixed reference voltage. During the delay the amplifiers remain in their DC operating mode but are isolated from the non-inverting inputs on pins 1 and 9.

Two thermal protection circuits are provided, one monitors the average junction temperature and the other the instantaneous temperature of the power transistors. Both protection circuits activate at 150 °C allowing safe operation to a maximum junction temperature of 150 °C without added distortion.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage	pin 7	$V_P = V_{7-3}$	–	+21	V
	pin 5	$-V_P = V_{5-3}$	–	−21	V
Non-repetitive peak output current	pins 4 and 6	I_{OSM}	–	4	A
Total power dissipation	see Fig. 2	P_{tot}			
Storage temperature range		T_{stg}	−55	+ 150	°C
Junction temperature		T_j	–	150	°C
Short-circuit time: outputs short-circuited to ground (full signal drive)	see note				
	symmetrical power supply	t_{sc}	–	1	hour
	asymmetrical power supply	t_{sc}	–	1	hour

Note

For asymmetrical power supplies (at short circuiting of the load) the maximum supply voltage is limited to V_P = 28 V.

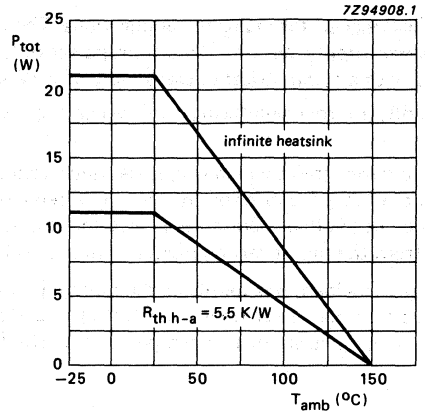


Fig. 2 Power derating curve.

THERMAL RESISTANCE

From junction to case $R_{th\ j-c} = 6$ K/W

HEATSINK DESIGN EXAMPLE

With derating of 6 K/W, the value of heatsink thermal resistance is calculated as follows:

given $R_L = 8\ \Omega$ and $V_P = \pm 12$ V, the measured maximum dissipation is 7,8 W; then, for a maximum ambient temperature of 60 °C, the required thermal resistance of the heatsink is

$$R_{th\ h-a} = \frac{150 - 60}{7,8} - 6 = 5,5\ \text{K/W}$$

Note: The metal tab (heatsink) has the same potential as pin 5 ($-V_P$).

CHARACTERISTICS

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage range						
operating mode		V_P	± 7,5	± 12,0	± 20,0	V
input mute mode		V_P	± 2,0	–	± 5,8	V
Repetitive peak output current		I_{ORM}	–	–	2,2	A
Operating mode: symmetrical power supply; test circuit as per Fig. 11; V_P = ± 12 V; R_L = 8 Ω; T_{amb} = 25 °C; f = 1 kHz						
Total quiescent current	without R_L	I_{tot}	18	40	70	mA
Output power	THD = 0,5%	P_o	5	6	–	W
	THD = 10%	P_o	6,5	8,0	–	W
Total harmonic distortion	P_o = 4 W	THD	–	0,15	0,2	%
Power bandwidth	THD = 0,5% note 1	B		20 to 16 k		Hz
Voltage gain		G_v	29	30	31	dB
Gain balance		ΔG_v	–	0,2	1,0	dB
Noise output voltage (r.m.s. value); unweighted (20 Hz to 20 kHz)	R_S = 2 kΩ	$V_{no(rms)}$	–	70	140	μV
Input impedance		$\|Z_i\|$	14	20	26	kΩ
Ripple rejection	note 2	SVRR	40	60	–	dB
Channel separation	R_S = 0 Ω	α	46	70	–	dB
Input bias current		I_{ib}	–	0,3	–	μA
DC output offset voltage	with respect to ground	V_{OFF}	–	30	200	mV
Input mute mode: symmetrical power supply; test circuit as per Fig. 11; V_P = ± 4 V; R_L = 8 Ω; T_{amb} = 25 °C; f = 1 kHz						
Total quiescent current	without R_L	I_{tot}	9	30	40	mA
Output voltage	V_i = 600 mV	V_{out}	–	0,6	1,8	mV
Noise output voltage (r.m.s. value); unweighted (20 Hz to 20 kHz)	R_S = 2 kΩ	$V_{no(rms)}$	–	70	140	μV
Ripple rejection	note 2	SVRR	35	55	–	dB
DC output offset voltage	with respect to ground	V_{OFF}	–	40	200	mV

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Operating mode: asymmetrical power supply; test circuit as per Fig. 12; V_P = 24 V; R_L = 8 Ω; T_{amb} = 25 °C; f = 1 kHz						
Total quiescent current		I_{tot}	18	40	70	mA
Output power	THD = 0,5%	P_o	5	6	–	W
	THD = 10%	P_o	6,5	8	–	W
Total harmonic distortion	P_o = 4 W	THD	–	0,13	0,2	%
Power bandwidth	THD = 0,5% note 1	B		40 to 16 k		Hz
Voltage gain		G_v	29	30	31	dB
Gain balance		ΔG_v	–	0,2	1,0	dB
Noise output voltage (r.m.s. value); unweighted (20 Hz to 20 kHz)	R_S = 2 kΩ	$V_{no(rms)}$	–	70	140	μV
Input impedance		$\|Z_i\|$	14	20	26	kΩ
Ripple rejection		SVRR	35	44	–	dB
Channel separation	R_S = 0 Ω	α	–	45	–	dB

Notes to the characteristics

1. Power bandwidth at $P_{o\ max}$ −3 dB.
2. Ripple rejection at R_S = 0 Ω, f = 100 Hz to 20 kHz; ripple voltage = 200 mV (r.m.s. value) applied to positive or negative supply rail.

APPLICATION INFORMATION

Input mute circuit

The input mute circuit operates only during switching on and off of the supply voltage. The circuit compares the ½ supply voltage (at pin 3) with an internally fixed reference voltage (V_{ref}), derived directly from the supply voltage. When the voltage at pin 3 is lower than V_{ref} the non-inverting inputs (pins 1 and 9) are disconnected from the amplifier. The voltage at pin 3 is determined by an internal voltage divider and the external 100 μF capacitor.
During switching on, a time delay is created between the reference voltage and the voltage at pin 3, during which the input terminal is disconnected, (as illustrated in Fig. 3).

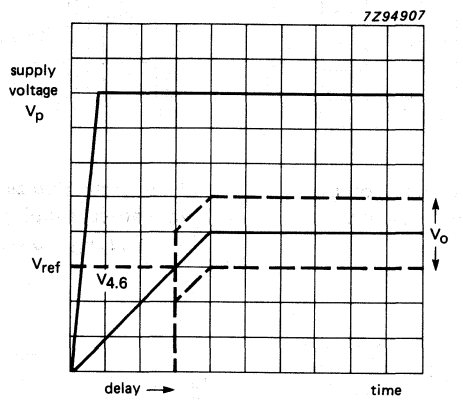


Fig. 3 Input mute circuit; time delay.

APPLICATION INFORMATION (continued)

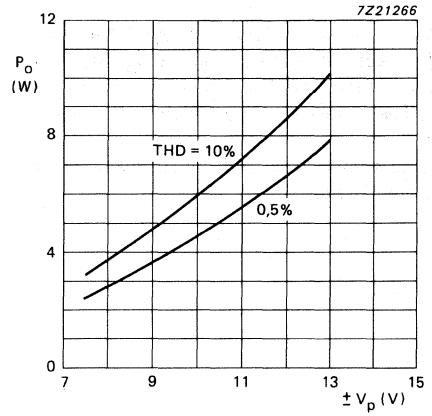


Fig. 4 Output power as a function of supply voltage; symmetrical supply; $R_L = 8\ \Omega$; f = 1 kHz.

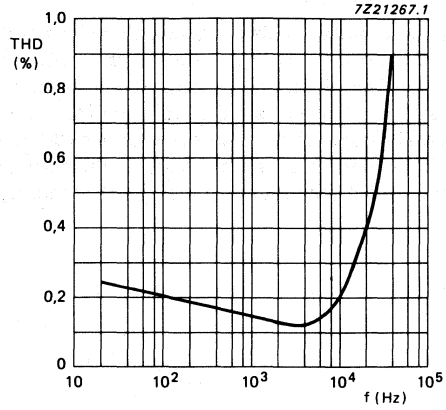


Fig. 5 Distortion as a function of frequency; symmetrical supply; $V_p = \pm 12$ V; $R_L = 8\ \Omega$; $P_o = 3$ W.

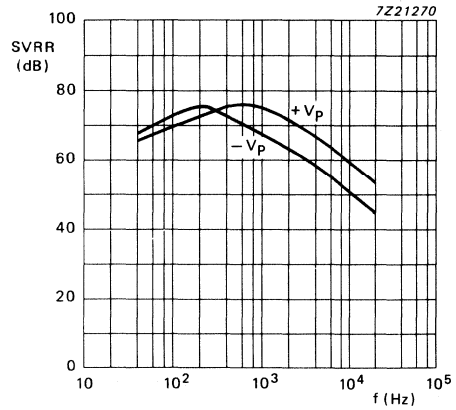


Fig. 6 Supply voltage ripple rejection; symmetrical supply, $V_P = \pm 12$ V; $V_{RR} = 200$ mV.

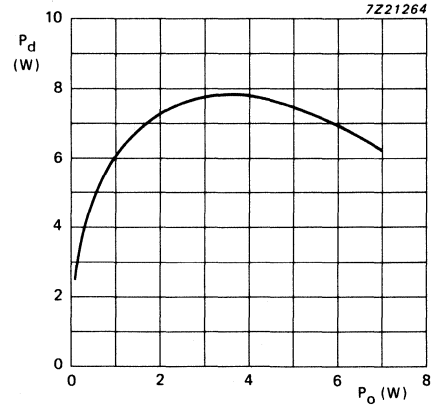


Fig. 7 Power dissipation as a function of output power; asymmetrical supply; $V_S = 24$ V; $R_L = 8\ \Omega$; f = 1 kHz.

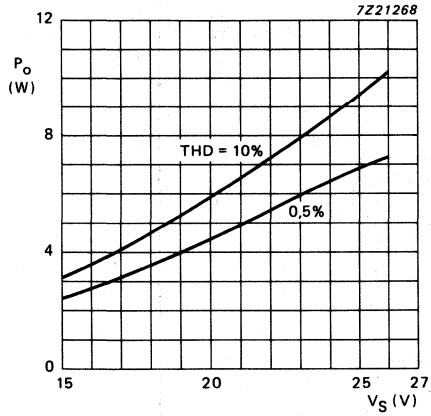


Fig. 8 Output power as a function of supply voltage; asymmetrical supply; $R_L = 8\ \Omega$; f = 1 kHz.

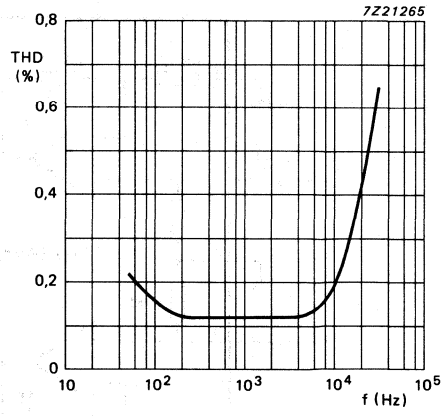


Fig. 9 Distortion as a function of frequency; asymmetrical supply; $V_S = 24$ V; $R_L = 8\ \Omega$; $P_o = 3$ W.

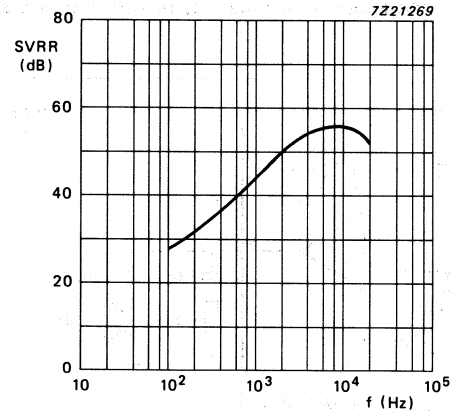
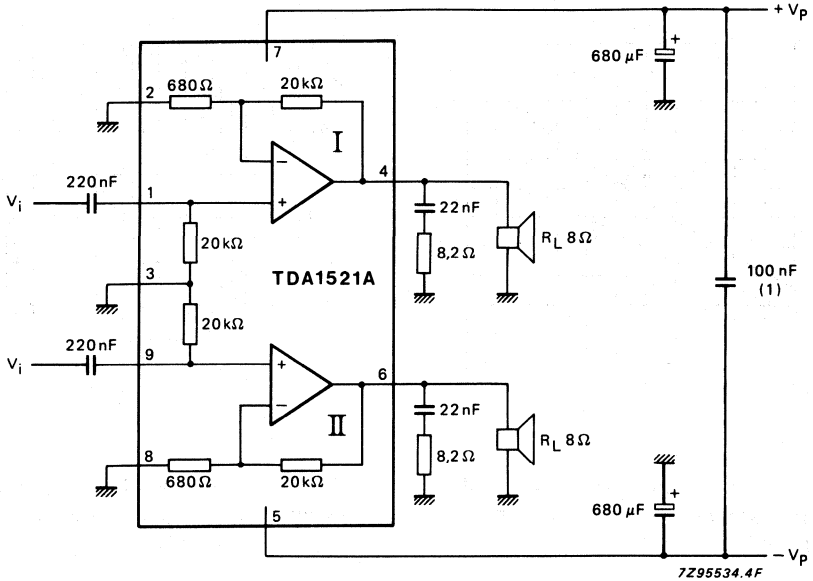


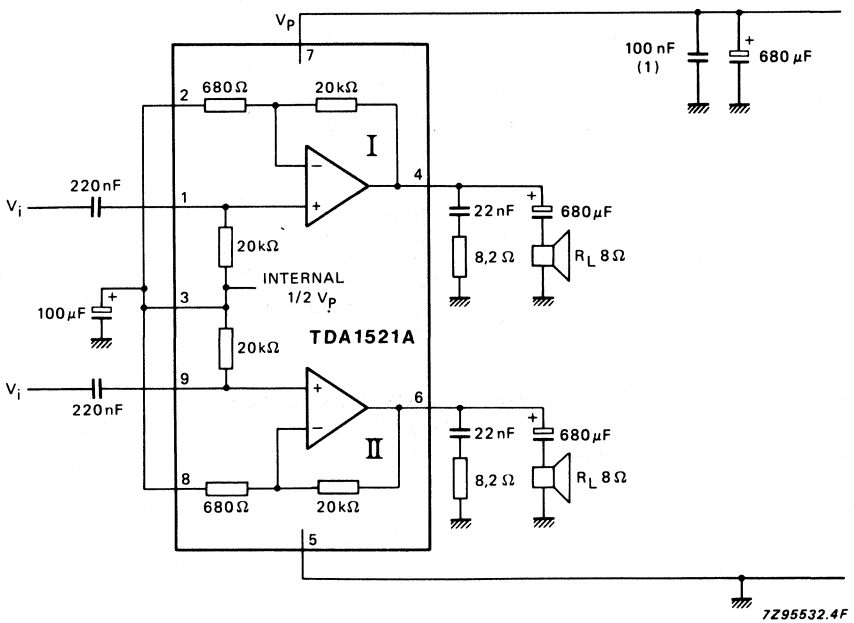
Fig. 10 Supply voltage ripple rejection; asymmetrical supply; $V_S = 24$ V; $V_{RR} = 200$ mW.

APPLICATION INFORMATION (continued)



(1) To be connected as close as possible to the I.C.

Fig. 11 Test and application circuit; symmetrical power supply.



(1) To be connected as close as possible to the I.C.

Fig. 12 Test and application circuit; asymmetrical power supply.

STEREO-TONE/VOLUME CONTROL CIRCUIT

GENERAL DESCRIPTION

The device is designed as an active stereo-tone/volume control for car radios, TV receivers and mains-fed equipment. It includes functions for bass and treble control, volume control with built-in contour (can be switched off) and balance. All these functions can be controlled by d.c. voltages or by single linear potentiometers.

Features

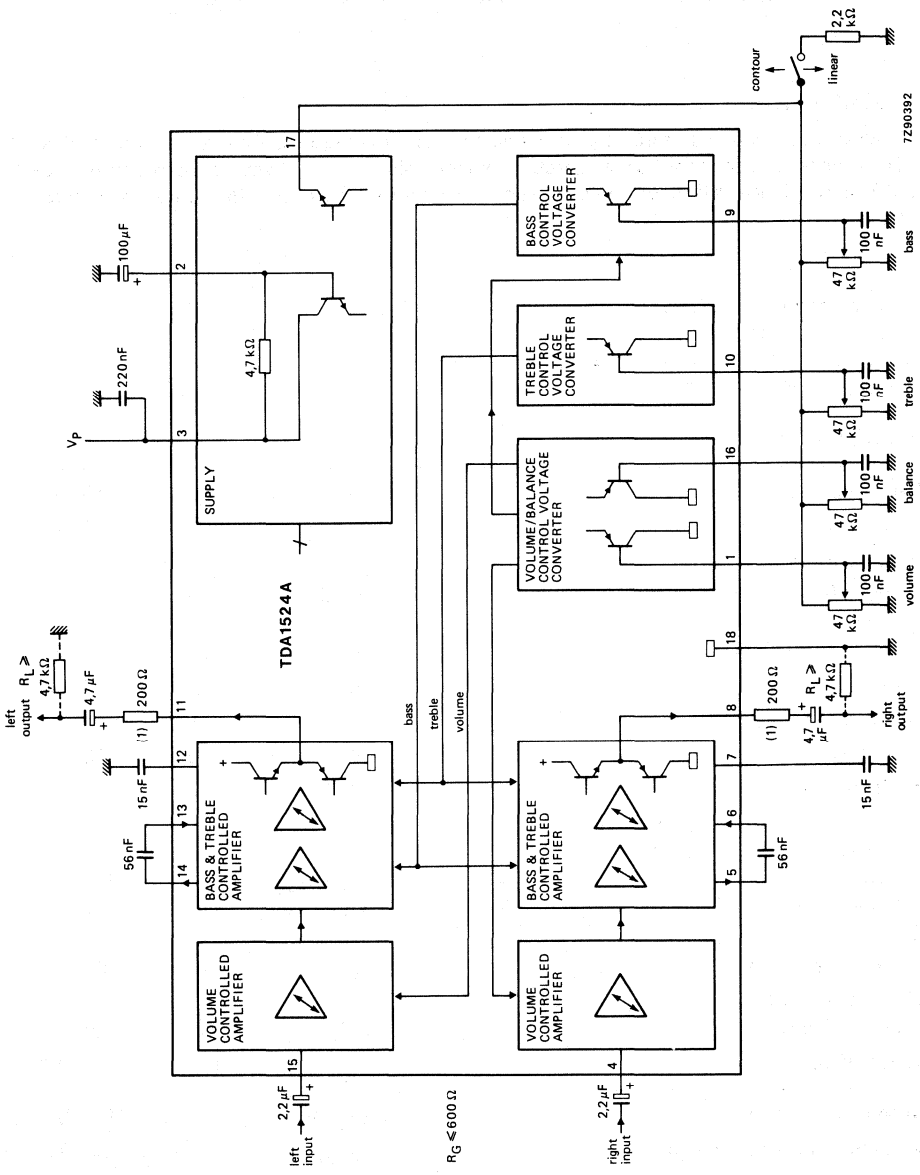
- Few external components necessary
- Low noise due to internal gain
- Bass emphasis can be increased by a double-pole low-pass filter
- Wide power supply voltage range

QUICK REFERENCE DATA

Supply voltage (pin 3)	$V_P = V_{3-18}$	typ.	12	V
Supply current (pin 3)	$I_P = I_3$	typ.	35	mA
Maximum input signal with d.c. feedback (r.m.s. value)	$V_{i(rms)}$	typ.	2,5	V
Maximum output signal with d.c. feedback (r.m.s. value)	$V_{o(rms)}$	typ.	3	V
Volume control range	G_v		−80 to + 21,5	dB
Bass control range at 40 Hz	ΔG_v		−19 to + 17	dB
Treble control range at 16 kHz	ΔG_v	typ.	± 15	dB
Total harmonic distortion	THD	typ.	0,3	%
Output noise voltage (unweighted; r.m.s. value) at f = 20 Hz to 20 kHz; V_P = 12 V;				
for max. voltage gain	$V_{no(rms)}$	typ.	310	μV
for voltage gain G_v = −40 dB	$V_{no(rms)}$	typ.	100	μV
Channel separation at G_v = −20 to + 21,5 dB	α_{cs}	typ.	60	dB
Tracking between channels at G_v = −20 to + 26 dB	ΔG_v	max.	2,5	dB
Ripple rejection at 100 Hz	RR	typ.	50	dB
Supply voltage range (pin 3)	$V_P = V_{3-18}$		7,5 to 16,5	V
Operating ambient temperature range	T_{amb}		−30 to + 80	°C

PACKAGE OUTLINE

18-lead DIL; plastic (SOT102).



(1) Series resistor is recommended in the event of the capacitive loads exceeding 200 pF.

Fig. 1 Block diagram and application circuit with single-pole filter.

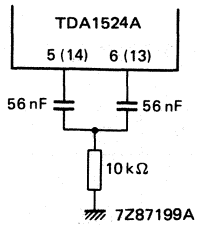


Fig. 2 Double-pole low-pass filter for improved bass-boost.

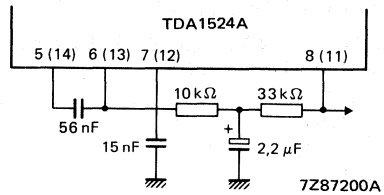


Fig. 3 D.C. feedback with filter network for improved signal handling.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 3)	$V_P = V_{3\text{-}18}$	max.	20 V
Total power dissipation	P_{tot}	max.	1200 mW
Storage temperature range	T_{stg}		−55 to + 150 °C
Operating ambient temperature range	T_{amb}		−30 to + 80 °C

D.C. CHARACTERISTICS

$V_P = V_{3-18} = 12$ V; $T_{amb} = 25$ °C; measured in Fig. 1; $R_G \leqslant 600\ \Omega$; $R_L \geqslant 4{,}7$ kΩ; $C_L \leqslant 200$ pF; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply (pin 3)					
Supply voltage	$V_P = V_{3-18}$	7,5	–	16,5	V
Supply current					
at $V_P = 8{,}5$ V	$I_P = I_3$	19	27	35	mA
at $V_P = 12$ V	$I_P = I_3$	25	35	45	mA
at $V_P = 15$ V	$I_P = I_3$	30	43	56	mA
D.C. input levels (pins 4 and 15)					
at $V_P = 8{,}5$ V	$V_{4,15-18}$	3,8	4,25	4,7	V
at $V_P = 12$ V	$V_{4,15-18}$	5,3	5,9	6,6	V
at $V_P = 15$ V	$V_{4,15-18}$	6,5	7,3	8,2	V
D.C. output levels (pins 8 and 11) under all control voltage conditions with d.c. feedback (Fig. 3)					
at $V_P = 8{,}5$ V	$V_{8,11-18}$	3,3	4,25	5,2	V
at $V_P = 12$ V	$V_{8,11-18}$	4,6	6,0	7,4	V
at $V_P = 15$ V	$V_{8,11-18}$	5,7	7,5	9,3	V
Pin 17					
Internal potentiometer supply voltage					
at $V_P = 8{,}5$ V	V_{17-18}	3,5	3,75	4,0	V
Contour on/off switch (control by I_{17})					
contour (switch open)	$-I_{17}$	–	–	0,5	mA
linear (switch closed)	$-I_{17}$	1,5	–	10	mA
Application without internal potentiometer supply voltage at $V_P \geqslant 10{,}8$ V (contour cannot be switched off)					
Voltage range forced to pin 17	V_{17-18}	4,5	–	$V_P/2-V_{BE}$	V
D.C. control voltage range for volume, bass, treble and balance (pins 1, 9, 10 and 16 respectively)					
at $V_{17-18} = 5$ V	$V_{1,9,10,16}$	1,0	–	4,25	V
using internal supply	$V_{1,9,10,16}$	0,25	–	3,8	V
Input current of control inputs (pins 1, 9, 10 and 16)	$-I_{1,9,10,16}$	–	–	5	μA

A.C. CHARACTERISTICS

$V_P = V_{3-18} = 8{,}5$ V; $T_{amb} = 25\ ^oC$; measured in Fig. 1; contour switch closed (linear position); volume, balance, bass, and treble controls in mid-position; $R_G \leqslant 600\ \Omega$; $R_L \geqslant 4{,}7$ kΩ; $C_L \leqslant 200$ pF; f = 1 kHz; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Control range					
Max. gain of volume (Fig. 5)	$G_{V\ max}$	20,5	21,5	23	dB
Volume control range; $G_{V\ max}/G_{V\ min}$	ΔG_V	90	100	–	dB
Balance control range; $G_V = 0$ dB (Fig. 6)	ΔG_V	–	−40	–	dB
Bass control range at 40 Hz (Fig. 7)	ΔG_V	–	−19 to + 17 ± 3		dB
Treble control range at 16 kHz (Fig. 8)	ΔG_V	–	± 15 ± 3	–	dB
Contour characteristics		see Figs 9 and 10			
Signal inputs, outputs					
Input resistance; pins 4 and 15 (note 1) at gain of volume control: $G_V = 20$ dB	$R_{i4,15}$	10	–	–	kΩ
$G_V = -40$ dB	$R_{i4,15}$	–	160	–	kΩ
Output resistance (pins 8 and 11)	$R_{o8,11}$	–	–	300	Ω
Signal processing					
Power supply ripple rejection at $V_{P(rms)} \leqslant 200$ mV; f = 100 Hz; $G_V = 0$ dB	RR	35	50	–	dB
Channel separation (250 Hz to 10 kHz) at $G_V = -20$ to + 21,5 dB	α_{cs}	46	60	–	dB
Spread of volume control with constant control voltage $V_{1-18} = 0{,}5\ V_{17-18}$	ΔG_V	–	–	±3	dB
Gain tolerance between left and right channel $V_{16-18} = V_{1-18} = 0{,}5\ V_{17-18}$	$\Delta G_{V,L-R}$	–	–	1,5	dB
Tracking between channels for $G_V = 21{,}5$ to −26 dB f = 250 Hz to 6,3 kHz; balance adjusted at $G_V = 10$ dB	ΔG_V	–	–	2,5	dB

A.C. CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Signal handling with d.c. feedback (Fig. 3)					
Input signal handling					
at V_P = 8,5 V; THD = 0,5%; f = 1 kHz (r.m.s. value)	$V_{i(rms)}$	1,4	–	–	V
at V_P = 8,5 V; THD = 0,7%; f = 1 kHz (r.m.s. value)	$V_{i(rms)}$	1,8	2,4	–	V
at V_P = 12 V; THD = 0,5%; f = 40 Hz to 16 kHz (r.m.s. value)	$V_{i(rms)}$	1,4	–	–	V
at V_P = 12 V; THD = 0,7%; f = 40 Hz to 16 kHz (r.m.s. value)	$V_{i(rms)}$	2,0	3,2	–	V
at V_P = 15 V; THD = 0,5%; f = 40 Hz to 16 kHz (r.m.s. value)	$V_{i(rms)}$	1,4	–	–	V
at V_P = 15 V; THD = 0,7%; f = 40 Hz to 16 kHz (r.m.s. value)	$V_{i(rms)}$	2,0	3,2	–	V
Output signal handling (note 2 and note 3)					
at V_P = 8,5 V; THD = 0,5%; f = 1 kHz (r.m.s. value)	$V_{o(rms)}$	1,8	2,0	–	V
at V_P = 8,5 V; THD = 10%; f = 1 kHz (r.m.s. value)	$V_{o(rms)}$	–	2,2	–	V
at V_P = 12 V; THD = 0,5%; f = 40 Hz to 16 kHz (r.m.s. value)	$V_{o(rms)}$	2,5	3,0	–	V
at V_P = 15 V; THD = 0,5%; f = 40 Hz to 16 kHz (r.m.s. value)	$V_{o(rms)}$	–	3,5	–	V
Noise performance (V_P = 8,5 V)					
Output noise voltage (unweighted; Fig. 15)					
at f = 20 Hz to 20 kHz (r.m.s. value)					
for maximum voltage gain (note 4)	$V_{no(rms)}$	–	260	–	μV
for G_v = −3 dB (note 4)	$V_{no(rms)}$	–	70	140	μV
Output noise voltage; weighted as DIN 45405 of 1981, CCIR recommendation 468-2 (peak value)					
for maximum voltage gain (note 4)	$V_{no(m)}$	–	890	–	μV
for maximum emphasis of bass and treble (contour off; G_v = −40 dB)	$V_{no(m)}$	–	360	–	μV
Noise performance (V_P = 12 V)					
Output noise voltage (unweighted; Fig. 15)					
at f = 20 Hz to 20 kHz (r.m.s. value; note 5)					
for maximum voltage gain (note 4)	$V_{no(rms)}$	–	310	–	μV
for G_v = −16 dB (note 4)	$V_{no(rms)}$	–	100	200	μV
Output noise voltage; weighted as DIN 45405 of 1981, CCIR recommendation 468-2 (peak value)					
for maximum voltage gain (note 4)	$V_{no(m)}$	–	940	–	μV
for maximum emphasis of bass and treble (contour off; G_v = −40 dB)	$V_{no(m)}$	–	400	–	μV

parameter	symbol	min.	typ.	max.	unit
Noise performance (V_P = 15 V)					
Output noise voltage (unweighted; Fig. 15)					
at f = 20 Hz to 20 kHz (r.m.s. value; note 5)					
for maximum voltage gain (note 4)	$V_{no(rms)}$	–	350	–	μV
for G_V = 16 dB (note 4)	$V_{no(rms)}$	–	110	220	μV
Output noise voltage; weighted as DIN 45405					
of 1981, CCIR recommendation 468-2 (peak value)					
for maximum voltage gain (note 4)	$V_{no(m)}$	–	980	–	μV
for maximum emphasis of bass and treble					
(contour off; G_V = −40 dB)	$V_{no(m)}$	–	420	–	μV

Notes to characteristics

1. Equation for input resistance (see also Fig. 4)

$$R_i = \frac{160\ k\Omega}{1 + G_V}\ ;\ G_{V\ max} = 12.$$

2. Frequencies below 200 Hz and above 5 kHz have reduced voltage swing, the reduction at 40 Hz and at 16 kHz is 30%.
3. In the event of bass boosting the output signal handling is reduced. The reduction is 1 dB for maximum bass boost.
4. Linear frequency response.
5. For peak values add 4,5 dB to r.m.s. values.

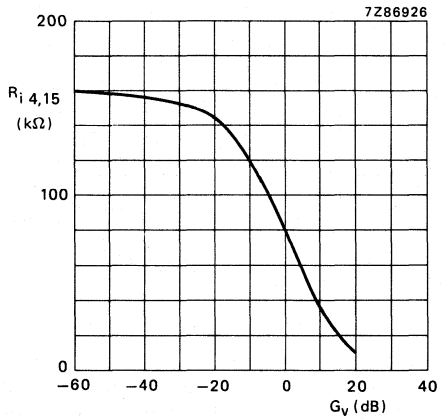


Fig. 4 Input resistance (R_i) as a function of gain of volume control (G_V). Measured in Fig. 1.

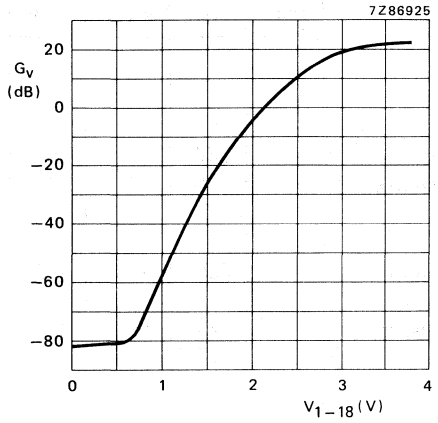


Fig. 5 Volume control curve; voltage gain (G_V) as a function of control voltage (V_{1-18}). Measured in Fig. 1 (internal potentiometer supply from pin 17 used); V_P = 8,5 V; f = 1 kHz.

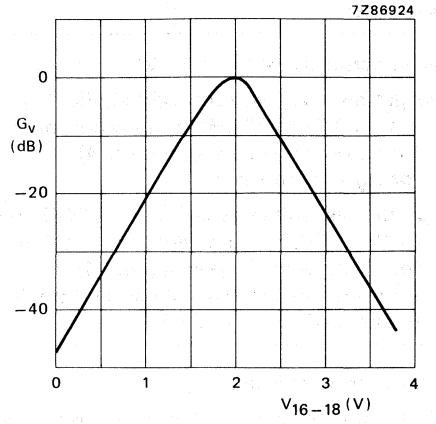


Fig. 6 Balance control curve; voltage gain (G_V) as a function of control voltage (V_{16-18}). Measured in Fig. 1 (internal potentiometer supply from pin 17 used); V_P = 8,5 V.

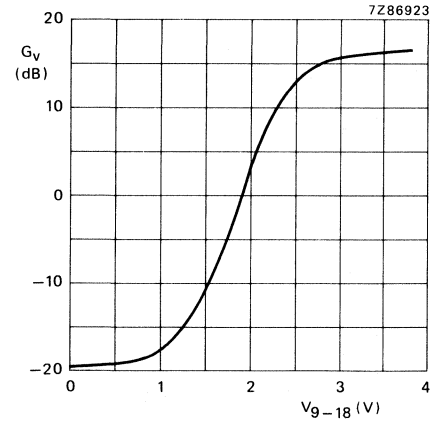


Fig. 7 Bass control curve; voltage gain (G_V) as a function of control voltage (V_{9-18}). Measured in Fig. 1 with single-pole filter (internal potentiometer supply from pin 17 used); V_P = 8,5 V; f = 40 Hz.

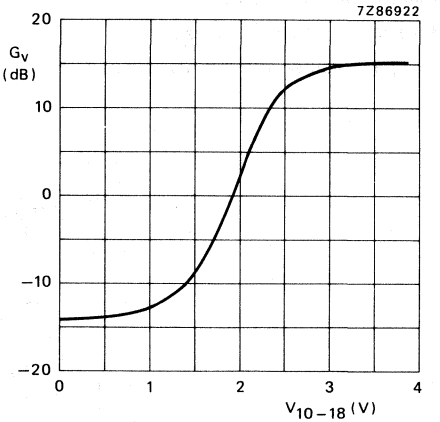


Fig. 8 Treble control curve; voltage gain (G_V) as a function of control voltage (V_{10-18}). Measured in Fig. 1 (internal potentiometer supply from pin 17 used); V_P = 8,5 V; f = 16 kHz.

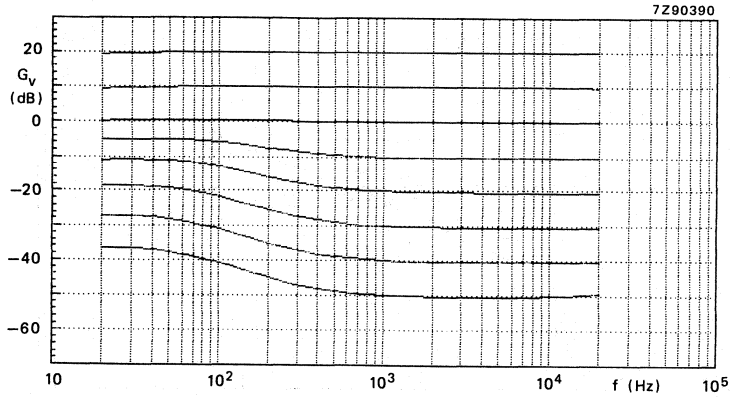


Fig. 9 Contour frequency response curves; voltage gain (G_V) as a function of audio input frequency. Measured in Fig. 1 with single-pole filter; V_P = 8,5 V.

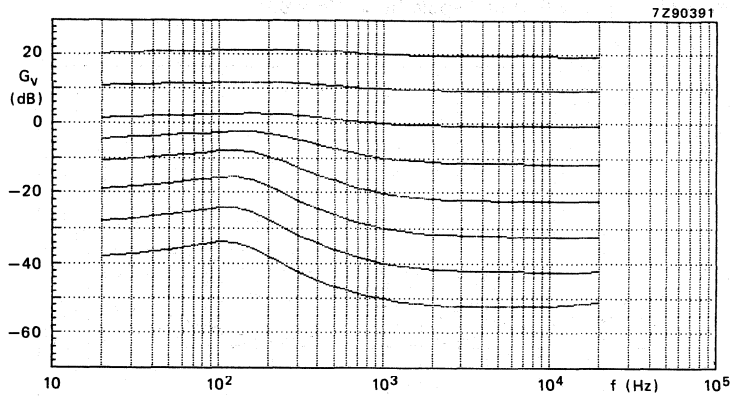


Fig. 10 Contour frequency response curves; voltage gain (G_V) as a function of audio input frequency. Measured in Fig. 1 with double-pole filter; V_P = 8,5 V.

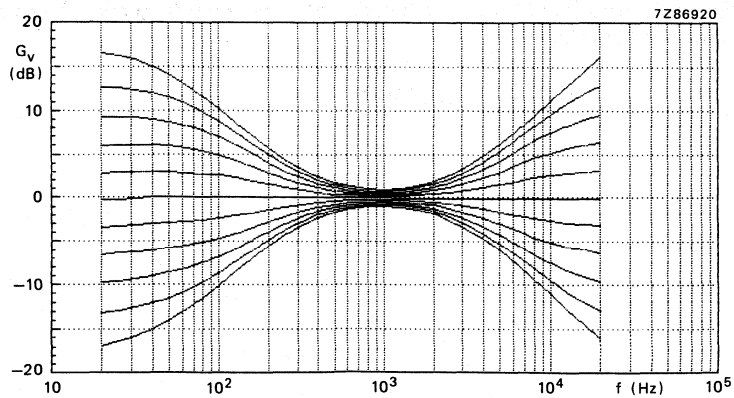


Fig. 11 Tone control frequency response curves; voltage gain (G_V) as a function of audio input frequency. Measured in Fig. 1 with single-pole filter; V_P = 8,5 V.

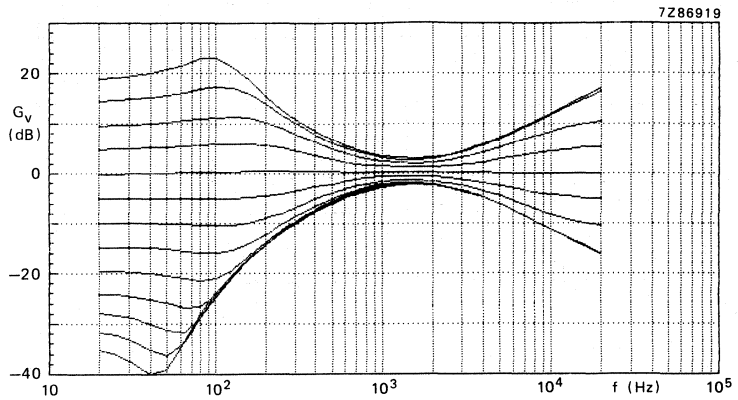


Fig. 12 Tone control frequency response curves; voltage gain (G_V) as a function of audio input frequency. Measured in Fig. 1 with double-pole filter; V_P = 8,5 V.

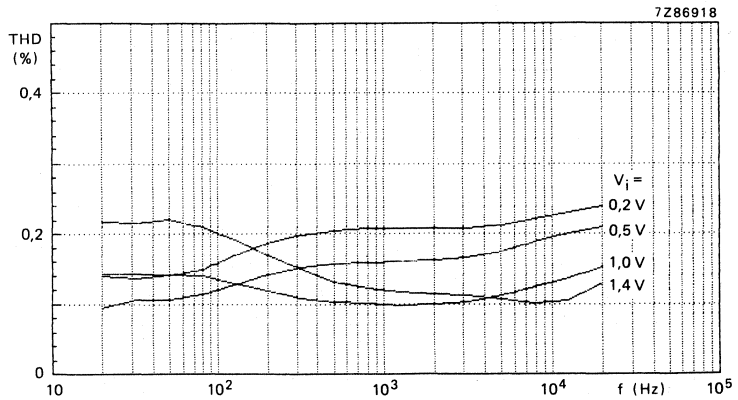


Fig. 13 Total harmonic distortion (THD); as a function of audio input frequency. Measured in Fig. 1; V_P = 8,5 V; volume control voltage gain at

$$G_V = 20 \log \frac{V_o}{V_i} = 0 \text{ dB}.$$

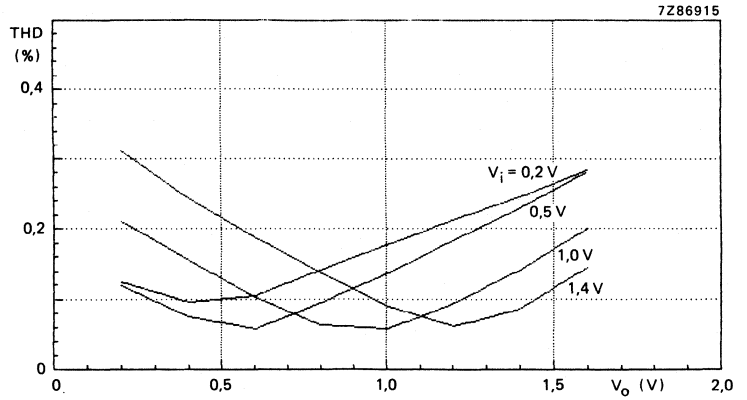
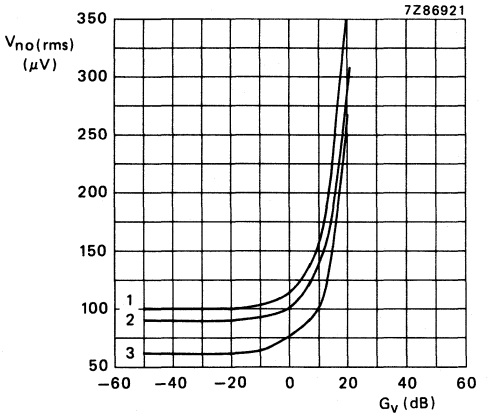


Fig. 14 Total harmonic distortion (THD); as a function of output voltage (V_O). Measured in Fig. 1; V_P = 8,5 V; f_i = 1 kHz.



(1) V_P = 15 V.
(2) V_P = 12 V.
(3) V_P = 8,5 V.

Fig. 15 Noise output voltage ($V_{no(rms)}$; unweighted); as a function of voltage gain (G_V). Measured in Fig. 1; f = 20 Hz to 20 kHz.

STEREO-TONE/VOLUME CONTROL CIRCUIT

GENERAL DESCRIPTION

The device is designed as an active stereo-tone/volume control for car radios, TV receivers and mains-fed equipment. It includes functions for bass and treble control, volume control with built-in contour (can be switched off) and balance. All these functions can be controlled by DC voltages or by single linear potentiometers.

Features

- Few external components necessary
- Low noise due to internal gain
- Bass emphasis can be increased by a double-pole low-pass filter
- Wide power supply voltage range

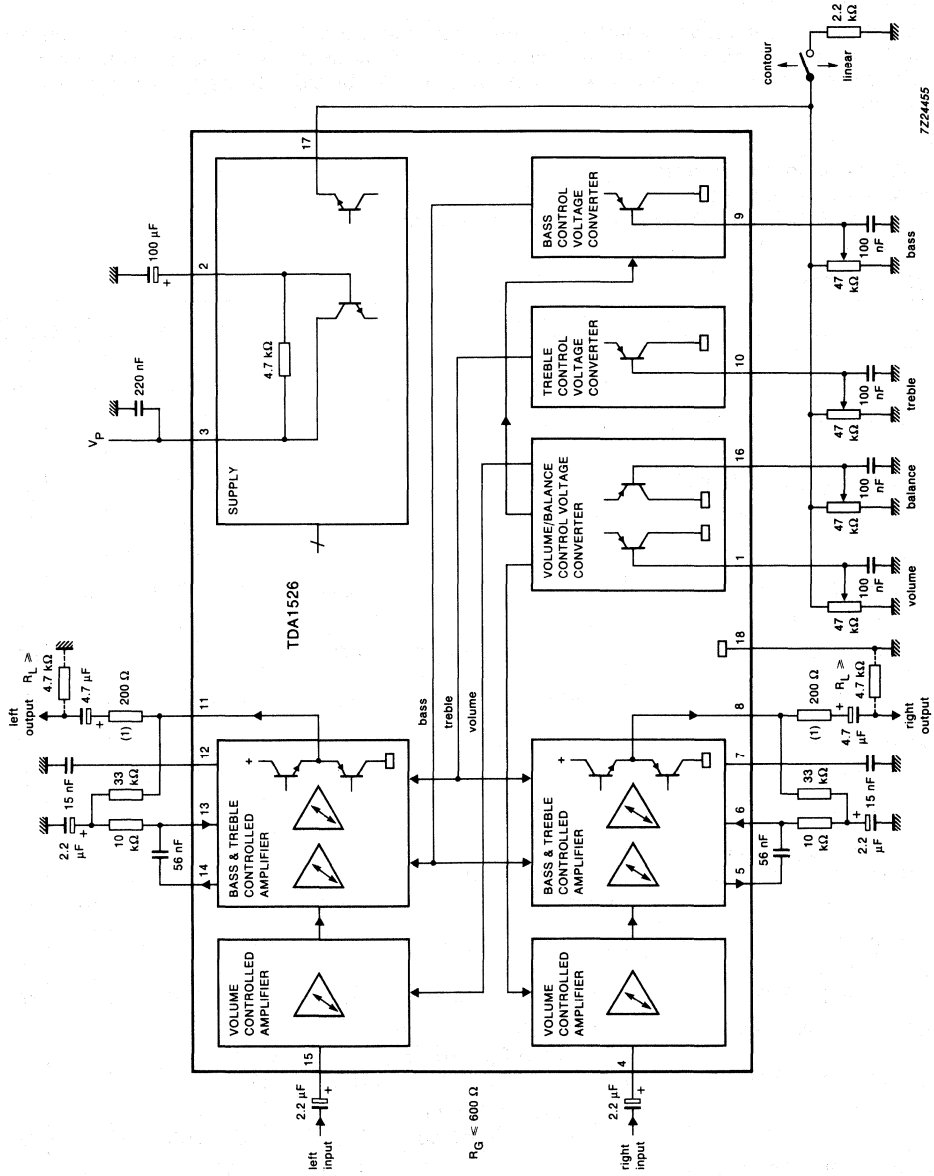
QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage (pin 3)		V_P	7.5	12	16.5	V
Supply current (pin 3)	V_P = 12 V	I_P	25	35	45	mA
Signal handling with DC feedback	V_P = 8.5 to 15 V; THD = 0.7%; f = 1 kHz					
Input signal handling (RMS value)		$V_{i(rms)}$	1.8	2.0	–	V
Output signal handling (RMS value)	notes 2 and 3	$V_{o(rms)}$	1.8	2.0	–	V
Control range						
Maximum gain of volume	see Fig. 4	$G_{V\,max}$	20.5	21.5	23	dB
Volume control range	$G_{V\,max}/G_{V\,min}$	ΔG_V	90	100	–	dB
Balance control range	G_V = 0 dB; see Fig. 5	ΔG_V	–	–40	–	dB
Bass control range	at 40 Hz; see Fig. 6	ΔG_V	–	–19 to +17 ±3	–	dB
Treble control range	at 16 kHz; see Fig. 7	ΔG_V	–	±15 ±3	–	dB
Total harmonic distortion		THD	–	–	0.5	%
Noise performance	V_P = 12 V					
Output noise voltage (unweighted) at f = 20 Hz to 20 kHz for G_V = –16 dB	RMS value; note 4 note 5	$V_{no(rms)}$	–	100	200	μV
Signal processing						
Channel separation at G_V = –20 to 21.5 dB	f = 250 Hz to 10 kHz	α_{cs}	46	60	–	dB
Tracking between channels for G_V = 21.5 to –26 dB	f = 250 Hz to 6.3 kHz; balance at G_V = 10 dB	ΔG_V	–	–	2.5	dB
Ripple rejection	$V_{P(rms)} = \leqslant 200$ mV; f = 100 Hz; G_V = 0 dB	RR	35	50	–	dB
Operating ambient temperature range		T_{amb}	–30	–	+85	°C

For explanation of notes see **Notes to the characteristics.**

PACKAGE OUTLINE

18-lead DIL; plastic (SOT102).



(1) Series resistor is recommended in the event of the capacitive loads exceeding 200 pF.

Fig.1 Block diagram and application circuit with single-pole filter.

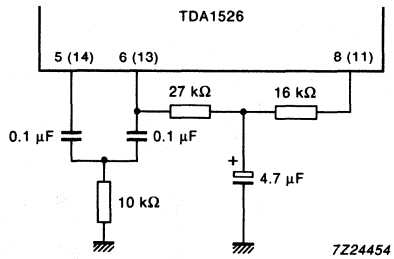


Fig.2 Double-pole low-pass filter for improved bass-boost.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage (pin 3)	V_P	–	20	V
Total power dissipation	P_{tot}	–	1200	mW
Storage temperature range	T_{stg}	–55	+ 150	°C
Operating ambient temperature range	T_{amb}	–30	+ 80	°C

DC CHARACTERISTICS

$V_P = V_{3-18} = 12$ V; $T_{amb} = 25$ °C; measured in Fig. 1; $R_G \leqslant 600\ \Omega$; $R_L \geqslant 4.7$ kΩ; $C_L \leqslant 200$ pF; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply (pin 3)					
Supply voltage	$V_P = V_{3-18}$	7.5	–	16.5	V
Supply current					
at V_P = 8.5 V	$I_P = I_3$	19	27	35	mA
at V_P = 12 V	$I_P = I_3$	25	35	45	mA
at V_P = 15 V	$I_P = I_3$	30	43	56	mA
DC input levels (pins 4 and 15)					
at V_P = 8.5 V	$V_{4,15-18}$	3.8	4.25	4.7	V
at V_P = 12 V	$V_{4,15-18}$	5.3	5.9	6.6	V
at V_P = 15 V	$V_{4,15-18}$	6.5	7.3	8.2	V
DC output levels (pins 8 and 11) under all control voltage conditions with DC feedback					
at V_P = 8.5 V	$V_{8,11-18}$	3.3	4.25	5.2	V
at V_P = 12 V	$V_{8,11-18}$	4.6	6.0	7.4	V
at V_P = 15 V	$V_{8,11-18}$	5.7	7.5	9.3	V
Pin 17					
Internal potentiometer supply voltage					
at V_P = 8.5 V	V_{17-18}	3.5	3.75	4.0	V
Contour on/off switch (control by I_{17})					
contour (switch open)	$-I_{17}$	–	–	0.5	mA
linear (switch closed)	$-I_{17}$	1.5	–	10	mA
Application without internal potentiometer supply voltage at $V_P \geqslant 10.8$ V (contour cannot be switched off)					
Voltage range forced to pin 17	V_{17-18}	4.5	–	$V_P/2-V_{BE}$	V
DC control voltage range for volume, bass, treble and balance (pins 1, 9, 10 and 16 respectively)					
at V_{17-18} = 5 V	$V_{1,9,10,16}$	1.0	–	4.25	V
using internal supply	$V_{1,9,10,16}$	0.25	–	3.8	V
Input current of control inputs (pins 1, 9, 10 and 16)	$-I_{1,9,10,16}$	–	–	5	μA

AC CHARACTERISTICS

$V_P = V_{3-18} = 8.5$ V; $T_{amb} = 25$ °C; measured in Fig. 1; contour switch closed (linear position); volume, balance, bass, and treble controls in mid-position; $R_G \leqslant 600\ \Omega$; $R_L \geqslant 4.7$ kΩ; $C_L \leqslant 200$ pF; f = 1 kHz; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Control range					
Maximum gain of volume (Fig. 4)	$G_{V\,max}$	20.5	21.5	23	dB
Volume control range; $G_{V\,max}/G_{V\,min}$	ΔG_V	90	100	–	dB
Balance control range; G_V = 0 dB (Fig. 5)	ΔG_V	–	–40	–	dB
Bass control range at 40 Hz (Fig. 6)	ΔG_V	–	–19 to +17 ±3		dB
Treble control range at 16 kHz (Fig. 7)	ΔG_V	–	±15 ±3	–	dB
Contour characteristics		see Figs 9 and 10			
Signal inputs, outputs					
Input resistance; pins 4 and 15 (note 1)					
at gain of volume control: G_V = 20 dB	$R_{i4,15}$	10	–	–	kΩ
G_V = –40 dB	$R_{i4,15}$	–	160	–	kΩ
Output resistance (pins 8 and 11)	$R_{o8,11}$	–	–	300	Ω
Signal processing					
Power supply ripple rejection					
at $V_{P(rms)} \leqslant 200$ mV; f = 100 Hz; G_V = 0 dB	RR	35	50	–	dB
Channel separation (250 Hz to 10 kHz)					
at G_V = –20 to +21.5 dB	α_{cs}	46	60	–	dB
Spread of volume control with					
constant control voltage $V_{1-18} = 0.5\,V_{17-18}$	ΔG_V	–	–	±3	dB
Gain tolerance between left and right					
channel $V_{16-18} = V_{1-18} = 0.5\,V_{17-18}$	$\Delta G_{V,L-R}$	–	–	1.5	dB
Tracking between channels					
for G_V = 21.5 to –26 dB					
f = 250 Hz to 6.3 kHz; balance adjusted at					
G_V = 10 dB	ΔG_V	–	–	2.5	dB

AC CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Signal handling with DC feedback					
Input signal handling at V_P = 8.5 V – 15 V; THD = 0.7%; f = 1 kHz (RMS value)	$V_{i(rms)}$	1.8	2.0	–	V
Output signal handling (note 2 and note 3) at V_P = 8.5 V; THD = 0.7%; f = 1 kHz (RMS value)	$V_{o(rms)}$	1.8	2.0	–	V
Noise performance (V_P = 12 V)					
Output noise voltage (unweighted; Fig. 14) at f = 20 Hz to 20 kHz (RMS value; note 4) for G_V = –16 dB (note 5)	$V_{no(rms)}$	–	100	200	μV

Notes to characteristics

1. Equation for input resistance (see also Fig. 3)

$$R_i = \frac{160\,k\Omega}{1 + G_V}; G_{V\,max} = 12.$$

2. Frequencies below 200 Hz and above 5 kHz have reduced voltage swing, the reduction at 40 Hz and at 16 kHz is 30%.
3. In the event of bass boosting the output signal handling is reduced. The reduction is 1 dB for maximum bass boost.
4. For peak values add 4.5 dB to RMS values.
5. Linear frequency response.

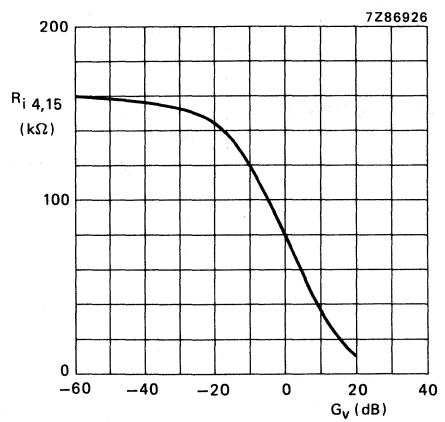


Fig.3 Input resistance (R_i) as a function of gain of volume control (G_V). Measured in Fig.1.

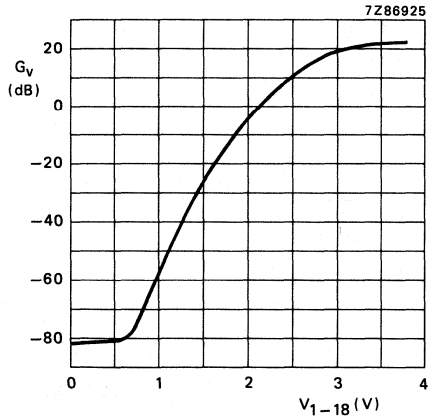


Fig.4 Volume control curve; voltage gain (G_V) as a function of control voltage ($V_{1\text{-}18}$). Measured in Fig.1 (internal potentiometer supply from pin 17 used); V_P = 8.5 V; f = 1 kHz.

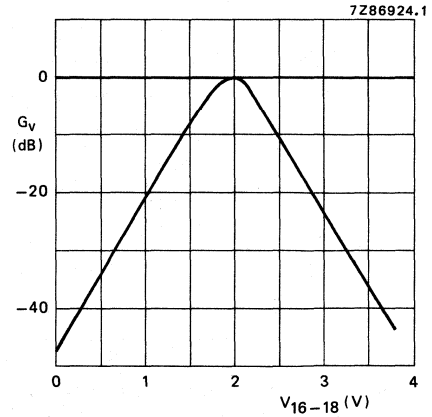


Fig.5 Balance control curve; voltage gain (G_V) as a function of control voltage ($V_{16\text{-}18}$). Measured in Fig.1 (internal potentiometer supply from pin 17 used); V_P = 8.5 V.

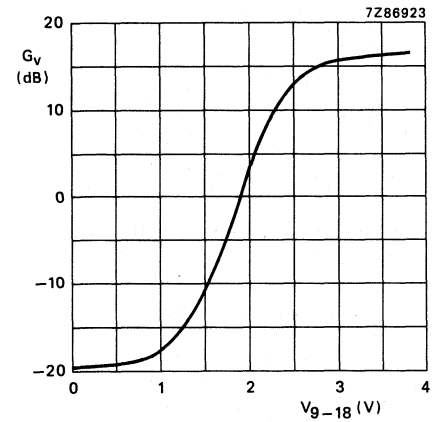


Fig.6 Bass control curve; voltage gain (G_V) as a function of control voltage ($V_{9\text{-}18}$). Measured in Fig.1 with single-pole filter (internal potentiometer supply from pin 17 used); V_P = 8.5 V; f = 40 Hz.

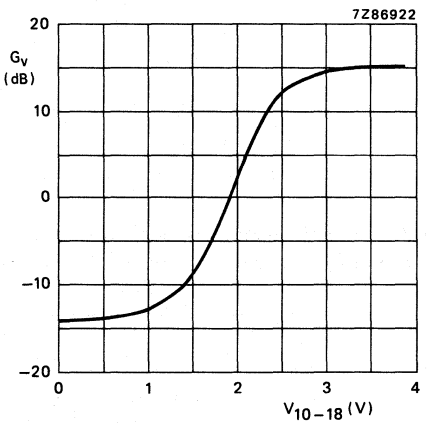


Fig.7 Treble control curve; voltage gain (G_V) as a function of control voltage ($V_{10\text{-}18}$). Measured in Fig.1 (internal potentiometer supply from pin 17 used); V_P = 8.5 V; f = 16 kHz.

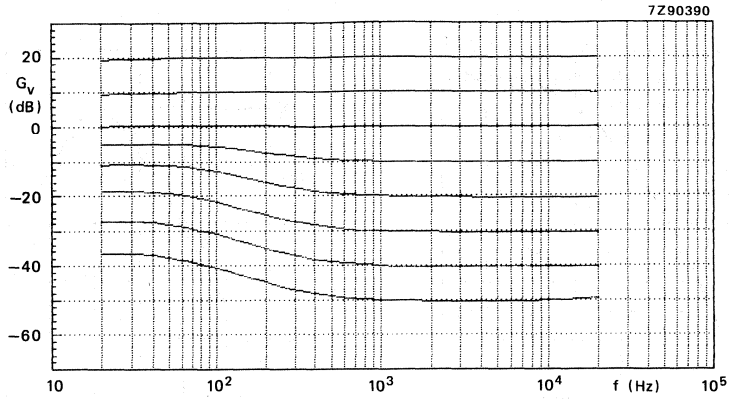


Fig.8 Contour frequency response curves; voltage gain (G_v) as a function of audio input frequency. Measured in Fig.1 with single-pole filter; V_P = 8.5 V.

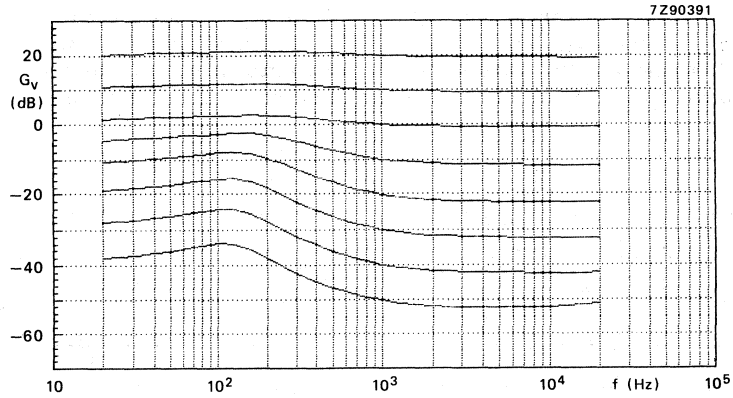


Fig.9 Contour frequency response curves; voltage gain (G_v) as a function of audio input frequency. Measured in Fig.1 with double-pole filter; V_P = 8.5 V.

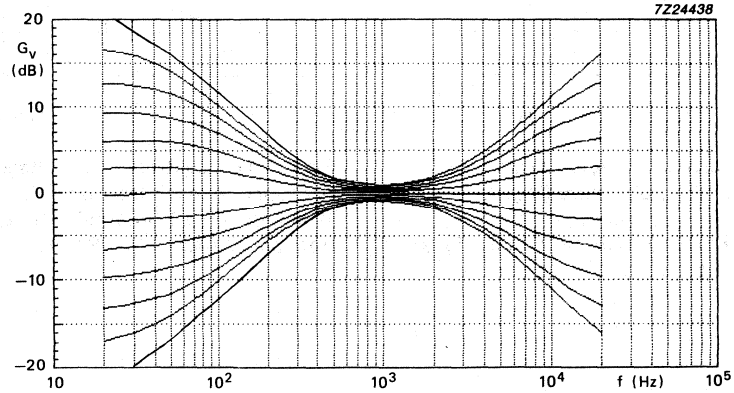


Fig.10 Tone control frequency response curves; voltage gain (G_v) as a function of audio input frequency. Measured in Fig.1 with single-pole filter; V_P = 8.5 V.

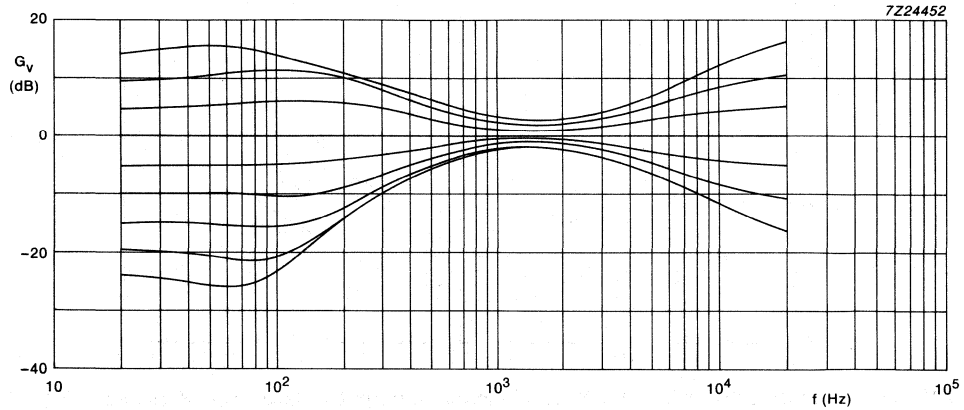


Fig.11 Tone control frequency response curves; voltage gain (G_V) as a function of audio input frequency. Measured in Fig.1 with double-pole filter; V_P = 8.5 V.

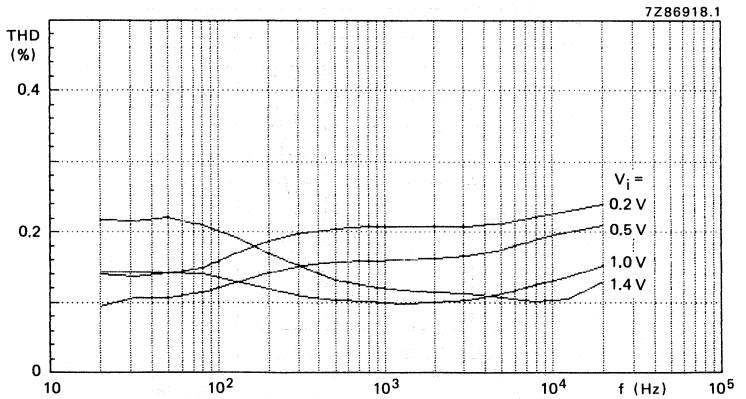


Fig.12 Total harmonic distortion (THD); as a function of audio input frequency. Measured in Fig.1; V_P = 8.5 V; volume control voltage gain at

$$G_V = 20 \log \frac{V_o}{V_i} = 0 \text{ dB}.$$

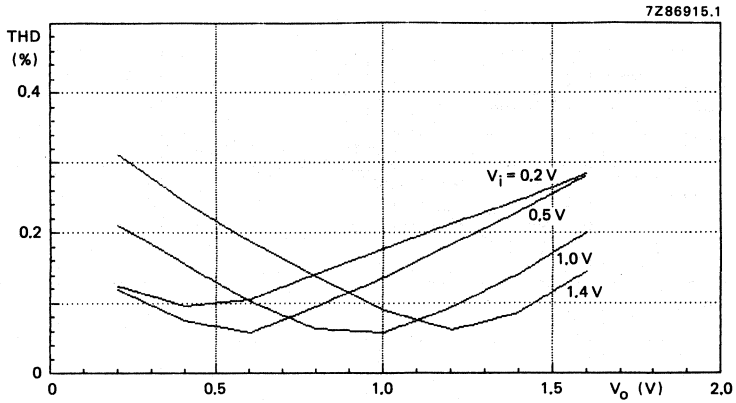


Fig.13 Total harmonic distortion (THD); as a function of output voltage (V_O). Measured in Fig.1; V_P = 8.5 V; f_i = 1 kHz.

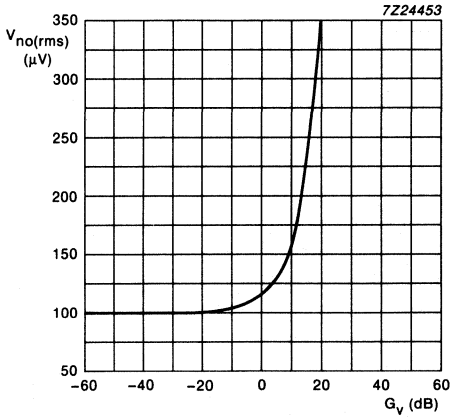


Fig.14 Noise output voltage ($V_{no(rms)}$; unweighted); as a function of voltage gain (G_V). Measured in Fig.1; V_P = 15 V; f = 20 Hz to 20 kHz.

DUAL 16-BIT DAC

GENERAL DESCRIPTION

The TDA1541 is a monolithic integrated dual 16-bit digital-to-analogue converter (DAC) designed for use in hi-fi digital audio equipment such as Compact Disc players, digital tape or cassette recorders.

Features

- Selectable two-channel input format: offset binary or two's complement
- Internal timing and control circuit
- TTL compatible digital inputs
- High maximum input bit-rate and fast settling time

QUICK REFERENCE DATA

Supply voltages			
pin 28	V_{DD}	typ.	5 V
pin 26	V_{DD1}	typ.	−5 V
pin 15	V_{DD2}	typ.	−15 V
Supply currents			
pin 28	I_{DD}	typ.	45 mA
pin 26	I_{DD1}	typ.	45 mA
pin 15	I_{DD2}	typ.	25 mA
Signal-to-noise ratio (full scale sine-wave) at analogue outputs (AOL; AOR)	S/N	typ.	95 dB
Non-linearity at T_{amb} = −20 to + 70 °C		typ.	½ LSB
Current settling time to ± 1 LSB	t_{cs}	typ.	1 μs
Maximum input bit rate at data input (pin 3)	BR_{max}	min.	6 Mbits/s
Maximum clock frequency			
at clock input (pin 2)	f_{BCKmax}	min.	6 MHz
at clock input (pin 4)	f_{SCKmax}	min.	12 MHz
Full scale temperature coefficient at analogue outputs (AOL; AOR)	TC_{FS}	typ.	± 200 x 10^{-6} K^{-1}
Operating ambient temperature range	T_{amb}		−20 to + 70 °C
Total power dissipation	P_{tot}	typ.	850 mW

PACKAGE OUTLINE

28-lead DIL; plastic (with internal heat spreader) (SOT-117).

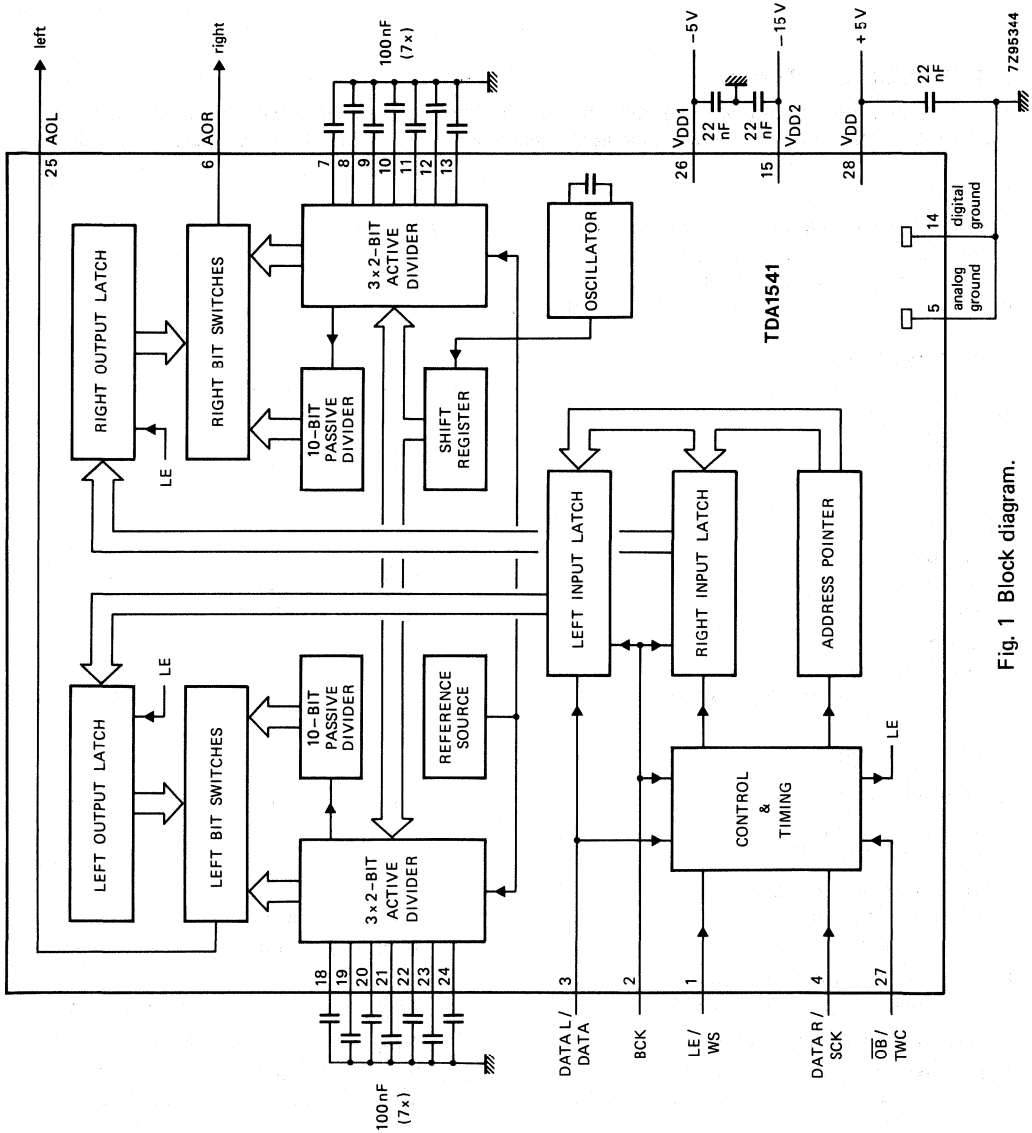


Fig. 1 Block diagram.

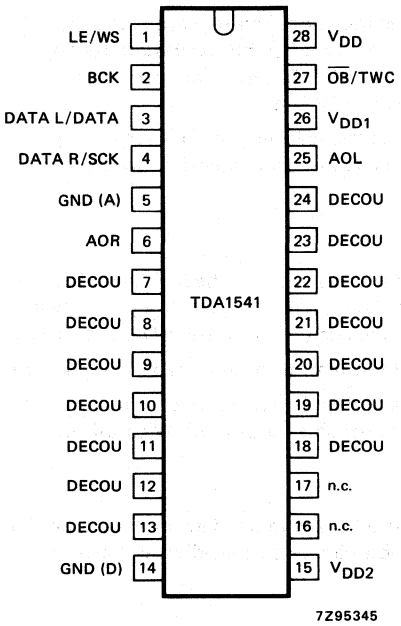


Fig. 2 Pinning diagram.

PINNING

1	LE/WS*	latch enable input / word select input
2	BCK*	bit clock input
3	DATA L/DATA*	data left channel input / data input (selected format)
4	DATA R/SYS*	data right channel input / system clock input
5	GND (A)	analogue ground
6	AOR	right channel output
7	DECOU	decoupling
8	DECOU	
9	DECOU	
10	DECOU	
11	DECOU	
12	DECOU	
13	DECOU	
14	GND (D)	digital ground
15	V_{DD2}	−15 V supply voltage
16	n.c.	not connected
17	n.c.	
18	DECOU	decoupling
19	DECOU	
20	DECOU	
21	DECOU	
22	DECOU	
23	DECOU	
24	DECOU	
25	AOL	left channel output
26	V_{DD1}	−5 V supply voltage
27	$\overline{OB}$/TWC*	mode selection input
28	V_{DD}	+ 5 V supply voltage

* See Table 1 data selection input.

FUNCTIONAL DESCRIPTION

The TDA1541 accepts input sample formats in time multiplexed mode or simultaneous mode with any bit length. The most significant bit (MSB) must always be first. This flexible input data format allows easy interfacing with signal processing chips such as interpolation filters, error correction circuits, pulse code modulation adaptors and audio signal processors (ASP).

The high maximum input bit-rate and fast settling time facilitates application in 4 x oversampling systems (44,1 kHz to 176,4 kHz) with the associated simple analogue filtering function (low order, linear phase filter).

Input data selection (see also Table 1)

With input $\overline{OB}$/TWC connected to ground, data input (offset binary format) must be in time multiplexed mode. It is accompanied with a word select (WS) and a bit clock input (BCK) signal. A separate system clock input (SCK) is provided for accurate, jitter-free timing of the analogue outputs AOL and AOR.

With $\overline{OB}$/TWC connected to V_{DD} the mode is the same but data format must be in two's complement.

When input $\overline{OB}$/TWC is connected to (V_{DD1}) the two channels of data (L/R) are input simultaneously via (DATA L) and (DATA R), accompanied with BCK and a latch-enable input (LE). With this mode selected the data must be in offset binary.

The format of data input signals is shown in figures 3, 4 and 5.

True 16-bit performance is achieved by each channel using three 2-bit active dividers, operating on the dynamic element matching principle, in combination with a 10-bit passive current-divider, based on emitter scaling. All digital inputs are TTL compatible.

Table 1 Input data selection

$\overline{OB}$/TWC	mode	pin 1	pin 2	pin 3	pin 4
−5 V	simultaneous	LE	BCK	DATA L	DATA R
0 V	time MUX OB	WS	BCK	DATA OB	SCK
+5 V	time MUX TWC	WS	BCK	DATA TWC	SCK

Where:

LE = latch enable
WS = word select
BCK = bit clock
DATA L = data left
DATA R = data right
DATA OB = data offset binary
DATA TWC = data two's complement
MUX OB = multiplexed offset binary
MUX TWC = multiplexed two's complement

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage ranges			
pin 28	V_{DD}	0 to + 7	V
pin 26	V_{DD1}	0 to −7	V
pin 15	V_{DD2}	0 to −17	V
Crystal temperature range	T_{XTAL}	−55 to + 150	°C
Storage temperature range	T_{stg}	−55 to + 150	°C
Operating ambient temperature range	T_{amb}	−20 to + 70	°C
Electrostatic handling*	V_{es}	−1000 to + 1000	V

THERMAL RESISTANCE

From junction to ambient	$R_{th\ j\text{-}a}$	=	35	K/W

* Discharging a 250 pF capacitor through a 1 kΩ series resistor.

CHARACTERISTICS

V_{DD} = + 5 V; V_{DD1} = −5 V; V_{DD2} = −12 V; T_{amb} = + 25 °C; measured in Fig. 1; unless otherwise specified.

parameter	symbol	min.	typ.	max.	unit
Supply					
Supply voltage ranges					
pin 28	V_{DD}	4,0	5,0	6,0	V
pin 26	$-V_{DD1}$	4,5	5,0	6,0	V
pin 15	$-V_{DD2}$	14	15	16	V
Supply currents					
pin 28	I_{DD}	–	45	tbf	mA
pin 26	$-I_{DD1}$	–	45	tbf	mA
pin 15	$-I_{DD2}$	–	25	tbf	mA
Resolution	Res	–	16	–	bits
Inputs					
Input current (pin 3 and pin 4)					
digital inputs LOW (< 0,8 V)	I_{IL}	–	–	tbf	mA
digital inputs HIGH (> 2,0 V)	I_{IH}	–	–	tbf	μA
Input frequency					
at clock input (pin 4)	f_{SCK}	–	–	12	MHz
at clock input (pin 2)	f_{BCK}	–	–	6	MHz
at data inputs (pin 3 and pin 4)	f_{DAT}	–	–	6	MHz
at word select input (pin 1)	f_{WS}	–	–	200	kHz
Input capacitance of digital inputs	C_I	–	12	–	pF
Oscillator					
Oscillator frequency with internal capacitor	f_{osc}	150	200	250	kHz
Analogue outputs (AOL; AOR)					
Output voltage compliance	V_{OC}	tbf	–	tbf	mV
Full scale current	I_{FS}	3,4	4,0	4,6	mA
Zero scale current	$\pm I_{ZS}$	–	tbf	–	nA
Full scale temperature coefficient T_{amb} = −20 to + 70 °C	TC_{FS}	–	$\pm 200 \times 10^{-6}$	–	K^{-1}
Linearity error integral					
at T_{amb} = 25 °C	E_1	–	0,5	–	LSB
at T_{amb} = −20 to + 70 °C	E_1	–	tbf	–	LSB
Linearity error differential					
at T_{amb} = 25 °C	E_{d1}	–	0,5	1	LSB
at T_{amb} = −20 to + 70 °C	E_{d1}	–	tbf	–	LSB

parameter	symbol	min.	typ.	max.	unit
Signal-to-noise ratio + THD*	S/N	90	95	–	dB
Settling time to ± 1 LSB	t_{cs}	–	1	–	μs
Channel separation	α	80	tbf	–	dB
Unbalance between outputs	ΔI_{FS}	–	0,1	0,2	dB
Time delay between outputs	t_d	–	–	1	μs
Power supply ripple rejection**					
V_{DD} = + 5 V	RR	–	tbf	–	dB
V_{DD1} = −5 V	RR	–	tbf	–	dB
V_{DD2} = −15 V	RR	–	tbf	–	dB
Signal-to-noise ratio at bipolar zero	S/N	–	−100	–	dB
Timing (see Figs 3, 4 and 5)					
Rise time	t_r	–	–	35	ns
Fall time	t_f	–	–	35	ns
Bit clock cycle time	t_{CY}	160	–	–	ns
Bit clock HIGH time	t_{HB}	48	–	–	ns
Bit clock LOW time	t_{LB}	48	–	–	ns
Bit clock fall time to latch rise time	t_{FBRL}	0	–	–	ns
Bit clock rise time to latch fall time	t_{RBFL}	0	–	–	ns
Data set-up time to bit clock	t_{SDB}	32	–	–	ns
Data hold time to bit clock	t_{HDB}	0	–	–	ns
Data set-up time to system clock	t_{SDS}	32	–	–	ns
Word select hold time to system clock	t_{HWS}	0	–	–	ns
Word select set-up time to system clock	t_{SWS}	32	–	–	ns
Bit clock fall time to system clock rise time	t_{FBRS}	32	–	–	ns
System clock rise time to bit clock fall time	t_{RSFB}	32	–	–	ns
System clock fall time to bit clock rise time	t_{FSRB}	50	–	–	ns
Bit clock rise time to system clock fall time	t_{RBFS}	0	–	–	ns
Latch enable LOW time	t_{LLE}	20	–	–	ns
Latch enable HIGH time	t_{HLE}	32	–	–	ns

* Signal-to-noise ratio + THD with 1 kHz full scale sinewave generated at a sampling rate of 176,4 kHz.

** V_{ripple} = 1% of supply voltage and f_{ripple} = 100 Hz.

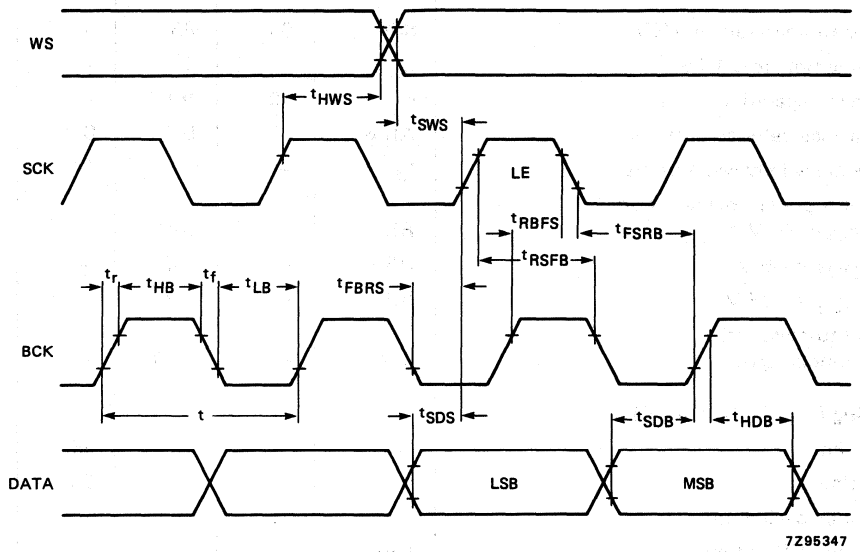


Fig. 3 Format of input signals; time multiplexed at $f_{SCK} = f_{BCK}$ (I^2S format).

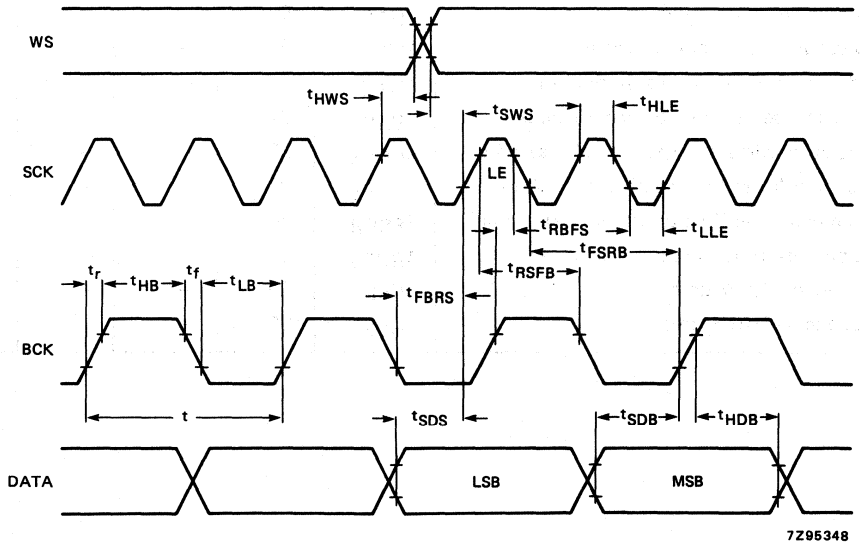


Fig. 4 Format of input signals; **time multiplexed** at $f_{SCK} = 2 \times f_{BCK}$.

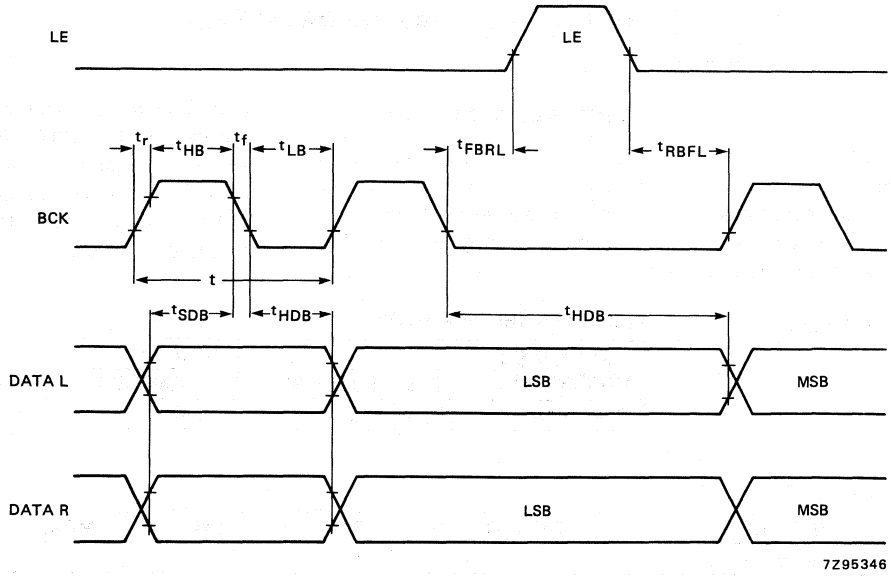


Fig. 5 Format of input signals; **simultaneous data.**

Philips Semiconductors

Data sheet	
status	Product specification
date of issue	February 1991

TDA1541A

Stereo high performance 16-bit DAC

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC01 OR DATASHEET

FEATURES

- High sound quality
- High performance: low noise and distortion, wide dynamic range
- 4 x or 8 x oversampling possible
- Selectable two-channel input format
- TTL compatible inputs

GENERAL DESCRIPTION

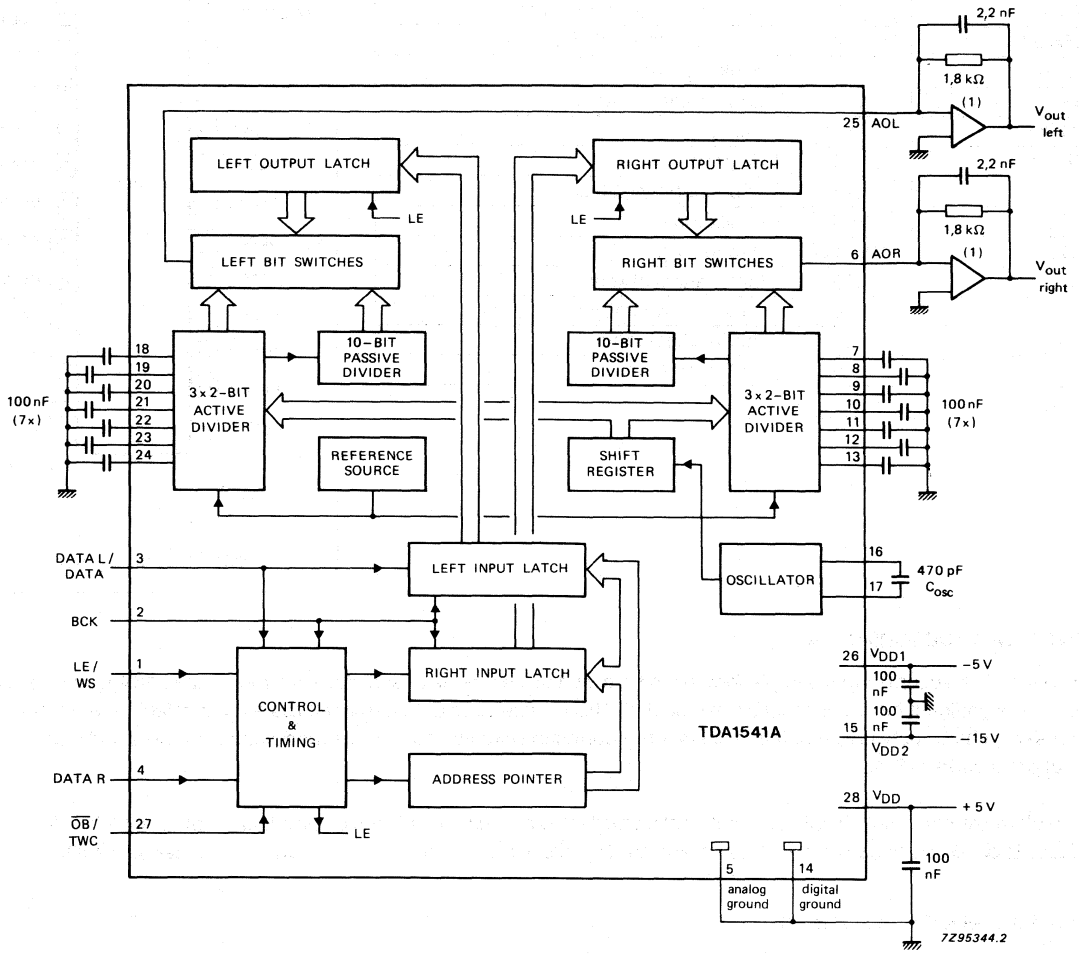
The TDA1541A is a stereo 16-bit digital-to-analog converter (DAC). The ingenious design of the electronic circuit guarantees a high performance and superior sound quality. The TDA1541A is therefore extremely suitable for use in top-end high-fi digital audio equipment such as high quality Compact Disc players or digital amplifiers.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA1541A	28	DIL	plastic	SOT117

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage; pin 28		4.5	5.0	5.5	V
$-V_{DD1}$	supply voltage; pin 26		4.5	5.0	5.5	V
$-V_{DD2}$	supply voltage; pin 15		14.0	15.0	16.0	V
I_{DD}	supply current; pin 28		-	27	40	mA
$-I_{DD1}$	supply current; pin 26		-	37	50	mA
$-I_{DD2}$	supply current; pin 15		-	25	35	mA
THD	total harmonic distortion	including noise	-	−95	−90	dB
		at 0 dB	-	0.0018	0.0032	%
THD	total harmonic distortion	including noise	-	−42	-	dB
		at −60 dB	-	0.79	-	%
NL	non-linearity	at T_{amb} = −20 to +85 °C	-	0.5	1.0	LSB
t_{cs}	current settling time to ±1 LSB		-	0.5	-	µs
BR	input bit rate at data input; (pin 3 and 4)		-	-	6.4	Mbits/s
f_{BCK}	clock frequency at clock input		-	-	6.4	MHz
TC_{FS}	full scale temperature coefficient	at analog outputs (AOL; AOR)	-	$\pm 200 \times 10^{-6}$	-	K^{-1}
T_{amb}	operating ambient temperature range		−40	-	+85	°C
P_{tot}	total power dissipation		-	700	-	mW



(1) TDA1542
(2) 2 x NE5534 or equivalent

Fig.1 Block diagram.

Stereo high performance 16-bit DAC TDA1541A

PINNING

SYMBOL	PIN	DESCRIPTION
LE/WS*	1	latch enable input / word select input
BCK*	2	bit clock input
DATA L /DATA*	3	data left channel input / data input (selected format)
DATA R*	4	data right channel input
GND(A)	5	analog ground
AOR	6	right channel output
DECOU	7 to 13	decoupling
GND (D)	14	digital ground
V_{DD2}	15	−15 V supply voltage
COSC	16,17	oscillator
DECOU	18 to 24	decoupling
AOL	25	left channel output
V_{DD1}	26	−5 V supply voltage
$\overline{OB}$/TWC*	27	mode select input
V_{DD}	28	+5 V supply voltage

* See Table 1 data selection input.

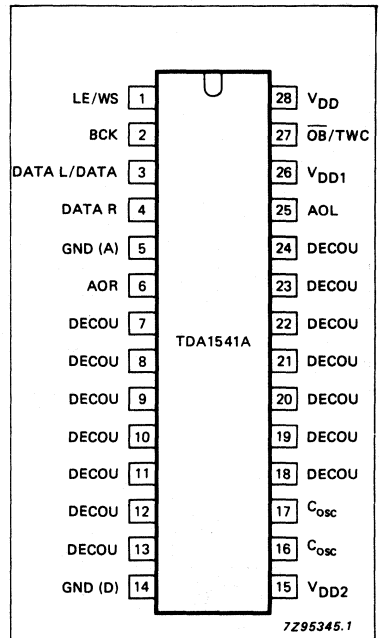


Fig.2 Pin configuration

FUNCTIONAL DESCRIPTION

The TDA1541A accepts input sample formats in time multiplexed mode or simultaneous mode up to 16-bit word length. The most significant bit (MSB) must always be first. This flexible input data format allows easy interfacing with signal processing chips such as interpolation filters, error correction circuits, pulse code modulation adaptors and audio signal processors (ASP).

The high maximum input bit-rate and fast settling facilitates application in 8 x oversampling systems (44.1 kHz to 352.8 kHz or 48 kHz to 384 kHz) with the associated simple analog filtering function (low order, linear phase filter).

Input data selection (see also Table 1)

With the input $\overline{OB}$/TWC connected to ground, data input (offset binary format) must be in time multiplexed mode. It is accompanied with a word select (WS) and a bit clock input (BCK) signal. The converted samples appear at the output, at the first positive going transition of the bit clock signal after a negative going transition of the word select signal.

With $\overline{OB}$/TWC connected to V_{DD} the mode is the same but the data format must be in the two's complement.

When input $\overline{OB}$/TWC input is connected to V_{DD1} the two channels of data (L/R) are input simultaneously via DATA L and DATA R, accompanied with BCK and a latch-enable input (LE). With this mode selected the data must be in offset binary. The converted samples appear at the output at the positive going transition of the latch enable signal.

The format of the data input signals is shown in fig.4 and 5.

True 16-bit performance is achieved by each channel using three 2-bit active dividers, operating on the dynamic element matching principle, in combination with a 10-bit passive current divider, based on emitter scaling. All digital inputs are TTL compatible.

Table 1 Input data selection

$\overline{OB}$/TWC	mode	pin 1	pin 2	pin 3	pin 4
−5 V	simultaneous	LE	BCK	DATA L	DATA R
0 V	time MUX OB	WS	BCK	DATA OB	not used
+5 V	time MUX TWC	WS	BCK	DATA TWC	not used

Where:

LE = latch enable
WS = word select, LOW = left channel; HIGH = right channel
BCK = bit clock
DATA L = data left
DATA R = data right
DATA OB = data offset binary
DATA TWC = data two's complement
MUX OB = mulitplexed offset binary
MUX TWC = multiplexed two's complement = I^2S-format

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage; pin 28		0	7	V
$-V_{DD1}$	supply voltage; pin 26		0	7	V
$-V_{DD2}$	supply voltage; pin 15		0	17	V
T_{stg}	storage temperature range		−55	+150	°C
T_{amb}	operating ambient temperature range		−40	+85	°C
V_{es}	electrostatic handling*		−1000	+1000	V

THERMAL RESISTANCE

SYMBOL	PARAMETER	TYP.	UNIT
$R_{th\ j\text{-}a}$	from junction to ambient	30	K/W

* Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

CHARACTERISTICS

V_{DD} = 5 V; $-V_{DD1}$ = 5 V; $-V_{DD2}$ = 15 V; T_{amb} = +25 °C; measured in the circuit of Fig.1; unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD}	supply voltage; pin 28		4.5	5.0	5.5	V
$-V_{DD1}$	supply voltage; pin 26		4.5	5.0	5.5	V
$-V_{DD2}$	supply voltage; pin 15		14.0	15.0	16.0	V
$V_{GND(A)} - V_{GND(D)}$	voltage difference between analog and digital ground		−0.3	0	+0.3	V
I_{DD}	supply current; pin 28		-	27	40	mA
$-I_{DD1}$	supply current; pin 26		-	37	50	mA
$-I_{DD2}$	supply current; pin 15		-	25	35	mA
Inputs						
$-I_{IL}$	input current pins (1, 2, 3 and 4) digital inputs LOW	V_I = 0.8 V	-	-	0.4	mA
I_{IH}	digital inputs HIGH	V_I = 2.0 V	-	-	20	µA
$\lvert I_{\overline{OB}/TWC}\rvert$	Digital input currents (pin 27) +5 V		-	-	1	µA
$\lvert I_{\overline{OB}/TWC}\rvert$	0 V		-	-	20	µA
$\lvert I_{\overline{OB}/TWC}\rvert$	−5 V		-	-	40	µA
f_{BCK}	input frequency/bit rate clock input pin 2		-	-	6.4	MHz
BR	bit rate data input pin 3 and 4		-	-	6.4	Mbits/s
f_{WS}	word select input pin 2		-	-	200	kHz
f_{LE}	latch enable input 1		-	-	200	kHz
C_I	input capacitance of digital inputs		-	12	-	pF
Analog outputs (AOL; AOR; see note 1)						
Res	resolution		-	16	-	bits
I_{FS}	full scale current		3.4	4.0	4.6	mA
$\lvert I_{ZS}\rvert$	zero scale current		-	25	50	nA
T_{CFS}	full scale temperature coefficient	T_{amb} = −20 to +85 °C	-	±200 x 10^{-6}	-	K^{-1}
Analog outputs (V_{ref})						
E_L	integral linearity error	T_{amb} = 25 °C	-	0.5	1.0	LSB
E_L	integral linearity error	T_{amb} = −20 to +85°C	-	-	1.0	LSB
E_{dL}	differential linearity error	T_{amb} = 20°C, note 2	-	0.5	1.0	LSB
E_{dL}	differential linearity error	T_{amb} = −20 to +85°C	-	-	1.0	LSB
THD	total harmonic distortion	at 0 dB; note 3	−100	-	dB	
			-	0.0010	-	%
THD	total harmonic distortion	including noise at 0 dB;	-	−95	−90	dB
		note 3, Fig.3	-	0.0018	0.0032	%
THD	total harmonic distortion	including noise at −60 dB;	-	−42	-	dB
		note 3, Fig.3	-	0.79	-	%

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
t_{cs}	settling time ±1 LSB		-	0.5	-	µs
α	channel separation		90	98	-	dB
$\lvert d_{IO} \rvert$	unbalance between outputs	note 4	-	< 0.1	0.3	dB
$\lvert t_d \rvert$	time delay between outputs		-	-	0.2	µs
SSVR	supply voltage ripple rejection	V_{DD} = +5 V; note 4	-	−76	-	dB
SSVR	supply voltage ripple rejection	V_{DD1} = −5 V; note 4	-	−84	-	dB
SSVR	supply voltage ripple rejection	V_{DD2} = −15 V; note 4	-	−58	-	dB
S/N	signal-to-noise ratio	at bipolar zero	-	110	-	dB
S/N	signal-to-noise ratio	at full scale	98	104	-	dB
Timing (Fig.4 and 5)						
t_r	rise time		-	-	32	ns
t_f	fall time		-	-	32	ns
t_{CY}	bit clock cycle time		156	-	-	ns
t_{HB}	bit clock HIGH time		46	-	-	ns
t_{LB}	bit clock LOW time		46	-	-	ns
t_{FBRL}	bit clock fall time to latch enable rise time		0	-	-	ns
t_{RBFL}	bit clock rise time to latch enable fall time		0	-	-	ns
$t_{SU;DAT}$	data set-up time		32	-	-	ns
$t_{HD;DAT}$	data hold time to bit clock		0	-	-	ns
$t_{HD;WS}$	word select hold time		0	-	-	ns
$t_{SU;WS}$	word select set-up time		32	-	-	ns

Notes to the characteristics

1. To ensure no performance losses, permitted output voltage compliance is ±25 mV maximum.

2. Selections have been made with respect to the maximum differential linearity error (E_{dL}):

   TDA1541A/N2 bit 1-16 $E_{dL} < 1$ LSB

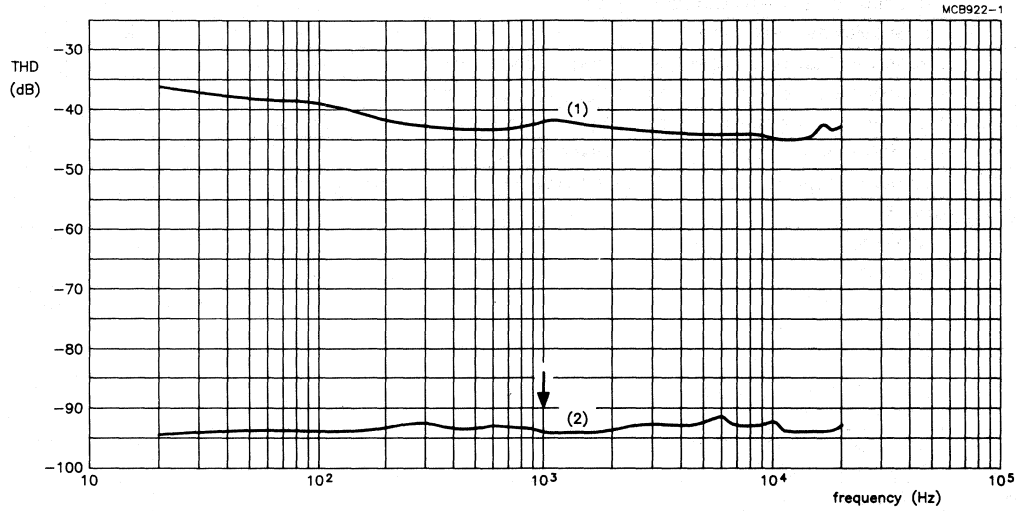
   TDA1541A/N2/R1 bit 1-16 $E_{dL} < 2$ LSB

   TDA1541A/N2/S1 bit 1-7 $E_{dL} < 0.5$ LSB
   bit 8-15 $E_{dL} < 1$ LSB
   bit 16 $E_{dL} < 0.75$ LSB

   The S1 version has been specially selected to achieve extremely good performance even for small signals.

3. Measured using a 1 kHz sinewave generated at a sampling rate of 176.4 kHz.

4. V_{ripple} = 100 mV and f_{ripple} = 100 Hz.

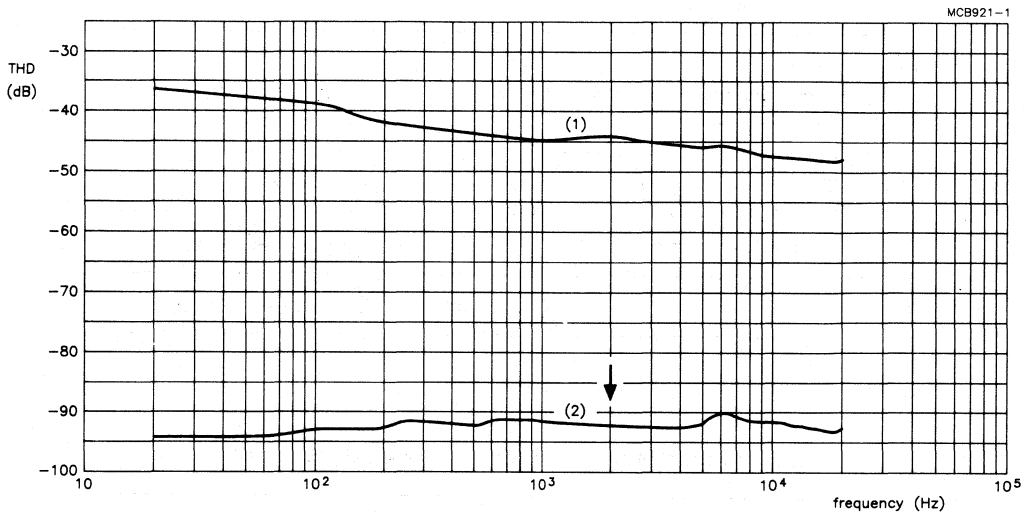


(1) Measured including all distortion plus noise at a signal level of –60 dB
(2) Measured including all distortion plus noise at a signal level of –0 dB

Fig.3a Distortion as a function of frequency (4FS)

Notes to Fig.3a

- The sample frequency 4FS: 176.4 kHz.
- Ref: 0 dB is the output level of a full scale digital sine wave stimulus.



(1) Measured including all distortion plus noise at a signal level of –60 dB
(2) Measured including all distortion plus noise at a signal level of –0 dB

Fig.3b Distortion as a function of frequency (8FS)

Notes to Fig.3b

- The sample frequency 8FS: 352.8 kHz.
- Ref: 0 dB is the output level of a full scale digital sine wave stimulus.

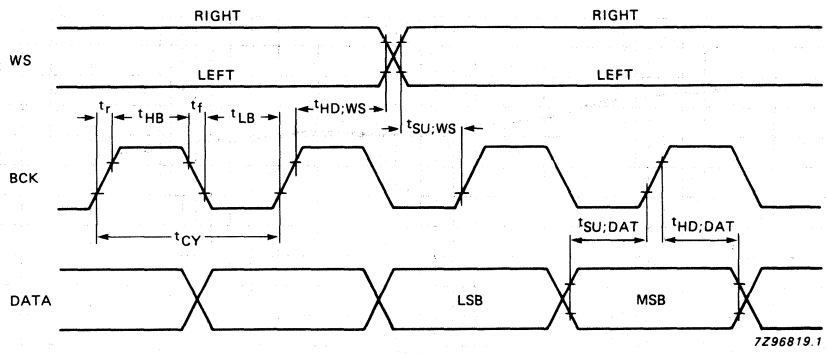


Fig.4 Format of input signals; time multiplexed (I^2S format).

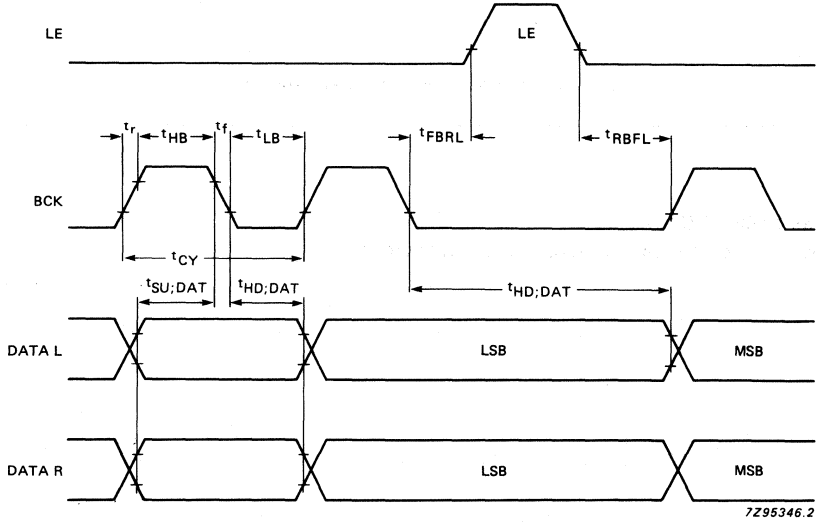


Fig.5 Format of input signals; simultaneous data.

ACTIVE ELEMENT FOR POST FILTERING

GENERAL DESCRIPTION

The TDA1542 is a dual channel monolithic integrated circuit encapsulated in a 28 pin DIL plastic package. Each channel incorporates five high performance amplifiers and is designed for use in hi-fi digital audio equipment such as a compact disc player.

Features

- Mute function for click and plop free switching (on and off)
- Switch function for activating a de-emphasis circuit
- Two separate output amplifiers per channel
- Flexible use of filtering
- Extremely low distortion
- High slew-rate input amplifier

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage						
pin 28		V_{DD1}	4.75	12.0	13.0	V
pin 1		V_{DD2}	4.5	5.0	5.5	V
pin 26		$-V_{DD3}$	4.75	12.0	13.0	V
Input amplifier (A)						
Slew-rate		$\Delta V/\Delta t$	–	30	–	V/μs
Line amplifier (D)						
Output voltage (pins 10 and 19) (r.m.s. value)		$V_{O(rms)}$	1.9	2	–	V
Signal to noise ratio		S/N	110	115	–	dB
Total harmonic distortion	R_L = 1 kΩ	THD	–	–110	–100	dB
Channel separation		α	95	100	–	dB
Headphone amplifier (E)						
Output voltage (pins 13 and 16) (r.m.s. value)		$V_{O(rms)}$	–	6	–	V
Signal to noise ratio		S/N	110	115	–	dB
Total harmonic distortion	R_L = 600 Ω	THD	–	–110	–100	dB
Channel separation		α	95	100	–	dB
Filter amplifiers (A, B and C)						
Amplifiers conform to line amplifier D, without mute function						

PACKAGE OUTLINE

28-lead DIL; plastic (with internal heat spreader) (SOT117).

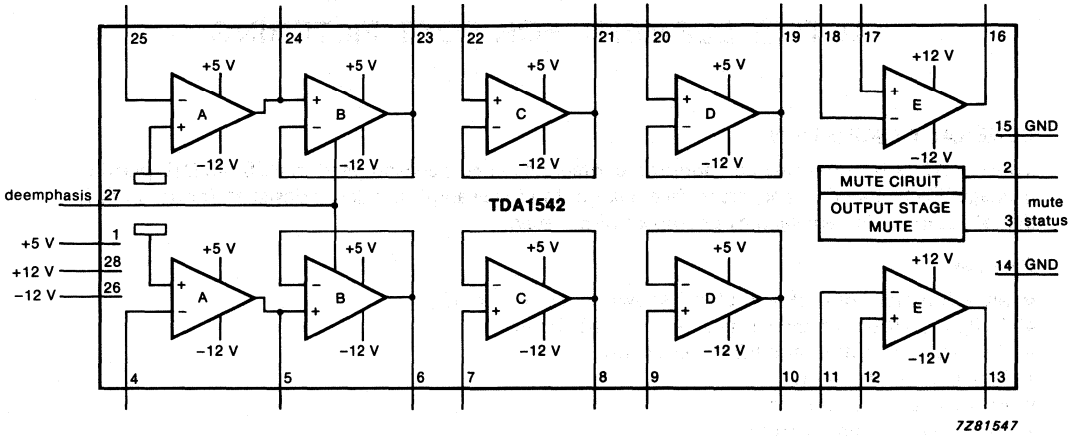


Fig. 1 Block diagram.

PINNING

1	+5 V supply voltage (V_{DD2})	15	Ground left
2	Mute timing capacitor	16	Amplifier E left output
3	Mute status	17	Amplifier E left non-inverting input
4	Amplifier A right input	18	Amplifier E left inverting input
5	Amplifier A right output/Amplifier B input	19	Amplifier D left output
6	Amplifier B right output	20	Amplifier D left input
7	Amplifier C right input	21	Amplifier C left output
8	Amplifier C right output	22	Amplifier C left input
9	Amplifier D right input	23	Amplifier B left output
10	Amplifier D right output	24	Amplifier A left output/Amplifier B input
11	Amplifier E right inverting input	25	Amplifier A left input
12	Amplifier E right non-inverting input	26	−12 V supply voltage (V_{DD3})
13	Amplifier E right output	27	De-emphasis on/off function
14	Ground right	28	+12 V supply voltage (V_{DD1})

FUNCTIONAL DESCRIPTION

The TDA1542 is a high performance, dual channel device designed to perform post filtering in a compact disc player. Since only the active part of the filter is integrated, the user has the option of selecting the desired filter type e.g. Bessel or Cauer etc. Each channel contains two separate output amplifiers, one with fixed gain for line output and the other with variable gain for driving low/high impedance headphones.

A switchable buffer amplifier is incorporated to enable the deemphasis function without producing clicks.

A mute circuit is incorporated to prevent spurious signals appearing at the output.

Both amplifiers are muted, for a preset period of time, when the 5 V supply is switched on or off.

An external capacitor determines the mute time. When the mute time has elapsed the signal path is switched directly to the output, without clicks. The mute circuit status is available externally.

The TDA1542 is designed to operate over a wide supply voltage range.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage ranges					
pin 28		V_{DD1}	0	18	V
pin 1		V_{DD2}	0	7	V
pin 26		$-V_{DD3}$	0	18	V
Storage temperature range		T_{stg}	−65	150	°C
Operating ambient temperature range		T_{amb}	−30	85	°C
Electrostatic handling *		V_{es}	−	600	V

THERMAL RESISTANCE

From junction to ambient $R_{th\ j\text{-}a}$ 30 K/W

* Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

DC CHARACTERISTICS

V_{DD1} = + 12 V; V_{DD2} = + 5 V; V_{DD3} = −12 V; T_{amb} = 25 °C

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage						
pin 28		V_{DD1}	4.75	12.0	13.0	V
pin 1		V_{DD2}	4.5	5.0	5.5	V
pin 26		$-V_{DD3}$	4.75	12.0	13.0	V
Supply current						
pin 28		I_{DD1}	–	12	18	mA
pin 1		I_{DD2}	–	34	51	mA
pin 26		$-I_{DD3}$	–	46	69	mA
Input current						
Amplifier A (pins 4 and 25)		I_{IA}	–	1	2	μA
Amplifier C (pins 7 and 22)		I_{IC}	–	320	600	nA
Amplifier D (pins 9 and 20)		I_{ID}	–	50	150	nA
Amplifier E (pins 11 and 18)		I_{IE}	–	300	600	nA
Amplifier E (pins 12 and 17)		I_{IE}	–	30	150	nA
Offset voltage						
Amplifier A (pins 4 and 25)		$\lvert V_{IAos}\rvert$	–	1.2	7.0	mV
Amplifier B (pins 6 and 23)		$\lvert V_{IBos}\rvert$	–	0.5	7.0	mV
Amplifier C (pins 8 and 21)		$\lvert V_{ICos}\rvert$	–	0.6	7.0	mV
Amplifier D (pins 10 and 19)		$\lvert V_{IDos}\rvert$	–	1.0	3.0	mV
Amplifier E (pins 11 and 18)		$\lvert V_{IEos}\rvert$	–	0.7	3.0	mV
Mute timing capacitor (pin 2)						
Switch-on voltage		V_{sw}	–	3.5	4.1	V
Loading current		$-I_L$	0.1	0.5	2.0	mA

AC CHARACTERISTICS

V_{DD1} = + 12 V; V_{DD2} = + 5 V; V_{DD3} = −12 V; T_{amb} = 25 °C; f = 1 kHz; measured in Fig. 2

parameter	conditions	symbol	min.	typ.	max.	unit
Amplifier A to Amplifier E						
Open loop gain		G_{ol}	–	90	–	dB
Overall distortion without de-emphasis		THD	–	−110	−100	dB
Slew rate (Amplifier A)		$\Delta V/\Delta t$	–	30	–	V/μs
Supply voltage ripple rejection						
V_{DD1}	note 1	SVRR	50	60	–	dB
V_{DD2}	note 2	SVRR	50	60	–	dB
V_{DD3}	note 2	SVRR	55	70	–	dB
Line amplifier D						
Output voltage (pins 10 and 19) (r.m.s. value)		$V_{O(rms)}$	1.9	2.0	–	V
Signal to noise ratio	B = 20 Hz to 20 kHz	S/N	110	115	–	dB
Total harmonic distortion		THD	–	−110	−100	dB
Channel separation		α	95	100	–	dB
Output impedance		Z_O	–	–	0.5	Ω
Difference between mute ON and mute OFF output voltage (pins 10 and 19)		V_O	–	–	4	mV
Headphone amplifier (E)						
Output voltage (pins 13 and 16) (r.m.s. value)	R_L = 600 Ω	$V_{O(rms)}$	–	6	–	V
	R_L = 132 Ω	$V_{O(rms)}$	–	5.5	–	V
Signal to noise ratio	B = 20 Hz to 20 kHz	S/N	110	115	–	dB
Total harmonic distortion	R_L = 600 Ω	THD	–	−110	−100	dB
Total harmonic distortion	R_L = 132 Ω	THD	–	−88	−80	dB
Channel separation	20 Hz to 20 kHz; R_L = 600 Ω	α	95	100	–	dB
Output impedance		Z_O	–	–	0.5	Ω
Difference between mute ON and OFF output voltage (pins 13 and 16)		V_O	–	–	6	mV

AC CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Mute status (pin 3)	open collector output					
Output voltage LOW (mute ON)	$-I_{OL}$ = 3 mA	–	–	–	0.4	V
Output voltage HIGH (mute OFF)	$I_{OL} \leqslant 1\ \mu A$		2.4	–	V_{DD1}	V
Mute timing	note 3					
De-emphasis switch						
Input voltage HIGH	De-emphasis ON	V_{IH}	2.4	–	V_{DD1}	V
Input voltage LOW	De-emphasis OFF	V_{IL}	0	–	1	V
Input current HIGH	De-emphasis ON	I_{IH}	–	–	5.0	μA
Input current LOW	De-emphasis OFF	$-I_{IL}$	–	–	25	μA

Notes to the characteristics

1. The ripple rejection is measured at the output of the line amplifier; amplitude = 0.5 V_{tt}; f = 100 Hz to 10 kHz.
2. The ripple rejection is measured at the output of the line amplifier; amplitude = 1 V_{tt}; f = 100 Hz to 10 kHz.
3. The mute timing is provided by an external capacitor connected to pin 2.

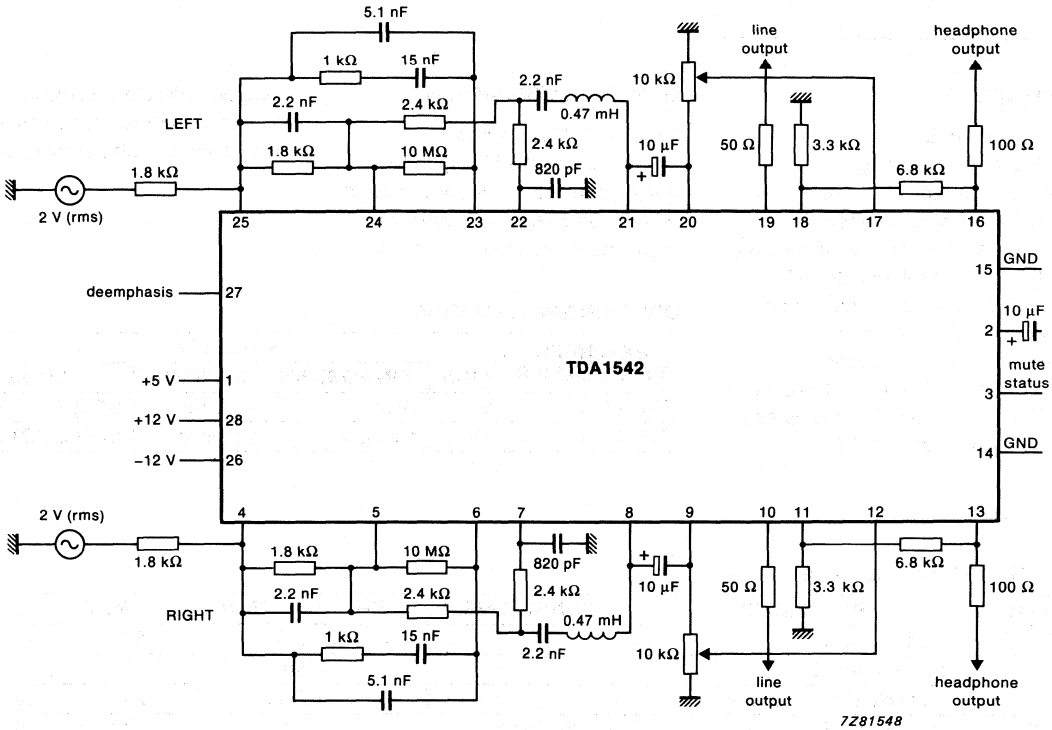


Fig. 2 Test and application circuit.

Philips Semiconductors

Data sheet	
status	Product specification
date of issue	February 1991

TDA1543

Dual 16-bit DAC (economy version) (I^2S input format)

FEATURES

- Low distortion
- 16-bit dynamic range
- 4 x oversampling possible
- Single 5 V power supply
- No external components required
- No requirement for external deglitcher circuitry due to fast settling output current
- Adjustable bias current
- Internal timing and control circuits
- I^2S input format: time multiplexed, two's complement, TTL

GENERAL DESCRIPTION

The TDA1543 is a monolithic integrated dual 16-bit digital-to-analog converter (DAC) designed as an economy version for use in hi-fi digital audio equipment such as Compact Disc players, digital tape or cassete recorders, digital sound in TV sets and in digital amplifiers.

ORDERING INFORMATION

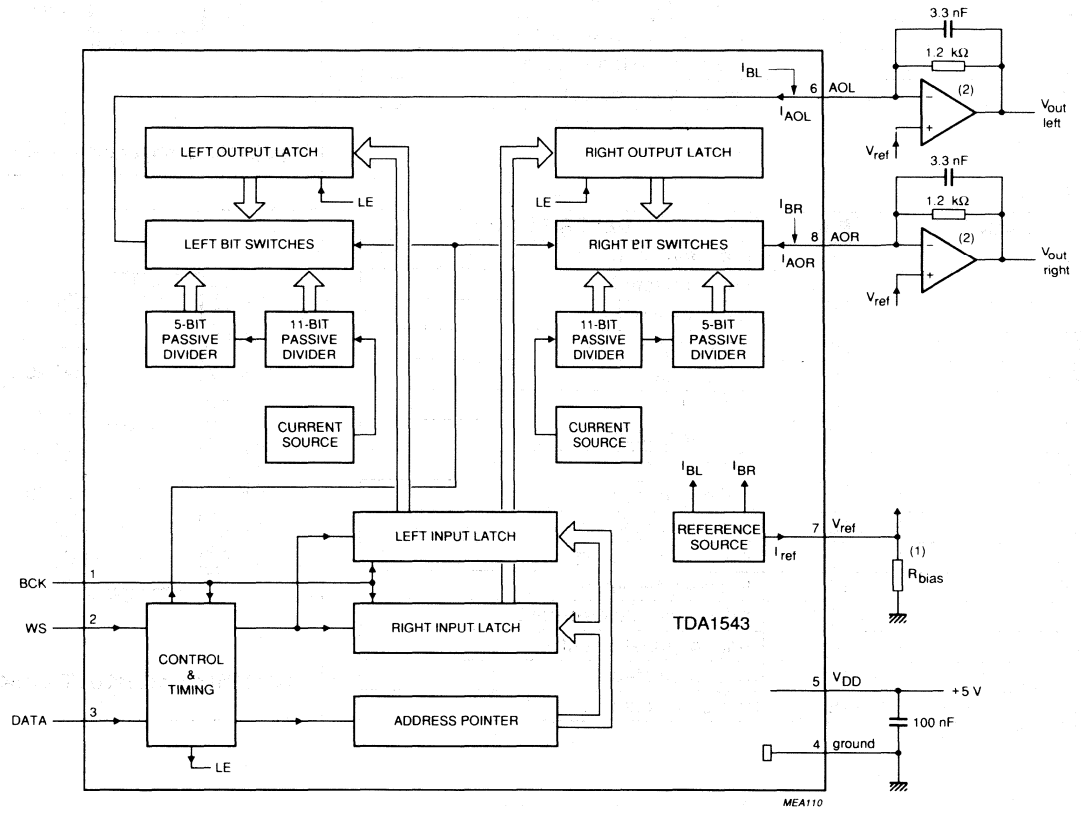
EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA1543	8	DIL	plastic	SOT97
TDA1543T	16	mini-pack	plastic	SO16L;SOT162A

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage		3.0	5.0	8.0	V
I_{DD}	supply current		-	50	60	mA
I_{FS}	full scale output current		1.95	2.30	2.65	mA
THD	total harmonic distortion	including noise	-	−75	−70	dB
		at 0 dB	-	0.018	0.032	%
THD	total harmonic distortion	including noise	-	−30	−23	dB
		at −60 dB	-	3.2	7.9	%
t_{cs}	current settling time to ±1 LSB		-	0.5	-	µs
BR	input bit rate at data input		-	-	9.2	Mbits/s
f_{BCK}	clock frequency at clock input		-	-	9.2	MHz
S/N	signal-to-noise ratio	at bipolar zero	90	96	-	dB
TC_{FS}	full scale temperature coefficient	at analog outputs (AOL; AOR)	-	$\pm 500 \times 10^{-6}$	-	K^{-1}
T_{amb}	operating ambient temperature range		−30	-	+85	°C
P_{tot}	total power dissipation		-	250	-	mW
I_{bias}	bias current (adjustable)		−0.6	-	5.0	mA

Dual 16-bit DAC (economy version) (I^2S input format)

TDA1543



(1) Optional
(2) 2 x 1/2 NE5532

Fig.1 Block diagram.

Dual 16-bit DAC (economy version) (I^2S input format)

TDA1543

PINNING

SYMBOL	PIN	DESCRIPTION
BCK	1	bit clock input
WS	2	word select input
DATA	3	data input
GND	4	ground
V_{DD}	5	+5 V supply voltage
AOL	6	left channel voltage output
V_{ref}	7	reference voltage output
AOR	8	right channel output

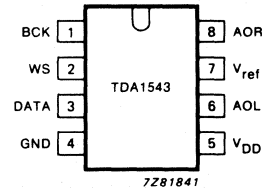


Fig.2(a) Pin configuration TDA1543.

PINNING

SYMBOL	PIN	DESCRIPTION
n.c.	1	not connected
n.c.	2	not connected
BCK	3	bit clock input
WS	4	word select input
DATA	5	data input
GND	6	ground
n.c.	7	not connected
n.c.	8	not connected
n.c.	9	not connected
n.c.	10	not connected
V_{DD}	11	+5 V supply voltage
AOL	12	left channel output
V_{ref}	13	reference voltage output
AOR	14	right channel output
n.c.	15	not connected
n.c.	16	not connected

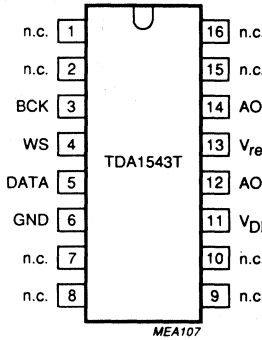
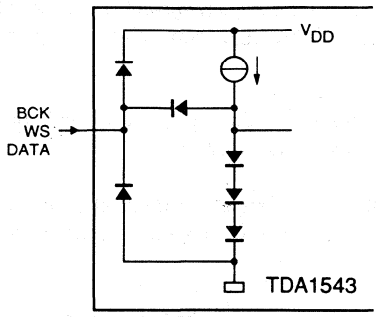
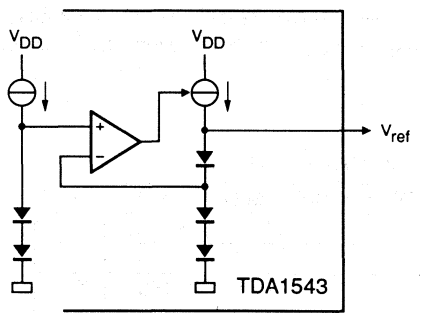


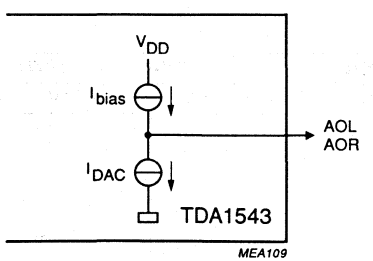
Fig.2(b) Pin configuration TDA1543T.



(a) input pins BCK, WS and DATA.



(b) output pin V_{ref}.



(c) output pins AOL and AOR.

Fig.3 Circuits at the input and output pins.

Dual 16-bit DAC (economy version) (I^2S input format)

TDA1543

FUNCTIONAL DESCRIPTION

The TDA1543 accepts input serial data formats in two's complement with any bit length. Left and right data words are time multiplexed. The most significant bit (bit 1) must always be first. The format of data input is shown in Fig.4 and Fig.5.

This flexible input data format (I^2S) allows easy interfacing with signal processing chips such as interpolation filters, error correction circuits and audio signal processor circuits (ASP).

The high maximum input bit-rate and fast settling current facilitates application in 4 x oversampling systems. An adjustable current is added to the output currents to bias output operational amplifiers (OP1; OP2) for maximum dynamic range (see Fig.1).

With a LOW level on the word select (WS) input data is placed in the left input register and with a HIGH level on the WS input data is placed in the right input register. The data in the input registers is simultaneously latched in the output registers which control the bit switches.

The output current of the DAC is a sink current. The current I_{ref} at the V_{ref} output is adjusted by a resistor or a current source. The current I_{ref} is amplified with gain A_{Ibias} to the bias currents (I_{BL}; I_{BR}) which are added to the output currents.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage range		0	9	V
T_{XTAL}	crystal temperature		-	+150	°C
T_{stg}	storage temperature range		-55	+150	°C
T_{amb}	operating ambient temperature range		-30	+85	°C
V_{es}	electrostatic handling*		-2000	+2000	V

THERMAL RESISTANCE

SYMBOL	PARAMETER	TYP.	UNIT
$R_{th\ j\text{-}a}$	from junction to ambient	100	K/W

* Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

CHARACTERISTICS

V_{DD} = 5 V; T_{amb} = +25 °C; I_{ref} = 0 mA; measured in the circuit of Fig.1; unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD}	supply voltage range		3.0	5.0	8.0	V
I_{DD}	supply current	note 1	-	50	60	mA
RR	ripple rejection	note 2	-	50	-	dB
Digital inputs						
I_{IL}	input current pins (1, 2 and 3) digital inputs LOW	V_I = 0.8 V	-	-	−0.4	mA
I_{IH}	digital inputs HIGH	V_I = 2.0 V	-	-	20	µA
f_{BCK}	input frequency/bit rate clock input pin 1		-	-	9.2	MHz
BR	bit rate data input pin 3		-	-	9.2	Mbits/s
f_{WS}	word select input pin 2		-	-	192	kHz
Analog outputs (AOL; AOR)						
Res	resolution		-	-	16	bits
	output voltage compliance					
$V_{OC(AC)}$	AC		-	±25	-	mV
$V_{OC(DC)}$	DC		1.8	-	V_{DD}−1.2	V
I_{FS}	full scale current		1.95	2.30	2.65	mA
T_{CFS}	full scale temperature coefficient		-	±500 x 10^{-6}	-	K^{-1}
I_{offset}	offset current	I_{ref} = 0 mA	−0.1	0.0	0.1	mA
I_{bias}	bias current (adjustable)		−0.6	-	5.0	mA
AI_{bias}	bias current gain		1.9	2.0	2.1	
Analog outputs (V_{ref})						
V_{ref}	reference voltage output		2.10	2.20	2.30	V
I_{ref}	reference current output		−0.3	-	2.5	mA
THD	total harmonic distortion	including noise at 0 dB;		−75	−70	dB
		note 3, Fig.6		0.018	0.032	%
THD	total harmonic distortion	including noise at −60 dB;	-	−30	−23	dB
		note 3, Fig.6	-	3.2	7.9	%
t_{cs}	settling time ±1 LSB		-	0.5	-	µs
α	channel separation		85	90	-	dB
$\lvert d_{IO} \rvert$	unbalance between outputs	note 4	-	< 0.2	0.3	dB
$\lvert t_d \rvert$	time delay between outputs		-	< 0.2	-	µs
S/N	signal-to-noise ratio	at bipolar zero; note 5	90	96	-	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Timing (Fig.4)						
t_r	rise time		-	-	32	ns
t_f	fall time		-	-	32	ns
t_{CY}	bit clock cycle time		108	-	-	ns
t_{HB}	bit clock HIGH time		22	-	-	ns
t_{LB}	bit clock LOW time		22	-	-	ns
$t_{SU;DAT}$	data set-up time		32	-	-	ns
$t_{HD;DAT}$	data hold time to bit clock	note 6	2	-	-	ns
$t_{HD;WS}$	word select hold time	note 6	2	-	-	ns
$t_{SU;WS}$	word select set-up time		32	-	-	ns

Notes to the characteristics

1. Measured at I_{AOL} = 0 mA and I_{AOR} = 0 mA (code 8000H) and I_{bias} = 0 mA.
2. V_{ripple} = 1% of supply voltage and f_{ripple} = 100 Hz.
3. Measured with 1 kHz sinewave generated at a sampling rate of 192 kHz.
4. Measured with 1 kHz full scale sinewave generated at a sampling rate of 192 kHz.
5. At code 0000H.
6. At this point $t_{HD;DAT}$ = 0 ns, this value has been fixed on 2 ns due to tolerances.

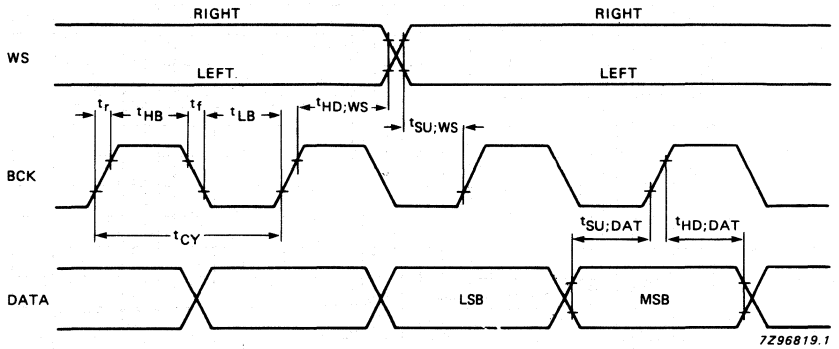


Fig.4 Format of input signals (I²S format).

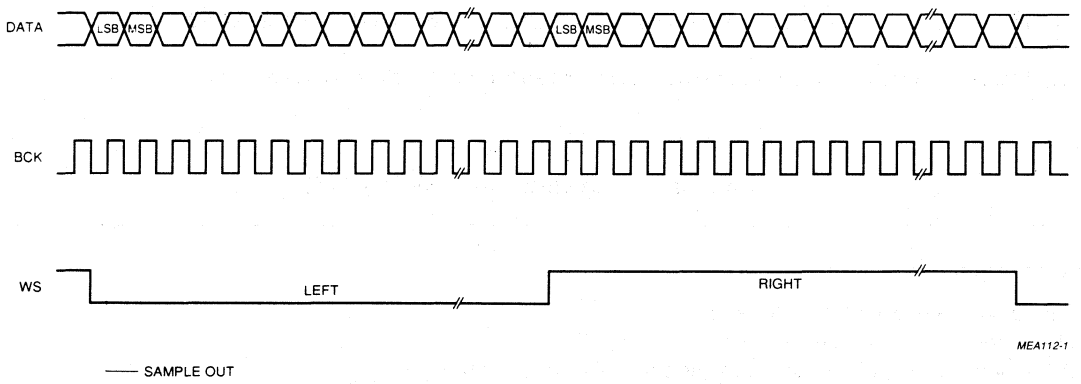
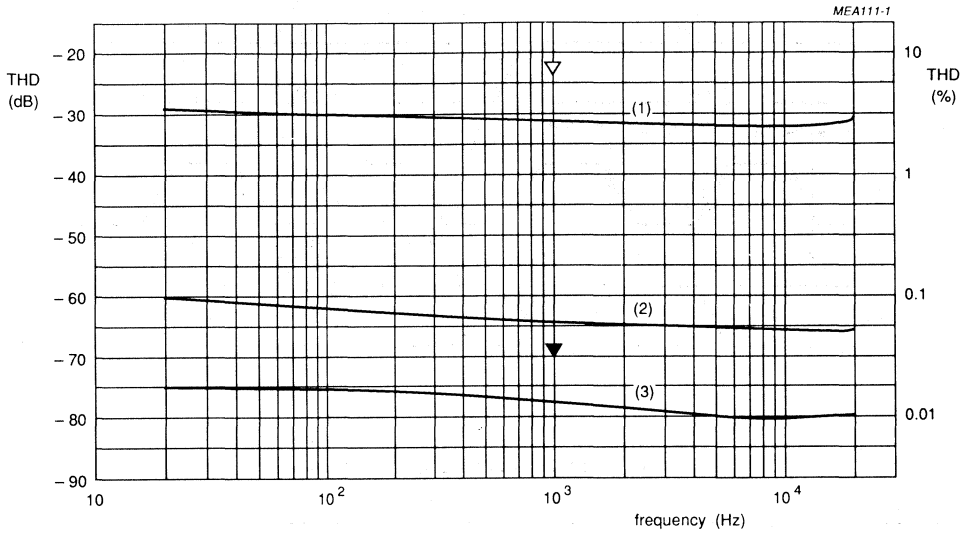


Fig.5 Format of input signals.



(1) Measured including all distortion plus noise over a 20 kHz bandwidth at a level of –60 dB

(2) Measured including all distortion plus noise over a 20 kHz bandwidth at a level of –24 dB

(3) Measured including all distortion plus noise over a 20 kHz bandwidth at a level of –0 dB

Fig.6 Distortion as a function of frequency (4FS)

Notes to Fig.6

- The sample frequency 4FS: 176.4 kHz.
- The supply voltage at the measurement = + 5 V (DC).
- Ref: 0 dB is the output level of a full scale digital sine wave stimulus.
- The graphs are constructed from average values of a small amount of engineering samples therefore no guarantee for typical values is implied.
- The arrows indicate the specification limits for 0 dB and –60 dB level signals.

Philips Semiconductors

Data sheet	
status	Product specification
date of issue	February 1991

TDA1543(A)/S6

Dual 16-bit low-cost economy DAC (relaxed version of TDA1543A)

GENERAL DESCRIPTION

The TDA1543(A)/S6 is a monolithic integrated dual 16-bit digital-to-analog converter (DAC) designed as a low-cost economy version for use in hi-fi digital audio equipment such as Compact Disc players, digital tape or cassete recorders, digital sound in television systems and digital amplifiers.

The S6 version is a relaxed version of the TDA1543(A). The differences in performance between the S6 selection and the standard version are limited to only three parameters:

QUICK REFERENCE VALUES STANDARD VERSION

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
THD	total harmonic distortion	including noise at 0 dB	-	–70	dB
T_{amb}	operating ambient temperature range		–30	+85	°C
AI_{bias}	bias current gain		1.9	2.1	

QUICK REFERENCE VALUES S6 VERSION

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
THD	total harmonic distortion	including noise at 0 dB	-	–60	dB
T_{amb}	operating ambient temperature range		–20	+75	°C
AI_{bias}	bias current gain		1.85	2.1	

The other characteristics of the S6 version can be found in the data sheets of the TDA1543 and the TDA1543A.

Philips Semiconductors

Data sheet	
status	Product specification
date of issue	February 1991

TDA1543A

Dual 16-bit DAC (economy version) (Japanese input format)

FEATURES

- Low distortion
- 16-bit dynamic range
- 4 x oversampling possible
- Single 5 V power supply
- No external components required
- No requirement for external deglitcher circuitry due to fast settling output current
- Adjustable bias current
- Internal timing and control circuits
- Japanese input format: time multiplexed, two's complement, TTL

GENERAL DESCRIPTION

The TDA1543A is a monolithic integrated dual 16-bit digital-to-analog converter (DAC) designed as an economy version for use in hi-fi digital audio equipment such as Compact Disc players, digital tape or cassete recorders and in digital amplifiers.

ORDERING INFORMATION

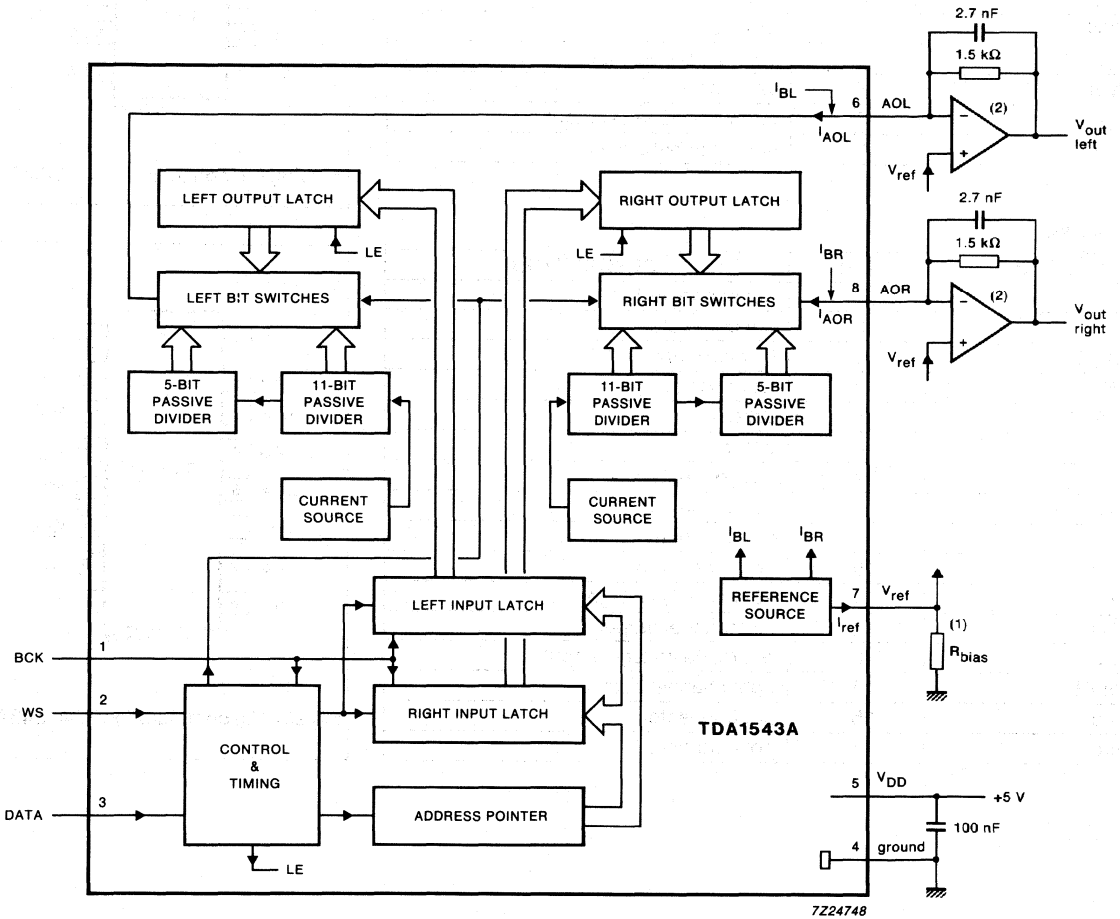
EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA1543A	8	DIL	plastic	SOT97
TDA1543AT	16	mini-pack	plastic	SO16L;SOT162A

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage		3.0	5.0	8.0	V
I_{DD}	supply current		-	50	60	mA
I_{FS}	full scale output current		1.95	2.30	2.65	mA
THD	total harmonic distortion	including noise	-	−75	−70	dB
		at 0 dB	-	0.018	0.032	%
THD	total harmonic distortion	including noise	-	−30	−23	dB
		at −60 dB	-	3.2	7.9	%
t_{cs}	current settling time to ±1 LSB		-	0.5	-	µs
BR	input bit rate at data input		-	-	9.2	Mbits/s
f_{BCK}	clock frequency at clock input		-	-	9.2	MHz
S/N	signal-to-noise ratio	at bipolar zero	90	96	-	dB
TC_{FS}	full scale temperature coefficient	at analog outputs (AOL; AOR)	-	$\pm 500 \times 10^{-6}$	-	K^{-1}
T_{amb}	operating ambient temperature range		−30	-	+85	°C
P_{tot}	total power dissipation		-	250	-	mW
I_{bias}	bias current (adjustable)		−0.6	-	5.0	mA

Dual 16-bit DAC (economy version) (Japanese input format)

TDA1543A



(1) Optional
(2) 2 x 1/2 NE5532

Fig.1 Block diagram.

Dual 16-bit DAC (economy version) (Japanese input format)

TDA1543A

PINNING

SYMBOL	PIN	DESCRIPTION
BCK	1	bit clock input
WS	2	word select input
DATA	3	data input
GND	4	ground
V_{DD}	5	+5 V supply voltage
AOL	6	left channel output
V_{ref}	7	reference voltage output
AOR	8	right channel output

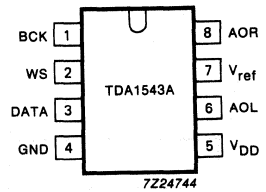


Fig.2(a) Pin configuration TDA1543A.

PINNING

SYMBOL	PIN	DESCRIPTION
n.c.	1	not connected
n.c.	2	not connected
BCK	3	bit clock input
WS	4	word select input
DATA	5	data input
GND	6	ground
n.c.	7	not connected
n.c.	8	not connected
n.c.	9	not connected
n.c.	10	not connected
V_{DD}	11	+5 V supply voltage
AOL	12	left channel output
V_{ref}	13	reference voltage output
AOR	14	right channel output
n.c.	15	not connected
n.c.	16	not connected

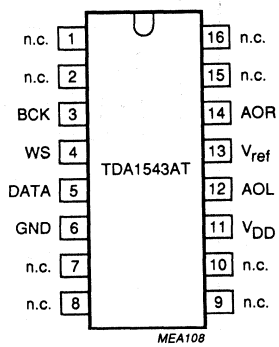
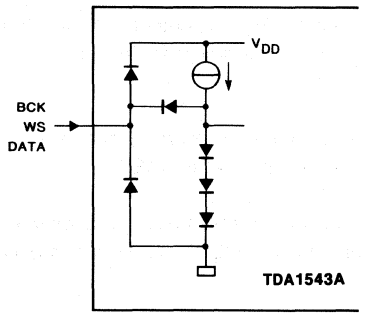
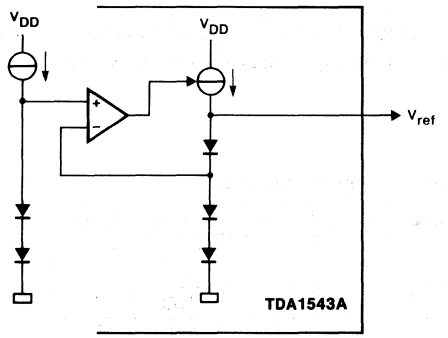


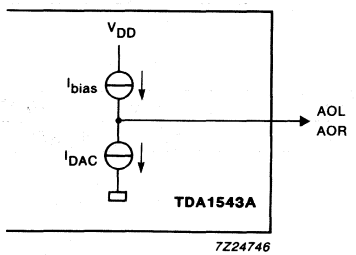
Fig.2(b) Pin configuration TDA1543AT.



(a) input pins BCK, WS and DATA.



(b) output pin V_{ref}.



(c) output pins AOL and AOR.

Fig.3 Circuits at the input and output pins.

FUNCTIONAL DESCRIPTION

The TDA1543A accepts input serial data formats in two's complement with any bit length. Left and right data words are time multiplexed. The most significant bit (bit 1) must always be first. The format of data input is shown in Fig.4 and Fig.5.

This flexible input data format (Japanese) allows easy interfacing with signal processing chips such as interpolation filters, error correction circuits and audio signal processor circuits (ASP).

The high maximum input bit-rate and fast settling current facilitates application in 4 x oversampling systems. An adjustable current is added to the output currents to bias output operational amplifiers (OP1; OP2) for maximum dynamic range (see Fig.1).

With a LOW level on the word select (WS) input data is placed in the right input register and with a HIGH level on the WS input data is placed in the left input register. The data in the input registers is simultaneously latched in the output registers which control the bit switches.

The output current of the DAC is a sink current. The current I_{ref} at the V_{ref} output is adjusted by a resistor or a current source. The current I_{ref} is amplified with gain A_{Ibias} to the bias currents (I_{BL}; I_{BR}) which are added to the output currents.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage range		0	9	V
T_{XTAL}	crystal temperature		-	+150	°C
T_{stg}	storage temperature range		−55	+150	°C
T_{amb}	operating ambient temperature range		−30	+85	°C
V_{es}	electrostatic handling*		−2000	+2000	V

THERMAL RESISTANCE

SYMBOL	PARAMETER	TYP.	UNIT
$R_{th\ j\text{-}a}$	from junction to ambient	100	K/W

* Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

CHARACTERISTICS

V_{DD} = 5 V; T_{amb} = +25 °C; I_{ref} = 0 mA; measured in the circuit of Fig.1; unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD}	supply voltage range		3.0	5.0	8.0	V
I_{DD}	supply current	note 1	-	50	60	mA
RR	ripple rejection	note 2	-	50	-	dB
Digital inputs						
I_{IL}	input current pins (1, 2 and 3) digital inputs LOW	V_I = 0.8 V	-	-	−0.4	mA
I_{IH}	digital inputs HIGH	V_I = 2.0 V	-	-	20	µA
f_{BCK}	input frequency/bit rate clock input pin 1		-	-	9.2	MHz
BR	bit rate data input pin 3		-	-	9.2	Mbits/s
f_{WS}	word select input pin 2		-	-	192	kHz
Analog outputs (AOL; AOR)						
Res	resolution		-	-	16	bits
	output voltage compliance					
$V_{OC(AC)}$	AC		-	±25	-	mV
$V_{OC(DC)}$	DC		1.8	-	V_{DD}−1.2	V
I_{FS}	full scale current		1.95	2.30	2.65	mA
T_{CFS}	full scale temperature coefficient		-	±500 x 10^{-6}	-	K^{-1}
I_{offset}	offset current	I_{ref} = 0 mA	−0.1	0.0	0.1	mA
I_{bias}	bias current (adjustable)		−0.6	-	5.0	mA
AI_{bias}	bias current gain		1.9	2.0	2.1	
Analog outputs (V_{ref})						
V_{ref}	reference voltage output		2.10	2.20	2.30	V
I_{ref}	reference current output		−0.3	-	2.5	mA
THD	total harmonic distortion	including noise at 0 dB;		−75	−70	dB
		note 3, Fig.6		0.018	0.032	%
THD	total harmonic distortion	including noise at −60 dB;	-	−30	−23	dB
		note 3, Fig.6	-	3.2	7.9	%
t_{cs}	settling time ±1 LSB		-	0.5	-	µs
α	channel separation		85	90	-	dB
$\lvert d_{IO} \rvert$	unbalance between outputs	note 4	-	< 0.2	0.3	dB
$\lvert t_d \rvert$	time delay between outputs		-	< 0.2	-	µs
S/N	signal-to-noise ratio	at bipolar zero; note 5	90	96	-	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Timing (Fig.4)						
t_r	rise time		-	-	32	ns
t_f	fall time		-	-	32	ns
t_{CY}	bit clock cycle time		108	-	-	ns
t_{HB}	bit clock HIGH time		22	-	-	ns
t_{LB}	bit clock LOW time		22	-	-	ns
$t_{SU;DAT}$	data set-up time		32	-	-	ns
$t_{HD;DAT}$	data hold time to bit clock	note 6	2	-	-	ns
$t_{HD;WS}$	word select hold time	note 6	2	-	-	ns
$t_{SU;WS}$	word select set-up time		32	-	-	ns

Notes to the characteristics

1. Measured at I_{AOL} = 0 mA and I_{AOR} = 0 mA (code 8000H) and I_{bias} = 0 mA.
2. V_{ripple} = 1% of supply voltage and f_{ripple} = 100 Hz.
3. Measured with 1 kHz sinewave generated at a sampling rate of 192 kHz.
4. Measured with 1 kHz full scale sinewave generated at a sampling rate of 192 kHz.
5. At code 0000H.
6. At this point t_{HD} = 0 ns, this value has been fixed on 2 ns due to tolerances.

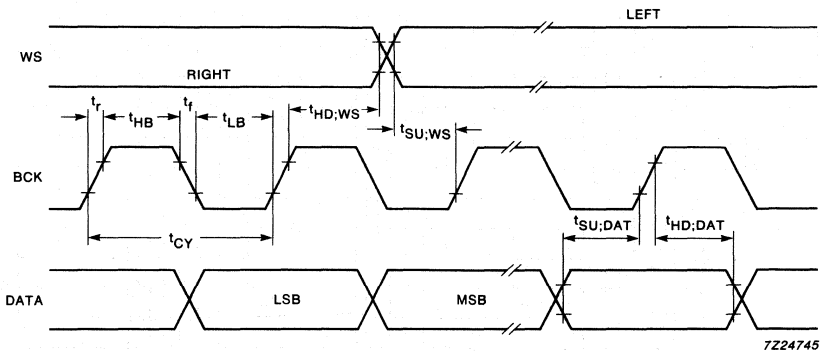


Fig.4 Format of input signals (Japanese format).

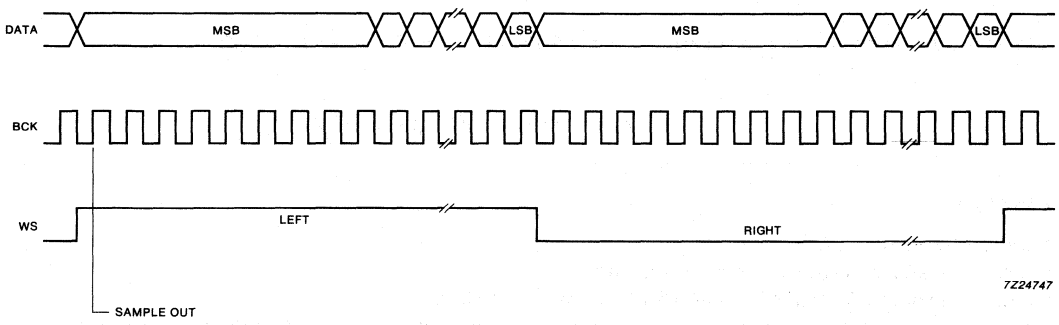
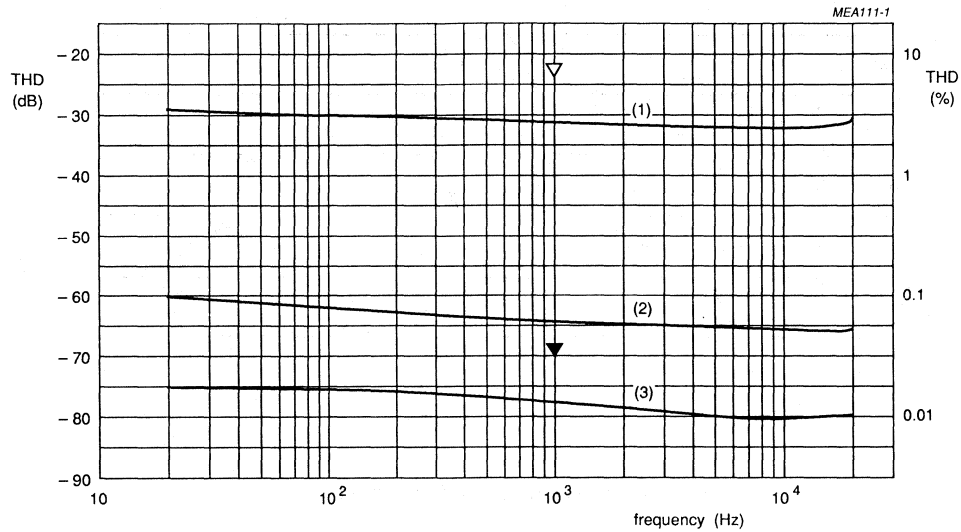


Fig.5 Format of input signals.



(1) Measured including all distortion plus noise over a 20 kHz bandwidth at a level of –60 dB

(2) Measured including all distortion plus noise over a 20 kHz bandwidth at a level of –24 dB

(3) Measured including all distortion plus noise over a 20 kHz bandwidth at a level of –0 dB

Fig.6 Distortion as a function of frequency (4FS)

Notes to Fig.6

- The sample frequency 4FS: 176.4 kHz.
- The supply voltage at the measurement = + 5 V (DC).
- Ref: 0 dB is the output level of a full scale digital sine wave stimulus.
- The graphs are constructed from average values of a small amount of engineering samples therefore no guarantee for typical values is implied.
- The arrows indicate the specification limits for 0 dB and –60 dB level signals.

Philips Semiconductors

Data sheet	
status	Objective specification
date of issue	February 1991

TDA1544
Dual 16-bit low-noise DAC

FEATURES

- 16-bit resolution and 4 x oversampling
- High performance: low distortion, wide dynamic range and high signal-to-noise ratio
- Single 5 V power supply
- No external components required
- Adjustable bias current
- Japanese-input format: time multiplexed, two's complement, TTL

GENERAL DESCRIPTION

The TDA1544 is a dual 16-bit digital-to-analog converter (DAC) and is designed for use in hi-fi digital audio equipment.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA1544	8	DIL	plastic	SOT97
TDA1544T	16	mini-pack	plastic	SO16L;SOT162A

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage		3.0	5.0	8.0	V
I_{DD}	supply current		-	50	60	mA
I_{FS}	full scale output current		2.7	3.0	3.3	mA
THD	total harmonic distortion	including noise	-	−75	−70	dB
		at 0 dB	-	0.018	0.032	%
THD	total harmonic distortion	including noise	-	−33	−23	dB
		at −60 dB	-	2.2	7.9	%
t_{cs}	current settling time to ±1 LSB		-	0.5	-	µs
BR	input bit rate at data input		-	-	9.2	Mbits/s
f_{BCK}	clock frequency at clock input		-	-	9.2	MHz
S/N	signal-to-noise ratio		99	101	-	dB
TC_{FS}	full scale temperature coefficient	at analog outputs (AOL; AOR)	-	$\pm 500 \times 10^{-6}$	-	K^{-1}
T_{amb}	operating ambient temperature range		−30	-	+85	°C
P_{tot}	total power dissipation		-	250	-	mW
I_{bias}	bias current (adjustable)		−0.6	-	5.0	mA

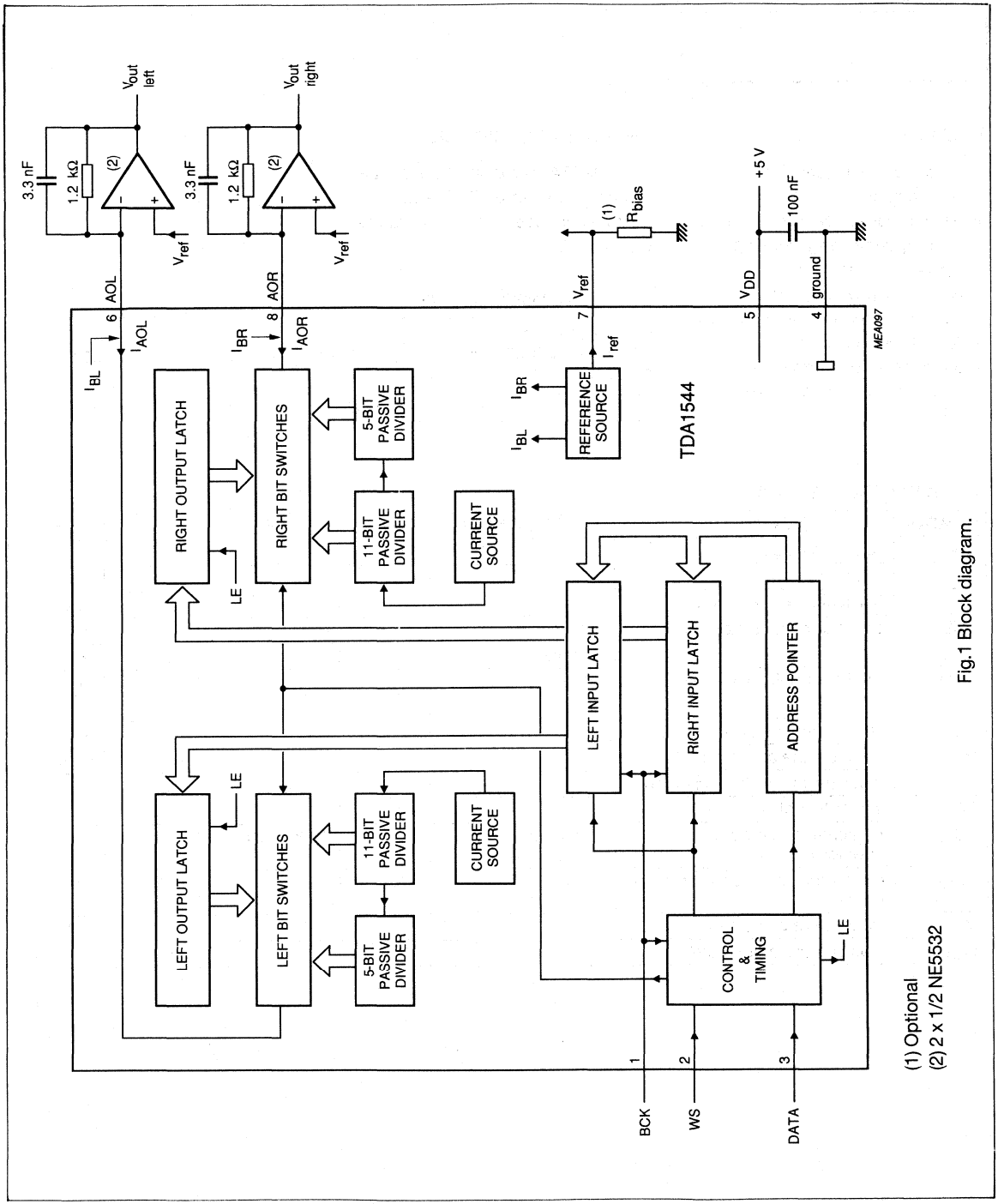


Fig.1 Block diagram.

(1) Optional
(2) 2 x 1/2 NE5532

PINNING

SYMBOL	PIN	DESCRIPTION
BCK	1	bit clock input
WS	2	word select input
DATA	3	data input
GND	4	ground
V_{DD}	5	+5 V supply voltage
AOL	6	left channel output
V_{ref}	7	reference voltage output
AOR	8	right channel output

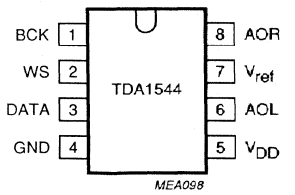


Fig.2(a) Pin configuration TDA1544.

PINNING

SYMBOL	PIN	DESCRIPTION
n.c.	1	not connected
n.c.	2	not connected
BCK	3	bit clock input
WS	4	word select input
DATA	5	data input
GND	6	ground
n.c.	7	not connected
n.c.	8	not connected
n.c.	9	not connected
n.c.	10	not connected
V_{DD}	11	+5 V supply voltage
AOL	12	left channel output
V_{ref}	13	reference voltage output
AOR	14	right channel output
n.c.	15	not connected
n.c.	16	not connected

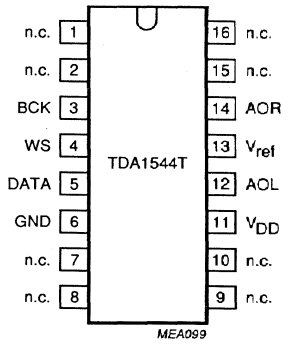
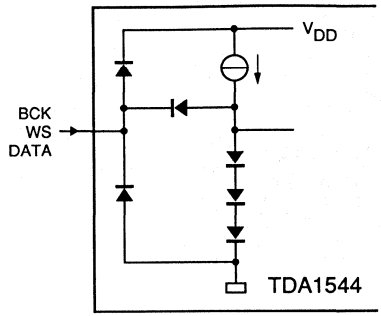
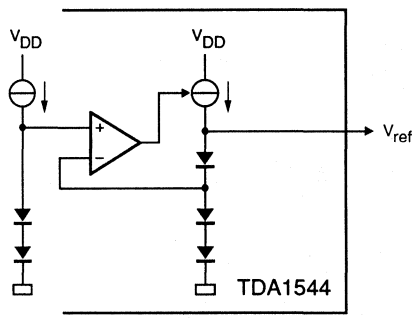


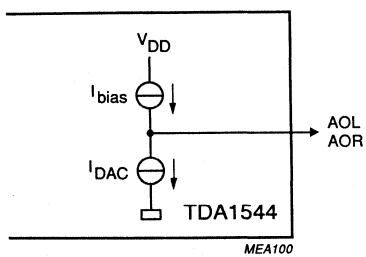
Fig.2(b) Pin configuration TDA1544T.



(a) input pins BCK, WS and DATA.



(b) output pin V_{ref}.



(c) output pins AOL and AOR.

Fig.3 Circuits at the input and output pins.

FUNCTIONAL DESCRIPTION

The TDA1544 accepts input serial data formats of 16-bit word length. Left and right data words are time multiplexed. The most significant bit (bit 1) must always be first. The format of data input is shown in Fig.4 and Fig.5.

The high maximum input bit-rate and fast settling current facilitates application in 4 x oversampling systems. An adjustable current is added to the output currents to bias output operational amplifiers (OP1; OP2) for maximum dynamic range (see Fig.1).

With a LOW level on the word select (WS) input data is placed in the right input register and with a HIGH level on the WS input data is placed in the left input register. The data in the input registers is simultaneously latched in the output registers which control the bit switches.

The output current of the DAC is a sink current. The current I_{ref} at the V_{ref} output is adjusted by a resistor or a current source. The current I_{ref} is amplified with gain A_{Ibias} to the bias currents (I_{BL}; I_{BR}) which are added to the output currents.

LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage range		0	9	V
T_{XTAL}	crystal temperature		-	+150	°C
T_{stg}	storage temperature range		−55	+150	°C
T_{amb}	operating ambient temperature range		−30	+85	°C
V_{es}	electrostatic handling*		−2000	+2000	V

THERMAL RESISTANCE

SYMBOL	PARAMETER	TYP.	UNIT
$R_{th\ j\text{-}a}$	from junction to ambient	100	K/W

* Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

CHARACTERISTICS

V_{DD} = 5 V; T_{amb} = +25 °C; I_{ref} = 0 mA; measured in the circuit of Fig.1; unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD}	supply voltage range		3.0	5.0	8.0	V
I_{DD}	supply current	note 1	-	50	60	mA
RR	ripple rejection	note 2	-	50	-	dB
Digital inputs						
I_{IL}	input current pins (1, 2 and 3) digital inputs LOW	V_I = 0.8 V	-	-	−0.4	mA
I_{IH}	digital inputs HIGH	V_I = 2.0 V	-	-	20	µA
f_{BCK}	input frequency/bit rate clock input pin 1		-	-	9.2	MHz
BR	bit rate data input pin 3		-	-	9.2	Mbits/s
f_{WS}	word select input pin 2		-	-	192	kHz
Analog outputs (AOL; AOR)						
Res	resolution		-	-	16	bits
$V_{OC(AC)}$	output voltage compliance AC		-	±25	-	mV
$V_{OC(DC)}$	DC		1.8	-	V_{DD}−1.2	V
I_{FS}	full scale current		2.7	3.0	3.3	mA
T_{CFS}	full scale temperature coefficient		-	±500 x 10^{-6}	-	K^{-1}
I_{offset}	offset current	I_{ref} = 0 mA V_{AO} = V_{ref}	−0.1	0.0	0.1	mA
I_{bias}	bias current (adjustable)		−0.6	-	5.0	mA
AI_{bias}	bias current gain		0.95	1.00	1.05	
Analog outputs (V_{ref})						
V_{ref}	reference voltage output		2.05	2.20	2.35	V
I_{ref}	reference current output		−0.6	-	5.0	mA
THD	total harmonic distortion	including noise		−75	−70	dB
		at 0 dB; note 3, Fig.6		0.018	0.032	%
THD	total harmonic distortion	including noise	-	−33	−23	dB
		at −60 dB; note 3, Fig.6	-	2.2	7.9	%
t_{cs}	settling time ±1 LSB		-	0.5	-	µs
α	channel separation		85	90	-	dB
$\|d_{IO}\|$	unbalance between outputs	note 4	-	< 0.2	0.3	dB
$\|t_d\|$	time delay between outputs		-	< 0.2	-	µs
S/N	signal-to-noise ratio at bipolar zero	note 5	99	101	-	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Timing (Fig.4)						
t_r	rise time		-	-	32	ns
t_f	fall time		-	-	32	ns
t_{CY}	bit clock cycle time		108	-	-	ns
t_{HB}	bit clock HIGH time		22	-	-	ns
t_{LB}	bit clock LOW time		22	-	-	ns
$t_{SU;DAT}$	data set-up time		32	-	-	ns
$t_{HD;DAT}$	data hold time to bit clock	note 6	2	-	-	ns
$t_{HD;WS}$	word select hold time	note 6	2	-	-	ns
$t_{SU;WS}$	word select set-up time		32	-	-	ns

Notes to the characteristics

1. Measured at I_{AOL} = 0 mA and I_{AOR} = 0 mA (code 8000H) and I_{bias} = 0 mA.
2. V_{ripple} = 1% of supply voltage and f_{ripple} = 100 Hz.
3. Measured with 1 kHz sinewave generated at a sampling rate of 192 kHz.
4. Measured with 1 kHz full scale sinewave generated at a sampling rate of 192 kHz.
5. At code 0000H.
6. At this point t_{HD} = 0 ns, this value has been fixed on 2 ns due to tolerances.

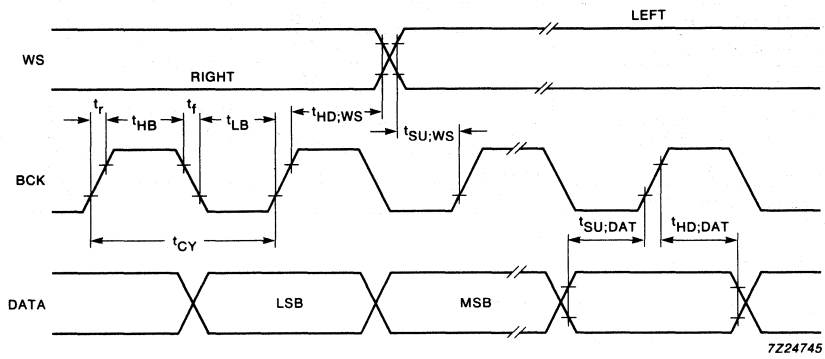


Fig.4 Format of input signals (Japanese format).

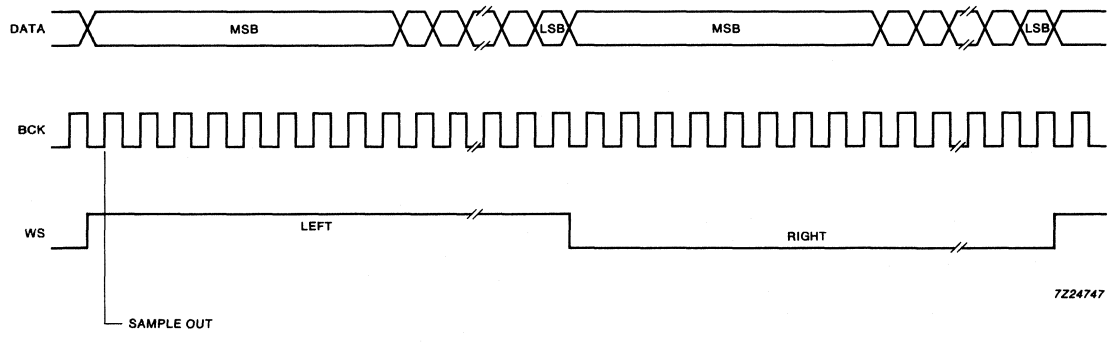
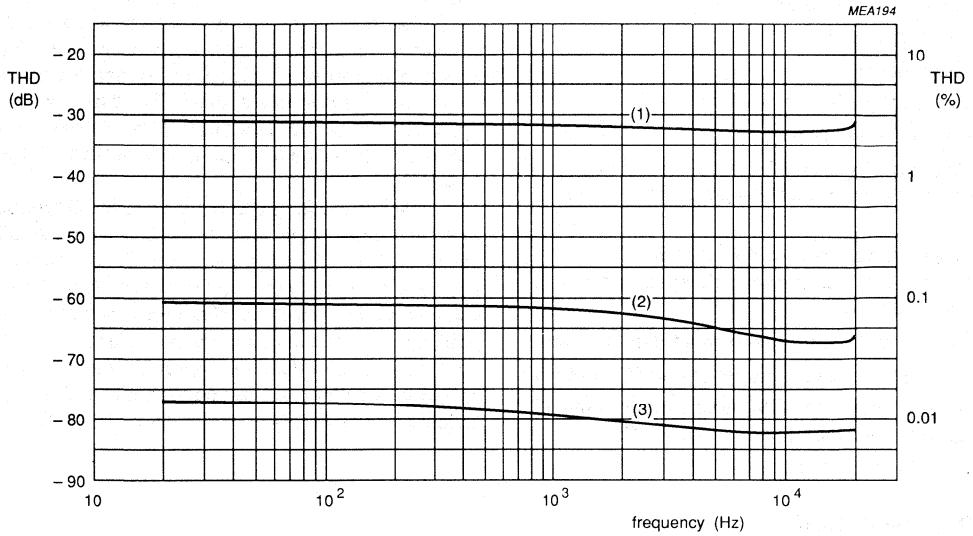


Fig.5 Format of input signals.



(1) Measured including all distortion plus noise over a 20 kHz bandwidth at a level of –60 dB

(2) Measured including all distortion plus noise over a 20 kHz bandwidth at a level of –24 dB

(3) Measured including all distortion plus noise over a 20 kHz bandwidth at a level of –0 dB

Fig.6 Distortion as a function of frequency (4FS)

Notes to Fig.6

- The sample frequency 4FS: 176.4 kHz.
- The supply voltage at the measurement = + 5 V (DC).
- Ref: 0 dB is the output level of a full scale digital sine wave stimulus.
- The graphs are constructed from average values of a small amount of engineering samples therefore no guarantee for typical values is implied.

Stereo continuous calibration DAC TDA1545A

FEATURES

- Space saving package (SO8 or DIL8)
- Low power consumption
- Low total harmonic distortion
- Wide dynamic range (16-bit resolution)
- Continuous calibration concept
- Easy application: single 3 to 5.5 V rail power supply and output- and bias current are proportional to the supply voltage
- Fast settling time permits 2 x, 4 x and 8 x oversampling (serial input) or double speed operation at 4 x oversampling
- Internal bias current ensures maximum dynamic range
- Wide operating temperature range of −40 °C to +85 °C
- Compatible with most of the Japanese input formats: time multiplexed, two's complement and TTL
- No zero crossing distortion.

GENERAL DESCRIPTION

The TDA1545A is the first device of a new generation of the digital-to-analog convertors which embodies the innovative technique of continuous calibration. The largest bit-currents are repeatedly generated by one single current reference source. This duplication is based upon an internal charge storage principle having an accuracy insensitive to ageing, temperature and process variations.

The device is fabricated in a 1.0 μm CMOS process and features an extremely low power dissipation, small package size and easy application. Furthermore, the accuracy of the high coarse current combined with the implemented symmetrical offset decoding method preclude zero-crossing distortion and ensures high quality audio reproduction. Therefore, the continuous calibration digital-to-analog convertor is eminently suitable for use in (portable) digital audio equipment.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA1545A	8	DIL	plastic	SOT97
TDA1545AT	8	mini-pack	plastic	SO8; SOT96A

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage		3	5	5.5	V
I_{DD}	supply current	V_{DD} = 5 V; at code 0000H	–	3.0	4.0	mA
I_{FS}	full scale output current					
		V_{DD} = 5 V	0.9	1.0	1.1	mA
		V_{DD} = 3 V	–	0.6	–	mA
THD	total harmonic distortion	including noise				
		at 0 dB	–	–88	–78	dB
		at 0 dB	–	0.004	0.01	%
		at –60 dB	–	–33	–24	dB
		at –60 dB	–	2.2	6	%
		at –60 dB; A-weighting	–	–35	–	dB
		at –60 dB; A-weighting	–	1.7	–	%
		at –60 dB; A-weighting; R3 = R4 = 11 kΩ; I_{FS} = 2 mA	–	1.4	–	%
S/N	signal-to-noise ratio at bipolar zero					
		A-weighting; at code 0000H	86	98	–	dB
		R3 = R4 = 11 kΩ; I_{FS} = 2 mA	–	101	–	dB
t_{cs}	current settling time to ±1 LSB		–	0.2	–	µs
BR	input bit rate at data input		–	–	18.4	Mbits/s
f_{BCK}	clock frequency at clock input		–	–	18.4	MHz
TC_{FS}	full scale temperature coefficient at analog outputs (IOL; IOR)		–	±400	–	ppm
P_{tot}	total power dissipation	at code 0000H				
		V_{DD} = 5 V	–	15	20	mW
		V_{DD} = 3 V	–	6	–	mW
T_{amb}	operating ambient temperature		–40	–	+85	°C

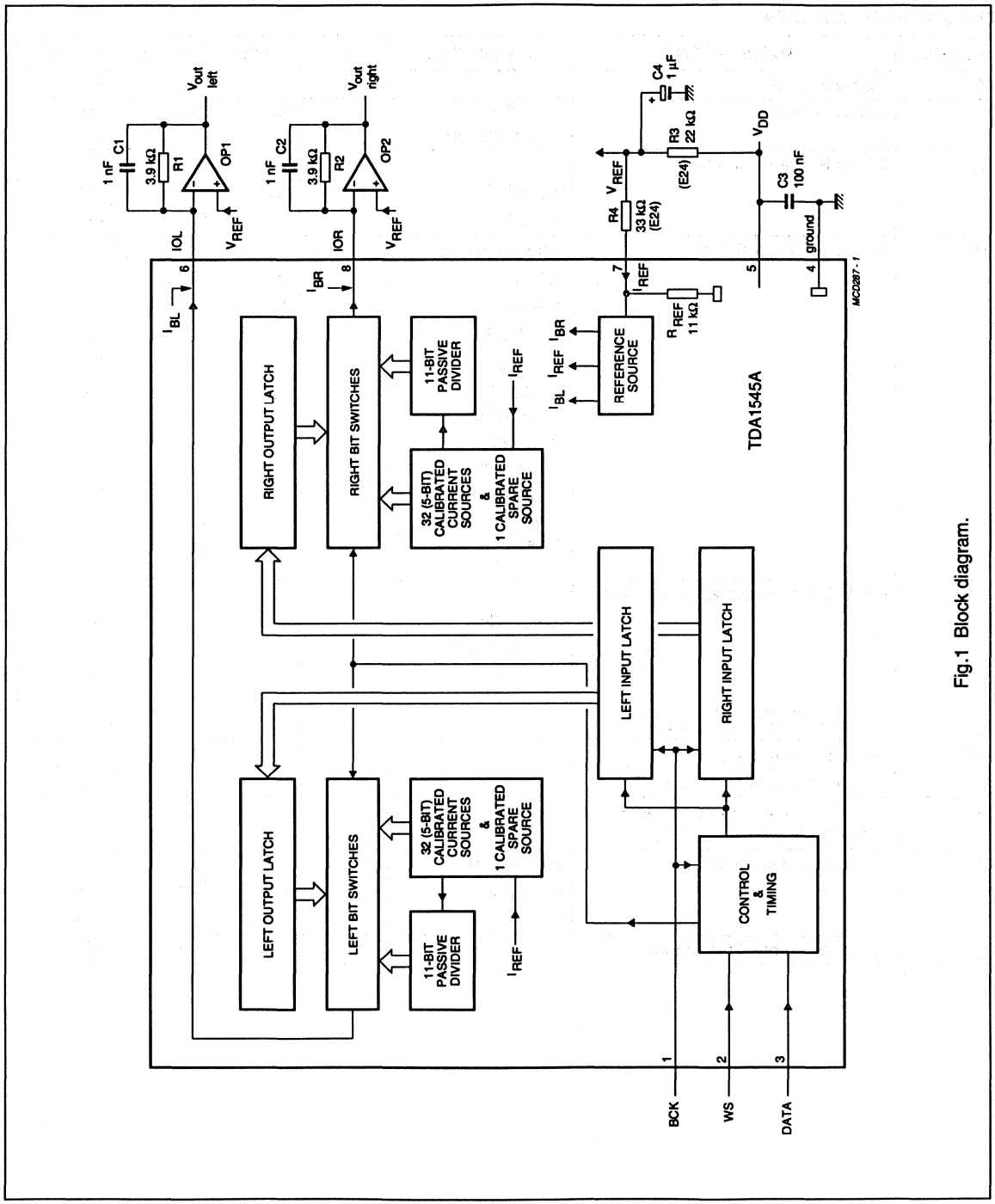


Fig.1 Block diagram.

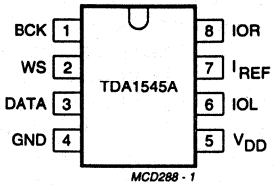


Fig.2 Pin configuration.

PINNING

SYMBOL	PIN	DESCRIPTION
BCK	1	bit clock input
WS	2	word select input
DATA	3	data input
GND	4	ground
V_{DD}	5	positive supply voltage
IOL	6	left channel output
I_{REF}	7	reference current input
IOR	8	right channel output

FUNCTIONAL DESCRIPTION

The basic operation of the continuous calibration DAC is illustrated in Fig.3. The figure shows the calibration principle (Fig.3a) and operation principle (Fig.3b). During calibration of the MOS current source (Fig.3a) transistor M1 is connected as a diode by applying a reference current. The voltage V_{gs} on the intrinsic gate-source capacitance C_{gs} of M1 is then determined by the transistor characteristics. After calibration of the drain current to the reference value I_{REF}, the switch S1 is opened and S2 is switched to the other position (Fig.3b). The gate-to-source voltage V_{gs} of M1 is not changed because the charge on C_{gs} is preserved. Therefore the drain current of M1 will still be equal to I_{REF} and this exact duplicate of I_{REF} is now available at the I_{out} terminal. The 32 current sources and the spare current source of the TDA1545A are continuously calibrated (see Fig.1). The spare current is included to allow for continuous convertor operation. The output of one calibrated source is connected to an 11-bit binary current divider consisting of 2048 transistors. A symmetrical offset decoding principle is incorporated and arranges the bit switching in such a way that the zero-crossing is performed only by the LSB currents. The TDA1545A accepts input serial data formats of 16-bit word length. Left and right data words are time multiplexed. The most significant bit (bit 1) must always be first. The format of data input is shown in Fig.4 and Fig.5. With a LOW level on the word select input (WS) input data is placed in the right input register and with a HIGH level on the WS input data is placed in the left input register. The data in the input registers is simultaneously latched in the output registers which control the bit switches. An internal bias current Ibias (see IBL and IBR in Fig.1) is added to the full scale output current IFS in order to achieve the maximum dynamic range at the outputs of OP1 and OP2 (see Fig.1). The reference input current IREF controls with gain AFS the current IFS which is a sink current and with gain Abias the I_{bias} which is a source current (note 1). The current I_{REF} is proportional to V_{DD} so the I_{FS} and I_{bias} will also be proportional to V_{DD} (note 2) because A_{FS} and A_{bias} are constant. The reference output voltage V_{REF} in Fig.1 is 2/3 V_{DD}. In this way the maximum dynamic range is achieved over the entire power supply range. The tolerance of the reference input current in Fig.1 depends on the tolerance of the resistors R3, R4 and R_{REF} (note 3).

Notes to the functional description

1. $I_{FS} = A_{FS} \times I_{REF}$ and $I_{bias} = A_{bias} \times I_{REF}$
2. $\frac{V_{DD1}}{V_{DD2}} = \frac{I_{FS1}}{I_{FS2}} = \frac{I_{bias1}}{I_{bias2}}$
3. $\Delta I_{REF} = I_{REF} - \frac{V_{DD}}{R3 + \Delta R3 + R4 + \Delta R4 + R_{REF} + \Delta R_{REF}}$

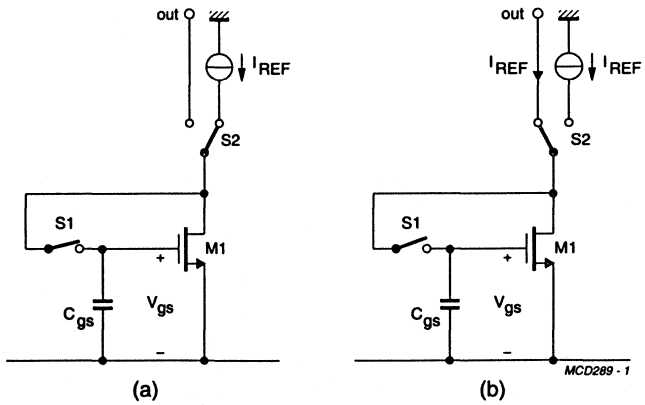


Fig.3 Calibration principle; (a) calibration, (b) operation.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_P	positive supply voltage	–	6	V
T_{XTAL}	maximum crystal temperature	–	+150	°C
T_{stg}	storage temperature	−55	+150	°C
T_{amb}	operating ambient temperature	−40	+85	°C
V_{es}	electrostatic handling (note 1)	−2000	+2000	V
V_{es}	electrostatic handling (note 2)	−200	+200	V

Notes

1. Equivalent to discharging a 100 pF capacitor via a 1.5 kΩ series resistor.
2. Machine model; C = 200 pF, L = 0.5 μH, R = 10 Ω, 3 zaps positive and negative.

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient in free air	
	SOT97	100 K/W
	SOT96A	210 K/W

CHARACTERISTICS

V_{DD} = 5 V; T_{amb} = +25 °C; measured in the circuit of Fig.1; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage		3.0	5.0	5.5	V
I_{DD}	supply current	note 1	–	3.0	4.0	mA
RR	ripple rejection	note 2	–	30	–	dB
Digital inputs (WS; BCK; DATA)						
$\|I_{IL}\|$	input leakage current LOW	V_I = 0.8 V	–	–	10	μA
$\|I_{IH}\|$	input leakage current HIGH	V_I = 2.4 V	–	–	10	μA
f_{BCK}	bit clock input frequency		–	–	18.4	MHz
BR	bit rate data input		–	–	18.4	Mbits/s
f_{WS}	word select input		–	–	384	kHz
Timing (Fig.4)						
t_r	rise time		–	–	12	ns
t_f	fall time		–	–	12	ns
t_{CY}	bit clock cycle time		54	–	–	ns
t_{HB}	bit clock HIGH time		15	–	–	ns
t_{LB}	bit clock LOW time		15	–	–	ns
$t_{SU;DAT}$	data set-up time		12	–	–	ns
$t_{HD;DAT}$	data hold time		2	–	–	ns
$t_{HD;WS}$	word select hold time		2	–	–	ns
$t_{SU;WS}$	word select set-up time		12	–	–	ns
Analog input (I_{REF})						
R_{REF}	reference resistor (see Fig.1)		7.4	11.0	14.6	kΩ
Analog outputs (IOL; IOR)						
Res	resolution		–	–	16	bit
V_{DCC}	DC output voltage compliance		2.0	–	V_{DD}–1	V
I_{FS}	full scale current		0.9	1.0	1.1	mA
T_{CFS}	full scale temperature coefficient		–	±400	–	ppm
I_{bias}	bias current		643	714	785	μA
A_{FS}	reference input current to full scale output current gain		–	13.2	–	
A_{bias}	reference input current to bias current gain		–	9.42	–	
THD	total harmonic distortion	including noise at 0 dB; note 3, see Fig.6	– –	–88 0.004	–78 0.01	dB %
THD	total harmonic distortion	including noise at –60 dB; note 3, Fig.6	– –	–33 2.2	–24 6	dB %

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
THD	total harmonic distortion	including noise at −60 dB, A-weigthing	–	−35	–	dB
			–	1.8	–	%
		R3 = R4 = 11 kΩ see Fig.1; I_{FS} = 2 mA	–	1.4	–	%
THD	total harmonic distortion	including noise at 0 dB; note 4	–	−84	−70	dB
			–	0.006	0.03	%
t_{cs}	settling time ±1 LSB		–	0.2	–	μs
α	channel separation		86	95	–	dB
$\lvert d_{IO}\rvert$	unbalance between outputs	note 3	–	0.2	0.3	dB
$\lvert t_d\rvert$	delay time between outputs		–	±0.2	–	μs
S/N	signal-to-noise ratio (A-weighting)	at bipolar zero; note 1	86	98	–	dB
S/N	signal-to-noise ratio (A-weighting)	at bipolar zero; note 5	–	101	–	dB

Notes

1. At code 0000H.
2. V_{ripple} = 1% of supply voltage and f_{ripple} = 100 Hz.
3. Measured with 1 kHz sinewave generated at a sampling rate of 192 kHz.
4. Measured with 1 kHz sinewave over a 20 Hz to 20 kHz bandwidth generated at a sampling rate of 192 kHz.
5. R3 = R4 = 11 kΩ; see Fig.1; I_{FS} = 2 mA.

TEST AND APPLICATION INFORMATION

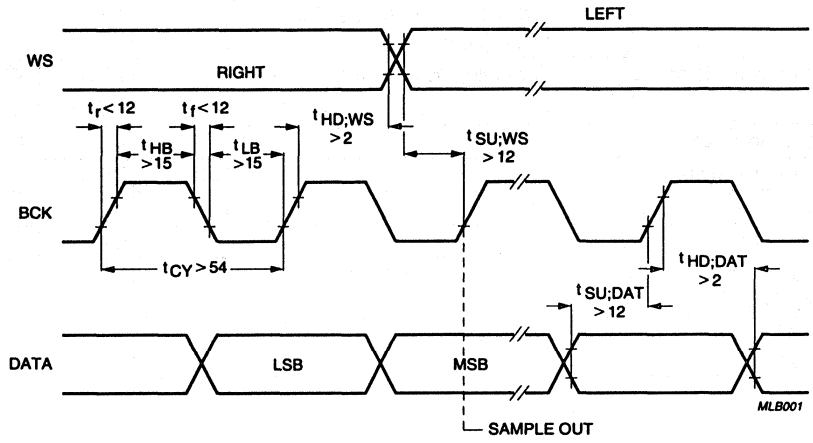


Fig.4 Timing and input signals.

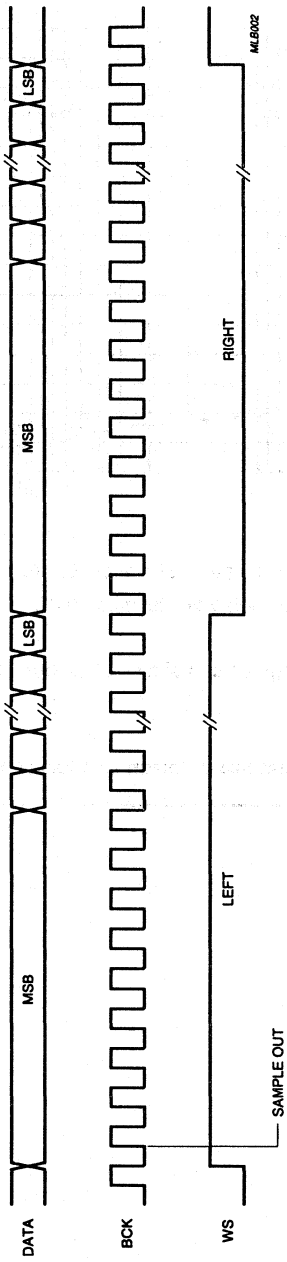
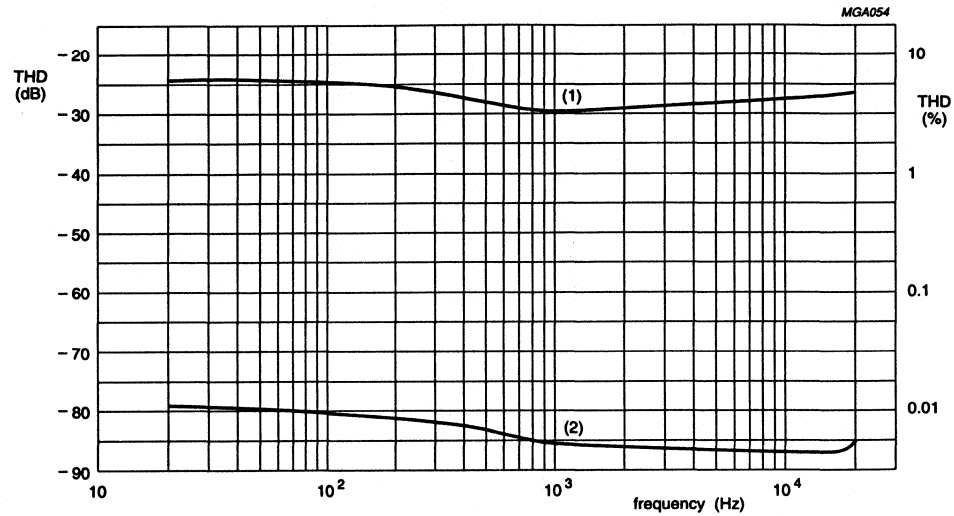


Fig.5 Format of input signals.

APPLICATION INFORMATION



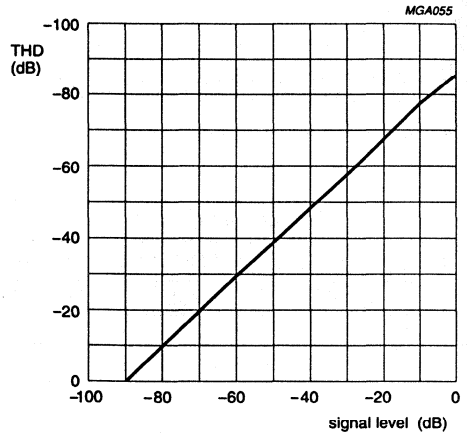
(1) Measured including all distortion plus noise at a level of −60 dB

(2) Measured including all distortion plus noise at a level of −0 dB

The sample frequency 4FS: 176.4 kHz

The graphs are constructed from average values of a small amount of engineering samples therefore no guarantee for typical values is implied

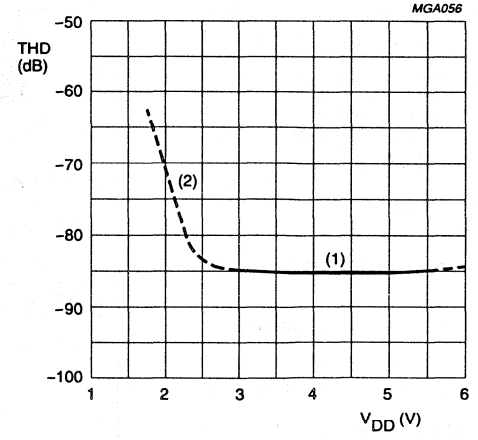
Fig.6 Total harmonic distortion as a function of frequency (4FS).



The sample frequency 4FS: 176.4 kHz

The graphs are constructed from average values of a small amount of engineering samples therefore no guarantee for typical values is implied

Fig.7 Total harmonic distortion as a function of signal level (4FS).



(1) Measured within the specified operating supply voltage range

(2) Measured outside the specified operating supply voltage range

The sample frequency 4FS: 176.4 kHz

The graphs are constructed from average values of a small amount of engineering samples therefore no guarantee for typical values is implied

Fig.8 Total harmonic distortion as a function of supply voltage V_{DD} (4FS).

Dual top-performance bitstream DAC

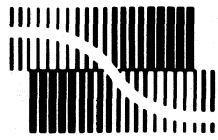
TDA1547

FEATURES

- Top-grade audio performance
  - very low harmonic distortion
  - high signal-to-noise ratio
  - wide dynamic range of approximately 108 dB (not A-weighted)
- High crosstalk immunity
- Bitstream concept
  - high over-sampling rate up to 192 f_s
  - pulse-density modulation
  - inherently monotonic
  - no zero-crossing distortion

GENERAL DESCRIPTION

The TDA1547 is a dedicated one-bit digital-to-analog converter to facilitate a high fidelity sound reproduction of digital audio. The TDA1547 is extremely suitable for use in high quality audio systems such as Compact Disc and DAT players, or in digital amplifiers and digital signal processing systems. The TDA1547 is used in combination with the SAA7350 bitstream circuit, which includes the third-order noise shaper. The excellent performance of the SAA7350 and TDA1547 bitstream conversion system is obtained by separating the noise shaping circuit and the one-bit conversion circuit over two IC's, thereby reducing the crosstalk between the digital and analog parts. The TDA1547 one-bit converter is processed in BIMOS. In the digital logic and drivers bipolar transistors are used to optimize speed and to reduce digital noise generation. In the analog part the bipolar transistors are used to obtain high performance of the operational amplifiers. Special layout precautions have been taken to achieve a high crosstalk immunity. The layout of the TDA1547 has fully separated left and right channels and supply voltage lines between the digital and analog sections.



ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA1547	32	SDIL	plastic	SOT232A

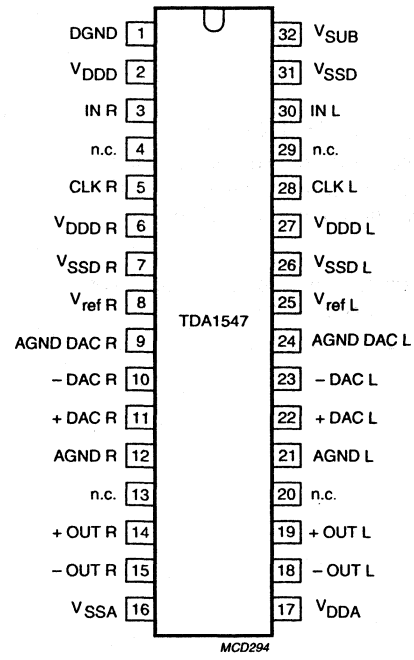


Fig.1 Pinning diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
DGND	1	0 V digital supply
V_{DDD}	2	5 V digital supply for both channels
IN R	3	serial one-bit data input for the right channel
n.c.	4	pin not connected; should preferably be connected to digital ground
CLK R	5	clock input for the right channel
$V_{DDD\ R}$	6	5 V digital supply for the right channel; this voltage determines the internal logic HIGH level in the right channel
$V_{SSD\ R}$	7	–3.5 V digital supply for the right channel; this voltage determines the internal logic LOW level in the right channel
$V_{ref\ R}$	8	–4 V reference voltage for the right channel switched capacitor DAC
AGND DAC R	9	0 V reference voltage for the right channel switched capacitor DAC; this pin should be connected to analog ground
–DAC R	10	output from the right negative switched capacitor DAC; feedback connection for the right negative operational amplifier
+DAC R	11	output from the right positive switched capacitor DAC; feedback connection for the right positive operational amplifier
AGND R	12	0 V reference voltage for both right channel operational amplifiers
n.c.	13	pin not connected; should preferably be connected to analog ground
+OUT R	14	+ output of the switched capacitor operational amplifier
–OUT R	15	– output of the switched capacitor operational amplifier
V_{SSA}	16	–5 V analog supply
V_{DDA}	17	5 V analog supply
–OUT L	18	– output of the switched capacitor operational amplifier
+OUT L	19	+ output of the switched capacitor operational amplifier
n.c.	20	pin not connected; should preferably be connected to analog ground
AGND L	21	0 V reference voltage for both left channel operational amplifiers
+DAC L	22	output from the left positive switched capacitor DAC; feedback connection for the left positive operational amplifier
–DAC L	23	output from the left negative switched capacitor DAC; feedback connection for the left negative operational amplifier
AGND DAC L	24	0 V reference voltage for the left channel switched capacitor DAC; this pin should be connected to analog ground
$V_{ref\ L}$	25	–4 V reference voltage for the left channel switched capacitor DAC
$V_{SSD\ L}$	26	–3.5 V digital supply for the left channel; this voltage determines the internal logic LOW level in the left channel
$V_{DDD\ L}$	27	5 V digital supply for the left channel; this voltage determines the internal logic HIGH level in the left channel

SYMBOL	PIN	DESCRIPTION
CLK L	28	clock input for the left channel
n.c.	29	pin not connected; should preferably be connected to digital ground
IN L	30	serial one-bit data input for the left channel
V_{SSD}	31	−5 V digital supply for both channels
V_{SUB}	32	−5 V substrate voltage

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
Supply voltages						
$V_{DDD\ L,\ R}$	positive digital supply voltage for one channel; pins 27 and 6		4.5	5.0	5.5	V
V_{DDD}	digital supply voltage for both channels; pin 2		4.5	5.0	5.5	V
$V_{SSD\ L,\ R}$	negative digital supply voltage for one channel; pins 26 and 7		−4.0	−3.5	−3.0	V
V_{SSD}	negative digital supply voltage for both channels; pin 31		−5.5	−5.0	−4.5	V
V_{DDA}	positive analog supply voltage; pin 17		4.5	5.0	6	V
V_{SSA}	negative analog supply voltage ; pin 16		−6.0	−5.0	−4.5	V
Supply current						
$I_{DDD\ L,\ R}$	positive digital supply current for one channel; pins 27 and 6		-	0.1	-	mA
I_{DDD}	digital supply current for both channels; pin 2		-	29.0	-	mA
$I_{SSD\ L,\ R}$	negative digital supply current for one channel; pins 26 and 7		-	−0.1	-	mA
I_{SSD}	negative supply current for both channels; pin 31		-	−28.0	-	mA
I_{DDA}	positive analog supply current; pin 17		-	51.0	-	mA
I_{SSA}	negative analog supply current; pin 16		-	−51.0	-	mA
P_{tot}	total power dissipation		-	800	-	mW
$V_{OUT(RMS)}$	output voltage (RMS value)	f_{CLK} = 8.46 MHz; notes 1 and 2	0.85	1.0	1.15	V

SYMBOL	PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
Supply current						
(THD + N)/S	THD + Noise; 0 dB	1 kHz; notes 2 and 3	-	−101	−96	dB
			-	0.0009	0.0016	%
(THD + N)/S	THD + Noise; 0 dB	f = 20 Hz to 20 kHz; notes 2 and 4	-	−101	-	dB
			-	0.0009	-	%
(THD + N)/S	THD + Noise; −20 dB	f = 1 kHz; notes 2 and 3	-	−88	−84	dB
(THD + N)/S	THD + Noise; −60 dB	f = 1 kHz; notes 2 and 3	-	−48	−44	dB
S/N	signal-to-noise ratio	pattern 0101..; notes 2 and 5	109	111	-	dB
S/N	signal-to-noise ratio; "A"-weighting	pattern 0101..; notes 2 and 5	-	113	-	dB
f_{CLK}	maximum clock frequency		-	-	10	MHz
α	channel separation	f = 1 kHz	101	115	-	dB
T_{amb}	operating ambient temperature		−20	-	70	°C

Notes to the quick reference data

1. Output level tracks linearly with both the clock frequency and the reference voltage ($V_{ref\ L}$ or $V_{ref\ R}$)
2. Device measured in differential mode with external components as shown in Fig.5.
3. Measured with a one-bit data signal generated by the SAA7350 from an 8 f_s (352.8 kHz), 20-bit, 1 kHz digital sinewave. Measured over a 20 Hz to 20 kHz bandwidth.
4. Measured with a one-bit data signal generated by the SAA7350 from an 8 f_s (352.8 kHz), 20-bit, 20 Hz to 20 kHz digital sinewave. Measured over a 20 Hz to 20 kHz bandwidth.
5. The specified signal-to-noise ratio includes noise introduced by the application components as shown in Fig.5.

FUNCTIONAL DESCRIPTION

Both channels are completely separated to reach the desired high crosstalk suppression level.
Each channel consists of the following functional parts:

- One-bit input, which latches the incoming data to the system clock.
- Switch driver circuit, which generates the non-overlapping clock- and data-signals that control the DAC switched capacitor networks.
- Switched capacitor network, this forms the actual DAC function, it supplies charge packets to the low-pass filter, under control of the incoming one-bit code.
- Two high performance operational amplifiers, that perform the charge packet to voltage conversion and deliver a differential output signal. The first pole of the low-pass filter is built around them.

THERMAL RESISTANCE

SYMBOL	PARAMETER	MAX.	UNIT
$R_{th\ j\text{-}a}$	from junction to ambient	60	K/W

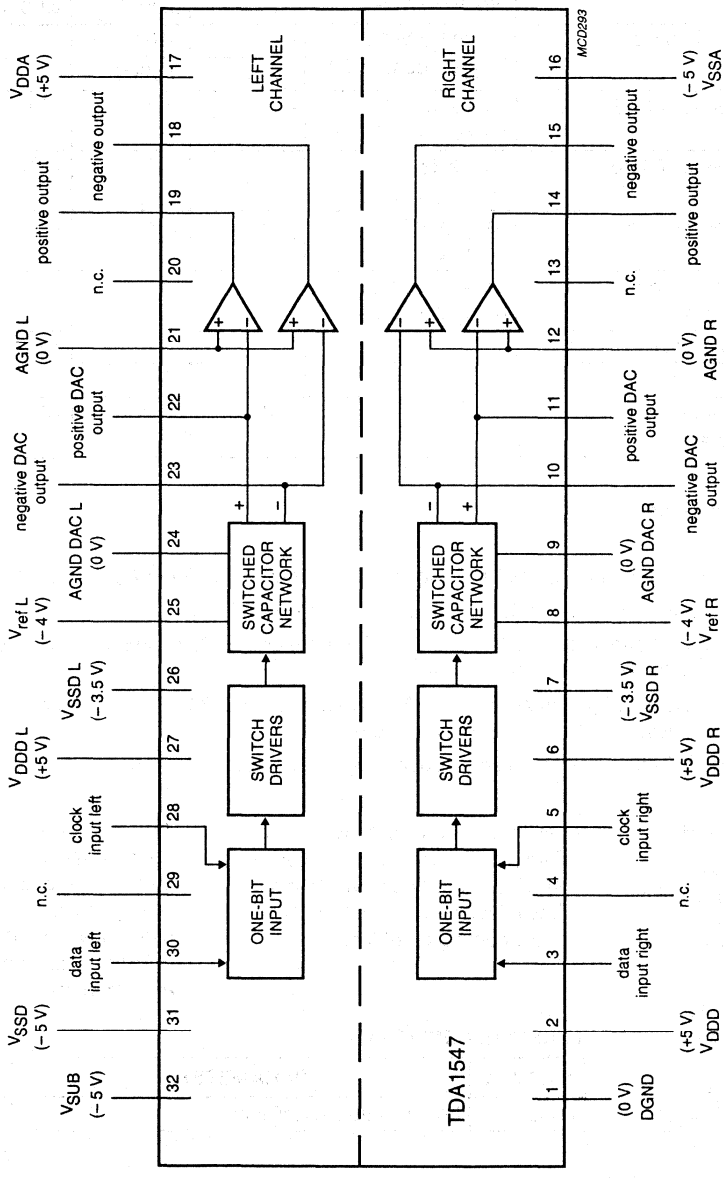


Fig.2 Block diagram.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX.	UNIT
V_{SUB}	negative substrate voltage; pin 32	note 1	−7.0	-	V
$V_{DDD\ L,\ R}$	positive digital supply voltage; pins 27 and 6		-	5.5	V
V_{DDD}	positive digital supply voltage; pin 2		-	5.5	V
$V_{SSD\ L,\ R}$	negative digital supply voltage; pins 26 and 7		−4.0	-	V
V_{SSD}	negative digital supply voltage; pin 31		−5.5	-	V
V_{DDA}	positive analog supply voltage; pin 17		-	6.0	V
V_{SSA}	negative analog supply voltage; pin 16		−6.0	-	V
$V_{DDD\ L,\ R}$ - $V_{SSD\ L,\ R}$	supply voltage difference between pins 27, 6 and pins 26, 7		-	9.0	V
P_{tot}	total power dissipation	T_{amb} = 70 °C	-	1300	mW
$V_{ref\ L,\ R}$	input reference voltage; pins 25 and 8		−6.0		V
$V_{CLK\ L,\ R}$	input voltage clock; pins 28 and 5		−0.5	V_{DDD}+0.5	V
$V_{I\ L}$	input voltage channel; pin 30		−0.5	V_{DDD}+0.5	V
$V_{I\ R}$	input voltage channel; pin 3		−0.5	V_{DDD}+0.5	V
T_{amb}	operating ambient temperature		−20	70	°C
T_{stg}	storage temperature		−40	150	°C
T_{XTAL}	maximum crystal temperature		-	150	°C
V_{ES}	electrostatic handling	note 2	-	2000	V

Notes to the limiting values

1. The substrate voltage must be lower than or equal to the lowest supply voltage.
2. Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

CHARACTERISTICS

V_{DDD}, $V_{DDD\ L.\ R}$, V_{DDA} = +5 V; V_{SSD}, V_{SSA} = −5 V, $V_{SSD\ L.\ R}$ = −3.5 V; $V_{ref\ L.\ R}$ = −4 V; T_{amb} = 25°C; f_{CLK} = 8.46 MHz; unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY						
V_{SUB}	negative substrate voltage; pin 32	note 1	−7.0	-	−4.5	V
$V_{DDD\ L.\ R}$	positive digital supply voltage for one channel; pins 27 and 6		4.5	5.0	5.5	V
V_{DDD}	digital supply voltage for both channels; pin 2		4.5	5.0	5.5	V
$V_{SSD\ L.\ R}$	negative digital supply voltage for one channel; pins 26 and 7		−4.0	−3.5	−3.0	V
V_{SSD}	negative digital supply voltage for both channels; pin 31		−5.5	−5.0	−4.5	V
V_{DDA}	positive analog supply voltage; pin 17		4.5	5.0	6.0	V
V_{SSA}	negative analog supply voltage; pin 16		−6.0	−5.0	−4.5	V
$V_{DDD\ L.\ R}$ - $V_{SSD\ L.\ R}$	supply voltage difference between pins 27, 6 and pins 26, 7		-	-	9.0	V
$V_{SSD\ L.\ R}$ - V_{SSD}	supply voltage difference between pins 26, 7 and pin 31		1.3	-	-	V
$I_{DDD\ L.\ R}$	positive digital supply current for one channel; pins 27 and 6		-	0.1	-	mA
I_{DDD}	digital supply current for both channels; pin 2			29.0	46	mA
$I_{SSD\ L.\ R}$	negative digital supply current for one channel; pins 26 and 7		-	−0.1	-	mA
I_{SSD}	negative supply current for both channels; pin 31		−45	−28.0	-	mA
$-I_{DDA}$	positive analog supply current; pin 17		-	51.0	63	mA
I_{SSA}	negative analog supply current; pin 16		−63.0	−51.0	-	mA
P_{SSR1}	power supply rejection ratio	$V_{DDD\ L.\ R}$; note 6	50	-	-	dB
P_{SSR2}	power supply rejection ratio	V_{DDD}; note 6	50	-	-	dB
P_{SSR3}	power supply rejection ratio	$V_{SSD\ L.\ R}$; note 6	60	-	-	dB
P_{SSR4}	power supply rejection ratio	V_{SSD}; note 6	50	-	-	dB
P_{SSR5}	power supply rejection ratio	V_{DDA}; note 6	60	-	-	dB
P_{SSR6}	power supply rejection ratio	V_{SSA}; note 6	60	-	-	dB
P_{tot}	total power dissipation		-	800	-	mW
Clock - Input						
V_{IL}	input voltage LOW		-	-	0.5	V
V_{IH}	input voltage HIGH		4.5	-	-	V
I_{IL}	input current LOW	V_i = 0.5 V	−10	-	10	µA

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Clock - Input						
I_{IH}	input current HIGH	V_i = 4.5 V	−10	-	10	µA
C_i	clock input capacitance		-	5	-	pF
f_{CLK}	clock input frequency		-	-	10	MHz
Channel left/right inputs						
V_{IL}	input voltage LOW		-	-	0.5	V
V_{IH}	input voltage HIGH		-	4.5	-	V
I_{IL}	input current LOW	V_i = 0.5 V	−10	-	10	µA
I_{IH}	input current HIGH	V_i = 4.5 V	−10	-	10	µA
C_i	channel input capacitance; pins 3, 30		-	5	-	pF
V_{ref}	reference input voltage; pins 8, 25	note 2	-	−4 ±0.4	-	V
Audio outputs						
$V_{OUT(RMS)}$	output voltage (RMS value); pins 14, 19; pins 15, 18	notes 2 and 3	0.85	1.0	1.15	V
(THD + N)/S	THD + Noise; 0 dB	f = 1 kHz; notes 3 and 4	-	−101	−96	dB
			-	0.0009	0.0016	%
(THD + N)/S	THD + Noise; 0 dB	20 Hz - 20 kHz; notes 3 and 5	-	−101	-	dB
			-	0.0009	-	%
(THD + N)/S	THD + Noise; −20 dB	f = 1 kHz; notes 3 and 4	-	−88	−84	dB
(THD + N)/S	THD + Noise; −60 dB	f = 1 kHz; notes 3 and 4	-	−48	−44	dB
S/N	signal-to-noise ratio	pattern 0101; notes 3 and 7	109	111	-	dB
S/N	signal-to-noise ratio; "A"-weighting	pattern 0101; notes 3 and 7	-	113	-	dB
α	channel separation	f = 1 kHz	101	115	-	dB
Timing						
t_r	rise time clock input	C_L = 20 pF	-	5	10	ns
t_f	fall time clock input	C_L = 20 pF	-	5	10	ns
$t_{CLK\ L}$	clock input LOW time		45	-	-	ns
$t_{CLK\ H}$	clock input HIGH time		45	-	-	ns
t_r	channel input rise time	C_L = 20 pF	-	10	15	ns
t_f	channel input fall time	C_L = 20 pF	-	10	15	ns
t_{HD}	channel input hold time		25	-	-	ns
t_{SU}	channel input set-up time		0	-	-	ns

Notes to the characteristics

1. The substrate voltage must be lower than or to equal than the lowest supply voltage.
2. Output level tracks linearly with both the clock frequency and the reference voltage ($V_{ref\ L}$ or $V_{ref\ R}$).
3. Device measured in differential mode with external components as shown in Fig.5.
4. Measured with a one-bit data signal generated by the SAA7350 from an 8 f_s (352.8 kHz), 20-bit, 1 kHz digital sinewave. Measured over a 20 Hz to 20 kHz bandwidth.
5. Measured with a one-bit data signal generated by the SAA7350 from an 8 f_s (352.8 kHz), 20-bit, 20 Hz to 20 kHz digital sinewave. Measured over a 20 Hz to 20 kHz bandwidth.
6. Power supply rejection ratio measured with f_{ripple} = 1 kHz and v_{ripple} = 100 mV.
7. The specified signal-to-noise ratio includes noise introduced by the application components as shown in Fig.5.

TIMING

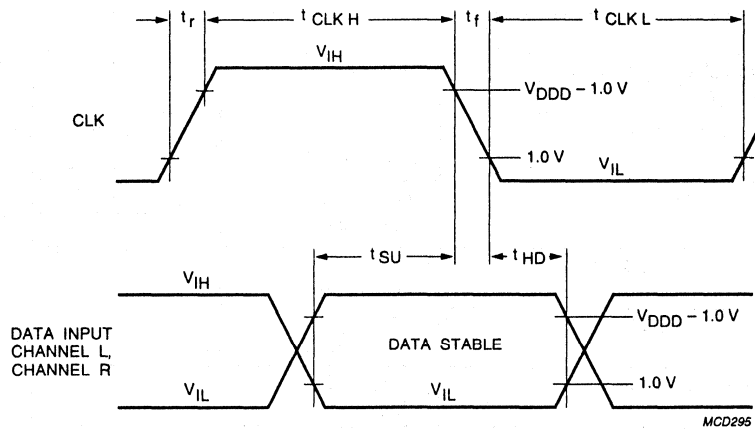


Fig.3 Timing waveform.

APPLICATION INFORMATION

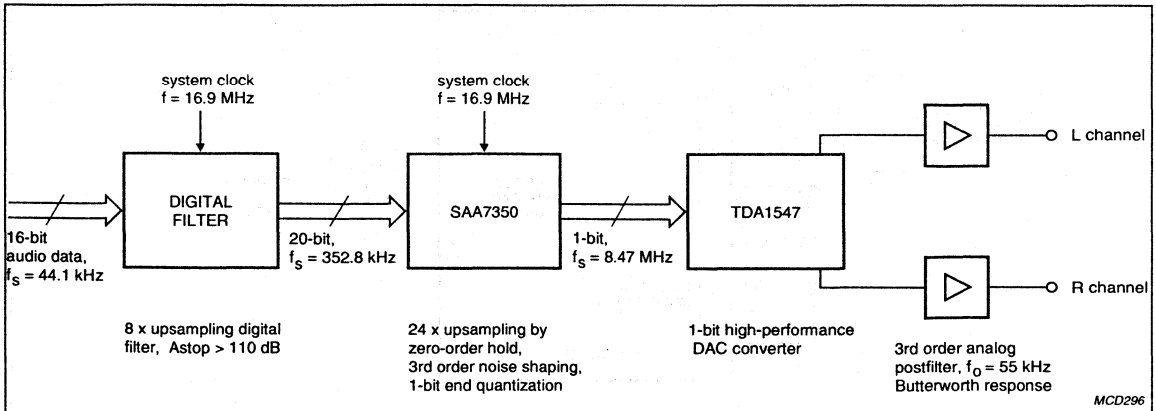


Fig.4 CD-range bitstream reconstruction system (192 f_s over-sampling).

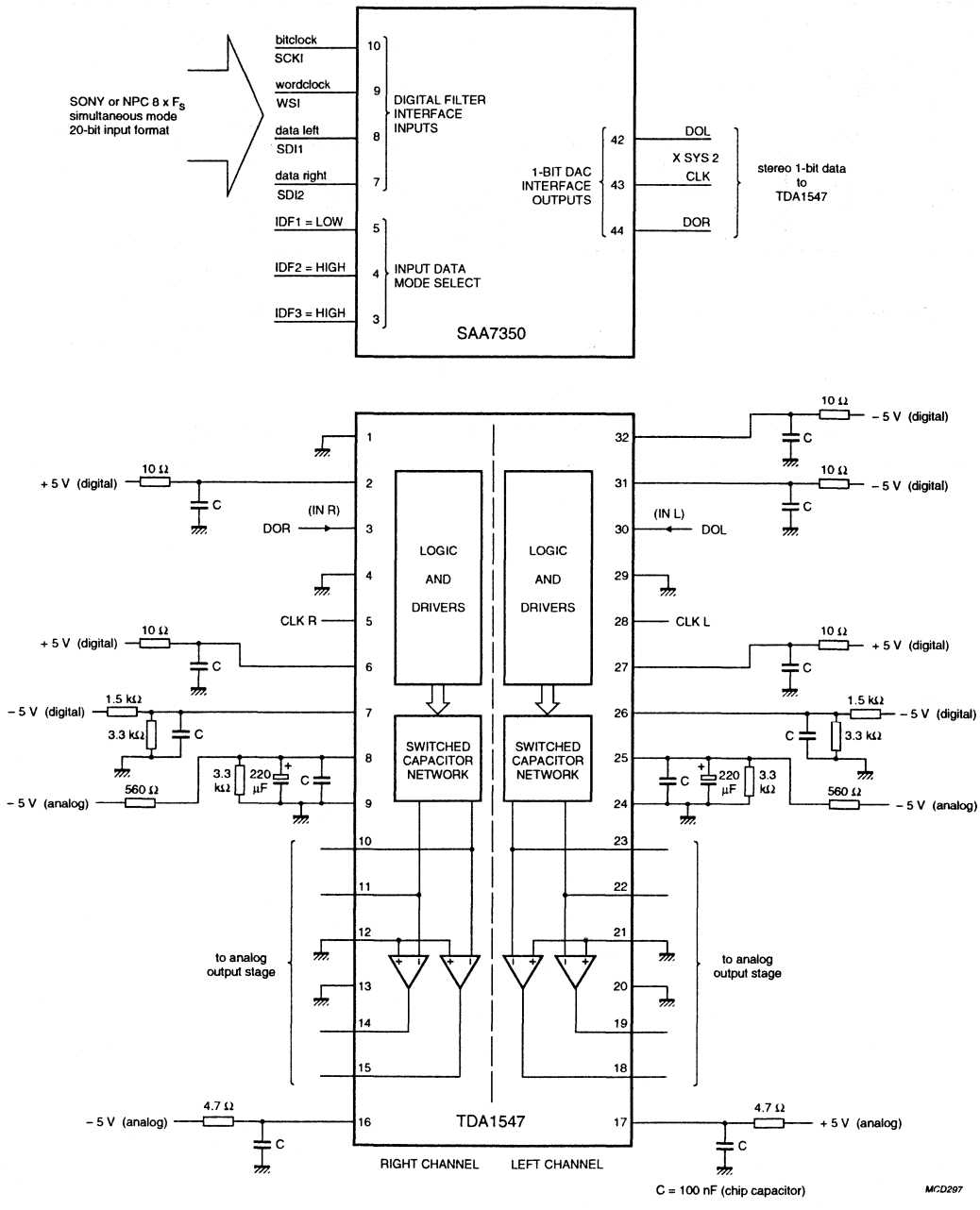


Fig.5 Application diagram.

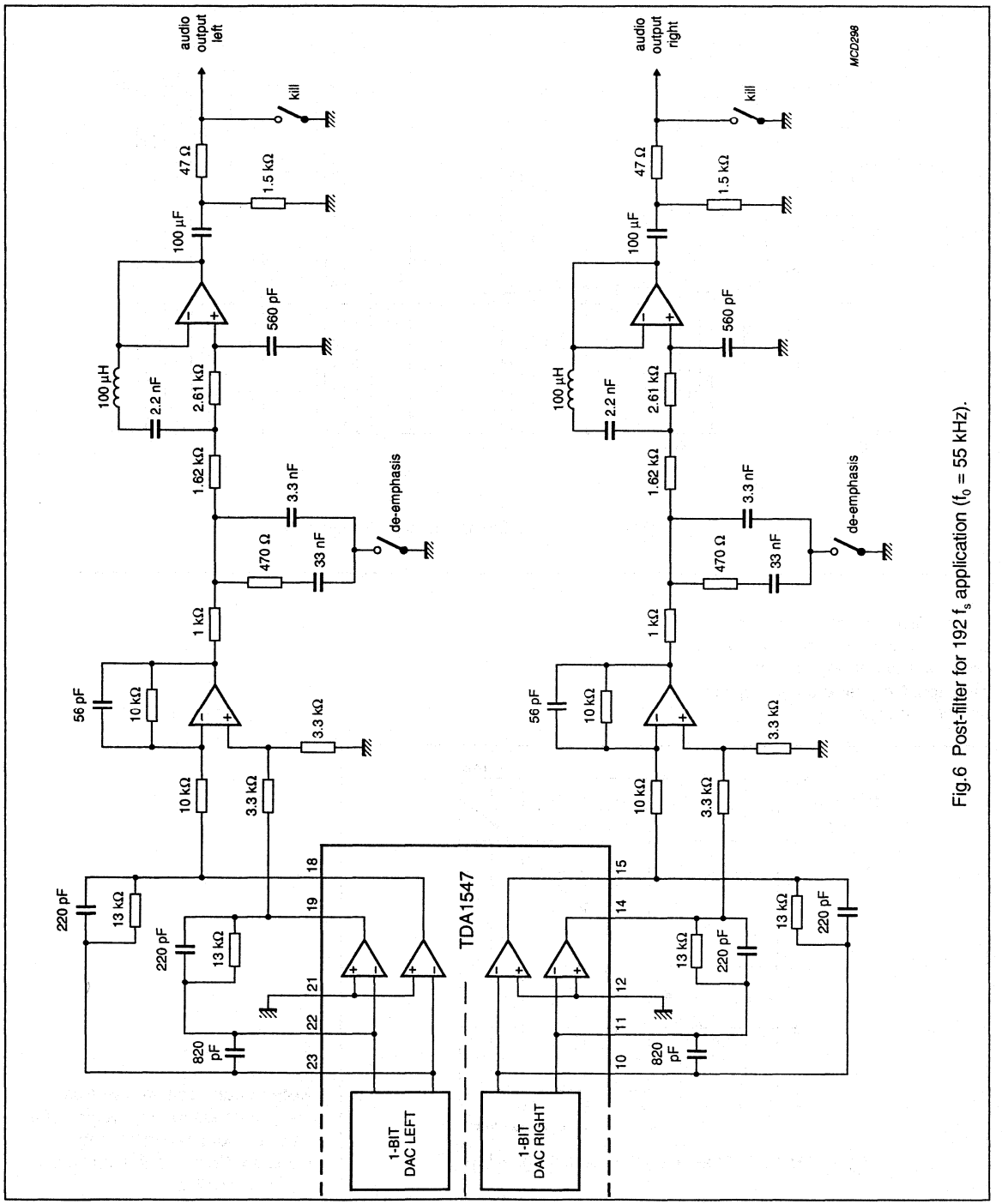


Fig.6 Post-filter for 192 f_s application (f_0 = 55 kHz).

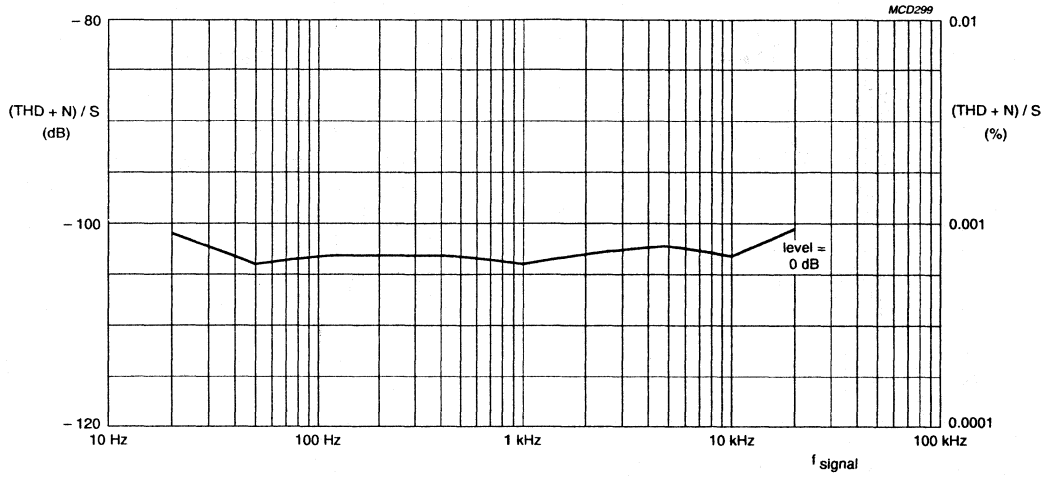


Fig.7 (THD + N)/S as a function of signal frequency.

Note : Graph constructed from average measurements values of a small amount of engineering samples. No guarantee for typical values is implied.

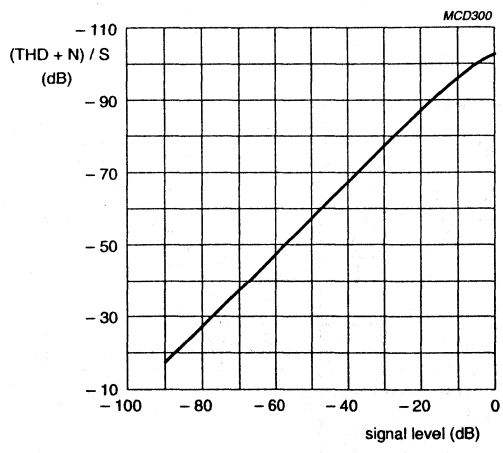


Fig.8 (THD + N)/S as a function of test signal level.

Note : Graph constructed from average measurement values of a small amount of engineering samples. No guarantee for typical values is implied.

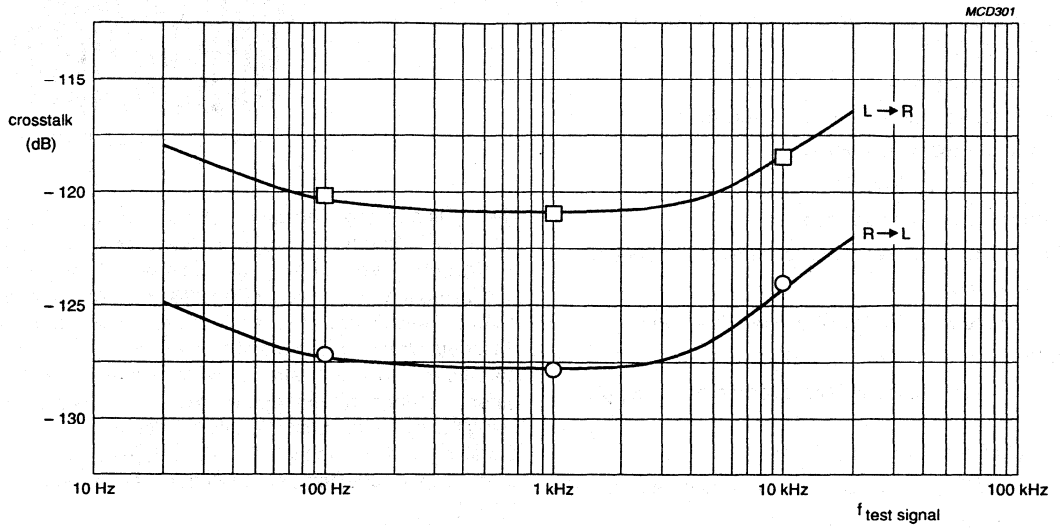


Fig.9 Inter-channel crosstalk as a function of signal frequency.

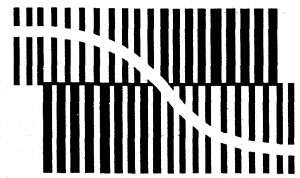
Note : Graph constructed from average measurements values of a small amount of engineering samples. No guarantee for typical values is implied.

Stereo $4f_s$ data input up-sampling filter with bitstream continuous calibration DAC (BCC-DAC1)

TDA1549T

FEATURES

- Easy application
- Finite-duration impulse-response (FIR) filtering and noise shaping incorporated
- 2nd-order noise shaper
- Wide dynamic range (true 18-bit resolution)
- Low total harmonic distortion
- No zero-crossing distortion
- Superior signal-to-noise ratio
- Bitstream continuous calibration conversion concept
- Inherently monotonic
- Voltage output (1.5 V RMS) at line drive level
- Single supply rail (3.8 to 5.5 V)
- Optimum output voltage level over the entire supply range
- Small outline packaging (SO16)
- Wide operating temperature range (–30 to +85 °C)
- Standard Japanese input format
- No analog post-filtering required
- Low power consumption
- Integrated operational amplifiers.



BITSTREAM CONVERSION

GENERAL DESCRIPTION

The TDA1549T (BCC-DAC1) is the first of a new generation of digital-to-analog converters featuring a unique combination of bitstream and continuous calibration concepts.

A system of digital filtering, high oversampling, 2nd order noise shaping and continuous calibration digital-to-analog conversion ensures that only simple 1st order analog filtering is required. The circuit accepts 18-bit four times oversampled input data ($4f_s$) in standard Japanese format. Internal FIR filters remove the main spectral components and increase the sampling rate to 96 times ($96f_s$). A 2nd order noise shaper converts this oversampled data to a 5-bit data stream. For low signal levels the converter operates in the 1-bit bitstream mode with attendant high differential linearity. Higher level signals are reproduced using the dynamic continuous calibration technique, thereby guaranteeing high linearity independent of process variations, temperature effects and product ageing.

High-precision, low-noise amplifiers convert the digital-to-analog current to an output voltage capable of driving a line output. Externally connected capacitors perform the required 1st order filtering so that no further post-filtering is required.

Internal reference circuitry ensures that the output voltage is proportional to the supply voltage, thereby making optimum use of the supply voltage over a wide range (3.8 to 5.5 V). This unique configuration of bitstream and continuous calibration techniques, together with a high degree of analog and digital integration, results in a digital-to-analog conversion system with true 18-bit dynamic range, high linearity and simple low-cost application.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA1549T	SO16	plastic small outline package; 16 leads; body width 7.5 mm	SOT162–1

Stereo $4f_s$ data input up-sampling filter with bitstream continuous calibration DAC (BCC-DAC1)

TDA1549T

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DDD}	digital supply voltage	note 1	3.8	5.0	5.5	V
V_{DDA}	analog supply voltage	note 1	3.8	5.0	5.5	V
V_{DDO}	operational amplifier supply voltage	note 1	3.8	5.0	5.5	V
I_{DDD}	digital supply current	note 2	–	12	18	mA
I_{DDA}	analog supply current	note 2	–	5.5	8	mA
I_{DDO}	operational amplifier supply current	note 2	–	6.5	9	mA
P_{tot}	total power dissipation	note 2	–	120	185	mW
		note 3	–	50	–	mW
$V_{FS(rms)}$	full-scale output voltage (RMS value)	$V_{DDD} = V_{DDA} = V_{DDO} = 5$ V	1.425	1.500	1.575	V
(THD + N)/S	total harmonic distortion plus noise-to-signal ratio	at 0 dB signal level	–	–90	–83	dB
			–	0.003	0.007	%
		at –60 dB signal level	–	–48	–40	dB
			–	0.40	1.0	%
		at –60 dB signal level; A-weighted	–	–50	–	dB
			–	0.38	–	%
S/N	signal-to-noise ratio at bipolar zero	A-weighted; at code 00000H	100	110	–	dB
t_{cs}	current setting time to ±1 LSB		–	0.1	–	µs
BR	input bit rate at data input		–	–	9.216	Mbits
f_{BCK}	input clock frequency		–	–	9.216	MHz
TC_{FS}	full-scale temperature coefficient at analog outputs (VOL and VOR)		–	$\pm 100 \times 10^{-6}$	–	
T_{amb}	operating ambient temperature		–30	–	+85	°C

Notes

1. All V_{DD} and ground pins must be connected externally to the same supply.
2. Measured with V_{DDD}, V_{DDA} and V_{DDO} = 5 V at input data code 00000H.
3. Measured with V_{DDD}, V_{DDA} and V_{DDO} = 3.8 V at input data code 00000H.

Stereo $4f_s$ data input up-sampling filter with bitstream continuous calibration DAC (BCC-DAC1) TDA1549T

BLOCK DIAGRAM

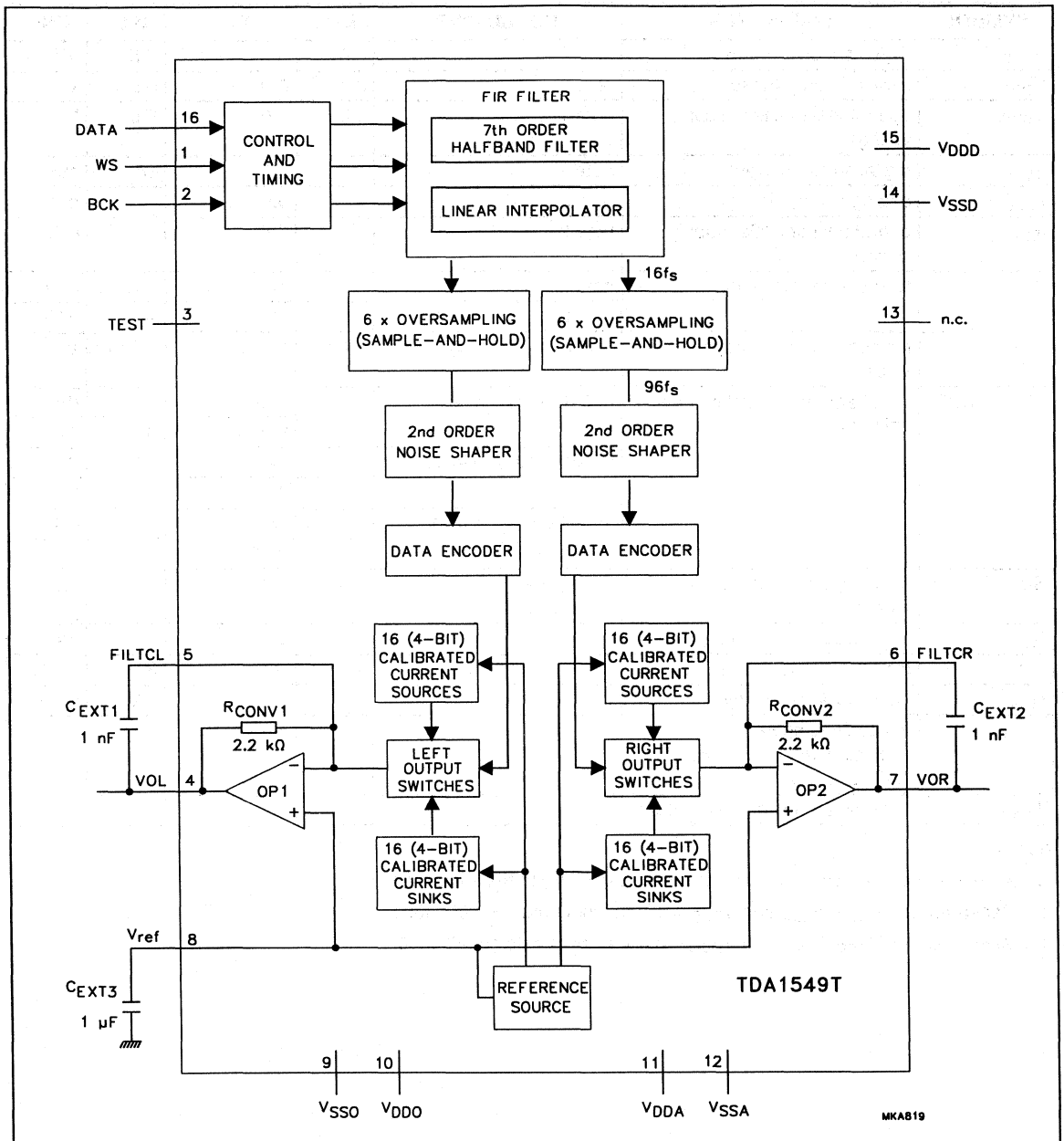


Fig.1 Block diagram.

Stereo $4f_s$ data input up-sampling filter with bitstream continuous calibration DAC (BCC-DAC1)

TDA1549T

PINNING

SYMBOL	PIN	DESCRIPTION
WS	1	word select input
BCK	2	bit clock input
TEST	3	test input; pin should be connected to ground
VOL	4	left channel output
FILTCL	5	capacitor for left channel 1st order filter function; should be connected between pins 4 and 5
FILTCR	6	capacitor for right channel 1st order filter function; should be connected between pins 6 and 7
VOR	7	right channel output
V_{ref}	8	internal reference voltage for output channels ($\frac{1}{2}V_{DD}$)
V_{SSO}	9	operational amplifier ground
V_{DDO}	10	operational amplifier supply voltage
V_{DDA}	11	analog supply voltage
V_{SSA}	12	analog ground
n.c.	13	not connected (this pin should be left open-circuit)
V_{SSD}	14	digital ground
V_{DDD}	15	digital supply voltage
DATA	16	data input

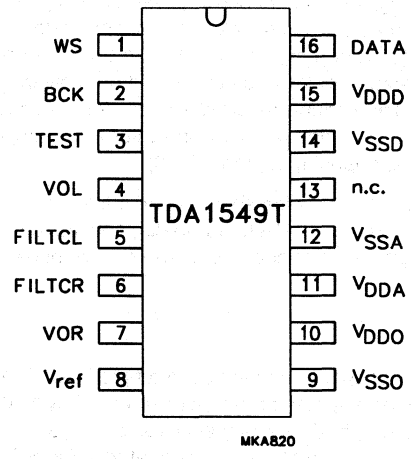


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

General

The TDA1549T CMOS digital-to-analog bitstream continuous calibration converter incorporates internal digital filtering which increases the oversampling rate of $4f_s$ input data to $96f_s$, and removes the spectral data components around $4f_s$, $8f_s$, and $12f_s$. A 2nd order noise shaper operating at $96f_s$ outputs a 5-bit data bitstream to the DACs. The filtering required for waveform smoothing and out-of-band noise reduction is achieved by simple 1st order analog post-filtering (see Fig.3).

The combination of noise shaping and bitstream continuous calibration digital-to-analog conversion enables high performance and extremely low noise to be achieved.

Input

The circuit accepts four times oversampled data in 18-bit two's complement standard Japanese format with MSB first. Left and right data channel words are time multiplexed. The input format is illustrated in Fig.5. The bit clock (BCK) operates at $192f_s$, i.e. 48 times the word select (WS) frequency of $4f_s$.

Oversampling filter

The oversampling filter consists of:

- A 7th order half-band low-pass FIR filter which increases the oversampling rate from 4 times to 8 times. This removes the spectral components around $4f_s$ and $12f_s$ (see Fig.3).
- A linear interpolation section which increases the oversampling rate to 16 times. This removes the spectral components around $8f_s$.
- A sample-and-hold section which provides another 6 times oversampling to 96 times.

The zero-order hold characteristic of this sample-and-hold section plus the 1st order analog filtering removes the spectral components around $16f_s$.

Passband ripple is within 0.1 dB. Stopband attenuation is >50 dB around multiples of the sampling frequency.

Noise Shaper

The 2nd-order digital noise shaper converts the 18-bit data at $96f_s$ into a 5-bit bitstream, while shifting in-band quantization noise to frequencies well above the audio band. For low signal levels the noise shaper output is a 1-bit bitstream. This noise shaping technique used in combination with a special data code and bitstream DAC enables extremely high signal-to-noise ratios to be achieved.

Data encoder

The data encoder converts the 5-bit two's complement output data from the noise shaper to a 32-bit thermometer code.

In traditional unidirectional current converters, half of the full-scale current flows to the output during small signal reproduction. The thermal noise and substrate crosstalk components present in this current severely restrict the dynamic range which can be attained. In this BCC-DAC1 true low-noise performance is achieved using a special data code and bidirectional current sources. The special data code guarantees that only small values of current flow to the output during small-signal passages while larger positive or negative signals are generated using the bidirectional current sources. For every change in the 18-bit input sample only one current source or current sink is switched on. This intrinsically monotonic thermometer code ensures the high differential linearity, zero crossover distortion and superior signal-to-noise ratio associated with bitstream conversion.

Continuous calibration DAC

The stereo 5-bit DAC uses the dynamic continuous calibration technique. The DAC currents (16 sources and 16 sinks) of each channel are repeatedly generated from one single reference current. This duplication is based on an internal charge storage principle and has an inherently high accuracy which is insensitive to ageing, temperature and process variations.

Figure 4 shows one such current calibration source. During calibration the cell is connected to the reference current sink I_{ref} via switch S2. The calibration transistor M1 is connected as an MOS diode via the switch S1 forcing its gate potential to assume a value so that the total current of the calibration cell is equal to the reference current. After calibration the gate of M1 is allowed to float. The gate capacitance C_{gs} retains its potential and the current through the cell remains exactly equal to the reference current. This current is now connected to the output. Each digital-to-analog current source and each current sink is calibrated precisely in this way.

Operational amplifiers

High precision, low-noise amplifiers together with the internal conversion resistors R_{CONV1} and R_{CONV2} convert the DAC output current to a voltage capable of driving a line output. This voltage is available at VOL and VOR (1.5 V RMS typical).

Connecting external capacitors C_{EXT1} and C_{EXT2} between FILTCL and VOL and FILTCR and VOR respectively, provides the required 1st-order post-filtering for the left and right channels (see Fig.1). The combinations of R_{CONV1} with C_{EXT1} and R_{CONV2} with C_{EXT2} determine the 1st order fall-off frequencies.

Internal reference circuitry

Internal reference circuitry ensures that the output voltage signal is proportional to the supply voltage, thereby maintaining maximum dynamic range for supply voltages from 3.8 to 5.5 V and making the circuit also suitable for battery-powered applications.

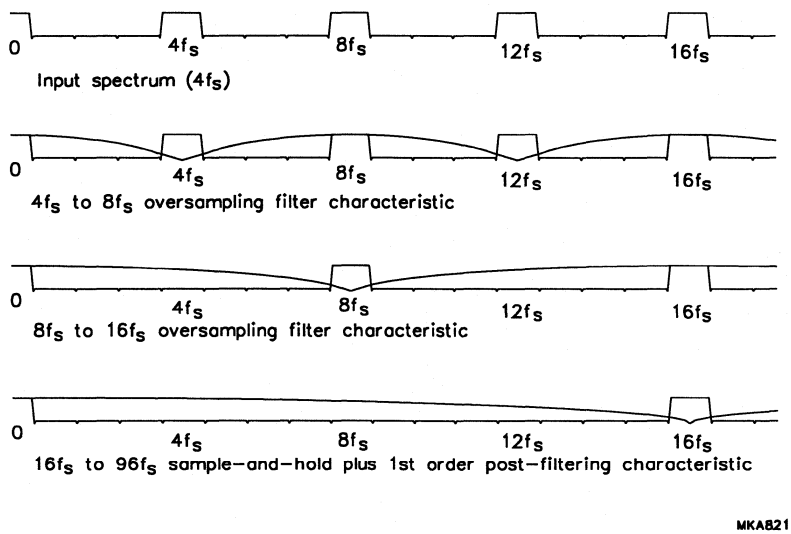
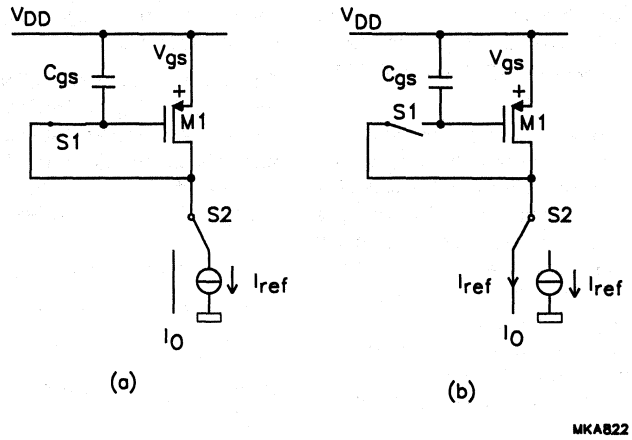


Fig.3 Filter and noise shaper characteristics.



(a) calibration.
(b) operation.

Fig.4 Calibration principle.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DDD}	digital supply voltage		–	7.0	V
V_{DDA}	analog supply voltage		–	7.0	V
V_{DDO}	operational amplifier supply voltage		–	7.0	V
T_{xtal}	maximum crystal temperature		–	+150	°C
T_{stg}	storage temperature		–65	+150	°C
T_{amb}	operating ambient temperature		–30	+85	°C
V_{es}	electrostatic handling	note 1	–2000	+2000	V
		note 2	–200	+200	V

Notes

1. Human body model: C = 100 pF; R = 1500 Ω.
2. Machine model: C = 200 pF; L = 0.5 μH; R = 10 Ω.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air	110	K/W

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices.

QUALITY SPECIFICATION

Quality specification in accordance with "*SNW-FQ-611*" is applicable.

CHARACTERISTICS

$V_{DDD} = V_{DDA} = V_{DDO} = 5$ V; $T_{amb} = 25$ °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DDD}	digital supply voltage	note 1	3.8	5.0	5.5	V
V_{DDA}	analog supply voltage	note 1	3.8	5.0	5.5	V
V_{DDO}	operational amplifier supply voltage	note 1	3.8	5.0	5.5	V
I_{DDD}	digital supply current	note 2	–	12	18	mA
I_{DDA}	analog supply current	note 2	–	5.5	8	mA
I_{DDO}	operational amplifier supply current	note 2	–	6.5	9	mA
P_{tot}	total power dissipation	note 2	–	120	185	mW
		note 3	–	50	–	mW
RR	ripple rejection	note 4	–	25	–	dB
Digital inputs; pins WS, BCK and DATA						
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	–	$V_{DD} + 0.5$	V
V_{IL}	LOW level input voltage		–0.5	–	$0.3V_{DD}$	V
$\|I_{LIH}\|$	HIGH level input leakage current	$V_{IH} = V_{DDD} = 5$ V	–	–	10	µA
$\|I_{LIL}\|$	LOW level input leakage current	$V_{IH} = V_{SSD} = 0$ V	–	–	10	µA
C_I	input capacitance		–	–	10	pF
Timing (see Fig.6)						
OPERATING FREQUENCY						
f_{BCK}	bit clock frequency		–	$192f_s$	–	Hz
f_{WS}	word select frequency		–	$f_{BCK}/48$	–	Hz
INPUT FREQUENCY						
f_{BCK}	clock frequency		–	–	9.216	MHz
BR	bit rate data input		–	–	9.216	MHz
f_{WS}	word select input frequency		–	–	192	kHz
t_r	rise time		–	–	32	ns
t_f	fall time		–	–	32	ns
T_{cy}	bit clock cycle time		108	–	–	ns
t_H	bit clock HIGH time		22	–	–	ns
t_L	bit clock LOW time		22	–	–	ns
t_{su}	data set-up time		32	–	–	ns
t_h	data hold time		2	–	–	ns
t_{hWS}	word select hold time		2	–	–	ns
t_{suWS}	word select set-up time		32	–	–	ns
Filter characteristics (see Fig.3)						
PBR	pass-band ripple	< 20 kHz	–	0.1	–	dB
SBA	stop-band attenuation	note 5	50	–	–	dB

Stereo $4f_s$ data input up-sampling filter with bitstream continuous calibration DAC (BCC-DAC1)

TDA1549T

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Reference values						
V_{ref}	reference voltage level		2.45	2.5	2.55	V
R_{CONV}	current-to-voltage conversion resistance		1.6	2.2	2.8	kΩ
Analog outputs; pins VOL and VOR						
RES	resolution		–	–	18	bit
$V_{FS(rms)}$	full-scale output voltage (RMS value)		1.425	1.5	1.575	V
V_{OFF}	output voltage DC offset with respect to reference voltage level V_{ref}		–80	–65	–50	mV
TC_{FS}	full-scale temperature coefficient		–	$\pm 100 \times 10^{-6}$	–	
(THD + N)/S	total harmonic distortion plus noise-to-signal ratio	at 0 dB input level; note 6	–	–90	–83	dB
			–	0.003	0.007	%
		at –60 dB input level; note 7	–	–48	–40	dB
			–	0.40	1.0	%
		at –60 dB input level; A-weighted; note 8	–	–50	–	dB
			–	0.32	–	%
		at 0 dB input level; 20 Hz to 20 kHz; note 9	–	–90	–83	dB
			–	0.003	0.007	%
S/N	signal-to-noise ratio at bipolar zero	A-weighted; at code 00000H	100	110	–	dB
t_{cs}	current setting time to ±1 LSB		–	0.1	–	ms
α_{cs}	channel separation		85	100	–	dB
$\lvert\Delta V_O\rvert$	unbalance between outputs		–	0.2	0.3	dB
$\lvert Z_O\rvert$	dynamic output impedance		–	10	–	W
R_L	output load resistance		3	–	–	kΩ
C_L	output load capacitance		–	–	200	pF

Notes

1. All V_{DD} and V_{SS} pins must be connected externally to the same supply.
2. Measured with $V_{DDD} = V_{DDA} = V_{DDO} = 5$ V at input data code 00000H.
3. Measured with $V_{DDD} = V_{DDA} = V_{DDO} = 3.8$ V at input data code 00000H.
4. V_{ripple} = 1% of the supply voltage and f_{ripple} = 100 Hz. Ripple rejection RR to V_{DDA} is dependent on the value of the external capacitor (C_{EXT3} in Fig.1) connected to V_{ref}. The value quoted here assumes C_{EXT3} = 1 µF.
5. Around multiples of $4f_s$.
6. Measured with a 1 kHz, 0 dB, 18-bit sine wave generated at a sampling rate of 192 kHz. (THD + N)/S measured over a bandwidth from 20 Hz to 20 kHz.
7. Measured with a 1 kHz, –60 dB, 18-bit sine wave generated at a sampling rate of 192 kHz. (THD + N)/S measured over a bandwidth from 20 Hz to 20 kHz.
8. Measured with a 1 kHz, –60 dB, 18-bit sine wave generated at a sampling rate of 192 kHz. (THD + N)/S measured over a bandwidth from 20 Hz to 20 kHz and filtered with A-weighted characteristic.
9. Measured with a 0 dB, 18-bit sine wave from 20 Hz to 20 kHz generated at a sampling rate of 192 kHz. (THD + N)/S measured over a bandwidth from 20 Hz to 20 kHz.

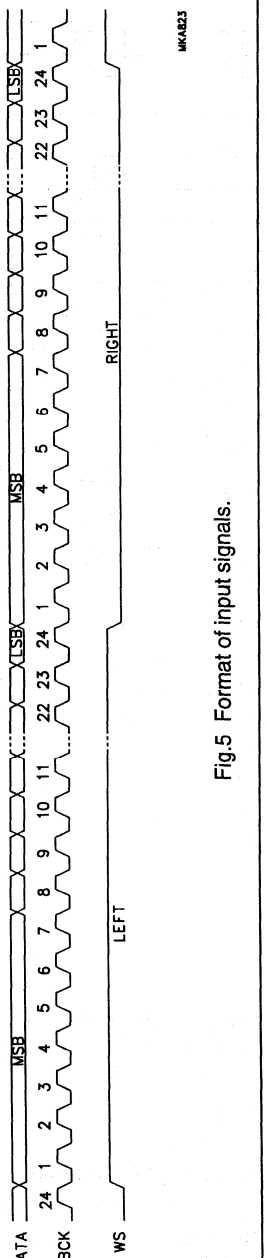


Fig.5 Format of input signals.

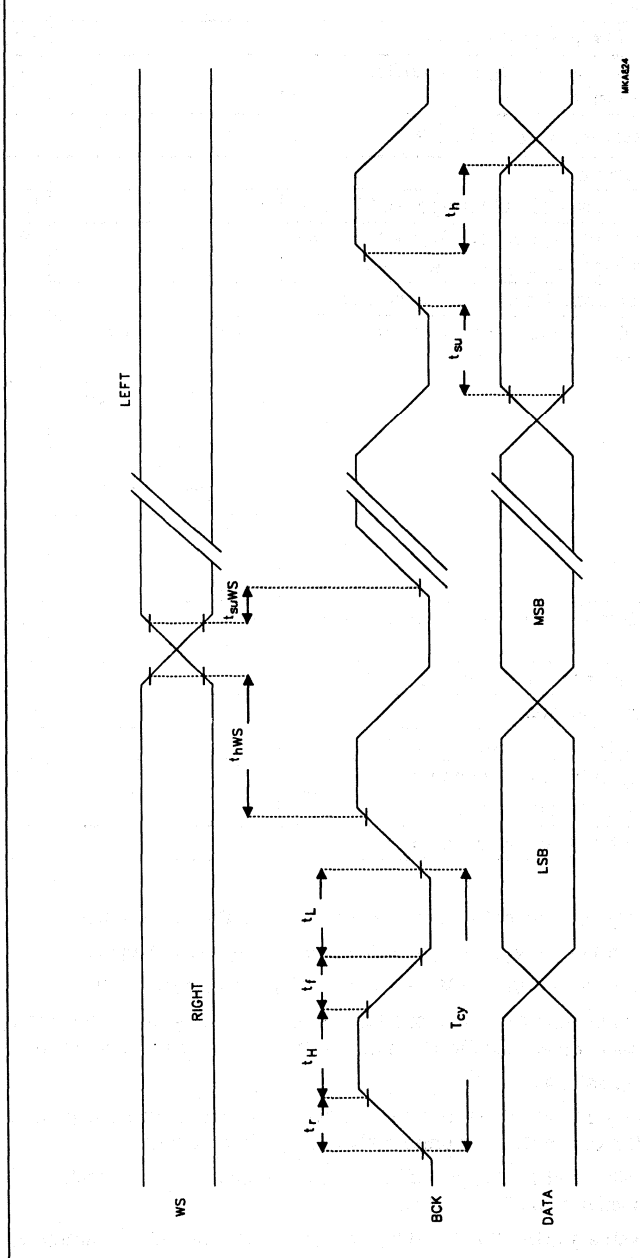
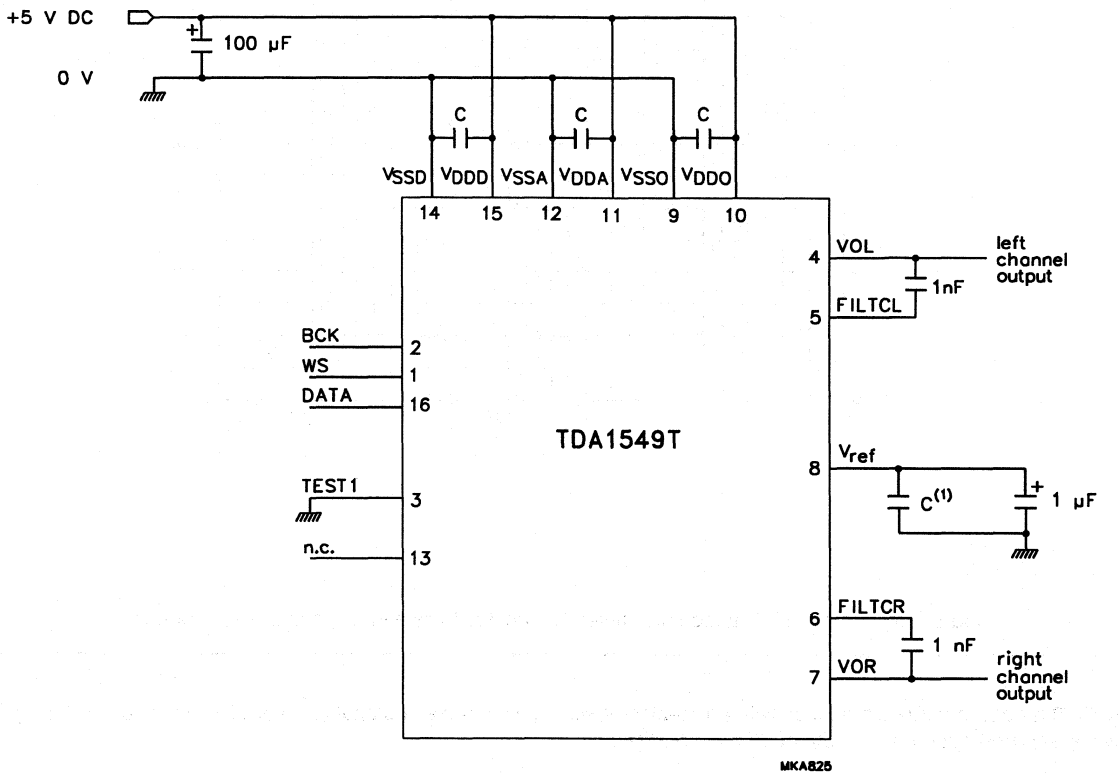


Fig.6 Timing of input signals.

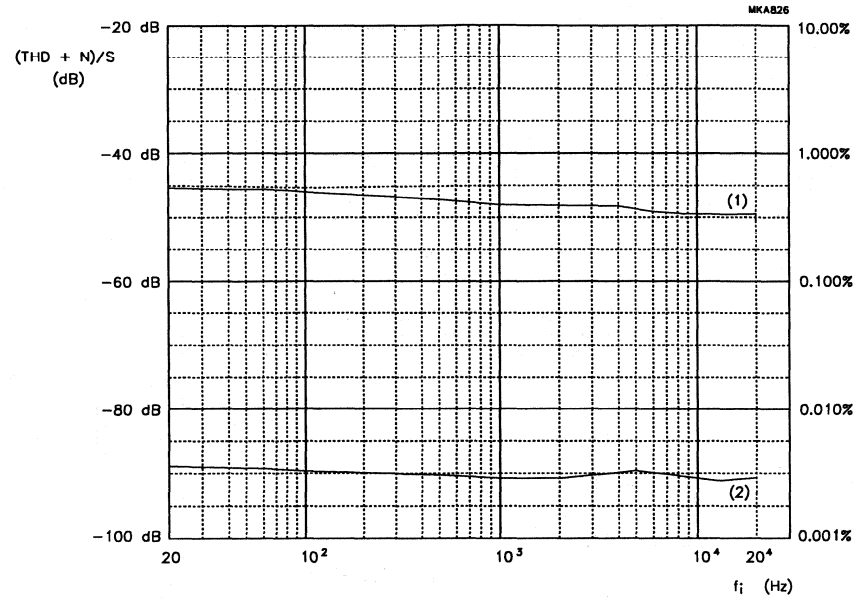
APPLICATION INFORMATION

A typical application diagram is illustrated in Fig.7. The left and right channel outputs can drive a line output directly.



(1) C = 100 nF (chip capacitor).

Fig.7 Application diagram.



(1) Level = −60 dB.
(2) Level = 0 dB.

Fig.8 Total harmonic distortion plus noise-to-signal ratio as a function of signal frequency.

In Fig.8 measurements were taken with an 18-bit sine wave generated at a sample rate of 192 kHz. The (THD + N)/S was measured over a bandwidth of 20 Hz to 20 kHz.

The graph was constructed from average measurement values of a small amount of engineering samples. No guarantee for typical values is implied.

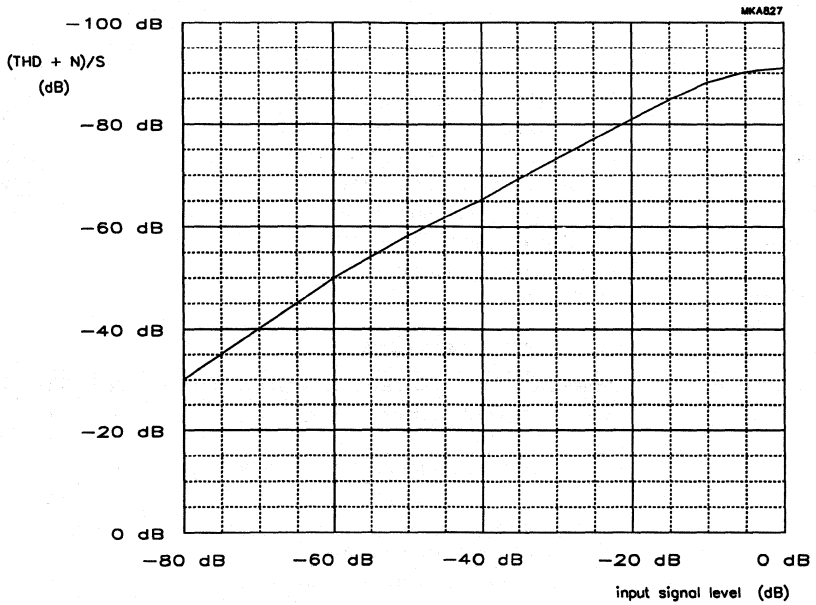


Fig.9 Total harmonic distortion plus noise-to-signal ratio as a function of signal level; (A-weighted).

In Fig.9 measurements were taken with an 18-bit sine wave generated at a sample rate of 192 kHz. The (THD + N)/S was measured over a bandwidth of 20 Hz to 20 kHz and filtered with A-weighted characteristic.

The graph was constructed from average measurement values of a small amount of engineering samples. No guarantee for typical values is implied.

Philips Semiconductors

Data sheet	
status	Preliminary specification
date of issue	July 1994

TDA1551Q

2 x 22 W BTL car radio power amplifier with diagnostic facility

FEATURES

- Requires very few external components
- Flexible in use – quad, single ended or stereo BTL
- I²C-bus control
- Dynamic distortion detector
- Thermal protection
- Output status information
- Power supply dip detection
- High output power
- MUTE/sleep mode by writing to I²C-bus
- Stand-by mode
- Fixed gain
- Good ripple rejection
- Load dump protection
- AC/DC short circuit safe to ground and V_P
- Reverse polarity safe
- Low offset voltage at output
- Capable of handling high energy at outputs (V_P = 0 V)
- Electrostatic discharge protection
- No switch-ON/switch-OFF plop
- Flexible leads
- Low thermal resistance
- Identical inputs (inverting and non-inverting).

DESCRIPTION

The TDA1551Q is an integrated class-B output amplifier encased in a 17-lead single-in-line plastic power package. The device contains 4 x 11 W single-ended (SE) or 2 x 22 W BTL amplifiers and is intended for use in car radio applications.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage range	operating	6	14.4	18	V
V_P	supply voltage	non-operating	-	-	30	V
I_P	total quiescent current		-	80	160	mA
Quad single-ended application						
P_o	output power	R_L = 4 Ω; THD = 10 %	-	6	-	W
		R_L = 2 Ω; THD = 10 %	-	11	-	W
V_{no}	output voltage noise	R_S = 0 Ω	-	50	-	μV
Stereo BTL application						
P_o	output power	R_L = 4 Ω; THD = 10 %	-	22	-	W
V_{no}	output voltage noise	R_S = 0 Ω	-	70	-	μV
ΔV_o	DC output offset voltage		-	-	100	mV

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA1551Q	17	SIL bent to DIL	plastic	SOT243R

2 x 22 W BTL car radio power amplifier with diagnostic facility

TDA1551Q

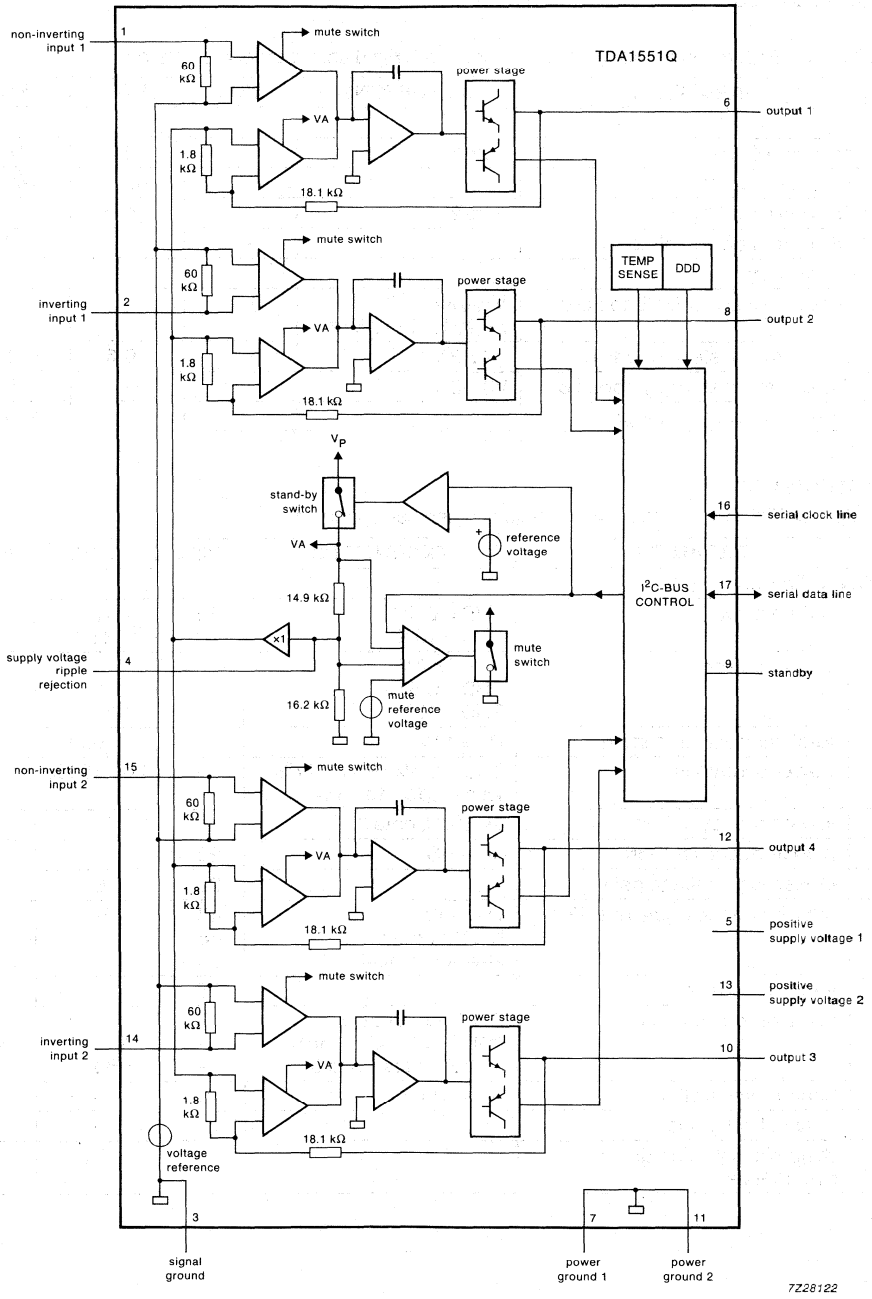


Fig.1 Block diagram.

DC CHARACTERISTICS

V_P = 14.4 V; T_{amb} = 25°C; measurements in accordance with Fig.6 unless otherwise stated.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_P	supply voltage	note 1	6	14.4	18	V
I_P	quiescent current		–	80	160	mA
V_O	DC output voltage	note 2	–	6.9	–	V
$\lvert\Delta V_o\rvert$	DC output offset voltage		–	–	100	mV
MUTE/sleep/standby						
V_O	output signal in MUTE position	$V_{I(max)}$ = 1 V; f = 20 Hz to 10 kHz	–	–	2	mV
I_P	DC current in sleep condition	V9 > 3 V	–	0.6	1	mA
I_P	DC current in standby condition	V9 < 2 V	–	–	0.1	mA
$\lvert\Delta V_o\rvert$	DC output offset voltage		–	–	100	mV

AC CHARACTERISTICS

V_P = 14.4 V; T_{amb} = 25°C; f = 1 kHz; R_L = 4 Ω; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Stereo BTL application (Fig.7)						
P_O	output power	THD = 0.5% THD = 10%	15 20	17 22	- -	W W
P_O	output power	V_P = 13.2 V THD = 0.5% THD = 10%	 - -	 12 17	 - -	 W W
THD	total harmonic distortion	P_O = 1 W	-	0.05	-	%
B	power bandwidth	THD = 0.5%; P_O = –1 dB with respect to 15 W	-	20 - 15000	-	Hz
f_{LOW}	low frequency roll-off	at –3 dB; note 3	-	25	-	Hz
f_{HIGH}	high frequency roll-off	at –1 dB	20	-	-	kHz
G_v	closed loop voltage gain		25	26	27	dB
V_{PRR}	supply voltage ripple rejection	ON; note 4 MUTE; note 4 standby; note 4	48 48 80	- - -	- - -	dB dB dB
$\lvert Z_i\rvert$	input impedance		25	30	38	kΩ
V_{no}	noise output voltage	ON; R_S = 0; note 5 ON; R_S = 10 kΩ; note 5 MUTE; notes 5 and 6	- - -	70 100 60	- 200 -	µV µV µV
α	channel separation	R_S = 10 kΩ	40	-	-	dB
$\lvert\Delta G_v\rvert$	channel unbalance		-	-	1	dB
	dynamic distortion detector switch level		-	3.5	-	%

FUNCTIONAL DESCRIPTION

The TDA1551Q contains four identical amplifiers with differential input stages (two inverting and two non-inverting) which can be used in SE or BTL applications. The gain of each amplifier is fixed at 20 dB for SE and 26 dB for BTL. The device also contains an I²C-bus facility which operates in the read or write mode.

In the **write** mode the device can be switched to either the sleep condition (low sleep current of 0.6 mA typ.), the MUTE condition or the ON condition.

In the **read** mode an 8-bit status word is available. Data bits D0 to D3 contain status information of each of the 4 outputs. If the device is switched to the ON or MUTE condition and there is a short-circuit at one or more outputs, the power transistors will be outside their safe operating area consequently one or more bits of D0 to D3 will be HIGH. Bits D0 to D3 are LOW when in the normal safe operating area. Bit D4 is normally LOW, if one or more channels reaches the clipping level D4 will go HIGH. Bit D5 is normally LOW, if the crystal temperature reaches 150 °C D5 will go HIGH. After a power-on reset bit 7 will go HIGH and a dip in the power supply will be noticed. Bit 7 will go LOW after the I²C-bus is read. When pin 9 is LOW the device will switch OFF and the supply current will be reduced to 0.1 mA (max.).

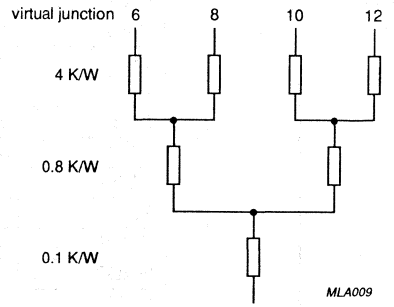


Fig.3 Thermal equivalent resistance network.

2 x 22 W BTL car radio power amplifier with diagnostic facility

TDA1551Q

PIN CONFIGURATION

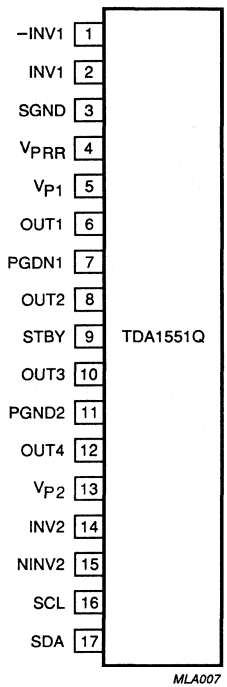


Fig.2 Pin configuration.

PINNING

SYMBOL	PIN	DESCRIPTION
−INV1	1	non-inverting input 1
INV1	2	inverting input 1
GND	3	signal ground
V_{PRR}	4	supply voltage ripple rejection
V_{p1}	5	positive supply voltage 1
OUT1	6	output 1
GND1	7	power ground 1
OUT2	8	output 2
SB	9	standby
OUT3	10	output 3
GND2	11	power ground 2
OUT4	12	output 4
V_{p2}	13	positive supply voltage 2
INV2	14	inverting input 2
−INV2	15	non-inverting input 2
SCL	16	serial clock line
SDA	17	serial data line

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC134)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
Supply voltage				
V_P	operating voltage	–	18	V
V_P	non-operating voltage	–	30	V
	load dump protect	–	45	V
IOSM	non-repetitive peak output current	–	6	A
IORM	repetitive peak output current	–	4	A
T_{stg}	storage temperature range	−55	150	°C
T_c	crystal temperature	–	150	°C
V_{Psc}	AC/DC short-circuit safe voltage	–	18	V
	energy handling capability at outputs (V_P = 0)	–	200	mJ
V_{Pr}	reverse polarity	–	6	V
P_{tot}	total power dissipation	–	60	W

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}c}$	from junction to case (Fig.3)	1.5 K/W
$R_{th\ j\text{-}a}$	from junction to ambient in free air	40 K/W

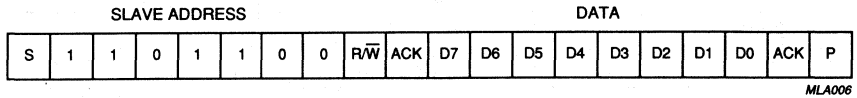
AC CHARACTERISTICS (continued)

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Quad single-ended application (Fig.6)						
P_O	output power	THD = 0.5%; note 7 THD = 10%; note 7	4 5.5	5 6	- -	W W
P_O	output power	R_L = 2 Ω THD = 0.5%; note 7 THD = 10%; note 7	 7.5 10	 8.5 11	 - -	 W W
THD	total harmonic distortion	P_O = 1 W	-	0.05	-	%
f_{LOW}	low frequency roll-off	at −3 dB; note 3	-	25	-	Hz
f_{HIGH}	high frequency roll-off	at −1 dB	20	-	-	kHz
G_v	closed loop voltage gain		19	20	21	dB
V_{PRR}	supply voltage ripple rejection	ON; note 4 MUTE; note 4 stand-by; note 4	48 48 80	- - -	- - -	dB dB dB
$\|Z_i\|$	input impedance		50	60	75	kΩ
V_{no}	noise output voltage	ON; R_S = 0; note 5 ON; R_S = 10 kΩ; note 5 MUTE; notes 5 and 6	- - -	50 70 60	- 100 -	μV μV μV
α	channel separation	R_S = 10 kΩ	40	-	-	dB
$\|\Delta G_v\|$	channel unbalance		-	-	1	dB
	dynamic distortion detector switch level		-	3.5	-	%
I²C-bus (see I²C-bus protocol)						
V_{IH}	input voltage HIGH		3	-	5.5	V
V_{IL}	input voltage LOW		− 0.3	-	1.5	V
I_{IH}	input current HIGH	V = 5.5 V	−10	-	10	μA
I_{IL}	input current LOW	V = GND	−10	-	10	μA
V_{OL}	output voltage LOW	I_L = 3 mA	-	-	0.4	V
Power-on reset (increasing supply voltage)						
V_P	start of reset end of reset		0.5 -	- -	- 5	V V
Standby (pin 9)						
V_9	input voltage HIGH input voltage LOW		3 -	- -	V_P 2	V V

Notes to the characteristics

1. The circuit is DC adjusted at V_P = 6 V and AC operating at V_P = 8 to 18 V.
2. At 18 V < V_P < 30 V the DC output voltage < V_P/2.
3. Frequency response externally fixed.
4. Ripple rejection measured at the output with a source impedance of 0 Ω and at a frequency of 100 Hz to 10 kHz (amplitude = 2 V(p-p)).
5. Noise voltage measured in a bandwidth of 20 Hz to 20 kHz.
6. Noise output voltage independent of R_S (V_I = 0 V).
7. Output power is measured directly at the output pins of the IC.

I²C-bus protocol



S start condition
R/$\overline{W}$ read/write bit; LOW = write, HIGH = read
ACK acknowledge, generated by the receiving device
DATA see Tables 1 and 2
P stop condition

Fig.4 I²C-bus protocol.

Table 1: WRITE definition (R/$\overline{W}$ = LOW)

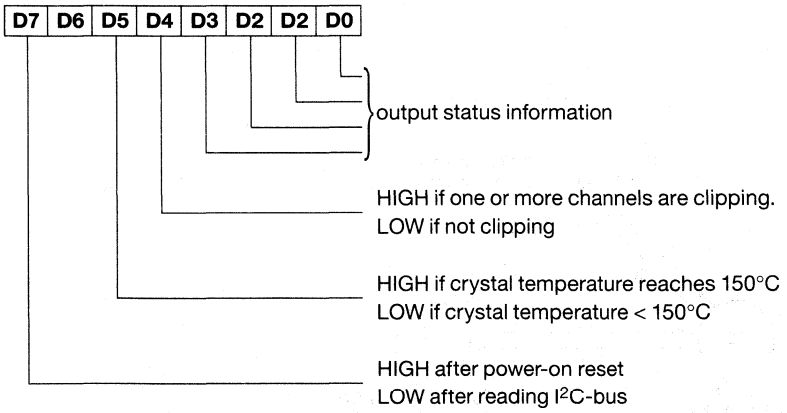
MSB			DATA				LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
0	0	0	0	0	0	0	0	SLEEP condition
0	0	0	0	0	0	0	1	MUTE condition
0	0	0	0	0	0	1	0	not allowed (1)
0	0	0	0	0	0	1	1	ON condition (2)

Bit D0 switches from SLEEP to the ON condition
Bit D1 switches the MUTE condition

(1) For test purposes only; I²C-bus is in the ON condition, amplifier is in the stand-by condition.

(2) To get into the ON condition without switch-on plops, the device should be switched from the SLEEP condition to the MUTE condition and then, after a period of 150 ms, to the ON condition.

Table 2: READ definition (R/$\overline{W}$ = HIGH)



If the device is sinewave driven bit D4 will be HIGH if the THD in one or more channels exceeds 3.5%.

Table 3: Fault conditions

DATA MSB				
D3	**D2**	**D1**	**D0**	**FUNCTION**
0	0	0	0	all output power transistors in the normal safe operating condition
-	-	-	1	fault condition pin 6
-	-	1	-	fault condition pin 8
-	1	-	-	fault condition pin 10
1	-	-	-	fault condition pin 12

If more outputs are in a fault condition (e.g. short-circuit) then more bits, D3 to D0, will be HIGH.

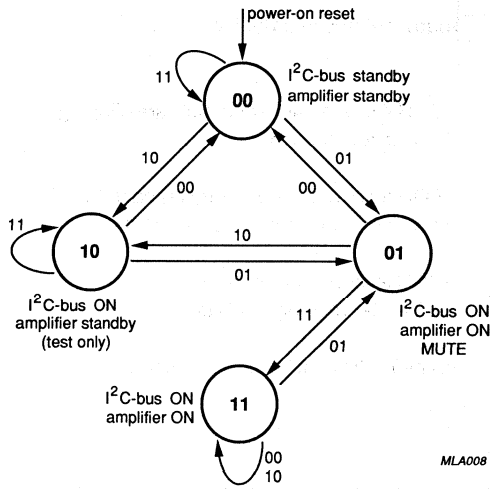


Fig.5 State diagram.

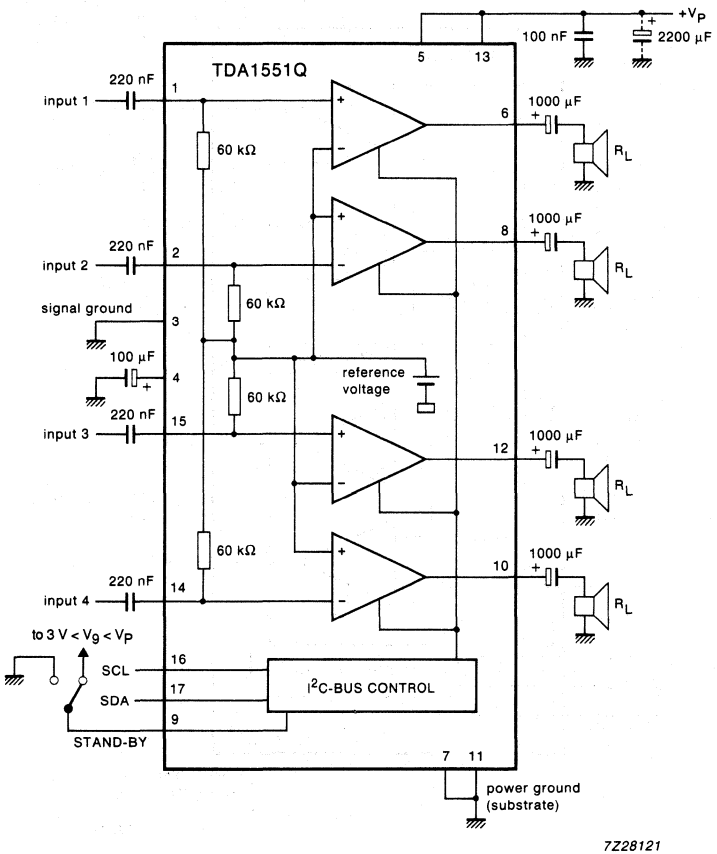


Fig.6 Test circuit quad single-ended.

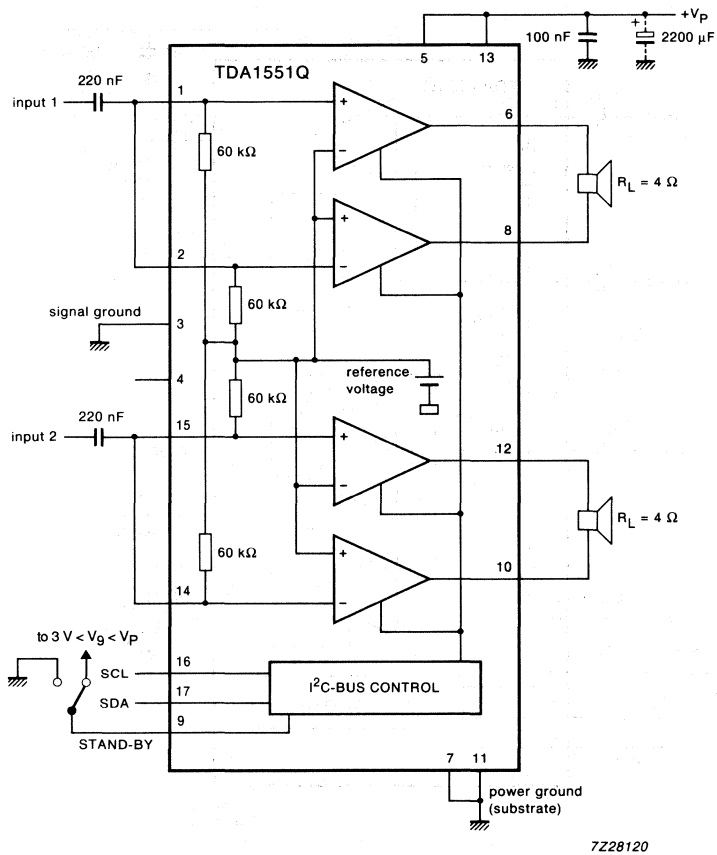


Fig.7 Test circuit stereo BTL.

QUALITY SPECIFICATION

Electrostatic handling.

SYMBOL	PINS	MIN.	MAX.	UNIT
Human body model; R_s = 1500 Ω; C = 100 pF				
V_{es}	1, 2, 14, 15, 16, and 17	−1.5	+1.5	kV
	other	−2	+2	kV
Machine model; R_s = 0 Ω; C = 200 pF				
V_{es}	1, 2, 14, 15, 16, and 17	−100	+100	V
	other	−200	+200	V

2 X 22 W BTL STEREO CAR RADIO POWER AMPLIFIER

GENERAL DESCRIPTION

The TDA1552Q is an integrated class-B output amplifier in a 13-lead single-in-line (SIL) plastic power package. The circuit contains 2 x 22 W amplifiers in Bridge Tied Load (BTL) configuration. The device is primarily developed for car radio applications.

Features

- Requires very few external components
- High output power
- Low offset voltage at outputs
- Fixed gain
- Good ripple rejection
- Mute/stand-by switch
- Load dump protection
- AC and DC short-circuit-safe to ground and V_P
- Thermally protected
- Reverse polarity safe
- Capability to handle high energy on outputs (V_P = 0 V)
- Protected against electrostatic discharge
- No switch on/switch off plop
- Low thermal resistance
- Flexible leads

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage range						
operating		V_P	6.0	14.4	18.0	V
non-operating		V_P	–	–	30	V
load dump protected		V_P	–	–	45	V
Repetitive peak output current		I_{ORM}	–	–	4	A
Total quiescent current		I_{tot}	–	80	160	mA
Stand-by current		I_{sb}	–	0.1	100	μA
Switch-on current		I_{sw}	–	–	60	μA
Input impedance		$\|Z_I\|$	50	60	75	kΩ
Junction temperature		T_j	–	–	150	°C
Stereo application						
Output power	R_L = 4 Ω; THD = 10%	P_o	20	22	–	W
Supply voltage ripple rejection	R_S = 0 Ω; f = 100 Hz to 10 kHz	RR	48	–	–	dB
DC output offset voltage		$\|\Delta V_O\|$	–	–	150	mV
Channel separation		α	40	–	–	dB
Channel unbalance		$\|\Delta G_v\|$	–	–	1	dB

PACKAGE OUTLINE

13-lead SIL-bent-to-DIL; plastic power (SOT141R).

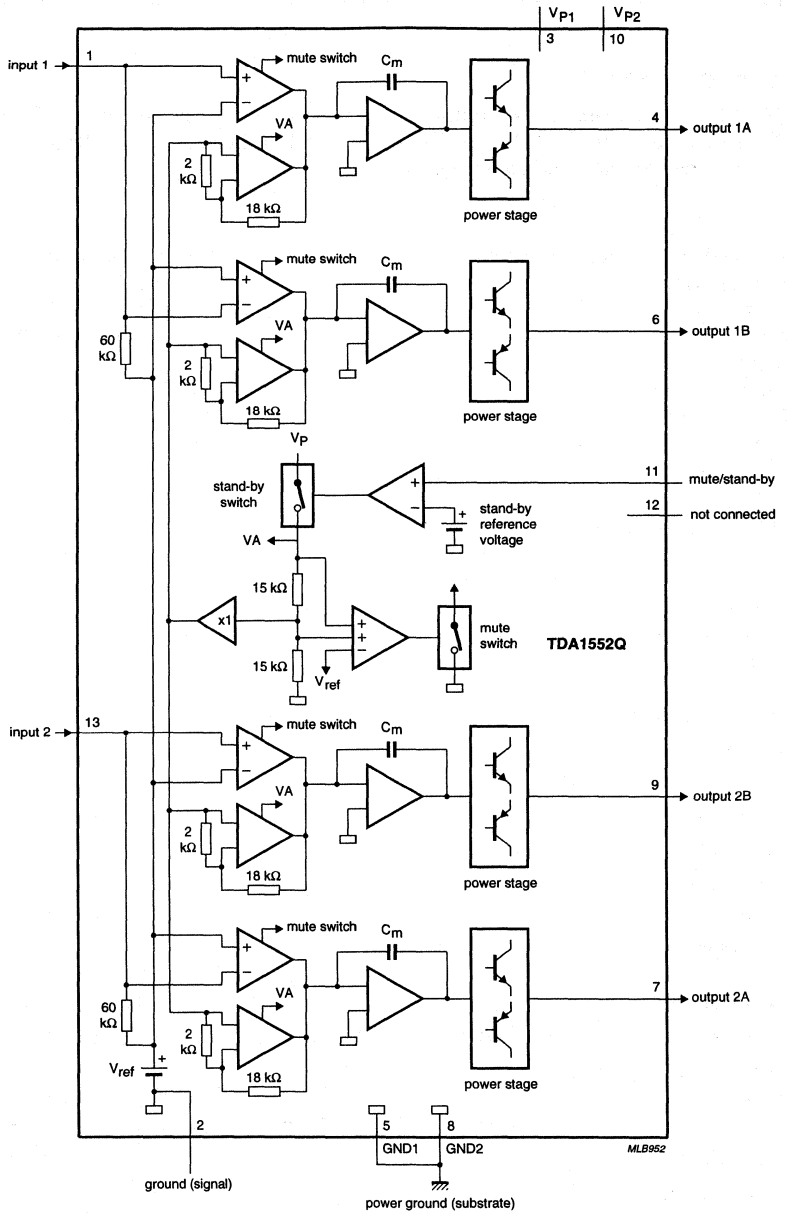


Fig.1 Block diagram.

PINNING

1	IP1	input 1
2	GND	ground (signal)
3	V_{P1}	positive supply voltage 1
4	OUT1A	output 1A
5	GND1	power ground 1 (substrate)
6	OUT1B	output 1B
7	OUT2A	output 2A
8	GND2	power ground 2 (substrate)
9	OUT2B	output 2B
10	V_{P2}	positive supply voltage 2
11	M/SS	mute/stand-by switch
12	n.c.	not connected
13	IP2	input 2

FUNCTIONAL DESCRIPTION

The TDA1552Q contains two identical amplifiers with differential input stages and can be used for bridge applications. The gain of each amplifier is fixed at 26 dB. A special feature of this device is:

Mute/stand-by switch

- low stand-by current ($< 100\ \mu A$)
- low mute/stand-by switching current (low cost supply switch)
- mute facility

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage					
operating		V_P	–	18	V
non-operating		V_P	–	30	V
load dump protected	during 50 ms; $t_r \geqslant 2.5$ ms	V_P	–	45	V
Non-repetitive peak output current		I_{OSM}	–	6	A
Repetitive peak output current		I_{ORM}	–	4	A
Storage temperature range		T_{stg}	−55	+ 150	°C
Junction temperature		T_j	–	150	°C
AC and DC short-circuit-safe voltage		V_{PSC}	–	18	V
Energy handling capability at outputs	$V_P = 0$ V		–	200	mJ
Reverse polarity		V_{PR}	–	6	V
Total power dissipation	see Fig.2	P_{tot}	–	60	W

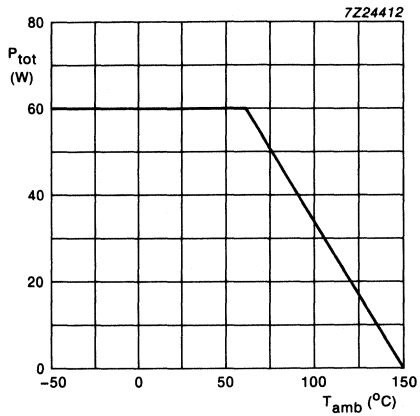


Fig.2 Power derating curve.

DC CHARACTERISTICS

V_P = 14.4 V; T_{amb} = 25 °C; measurements taken using Fig.3; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage range	note 1	V_P	6.0	14.4	18.0	V
Total quiescent current		I_{tot}	–	80	160	mA
DC output voltage	note 2	V_O	–	6.9	–	V
DC output offset voltage		$\lvert\Delta V_O\rvert$	–	–	150	mV
Mute/stand-by switch						
Switch-on voltage level		V_{ON}	8.5	–	–	V
Mute condition		V_{mute}	3.3	–	6.4	V
Output signal in mute position	V_I = 1 V (max); f = 1 kHz	V_O	–	–	2	mV
DC output offset voltage (between pins 4 to 6 and 7 to 9)		$\lvert\Delta V_O\rvert$	–	–	150	mV
Stand-by condition		V_{sb}	0	–	2	V
DC current in stand-by condition	$V_{II} < 0.5$ V	I_{sb}	–	–	100	μA
	$0.5 \text{ V} \leqslant V_{II} < 2$ V	I_{sb}	–	–	500	μA
Switch-on current		I_{sw}	–	25	60	μA
Supply current	short-circuit to GND note 3	I_P	–	5.5	–	mA

AC CHARACTERISTICS

V_P = 14.4 V; R_L = 4 Ω; f = 1 kHz; T_{amb} = 25 °C; measurements taken using Fig.3; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Output power	THD = 0.5%	P_o	15	17	–	W
	THD = 10%	P_o	20	22	–	W
Output power at V_P = 13.2 V	THD = 0.5%	P_o	–	12	–	W
	THD = 10%	P_o	–	17	–	W
Total harmonic distortion	P_o = 1 W	THD	–	0.1	–	%
Power bandwidth	THD = 0.5% P_o = −1 dB w.r.t. 15 W	B_W	–	20 to 15 000	–	Hz
Low frequency roll-off	note 4 −1 dB	f_L	–	25	–	Hz
High frequency roll-off	−1 dB	f_H	20	–	–	kHz
Closed loop voltage gain		G_v	25	26	27	dB
Supply voltage ripple rejection	notes 5, 6	RR	42	–	–	dB
ON	notes 5, 7	RR	48	–	–	dB
mute	notes 5, 6, 7	RR	48	–	–	dB
stand-by	notes 5, 6, 7	RR	80	–	–	dB
Input impedance		$\|Z_i\|$	50	60	75	kΩ
Noise output voltage (RMS value)						
ON	R_S = 0 Ω; note 8	$V_{no(rms)}$	–	70	120	μV
ON	R_S = 10 kΩ; note 8	$V_{no(rms)}$	–	100	–	μV
mute	notes 8, 9	$V_{no(rms)}$	–	60	–	μV
Channel separation		α	40	–	–	dB
Channel unbalance		$\|\Delta G_V\|$	–	–	1	dB

Notes to the characteristics

1. The circuit is DC adjusted at V_P = 6 V to 18 V and AC operating at V_P = 8.5 V to 18 V.
2. At 18 V < V_P < 30 V the DC output voltage ⩽ $V_P/2$.
3. Conditions: 1. V_{11} = 0 V
   2. short-circuit to GND
   3. switch V_{11} to MUTE or ON condition (rise time ⩾ 10 μs).
4. Frequency response externally fixed.
5. Ripple rejection measured at the output with a source impedance of 0 Ω (maximum ripple amplitude of 2 V).
6. Frequency f = 100 Hz.
7. Frequency between 1 kHz and 10 kHz.
8. Noise voltage measured in a bandwidth of 20 Hz to 20 kHz.
9. Noise output voltage independent of R_S (V_I = 0 V).

APPLICATION INFORMATION

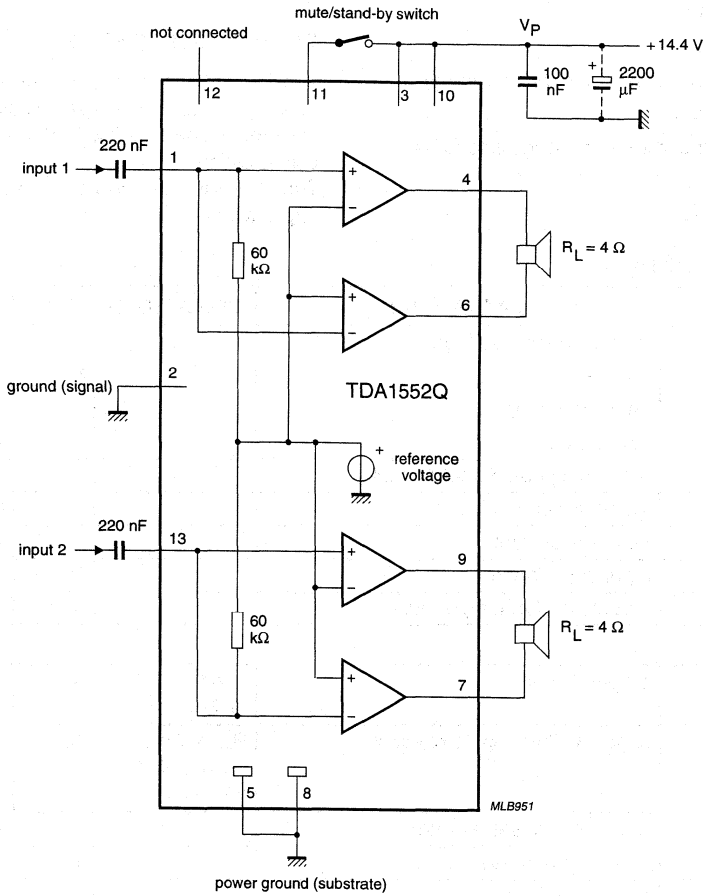


Fig.3 Application circuit diagram.

2 x 22 W stereo BTL car radio power amplifier with loudspeaker protection and 3-state mode switch

TDA1553CQ

FEATURES

- Few peripheral components
- High output power
- Low output offset voltage
- Fixed gain
- Loudspeaker protection
- Good ripple rejection
- 3-state mode switch (operating, mute, stand-by)
- Load dump protection
- AC and DC short-circuit safe to ground and to V_P
- Thermally protected
- Reverse polarity safe
- High energy handling capability at the outputs (V_P = 0)
- Electrostatic discharge protection
- No switch-on/switch-off plop
- Flexible leads
- Low thermal resistance

GENERAL DESCRIPTION

The TDA1553CQ is a monolithic integrated class-B output amplifier in a 13-lead single-in-line (SIL) power package. It contains 2 x 22 W amplifiers in BTL configuration.
The device is primarily developed for car radio applications.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	positive supply voltage					
	operating		6	14.4	18	V
	non-operating		–	–	30	V
	load dump		–	–	45	V
I_{ORM}	repetitive peak output current		–	–	4	A
I_P	total quiescent current		–	80	–	mA
I_{sb}	stand-by current		–	40	100	μA
$\|Z_i\|$	input impedance		50	–	–	kΩ
T_{vj}	virtual junction temperature		–	–	150	°C
Stereo application						
P_O	output power	at 4 Ω; THD = 10%	–	22	–	W
RR	supply voltage ripple rejection	R_s = 0 Ω; f = 100 Hz to 10 kHz	48	–	–	dB
$\|\Delta V_O\|$	DC output offset voltage		–	–	150	mV
α	channel separation		40	–	–	dB
$\|\Delta G_v\|$	channel unbalance		–	–	1	dB

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA1553CQ	13	SIL	plastic	SOT141R

2 x 22 W stereo BTL car radio power amplifier with loudspeaker protection and 3-state mode switch

TDA1553CQ

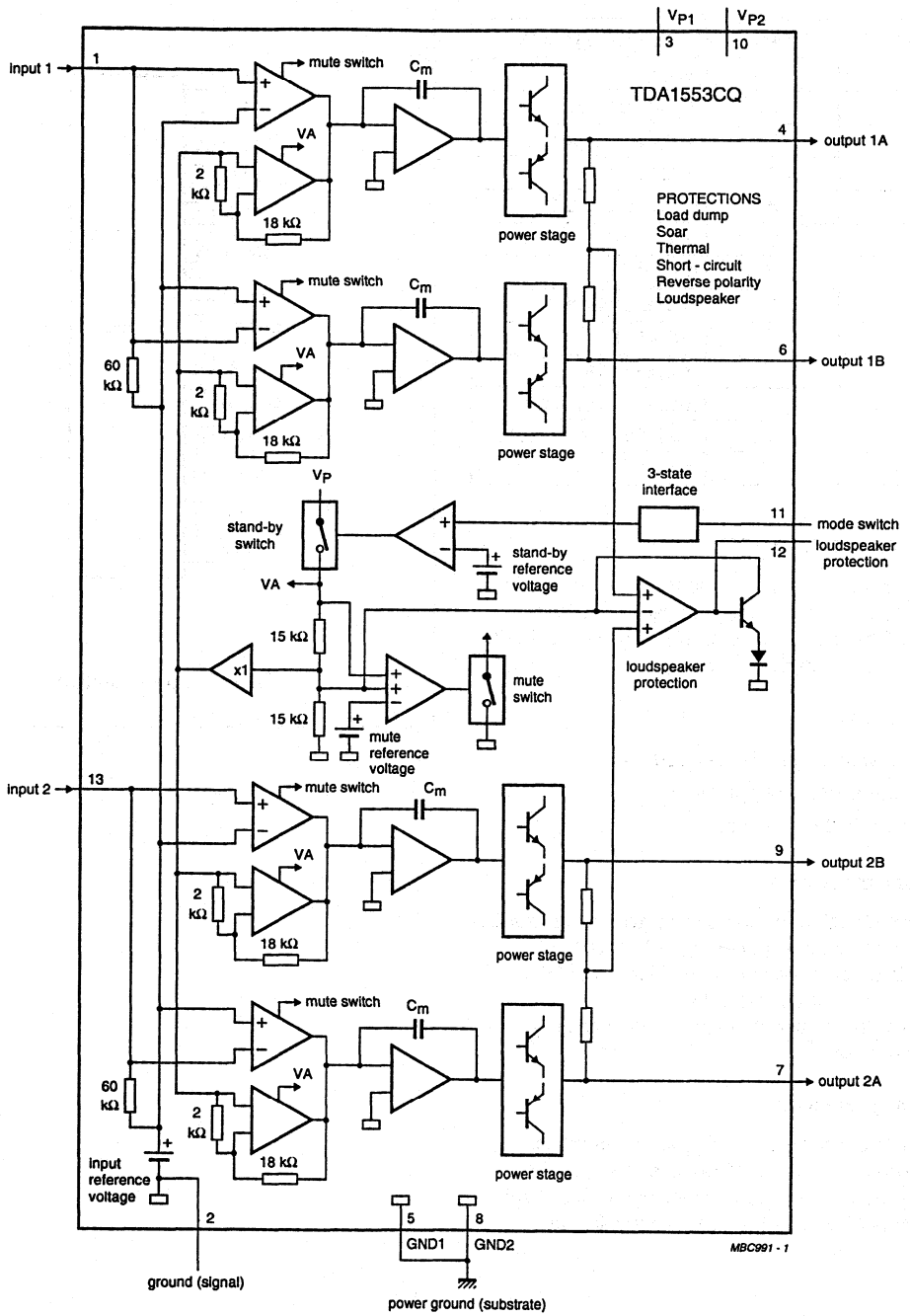


Fig.1 Block diagram.

2 x 22 W stereo BTL car radio power amplifier with loudspeaker protection and 3-state mode switch

TDA1553CQ

PINNING

SYMBOL	PIN	DESCRIPTION
IN 1	1	input 1
GND(S)	2	signal ground
V_{P1}	3	supply voltage
OUT 1A	4	output 1A
GND1	5	power ground 1
OUT 1B	6	output 1B
OUT 2A	7	output 2A
GND2	8	power ground 2
OUT 2B	9	output 2B
V_{P2}	10	supply voltage
MODE	11	mode switch input
LSP	12	loudspeaker protection
IN 2	13	input 2

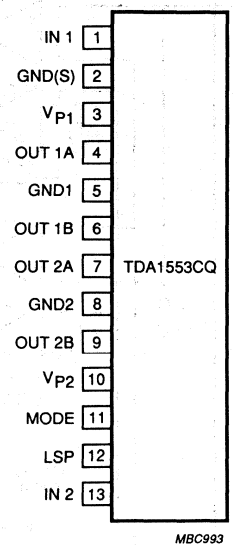


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The TDA1553CQ contains two identical amplifiers with differential input stages and can be used for bridge applications. The gain of each amplifier is fixed at 26 dB. Special features of the device are:

3-state mode switch

- standby : low supply current (< 100 μA)
- mute : input signal suppressed
- operating: normal on condition

Loudspeaker protection

When a short-circuit to ground occurs, which forces a DC voltage across the loudspeaker of ≥ 1 V, a built-in protection circuit becomes active and limits the DC voltage across the loudspeaker to ≤ 1 V.
Pin 12 detects the status of the protection circuit, (e.g. for diagnostic purposes).

Short-circuit protection

If any output is short-circuited to ground during the stand-by mode, it becomes impossible to switch the circuit to the mute or operating condition. In this event the supply current will be limited to a few milliamps.

LIMITING VALUES

In accordance with the absolute maximum system (IEC 134)

SYMBOL	PARAMETER	CONDITION	MIN.	MAX.	UNIT
V_P	positive supply voltage				
	operating		–	18	V
	non-operating		–	30	V
	load dump protection	during 50 ms; $t_r \geq 2.5$ ms	–	45	V
I_{OSM}	non-repetitive peak output current		–	6	A
I_{ORM}	repetitive peak output current		–	4	A
T_{stg}	storage temperature range		–55	150	°C
T_{amb}	operating ambient temperature range		–40	85	°C
T_{vj}	virtual junction temperature		–	150	°C
V_{psc}	AC and DC short-circuit safe voltage		–	18	V
	energy handling capability at outputs	$V_P = 0$	–	200	mJ
V_{pr}	reverse polarity		–	6	V
P_{tot}	total power dissipation		–	60	W

THERMAL RESISTANCE

In accordance with IEC 747-1

SYMBOL	PARAMETER	CONDITIONS	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient in free air		40 K/W
$R_{th\ j\text{-}c}$	from junction to case	see Fig.3	1.5 K/W

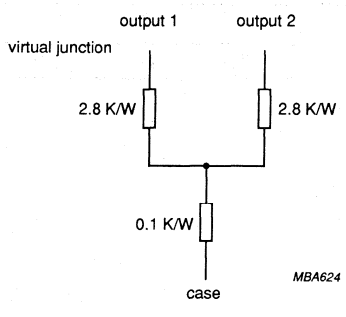


Fig.3 Equivalent thermal resistance network.

DC CHARACTERISTICS

V_P = 14.4 V; T_{amb} = 25 °C; measured in Fig.4; unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_P	positive supply voltage	note 1	6	14.4	18	V
I_P	quiescent current					
		$R_L = \infty$	–	80	160	mA
		note 2	–	5.5	–	mA
Operating condition						
V_{11}	mode switch voltage level		2.2	–	7	V
I_{11}	mode switch current	V_{11} = 2.2 V	–	50	100	μA
V_O	DC output voltage	note 3	–	6.9	–	V
$\lvert\Delta V_O\rvert$	DC output offset voltage		–	–	150	mV
Mute condition						
V_{11}	mode switch voltage level		0	–	0.6	V
$-I_{11}$	mode switch current	V_{11} = 0.6 V	–	50	100	μA
V_O	DC output voltage	note 3	–	6.9	–	V
$\lvert\Delta V_O\rvert$	DC output offset voltage		–	–	150	mV
Stand-by condition						
$\lvert I_{11}\rvert$	mode switch 3-state leakage current		–	–	10	μA
I_{sb}	stand-by current	I_{11} = 0 μA	–	40	100	μA
Loudspeaker protection						
$\lvert\Delta V_{4-6}\rvert$ or $\lvert\Delta V_{7-9}\rvert$	DC voltage across R_L		–	–	1	V
Protection active ($\lvert\Delta V_{4-6}\rvert$ or $\lvert\Delta V_{7-9}\rvert \geq 1.0$ V)						
I_{12}	current information		–	25	–	μA
V_{12}	voltage information		3.6	–	–	V
Protection not active ($\lvert\Delta V_{4-6}\rvert$ and $\lvert\Delta V_{7-9}\rvert \leq 0.15$ V)						
V_{12}	voltage information		–	–	0.3	V

AC CHARACTERISTICS

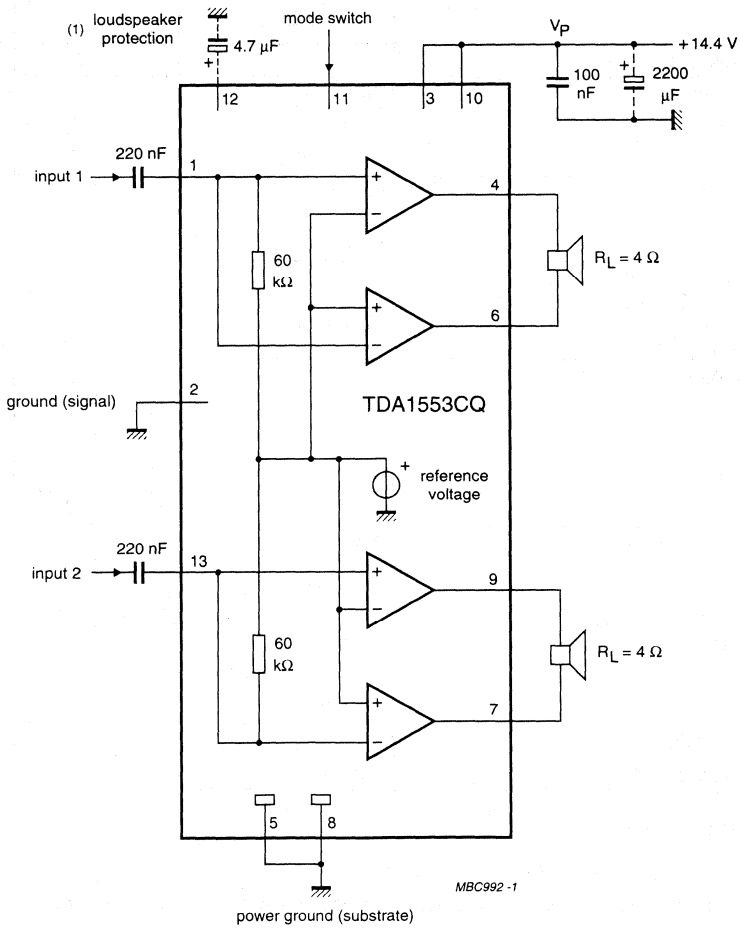
V_P = 14.4 V; R_L = 4 Ω; f = 1 kHz; T_{amb} = 25 °C; measured in Fig.4; unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
P_O	output power	V_P = 14.4 V				
		THD = 0.5%	15	17	–	W
		THD = 10%	20	22	–	W
THD	total harmonic distortion	P_O = 1 W	–	0.1	–	%
P_O	output power	V_P = 13.2 V				
		THD = 0.5%	–	12	–	W
		THD = 10%	–	17	–	W
B	power bandwidth	THD = 0.5%; P_o = –1 dB; with respect to 15 W	–	20 - 15000	–	Hz
f_l	low frequency roll-off	at –1 dB; note 4	–	25	–	Hz
f_h	high frequency roll-off	at –1 dB	20	–	–	kHz
G_v	closed loop voltage gain		25	26	27	dB
RR	supply voltage ripple rejection	note 5				
	on		48	–	–	dB
	mute		48	–	–	dB
	stand-by		80	–	–	dB
$\|Z_I\|$	input impedance		50	60	75	kΩ
V_{no}	noise output voltage	note 6				
	on	R_S = 0 Ω	–	70	120	μV
	on	R_S = 10 kΩ	–	100	–	μV
V_{no}	noise output voltage	notes 6 and 7				
	mute		–	60	–	μV
α	channel separation	R_S = 10 kΩ	40	–	–	dB
$\|\Delta G_v\|$	channel unbalance		–	–	1	dB
V_O	output voltage in mute	note 8	–	–	2	mV

Notes to the characteristics

1. The circuit is DC adjusted at V_P = 6 to 18 V and AC operating at V_P = 9 to 18 V.
2. If any output is short-circuited to ground during the stand-by mode and in this condition the circuit is switched to mute or operating.
3. At 18 V < V_P < 30 V the DC output voltage ≤ V_P/2.
4. Frequency response externally fixed.
5. Ripple rejection measured at the output with a source-impedance of 0 Ω, maximum ripple amplitude of 2 V p-p and at a frequency between 100 Hz and 10 kHz.
6. Noise measured in a bandwidth of 20 Hz to 20 kHz.
7. Noise output voltage independent of R_S (V_I = 0 V).
8. $V_I = V_{Imax}$ = 1 V RMS.

TEST/APPLICATION INFORMATION



(1) With C = 4.7 µF the delay time of the loudspeaker protection is typically 0.5 s.

Fig.4 Stereo BTL application diagram.

2 X 22 W BTL STEREO CAR RADIO POWER AMPLIFIER WITH LOUDSPEAKER PROTECTION

GENERAL DESCRIPTION

The TDA1553Q is an integrated class-B output amplifier in a 13-lead single-in-line (SIL) plastic power package. The circuit contains 2 x 22 W amplifiers in Bridge Tied Load (BTL) configuration. The device is primarily developed for car radio applications.

Features

- Requires very few external components
- High output power
- Low offset voltage at outputs
- Fixed gain
- Good ripple rejection
- Mute/stand-by switch
- Load dump protection
- AC and DC short-circuit-safe to ground and V_P
- Loudspeaker protection (LSP)
- Thermally protected
- Reverse polarity safe
- Capability to handle high energy on outputs (V_P = 0 V)
- Protected against electrostatic discharge
- No switch-on/switch-off plop
- Low thermal resistance
- Flexible leads

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage range						
operating		V_P	6.0	14.4	18.0	V
non-operating		V_P	–	–	30	V
load dump protected		V_P	–	–	45	V
Repetitive peak output current		I_{ORM}	–	–	4	A
Total quiescent current		I_{tot}	–	80	160	mA
Stand-by current		I_{sb}	–	0.1	100	μA
Switch-on current		I_{sw}	–	–	60	μA
Input impedance		$\|Z_I\|$	50	60	75	kΩ
Junction temperature		T_j	–	–	150	°C
Stereo application						
Output power	R_L = 4 Ω; THD = 10%	P_o	20	22	–	W
Supply voltage ripple rejection	R_S = 0 Ω; f = 100 Hz to 10 kHz	RR	48	–	–	dB
DC output offset voltage		$\|\Delta V_O\|$	–	–	150	mV
Channel separation		α	40	–	–	dB
Channel unbalance		$\|\Delta G_v\|$	–	–	1	dB

PACKAGE OUTLINE

13-lead SIL-bent-to-DIL; plastic power (SOT141R).

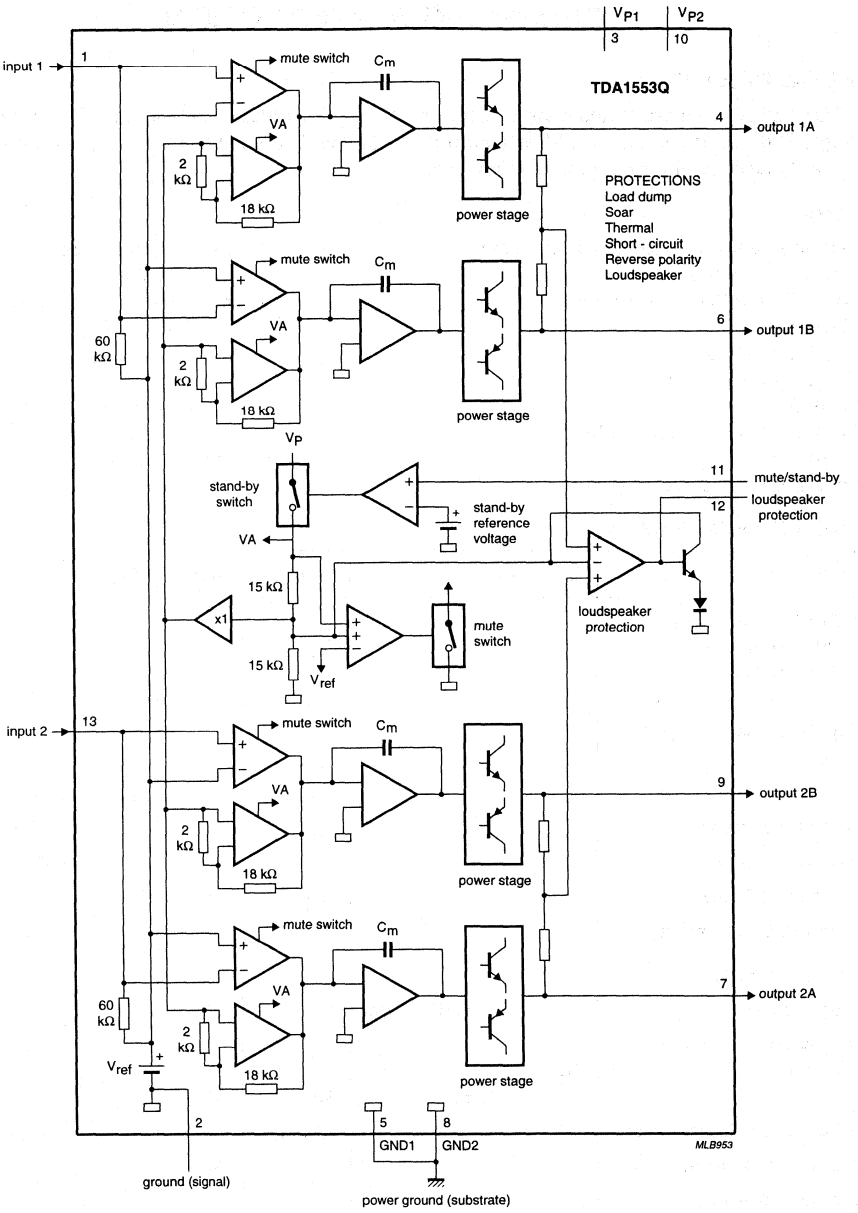


Fig.1 Block diagram.

PINNING

1	IP1	input 1
2	GND	ground (signal)
3	V_{P1}	positive supply voltage 1
4	OUT1A	output 1A
5	GND1	power ground 1 (substrate)
6	OUT1B	output 1B
7	OUT2A	output 2A
8	GND2	power ground 2 (substrate)
9	OUT2B	output 2B
10	V_{P2}	positive supply voltage 2
11	M/SS	mute/stand-by switch
12	LSP	loudspeaker protection
13	IP2	input 2

FUNCTIONAL DESCRIPTION

The TDA1553Q contains two identical amplifiers with differential input stages and can be used for bridge applications. The gain of each amplifier is fixed at 26 dB. Special features of this device are:

Mute/stand-by switch

- low stand-by current ($< 100\ \mu A$)
- low mute/stand-by switching current (low cost supply switch)
- mute facility

Loudspeaker protection

When a short-circuit to ground is made, which forces a DC voltage across the loudspeaker of $\geqslant 1$ V, a built-in protection circuit becomes active and limits the DC voltage across the loudspeaker to $\leqslant 1$ V. The delay time of the protection circuit can be controlled by an external capacitor connected to pin 12.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage					
operating		V_P	–	18	V
non-operating		V_P	–	30	V
load dump protected	during 50 ms; $t_r \geqslant 2.5$ ms	V_P	–	45	V
Non-repetitive peak output current		I_{OSM}	–	6	A
Repetitive peak output current		I_{ORM}	–	4	A
Storage temperature range		T_{stg}	−55	+ 150	°C
Junction temperature		T_j	–	150	°C
AC and DC short-circuit-safe voltage		V_{PSC}	–	18	V
Energy handling capability at outputs	$V_P = 0$ V		–	200	mJ
Reverse polarity		V_{PR}	–	6	V
Total power dissipation	see Fig.2	P_{tot}	–	60	W

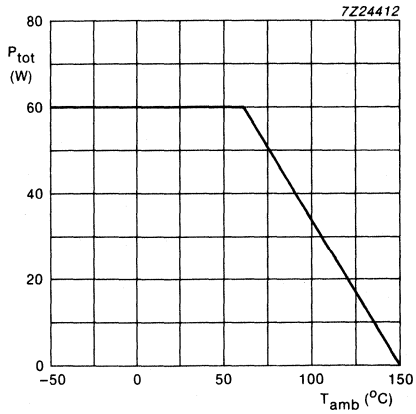


Fig.2 Power derating curve.

DC CHARACTERISTICS

V_P = 14.4 V; T_{amb} = 25 °C; measurements taken using Fig.3; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage range	note 1	V_P	6.0	14.4	18.0	V
Total quiescent current		I_{tot}	–	80	160	mA
DC output voltage	note 2	V_O	–	6.9	–	V
DC output offset voltage		$\lvert\Delta V_O\rvert$	–	–	150	mV
Mute/stand-by switch						
Switch-on voltage level		V_{ON}	8.5	–	–	V
Mute condition		V_{mute}	3.3	–	6.4	V
Output signal in mute position	V_I = 1 V (max.); f = 1 kHz	V_O	–	–	2	mV
DC output offset voltage (between pins 4 to 6 and 7 to 9)		$\lvert\Delta V_O\rvert$	–	–	150	mV
Stand-by condition		V_{sb}	0	–	2	V
DC current in stand-by condition	$V_{I1} < 0.5$ V	I_{sb}	–	–	100	μA
	$0.5 \leqslant V_{I1} < 2$ V	I_{sb}	–	–	500	μA
Switch-on current		I_{sw}	–	25	60	μA
Supply current	short-circuit to ground note 3	I_p	–	5.5	–	mA
Loudspeaker protection						
DC voltage across R_L pin 4 to pin 6		ΔV_{4-6}	–	–	1	V
pin 7 to pin 9		ΔV_{7-9}	–	–	1	V
Delay time		t_d	–	0.5	–	s
Protection active	$\lvert\Delta V_{4-6}\rvert$ or $\lvert\Delta V_{7-9}\rvert \geqslant 1.0$ V					
Current information		I_{12}	–	25	–	μA
Voltage information		V_{12}	2	–	–	V
Protection not active	$\lvert\Delta V_{4-6}\rvert$ and $\lvert\Delta V_{7-9}\rvert \leqslant 0.1$ V					
Voltage information		V_{12}	–	–	0.3	V

AC CHARACTERISTICS

V_P = 14.4 V; R_L = 4 Ω; f = 1 kHz; T_{amb} = 25 °C; measurements taken using Fig.3; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Output power	THD = 0.5%	P_o	15	17	–	W
	THD = 10%	P_o	20	22	–	W
Output power at V_P = 13.2 V	THD = 0.5%	P_o	–	12	–	W
	THD = 10%	P_o	–	17	–	W
Total harmonic distortion	P_o = 1 W	THD	–	0.1	–	%
Power bandwidth	THD = 0.5% P_o = −1 dB w.r.t. 15 W	B_w	–	20 to 15 000	–	Hz
Low frequency roll-off	note 4 −1 dB	f_L	–	25	–	Hz
High frequency roll-off	−1 dB	f_H	20	–	–	kHz
Closed loop voltage gain		G_v	25	26	27	dB
Supply voltage ripple rejection	notes 5, 6	RR	42	–	–	dB
ON	notes 5, 7	RR	48	–	–	dB
mute	notes 5, 6, 7	RR	48	–	–	dB
stand-by	notes 5, 6, 7	RR	80	–	–	dB
Input impedance		$\|Z_i\|$	50	60	75	kΩ
Noise output voltage (RMS value)						
ON	R_S = 0 Ω; note 8	$V_{no(rms)}$	–	70	120	μV
ON	R_S = 10 kΩ; note 8	$V_{no(rms)}$	–	100	–	μV
mute	notes 8, 9	$V_{no(rms)}$	–	60	–	μV
Channel separation		α	40	–	–	dB
Channel unbalance		$\|\Delta G_v\|$	–	–	1	dB

Notes to the characteristics

1. The circuit is DC adjusted at V_P = 6 V to 18 V and AC operating at V_P = 8.5 V to 18 V.
2. At 18 V < V_P < 30 V the DC output voltage ⩽ V_P/2.
3. Conditions: 1. V_{11} = 0 V
   2. short-circuit to GND
   3. switch V_{11} to MUTE or ON condition (rise time ⩾ 10 μs).
4. Frequency response externally fixed.
5. Ripple rejection measured at the output with a source impedance of 0 Ω (maximum ripple amplitude of 2 V).
6. Frequency f = 100 Hz.
7. Frequency between 1 kHz and 10 kHz.
8. Noise voltage measured in a bandwidth of 20 Hz to 20 kHz.
9. Noise output voltage independent of R_S (V_I = 0 V).

APPLICATION INFORMATION

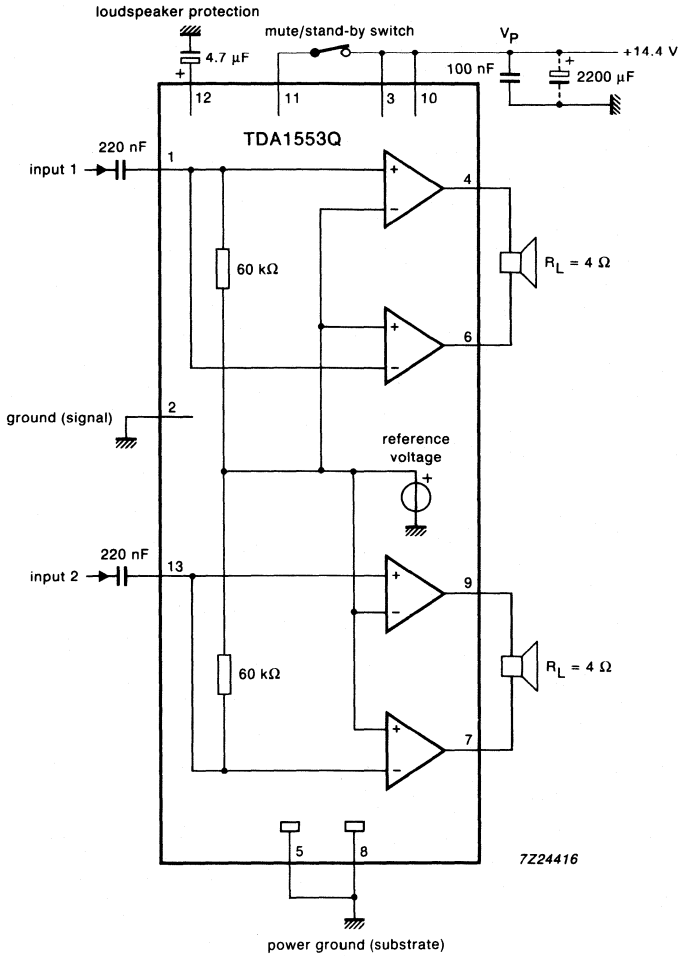


Fig.3 Application circuit diagram.

4 X 11 W SINGLE-ENDED OR 2 X 22 W POWER AMPLIFIER

GENERAL DESCRIPTION

The TDA1554Q is an integrated class-B output amplifier in a 17-lead single-in-line (SIL) plastic power package. The circuit contains 4 x 11 W single-ended or 2 x 22 W bridge amplifiers. The device is primarily developed for car radio applications.

Features

- Requires very few external components
- Flexibility in use — Quad single-ended or stereo BTL
- High output power
- Low offset voltage at outputs (important for BTL)
- Fixed gain
- Good ripple rejection
- Mute/stand-by switch
- Load dump protection
- AC and DC short-circuit-safe to ground and V_P
- Thermally protected
- Reverse polarity safe
- Capability to handle high energy on outputs (V_P = 0 V)
- Protected against electrostatic discharge
- No switch-on/switch-off plop
- Low thermal resistance
- Identical inputs (inverting and non-inverting)
- Flexible leads

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage range operating		V_P	6.0	14.4	18.0	V
Repetitive peak output current		I_{ORM}	–	–	4	A
Total quiescent current		I_{tot}	–	80	160	mA
Stand-by current		I_{sb}	–	0.1	100	μA
Stereo BTL application						
Output power	R_L = 4 Ω; THD = 10%	P_o	20	22	–	W
Supply voltage ripple rejection		RR	48	–	–	dB
Noise output voltage (RMS value)	R_S = 0 Ω	$V_{no(rms)}$	–	70	–	μV
Input impedance		$\|Z_I\|$	25	30	38	kΩ
DC output offset voltage		$\|\Delta V_O\|$	–	–	100	mV
Quad single-ended application						
Output power	THD = 10%					
	R_L = 4 Ω	P_o	–	6	–	W
	R_L = 2 Ω	P_o	–	11	–	W
Supply voltage ripple rejection		RR	48	–	–	dB
Noise output voltage (RMS value)	R_S = 0 Ω	$V_{no(rms)}$	–	50	–	μV
Input impedance		$\|Z_I\|$	50	60	75	kΩ

PACKAGE OUTLINE

17-lead SIL-bent-to-DIL; plastic power (SOT243R).

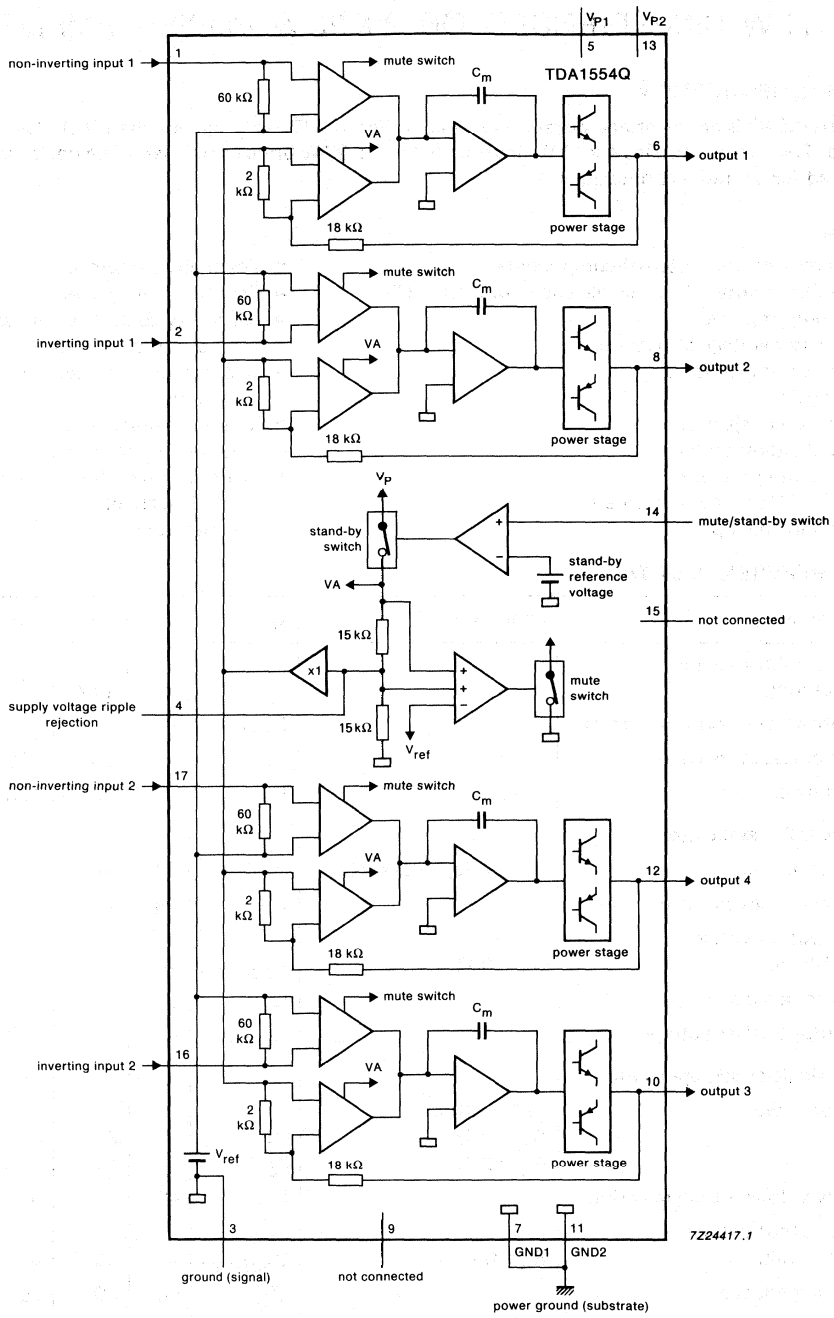


Fig.1 Block diagram.

PINNING

1	NINV1	non-inverting input 1
2	INV1	inverting input 1
3	GND	ground (signal)
4	RR	supply voltage ripple rejection
5	V_{P1}	positive supply voltage 1
6	OUT1	output 1
7	GND1	power ground 1 (substrate)
8	OUT2	output 2
9	n.c.	not connected
10	OUT3	output 3
11	GND2	power ground 2 (substrate)
12	OUT4	output 4
13	V_{P2}	positive supply voltage 2
14	M/SS	mute/stand-by switch
15	n.c.	not connected
16	INV2	inverting input 2
17	NINV2	non-inverting input 2

FUNCTIONAL DESCRIPTION

The TDA1554Q contains four identical amplifiers with differential input stages (two inverting and two non-inverting) and can be used for single-ended or bridge applications. The gain of each amplifier is fixed at 20 dB (26 dB in BTL). A special feature of this device is:

Mute/stand-by switch

- low stand-by current ($< 100\ \mu A$)
- low mute/stand-by switching current (low cost supply switch)
- mute facility

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage					
operating		V_P	–	18	V
non-operating		V_P	–	30	V
load dump protected	during 50 ms; $t_r \geqslant 2.5$ ms	V_P	–	45	V
Non-repetitive peak output current		I_{OSM}	–	6	A
Repetitive peak output current		I_{ORM}	–	4	A
Storage temperature range		T_{stg}	–55	+ 150	°C
Junction temperature		T_j	–	150	°C
AC and DC short-circuit-safe voltage		V_{PSC}	–	18	V
Energy handling capability at outputs	$V_P = 0$ V		–	200	mJ
Reverse polarity		V_{PR}	–	6	V
Total power dissipation	see Fig.2	P_{tot}	–	60	W

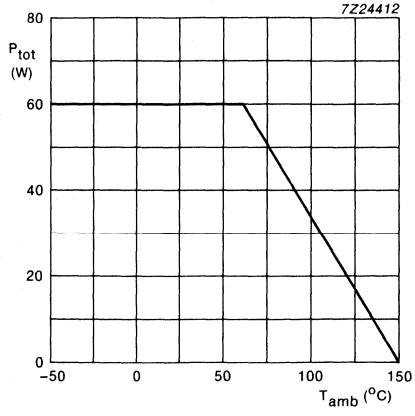


Fig.2 Power derating curve.

DC CHARACTERISTICS

V_P = 14.4 V; T_{amb} = 25 °C; measurements taken using Fig.4; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage range	note 1	V_P	6.0	14.4	18.0	V
Total quiescent current		I_{tot}	–	80	160	mA
DC output voltage	note 2	V_O	–	6.9	–	V
DC output offset voltage		$\lvert\Delta V_O\rvert$	–	–	100	mV
Mute/stand-by switch						
Switch-on voltage level		V_{ON}	8.5	–	–	V
Mute condition		V_{mute}	3.3	–	6.4	V
Output signal in mute position	V_I = 1 V (max); f = 1 kHz	V_O	–	–	2	mV
DC output offset voltage (between pins 6 to 8 and 10 to 12)		$\lvert\Delta V_O\rvert$	–	–	100	mV
Stand-by condition		V_{sb}	0	–	2	V
DC current in stand-by condition		I_{sb}	–	–	100	μA
Switch-on current		I_{sw}	–	12	40	μA

AC CHARACTERISTICS

V_P = 14.4 V; R_L = 4 Ω; f = 1 kHz; T_{amb} = 25 °C; measurements taken using Fig.3 for stereo BTL application and Fig.4 for quad single-ended application unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Stereo BTL application						
Output power	THD = 0.5%	P_o	15	17	–	W
	THD = 10%	P_o	20	22	–	W
Output power at V_P = 13.2 V	THD = 0.5%	P_o	–	12	–	W
	THD = 10%	P_o	–	17	–	W
Total harmonic distortion	P_o = 1 W	THD	–	0.1	–	%
Power bandwidth	THD = 0.5% P_o = −1 dB w.r.t. 15 W	B_W	–	20 to 15 000	–	Hz
Low frequency roll-off	note 3 −1 dB	f_L	–	45	–	Hz
High frequency roll-off	−1 dB	f_H	20	–	–	kHz
Closed loop voltage gain		G_v	25	26	27	dB
Supply voltage ripple rejection	note 4					
ON		RR	48	–	–	dB
mute		RR	48	–	–	dB
stand-by		RR	80	–	–	dB
Input impedance		$\|Z_i\|$	25	30	38	kΩ
Noise output voltage (RMS value)						
ON	R_S = 0 Ω; note 5	$V_{no(rms)}$	–	70	–	μV
ON	R_S = 10 kΩ; note 5	$V_{no(rms)}$	–	100	200	μV
mute	notes 5 and 6	$V_{no(rms)}$	–	60	–	μV
Channel separation	R_S = 10 kΩ	α	40	–	–	dB
Channel unbalance		$\|\Delta G_v\|$	–	–	1	dB

parameter	conditions	symbol	min.	typ.	max.	unit
Quad single-ended application						
Output power	note 7					
	THD = 0.5%	P_o	4	5	–	W
	THD = 10%	P_o	5.5	6	–	W
Output power at R_L = 2 Ω	note 7					
	THD = 0.5%	P_o	7.5	8.5	–	W
	THD = 10%	P_o	10	11	–	W
Total harmonic distortion	P_o = 1 W	THD	–	0.1	–	%
Low frequency roll-off	note 3					
	−3 dB	f_L	–	45	–	Hz
High frequency roll-off	−1 dB	f_H	20	–	–	kHz
Closed loop voltage gain		G_v	19	20	21	dB
Supply voltage ripple rejection	note 4					
ON		RR	48	–	–	dB
mute		RR	48	–	–	dB
stand-by		RR	80	–	–	dB
Input impedance		$\|Z_i\|$	50	60	75	kΩ
Noise output voltage (RMS value)						
ON	R_S = 0 Ω; note 5	$V_{no(rms)}$	–	50	–	μV
ON	R_S = 10 kΩ; note 5	$V_{no(rms)}$	–	70	100	μV
mute	notes 5 and 6	$V_{no(rms)}$	–	50	–	μV
Channel separation	R_S = 10 kΩ	α	40	–	–	dB
Channel unbalance		$\|\Delta G_v\|$	–	–	1	dB

Notes to the characteristics

1. The circuit is DC adjusted at V_P = 6 V to 18 V and AC operating at V_P = 8.5 V to 18 V.
2. At 18 V < V_P < 30 V the DC output voltage ⩽ $V_P/2$.
3. Frequency response externally fixed.
4. Ripple rejection measured at the output with a source impedance of 0 Ω (maximum ripple amplitude of 2 V) and a frequency between 100 Hz and 10 kHz.
5. Noise voltage measured in a bandwidth of 20 Hz to 20 kHz.
6. Noise output voltage independent of R_S (V_I = 0 V).
7. Output power is measured directly at the output pins of the IC.

APPLICATION INFORMATION

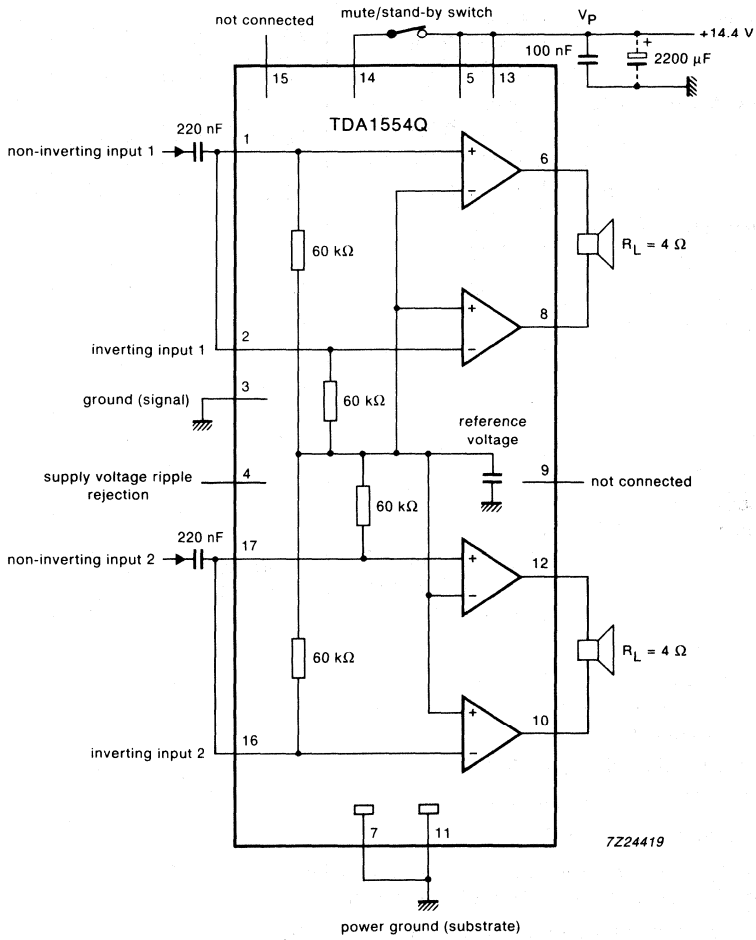


Fig.3 Stereo BTL application circuit diagram.

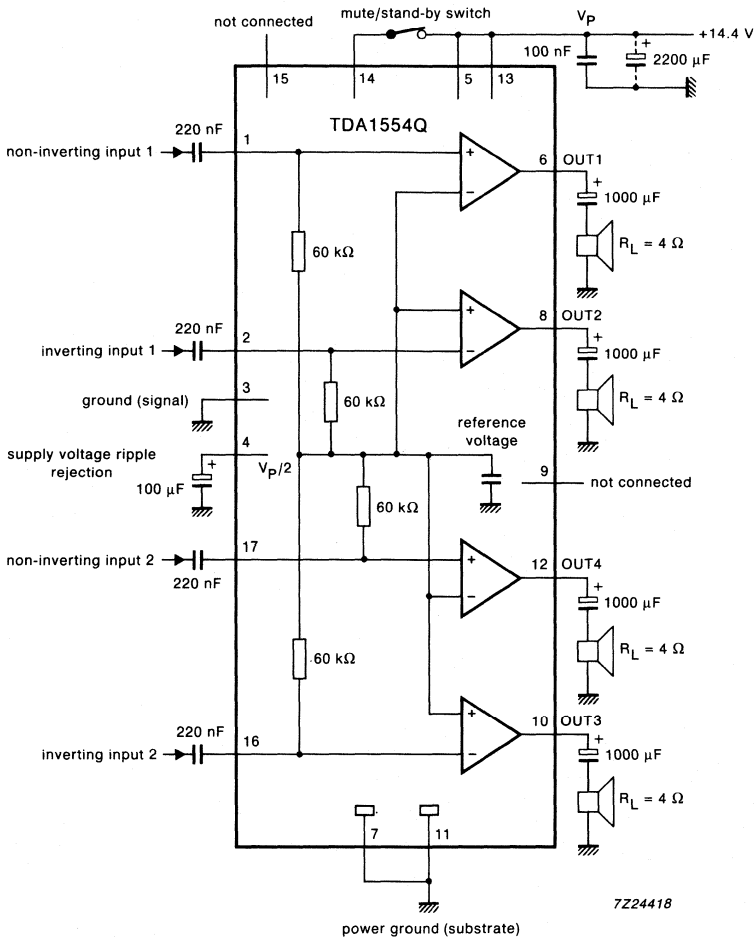


Fig.4 Quad single-ended application circuit diagram.

4 X 11 W SINGLE-ENDED OR 2 X 22 W POWER AMPLIFIER WITH DISTORTION DETECTOR

GENERAL DESCRIPTION

The TDA1555Q is an integrated class-B output amplifier in a 17-lead single-in-line (SIL) plastic power package. The circuit contains 4 x 11 W single-ended or 2 x 22 W bridge amplifiers. The device is primarily developed for car radio applications.

Features

- Requires very few external components
- Flexibility in use – Quad single-ended or stereo BTL
- High output power
- Low offset voltage at outputs (important for BTL)
- Fixed gain
- Good ripple rejection
- Mute/stand-by switch
- Load dump protection
- AC and DC short-circuit-safe to ground and V_P
- Thermally protected
- Reverse polarity safe
- Capability to handle high energy on outputs (V_P = 0 V)
- Protected against electrostatic discharge
- No switch-on/switch-off plop
- Low thermal resistance
- Identical inputs (inverting and non-inverting)
- Flexible leads
- Distortion detector

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage range operating		V_P	6.0	14.4	18.0	V
Repetitive peak output current		I_{ORM}	–	–	4	A
Total quiescent current		I_{tot}	–	80	160	mA
Stand-by current		I_{sb}	–	0.1	100	μA
Stereo BTL application						
Output power	R_L = 4 Ω; THD = 10%	P_o	20	22	–	W
Supply voltage ripple rejection		RR	48	–	–	dB
Noise output voltage (RMS value)	R_S = 0 Ω	$V_{no(rms)}$	–	70	–	μV
Input impedance		$\|Z_I\|$	25	30	38	kΩ
DC output offset voltage		$\|\Delta V_O\|$	–	–	100	mV
Quad single-ended application						
Output power	THD = 10%					
	R_L = 4 Ω	P_o	–	6	–	W
	R_L = 2 Ω	P_o	–	11	–	W
Supply voltage ripple rejection		RR	48	–	–	dB
Noise output voltage (RMS value)	R_S = 0 Ω	$V_{no(rms)}$	–	50	–	μV
Input impedance		$\|Z_I\|$	50	60	75	kΩ

PACKAGE OUTLINE

17-lead SIL-bent-to-DIL; plastic power (SOT243R).

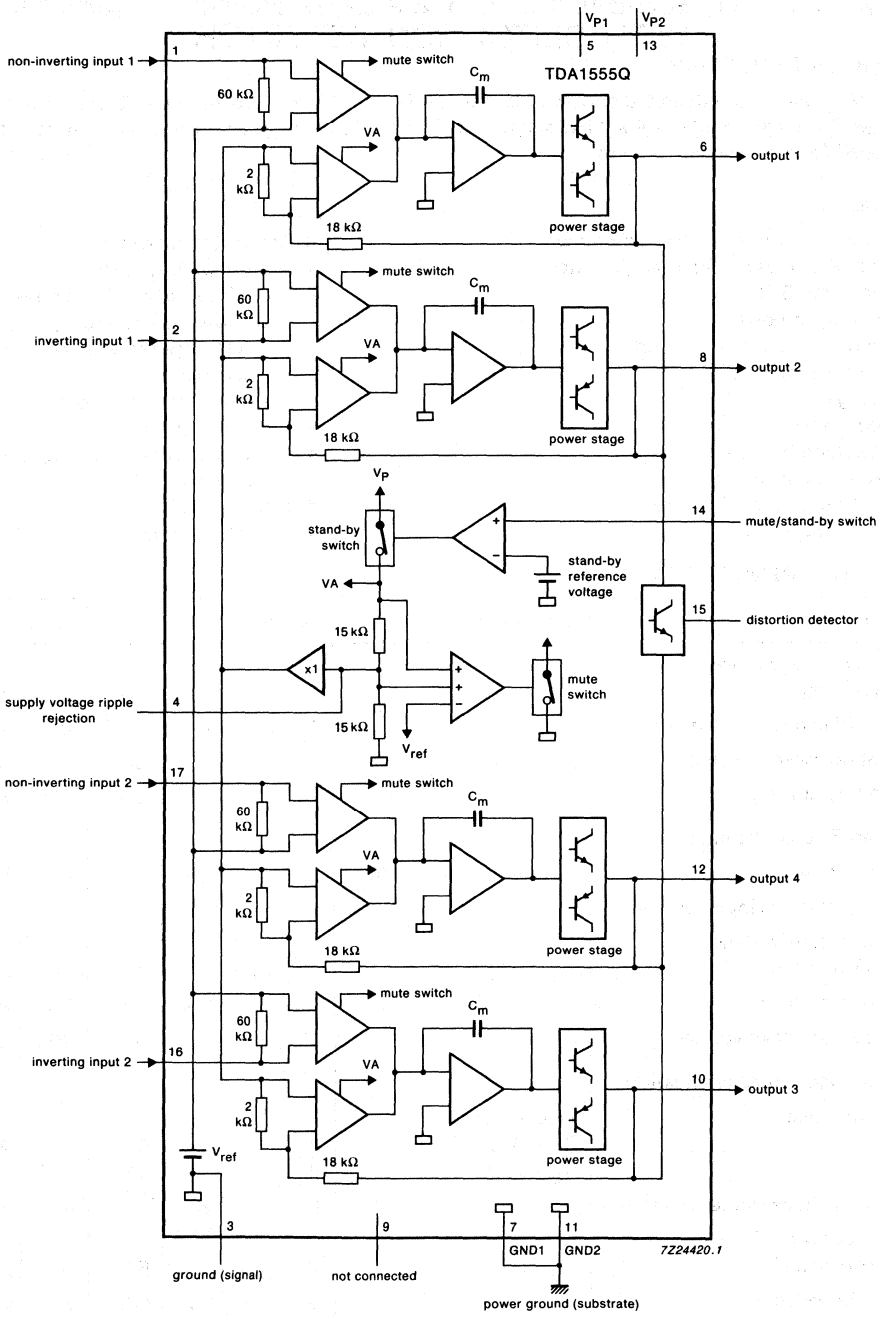


Fig.1 Block diagram.

PINNING

1	NINV1	non-inverting input 1
2	INV1	inverting input 1
3	GND	ground (signal)
4	RR	supply voltage ripple rejection
5	V_{P1}	positive supply voltage 1
6	OUT1	output 1
7	GND1	power ground 1 (substrate)
8	OUT2	output 2
9	n.c.	not connected
10	OUT3	output 3
11	GND2	power ground 2 (substrate)
12	OUT4	output 4
13	V_{P2}	positive supply voltage 2
14	M/SS	mute/stand-by switch
15	DD	distortion detector
16	INV2	inverting input 2
17	NINV2	non-inverting input 2

FUNCTIONAL DESCRIPTION

The TDA1555Q contains four identical amplifiers with differential input stages (two inverting and two non-inverting) and can be used for single-ended or bridge applications. The gain of each amplifier is fixed at 20 dB (26 dB in BTL). Special features of this device are:

Mute/stand-by switch

- low stand-by current ($< 100\ \mu A$)
- low mute/stand-by switching current (low cost supply switch)
- mute facility

Distortion detector

- At onset of clipping of one or more channels the distortion detector (pin 15) becomes active. This information can be used to drive a sound processor or DC volume control to decrease the input signal and so limit distortion.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage					
operating		V_P	–	18	V
non-operating		V_P	–	30	V
load dump protected	during 50 ms; $t_r \geqslant 2.5$ ms	V_P	–	45	V
Non-repetitive peak output current		I_{OSM}	–	6	A
Repetitive peak output current		I_{ORM}	–	4	A
Storage temperature range		T_{stg}	−55	+ 150	°C
Junction temperature		T_j	–	150	°C
AC and DC short-circuit-safe voltage		V_{PSC}	–	18	V
Energy handling capability at outputs	$V_P = 0$ V		–	200	mJ
Reverse polarity		V_{PR}	–	6	V
Total power dissipation	see Fig.2	P_{tot}	–	60	W

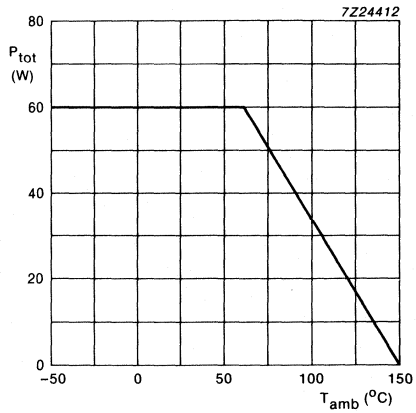


Fig.2 Power derating curve.

DC CHARACTERISTICS

V_P = 14.4 V; T_{amb} = 25 °C; measurements taken using Fig.4; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage range	note 1	V_P	6.0	14.4	18.0	V
Total quiescent current		I_{tot}	–	80	160	mA
DC output voltage	note 2	V_O	–	6.9	–	V
DC output offset voltage		$\lvert\Delta V_O\rvert$	–	–	100	mV
Mute/stand-by switch						
Switch-on voltage level		V_{ON}	8.5	–	–	V
Mute condition		V_{mute}	3.3	–	6.4	V
Output signal in mute position	V_I = 1 V (max.); f = 1 kHz	V_O	–	–	2	mV
DC output offset voltage (between pins 6 to 8 and 10 to 12)		$\lvert\Delta V_O\rvert$	–	–	100	mV
Stand-by condition		V_{sb}	0	–	2	V
DC current in stand-by condition		I_{sb}	–	–	100	μA
Switch-on current		I_{sw}	–	12	40	μA

AC CHARACTERISTICS

V_P = 14.4 V; R_L = 4 Ω; f = 1 kHz; T_{amb} = 25 °C; measurements taken using Fig.3 for stereo BTL application and Fig.4 for quad single-ended application unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Stereo BTL application						
Output power	THD = 0.5%	P_o	15	17	–	W
	THD = 10%	P_o	20	22	–	W
Output power at V_P = 13.2 V	THD = 0.5%	P_o	–	12	–	W
	THD = 10%	P_o	–	17	–	W
Total harmonic distortion	P_o = 1 W	THD	–	0.1	–	%
Power bandwidth	THD = 0.5% P_o = −1 dB w.r.t. 15 W	B_w	–	20 to 15 000	–	Hz
Low frequency roll-off	note 3 −1 dB	f_L	–	45	–	Hz
High frequency roll-off	−1 dB	f_H	20	–	–	kHz
Closed loop voltage gain		G_v	25	26	27	dB
Supply voltage ripple rejection	note 4					
ON		RR	48	–	–	dB
mute		RR	48	–	–	dB
stand-by		RR	80	–	–	dB
Input impedance		$\|Z_i\|$	25	30	38	kΩ
Noise output voltage (RMS value)						
ON	R_S = 0 Ω; note 5	$V_{no(rms)}$	–	70	–	μV
ON	R_S = 10 kΩ; note 5	$V_{no(rms)}$	–	100	200	μV
mute	notes 5 and 6	$V_{no(rms)}$	–	60	–	μV
Channel separation	R_S = 10 kΩ	α	40	–	–	dB
Channel unbalance		$\|\Delta G_v\|$	–	–	1	dB
Distortion detector	$\hat{I}_{DD}$ = 50 μA	THD	2	–	5	%

parameter	conditions	symbol	min.	typ.	max.	unit
Quad single-ended application						
Output power	note 7					
	THD = 0.5%	P_o	4	5	–	W
	THD = 10%	P_o	5.5	6	–	W
Output power at R_L = 2 Ω	note 7					
	THD = 0.5%	P_o	7.5	8.5	–	W
	THD = 10%	P_o	10	11	–	W
Total harmonic distortion	P_o = 1 W	THD	–	0.1	–	%
Low frequency roll-off	note 3					
	−3 dB	f_L	–	45	–	Hz
High frequency roll-off	−1 dB	f_H	20	–	–	kHz
Closed loop voltage gain		G_v	19	20	21	dB
Supply voltage ripple rejection	note 4					
ON		RR	48	–	–	dB
mute		RR	48	–	–	dB
stand-by		RR	80	–	–	dB
Input impedance		$\|Z_i\|$	50	60	75	kΩ
Noise output voltage (RMS value)						
ON	R_S = 0 Ω; note 5	$V_{no(rms)}$	–	50	–	μV
ON	R_S = 10 kΩ; note 5	$V_{no(rms)}$	–	70	100	μV
mute	notes 5 and 6	$V_{no(rms)}$	–	50	–	μV
Channel separation	R_S = 10 kΩ	α	40	–	–	dB
Channel unbalance		$\|\Delta G_v\|$	–	–	1	dB
Distortion detector	$\hat{I}_{DD}$ = 50 μA	THD	2	–	5	%

Notes to the characteristics

1. The circuit is DC adjusted at V_P = 6 V to 18 V and AC operating at V_P = 8.5 to 18 V.
2. At 18 V < V_P < 30 V the DC output voltage ⩽ V_P/2.
3. Frequency response externally fixed.
4. Ripple rejection measured at the output with a source impedance of 0 Ω (maximum ripple amplitude of 2 V) and a frequency between 100 Hz and 10 kHz.
5. Noise voltage measured in a bandwidth of 20 Hz to 20 kHz.
6. Noise output voltage independent of R_S (V_I = 0 V).
7. Output power is measured directly at the output pins of the IC.

APPLICATION INFORMATION

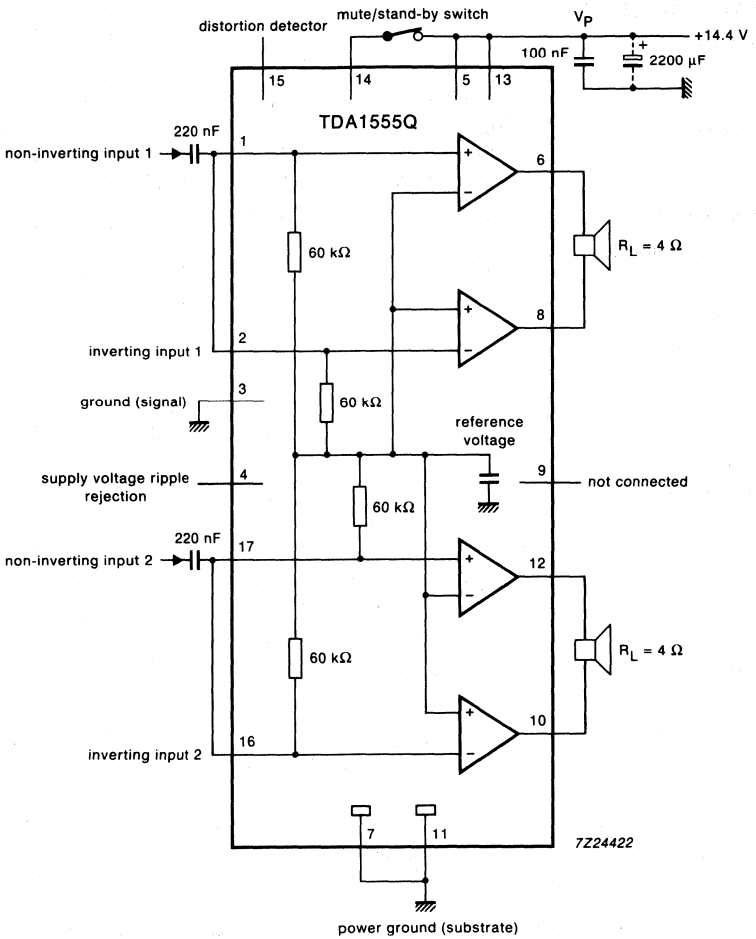


Fig.3 Stereo BTL application circuit diagram.

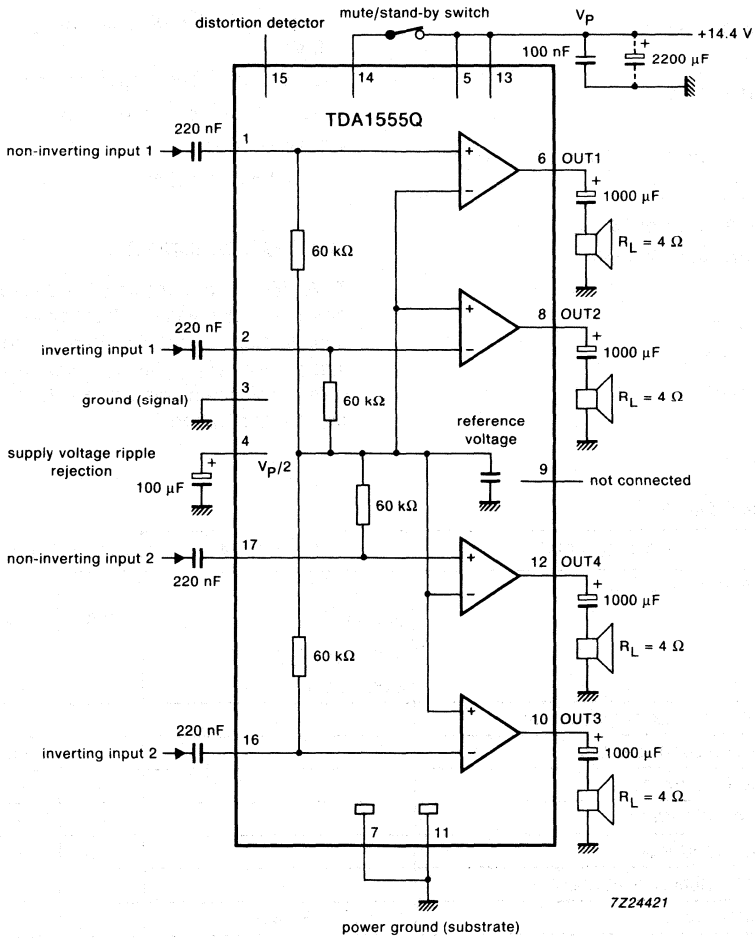


Fig.4 Quad single-ended application circuit diagram.

2 x 22 W stereo BTL differential amplifier with speaker protection and dynamic distortion detector

TDA1556Q

FEATURES

- Few peripheral components
- High output power
- Low output offset voltage
- Fixed gain
- Loudspeaker protection (with diagnostic facility)
- Differential inputs
- Dynamic Distortion Detector (DDD)
- High common mode input signal
- Very high CMRR
- Good ripple rejection
- Mute/stand-by switch
- Load dump protection
- Short-circuit safe
- Thermally protected
- Reverse polarity safe
- High energy handling capability at the outputs (V_P = 0 V)
- Electrostatic discharge protection
- No switch-on/switch-off plop
- Flexible leads
- Low thermal resistance

GENERAL DESCRIPTION

TDA1556Q is a monolithic integrated class-B output amplifier containing two 22 Watt amplifiers in a BTL configuration. The device is contained in a 17-lead single-in-line (SIL) plastic power package. It has two differential inputs and is primarily intended for car booster applications.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
V_P	positive supply voltage					
		operating	6.0	14.4	18	V
		non-operating	–	–	30	V
		load dump	–	–	45	V
I_{ORM}	repetitive peak output current		–	—	4	A
I_P	total quiescent current		–	80	–	mA
I_{sb}	stand-by current		–	0.1	100	μA
I_{sw}	switch-on current		–	–	60	μA
$\|Z_i\|$	input impedance		50	–	–	kΩ
T_{vj}	virtual junction temperature		–	–	150	°C
P_O	output power	4 Ω; THD = 10%	–	22	–	W
SVRR	supply voltage ripple rejection	R_S = 0 Ω; f = 100 Hz to 10 kHz	48	–	–	dB
V_{os}	DC output offset voltage		–	–	100	mV
α	channel separation		40	–	–	dB
ΔG_v	channel unbalance		–	–	1	dB
CMRR	rejection ratio		–	72	–	dB

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA1556Q	17	SIL	plastic	SOT243R

2 x 22 W stereo BTL differential amplifier with speaker protection and dynamic distortion detector

TDA1556Q

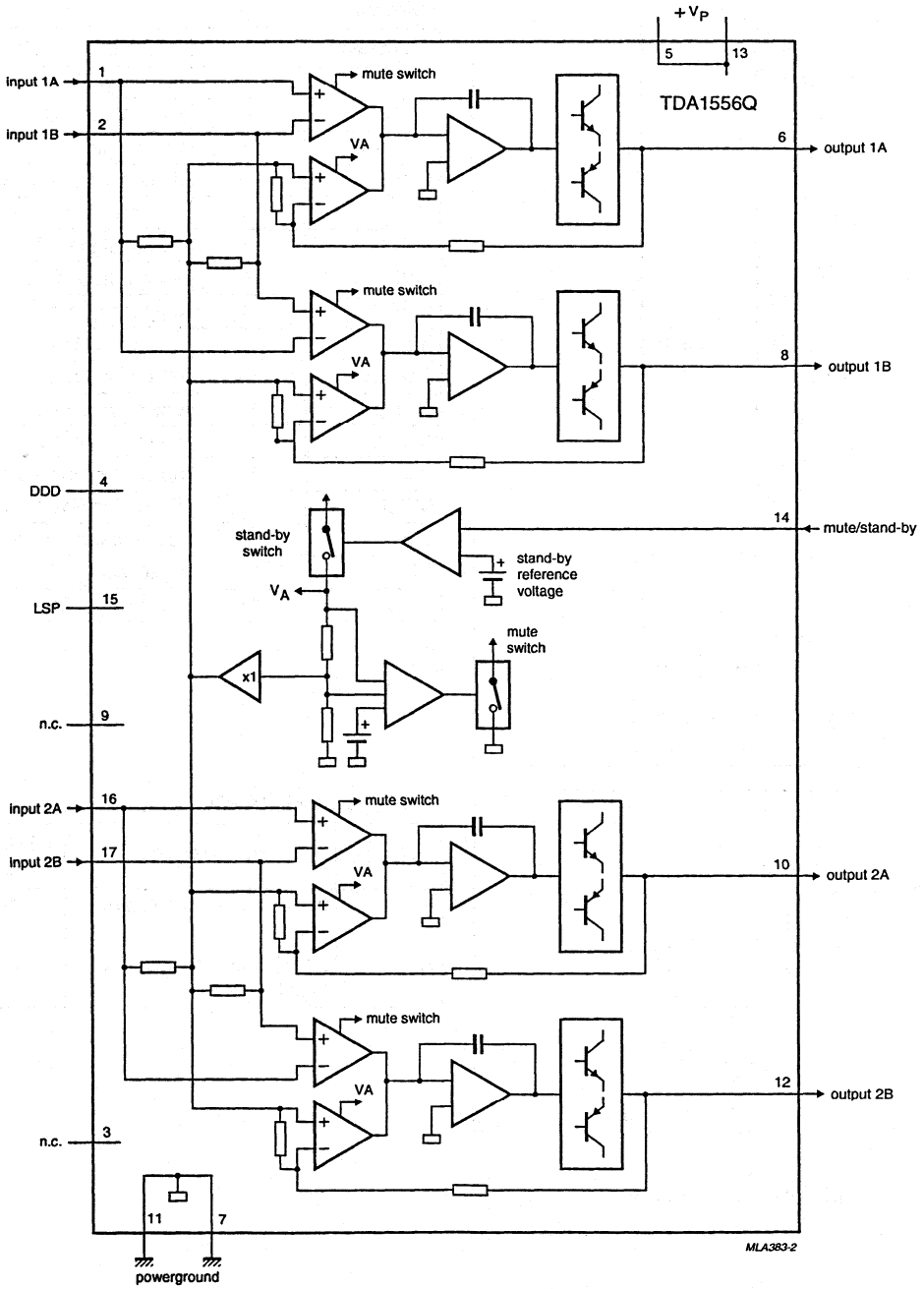


Fig.1 Block diagram.

2 x 22 W stereo BTL differential amplifier with speaker protection and dynamic distortion detector

TDA1556Q

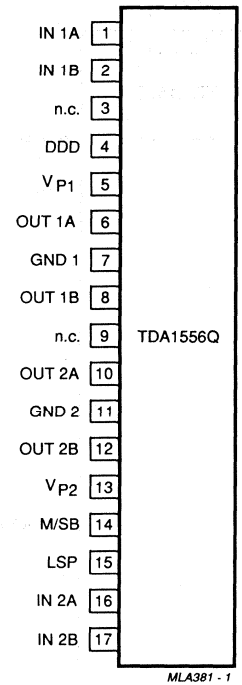


Fig.2 Pin configuration.

PINNING

SYMBOL	PIN	DESCRIPTION
IN1A	1	input signal 1A
IN1B	2	input signal 1B
n.c.	3	not connected
DDD	4	dynamic distortion detector
V_{P1}	5	positive supply voltage 1
OUT1A	6	output signal 1A
GND1	7	power ground 1
OUT1B	8	output signal 1B
n.c.	9	not connected
OUT2A	10	output signal 2A
GND2	11	power ground 2
OUT2B	12	output signal 2B
V_{P2}	13	positive supply voltage 2
M/SB	14	mute/stand-by switch
LSP	15	loudspeaker protection
IN2A	16	input signal 2B
IN2B	17	input signal 2A

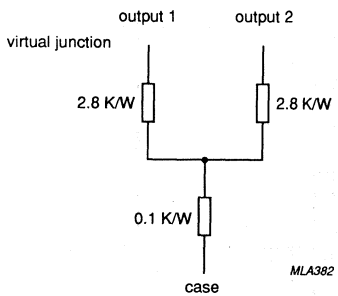


Fig.3 Thermal resistance.

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient in free air	40 K/W
$R_{th\ j\text{-}c}$	from junction to case (see Figs 3 and 4)	1.5 K/W

2 x 22 W stereo BTL differential amplifier with speaker protection and dynamic distortion detector

TDA1556Q

FUNCTIONAL DESCRIPTION

The TDA1556Q contains two identical amplifiers each with a fixed gain of 26 dB and differential input stages. The device can be used for bridge-tied-load applications. The circuit has the following features:

- low stand-by current (< 100 μA)
- low mute/stand-by switching current (low cost supply switch)
- mute facility

Loudspeaker protection

Should a short circuit to ground occur, thereby forcing a DC voltage ≥ 1 V across the loudspeaker, a built-in protection circuit is activated to limit the DC voltage across the speaker to ≤ 1 V. The delay time of the protection circuit can be influenced by an external capacitor connected to pin 15.

A dynamic distortion detector (DDD) is activated when clipping occurs at one or both output stages. Its information may be used to operate a sound processor or DC volume control to attenuate the input signal, thereby minimizing the distortion.

LIMITING VALUES

In accordance with the absolute maximum system (IEC 134)

SYMBOL	PARAMETER	CONDITION	MIN.	MAX.	UNIT
V_P	positive supply voltage				
		operating	–	18	V
		non-operating	–	30	V
		during 50 ms (load dump protection); rise time ≥ 2.5 ms	–	45	V
I_{OSM}	non-repetitive peak output current		–	6	A
I_{ORM}	repetitive peak output current		–	4	A
T_{stg}	storage temperature range		−55	+150	°C
T_{vj}	virtual junction temperature		–	+150	°C
V_{psc}	AC and DC short-circuit safe voltage		–	18	V
	energy handling capability at outputs	$V_P = 0$	–	200	mJ
V_{pr}	reverse polarity		–	6	V
P_{tot}	total power dissipation		–	60	W

DC CHARACTERISTICS

V_P = 14.4 V; T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_P	positive supply voltage	note 1	6.0	14.4	18	V
I_P	quiescent current		–	80	160	mA
V_O	DC output voltage	note 2	–	6.9	–	V
V_{os}	DC output offset voltage	operating	–	–	100	mV
Mute/stand-by						
V_{ON}	switch-on voltage level		8.5	–	–	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
MUTE CONDITION						
V_{mute}	mute voltage		3.3	–	6.4	V
V_O	output signal in mute position	$V_{I\ max}$ = 1 V; f = 1 kHz	–	–	2	mV
V_{os}	DC output offset voltage		–	–	100	mV
STANDBY CONDITION						
V_{sb}	stand-by voltage		0	–	2	V
I_{sb}	DC standby current	V_{14} < 0.5 V	–	–	100	µA
		0.5 V ≤ V_{14} ≤ 2.0 V	–	–	500	µA
I_{sw}	switch-on current		–	25	60	µA
I_{PSC}	supply current	short-circuit to ground; note 3	–	10	–	mA
Loudspeaker protection						
$\lvert\Delta V_{6\text{-}8,\ 10\text{-}12}\rvert$	DC voltage across R_L		–	–	1.0	V
t_d	delay time		–	0.5	–	s
Protection active ($\lvert\Delta V_{4\text{-}6}\rvert$ or $\lvert\Delta V_{7\text{-}9}\rvert \leq 1.0$ V						
I_{15}	current information		–	25	–	µA
V_{15}	voltage information		3.6	–	–	V
Protection inactive ($\lvert\Delta V_{6\text{-}8}\rvert$ and $\lvert\Delta V_{10\text{-}12}\rvert \leq 0.1$ V)						
V_{15}	voltage information		–	–	0.3	V

Notes to the DC characteristics

1. The circuit is DC adjusted at V_P = 6 to 18 V and AC operating at V_P = 8.5 to 18 V
2. At 18 V < V_P < 30 V the DC output voltage ≤ $V_P/2$
3. Conditions: V_{14} = 0 V; short-circuit to ground; switch V_{14} to MUTE or ON condition, rise time at V_{14} = ≥ 10 µs
4. Frequency response externally fixed
5. Ripple rejection measured at the output with a source-impedance of 0 Ω (maximum ripple amplitude of 2 V) and a frequency between 100 Hz and 10 kHz
6. Mismatching is given by the following equation:

$$\lvert\Delta Z_i\rvert = \frac{Z_{i1} - Z_{i2}}{Z_{i1}} \times 100\%$$

$$\lvert\Delta Z_i\rvert = \frac{Z_{i3} - Z_{i4}}{Z_{i3}} \times 100\%$$

7. Noise measured in a bandwidth of 20 Hz to 20 kHz
8. Noise output voltage independent of R_S (V_I = 0 V)
9. Common mode rejection ratio measured at the output with both inputs tied together. $V_{I(RMS)}$ < 3.5 V; f = 100 Hz - 10 kHz

AC CHARACTERISTICS

V_P = 14.4 V; R_L = 4 Ω; f = 1 kHz; T_{amb} = 25 °C; unless otherwise specified

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
P_O	output power	THD = 0.5%	15	17	–	W
		THD = 10%	20	22	–	W
		THD = 0.5%; V_p = 13.2 V	–	12	–	W
		THD = 10%; V_p = 13.2 V	–	17	–	W
THD	total harmonic distortion	P_O = 1 W	–	0.1	–	%
B	power bandwidth	THD = 0.5%; P_O = −1 dB; with respect to 15 W	–	20 to 15000	–	Hz
f_l	low frequency roll-off	−1 dB; note 4	–	25	–	Hz
f_h	high frequency roll-off	−1 dB	20	–	–	kHz
G_v	closed loop voltage gain		25	26	27	dB
SVRR	supply voltage ripple rejection	note 5				
		ON condition	48	–	–	dB
		MUTE condition	48	–	–	dB
		stand-by condition	80	–	–	dB
$\|Z_I\|$	input impedance		100	120	150	kΩ
$\|\Delta Z_I\|$	input impedance	note 6	–	4	–	%
V_{no}	noise output voltage	ON: R_S = 0 Ω; note 7	–	70	120	μV
		ON: R_S = 10 kΩ; note 7	–	100	–	μV
		MUTE: R_S = 10 kΩ; notes 7 and 8	–	60	–	μV
α	channel separation	R_S = 10 kΩ	40	–	–	dB
ΔG_v	channel unbalance		–	–	1	dB
CMRR	common mode rejection ratio	note 9	64	72	–	dB
THD	total harmonic distortion	I_{DDD} = 50 μA (peak)	–	3.5	–	%

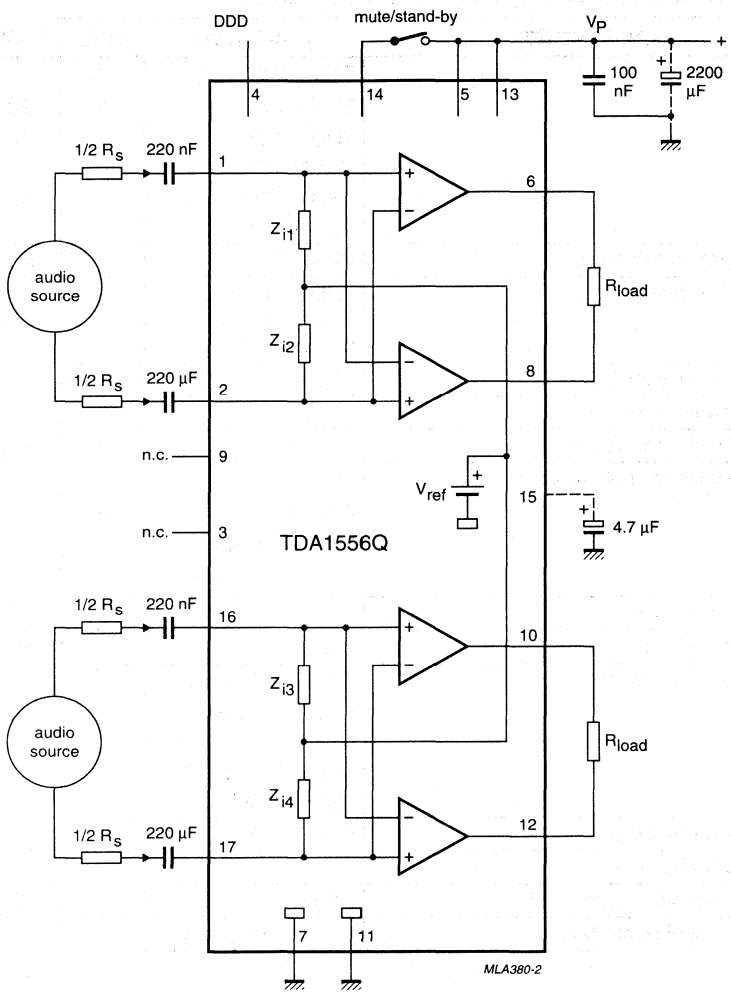


Fig.4 Stereo BTL test diagram.

2 x 22 W BTL stereo car radio power amplifier with speaker protection

TDA1557Q

FEATURES

- Requires very few external components
- High output power
- Low offset voltage at output
- Fixed gain
- Good ripple rejection
- Mute/stand-by switch
- Load dump protection
- AC and DC short-circuit-safe to ground and V_P
- Thermally protected
- Reverse polarity safe
- Capability to handle high energy on outputs (V_P = 0)
- Protected against electrostatic discharge
- No switch-on/switch-off plop
- Flexible leads
- Low thermal resistance.

GENERAL DESCRIPTION

The TDA1557Q is a monolithic integrated class-B output amplifier in a 13-lead single-in-line (SIL) plastic power package. The device contains 2 x 22 W amplifiers in BTL configuration and has been primarily developed for car radio applications.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	positive supply voltage range					
		operating	6.0	14.4	18	V
		non-operating	–	–	30	V
		load dump	–	–	45	V
IORM	repetitive peak output current		–	–	4	A
I_{tot}	total quiescent current		–	80	–	mA
I_{sb}	stand-by current		–	0.1	100	μA
I_{sw}	switch-on current		–	–	60	μA
$\|Z_I\|$	input impedance		25	–	–	kΩ
T_{XTAL}	crystal temperature		–	–	+150	°C
Stereo application						
P_O	output power	THD = 10%; 4 Ω	–	22	–	W
SVRR	supply voltage ripple rejection	R_S = 0; f = 100 Hz to 10 kHz	45	–	–	dB
$\|\Delta V_O\|$	DC output offset voltage		–	–	250	mV
α	channel separation		40	–	–	dB
$\|\Delta G_v\|$	channel unbalance		–	–	1	dB
G_v	closed loop voltage gain		45	46	47	dB

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA1557Q	13	DIL	plastic	SOT141R

2 x 22 W BTL stereo car radio power amplifier with speaker protection

TDA1557Q

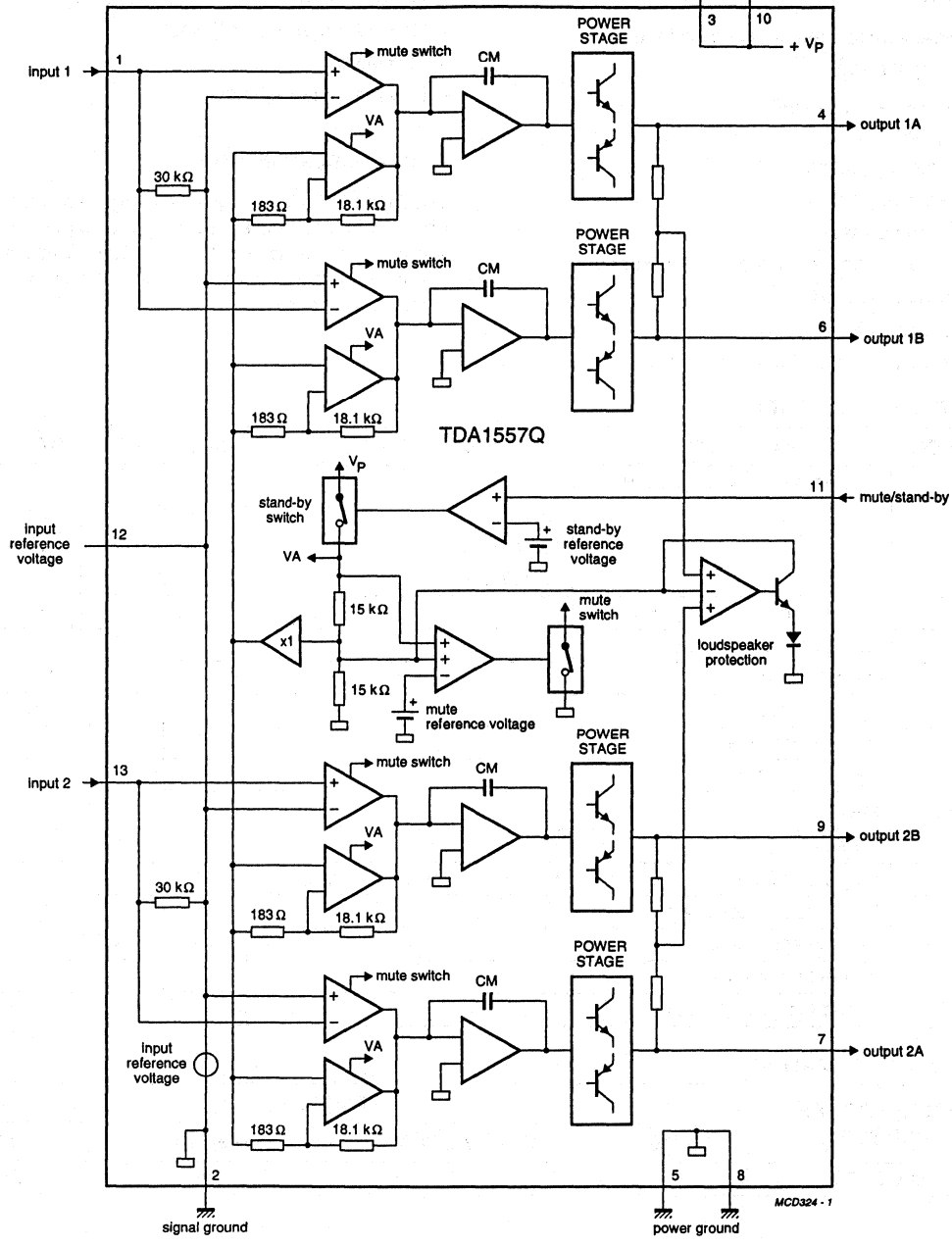


Fig.1 Block diagram.

2 x 22 W BTL stereo car radio power amplifier with speaker protection

TDA1557Q

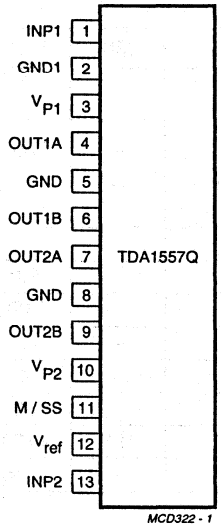


Fig.2 Pin configuration.

PINNING

SYMBOL	PIN	DESCRIPTION
INP1	1	input 1
GND1	2	ground (signal)
V_{P1}	3	supply voltage 1
OUT1A	4	output 1A
GND	5	power ground 1
OUT1B	6	output 1B
OUT2A	7	output 2A
GND	8	power ground 2
OUT2B	9	output 2B
V_{P2}	10	supply voltage 2
M/SS	11	mute/stand-by switch
V_{ref}	12	input reference voltage
INP2	13	input 2

FUNCTIONAL DESCRIPTION

The TDA1557Q contains two identical amplifiers with differential input stages, and can be used for bridge applications. The gain of each amplifier is fixed at 46 dB. Special features of this device are:

a. mute/stand-by switch

low stand-by current

low mute/stand-by switching current (low cost supply switch)

mute facility

b. loudspeaker protection

when a short circuit to ground is made, which forces a DC voltage of ≥ 1 V across the loudspeaker, a built-in protection circuit becomes active and limits the DC voltage across the loudspeaker to ≤ 1 V

c. the harmonic distortion at low frequencies can be decreased by connecting two diodes to ground at pin 12.

LIMITING VALUES

In accordance with the Absolute maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_P	positive supply voltage				
		operating	–	18	V
		non-operating	–	30	V
		load dump protected; during 50 ms; rise time ≥ 2.5 ms	–	45	V
V_{PSC}	AC and DC short-circuit safe voltage		–	18	V
V_{PR}	reverse polarity		–	6.0	V
	energy handling capability at outputs	$V_P = 0$	–	200	mJ
IOSM	non-repetitive peak output current		–	6	A
IORM	repetitive peak output current		–	4	A
P_{tot}	total power dissipation		–	60	W
T_{stg}	storage temperature range		−55	+150	°C
Tj	junction temperature		–	+150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ vj\text{-}a}$	from virtual junction to ambient in free air	40 K/W
$R_{th\ vj\text{-}c}$	from virtual junction to case (see Fig.3)	1.5 K/W

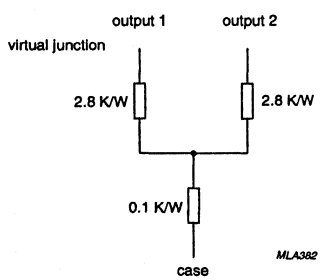


Fig.3 Equivalent thermal resistance network.

DC CHARACTERISTICS

V_P = 14.4 V, T_{amb} = 25 °C, unless otherwise specified. See note 1.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_P	positive supply voltage range	note 2	6.0	14.4	18	V
I_P	quiescent current		–	80	160	mA
V_O	DC output voltage	note 3	–	6.9	–	V
$\lvert\Delta V_{os}\rvert$	DC output offset voltage		–	–	250	mV
Mute/stand-by switch						
V_{sw}	switch-on voltage level		8.5	–	–	V
MUTE CONDITION						
V_{mute}	mute voltage		3.3	–	6.4	V
V_O	output signal in mute position	V_I = 1 V max; f = 1 kHz	–	–	20	mV
$\lvert\Delta V_{os}\rvert$	DC output offset voltage		–	–	250	mV
STAND-BY CONDITION						
V_{sb}	stand-by voltage		0	–	2.0	V
I_{sb}	DC current in stand-by condition	$V_{11} \leq 0.5$ V	–	–	100	µA
		$0.5 < V_{11} \leq 2$ V	–	–	500	µA
I_{sw}	switch-on current		–	30	60	µA
I_P	positive supply current	short-circuit to GND; note 4	–	5.5	–	mA
Loudspeaker protection						
$\lvert\Delta V_{4\text{-}6,\ 7\text{-}9}\rvert$	DC voltage across R_L		–	–	1.0	V

AC CHARACTERISTICS

V_P = 14.4 V; R_L = 4 Ω; f = 1 kHz; T_{amb} = 25 °C; unless otherwise specified. See note 1.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
P_O	output power					
		THD = 0.5%	15	17	–	W
		THD = 10%	20	22	–	W
		V_P = 13.2 V; THD = 0.5%	–	12	–	W
		V_P = 13.2 V; THD = 10%	–	17	–	W
THD	total harmonic distortion	P_O = 1 W	–	0.1	–	%
B	power bandwidth	THD = 0.5%; P_O = −1 dB with respect to 15 W	–	20 to 15 000	–	Hz
f_{low}	low frequency roll-off	−1 dB; note 5	–	25	–	Hz
f_{high}	high frequency roll-off	−1 dB	20	–	–	kHz
G_v	closed loop voltage gain		45	46	47	dB
SVRR	supply voltage ripple rejection					
		ON; note 6	34	–	–	dB
		ON; note 7	38	–	–	dB
		ON; note 8	45	–	–	dB
		MUTE; notes 6 and 7	45	–	–	dB
		stand-by; notes 6 and 7	80	–	–	dB
$\|Z_I\|$	input impedance		25	30	36	kΩ
V_{no}	noise output voltage					
		ON; R_S = 0; note 9	–	325	500	μV
		R_S = 10 kΩ; note 9	–	350	–	μV
		MUTE; notes 9 & 10	–	180	–	μV
α	channel separation		40	–	–	dB
$\|\Delta G_v\|$	channel unbalance		–	–	1	dB

Notes to the characteristics

1. All characteristics are measured using the circuit shown in Fig.4
2. The circuit is DC adjusted at V_P = 6 to 18 V and AC operating at V_P = 8.5 to 18 V
3. At 18 V < V_P < 30 V, the DC output voltage ≤ V_P/2
4. Conditions: V_{11} = 0; short-circuit output to GND; switch V_{11} to MUTE or ON condition (rise time V_{11} > 10 μs).
5. Frequency response externally fixed.
6. Ripple rejection measured at the output with a source-impedance of 0 Ω (max. ripple amplitude of 2 V) and a frequency of 100 Hz.
7. Ripple rejection measured at the output with a source-impedance of 0 Ω (max. ripple amplitude of 2 V) and a frequency between 1 and 10 kHz.
8. Ripple rejection measured at the output with a source-impedance of 0 Ω (max. ripple amplitude of 2 V) and a frequency between 100 Hz and 10 kHz. Pin 12 is decoupled with two diodes to ground.
9. Noise voltage measured in a bandwidth of 20 Hz to 20 kHz.
10. Noise output voltage independent of R_S (V_{in} = 0).

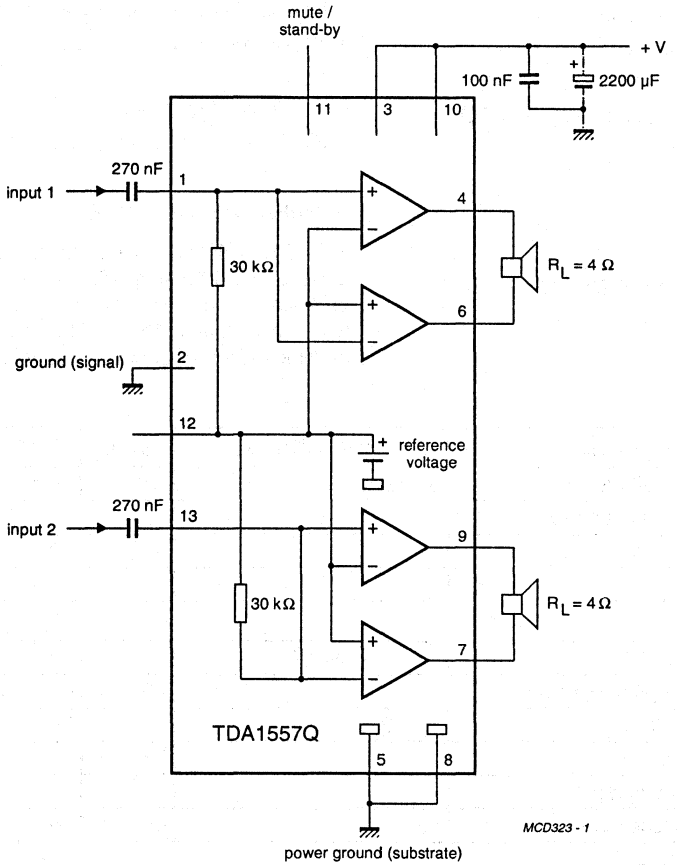


Fig.4 Stereo BTL application.

2 x 22 W or 4 x 11 W single-ended car radio power amplifier

TDA1558Q

FEATURES

- Requires very few external components
- Flexibility in use Quad single-ended or stereo BTL
- High output power
- Low offset voltage at output (important for BTL)
- Fixed gain
- Good ripple rejection
- Mute/stand-by switch
- Load dump protection
- AC and DC short-circuit-safe to ground and V_P
- Thermally protected
- Reverse polarity safe
- Capability to handle high energy on outputs (V_P = 0)
- Protected against electrostatic discharge
- No switch-on/switch-off plop
- Flexible leads
- Low thermal resistance
- Identical inputs (inverting and non-inverting).

GENERAL DESCRIPTION

The TDA1558Q is a monolithic integrated class-B output amplifier in a 17-lead single-in-line (SIL) plastic power package. The device contains 4 x 11 W single-ended or 2 x 22 W BTL amplifiers and has been primarily developed for car radio applications.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	positive supply voltage range	operating	6.0	14.4	18	V
I_{ORM}	repetitive peak output current		–	–	4	A
I_{tot}	total quiescent current		–	80	–	mA
I_{sb}	stand-by current		–	0.1	100	μA
Stereo BTL application						
P_O	output power	THD = 10%; 4 Ω	–	22	–	W
SVRR	supply voltage ripple rejection		45	–	–	dB
V_{no}	noise output voltage	R_S = 0	–	200	–	μV
$\|Z_I\|$	input impedance		25	–	–	kΩ
$\|\Delta V_{os}\|$	DC output offset voltage		–	–	250	mV
G_v	closed loop voltage gain		45	46	47	dB
Quad single-ended application						
P_O	output power	THD = 10%; 4 Ω	–	6	–	W
		THD = 10%; 2 Ω	–	11	–	W
SVRR	supply voltage ripple rejection		44	–	–	dB
V_{no}	noise output voltage	R_S = 0	–	150	–	μV
$\|Z_I\|$	input impedance		50	–	–	kΩ
G_v	closed loop voltage gain		39	40	41	dB

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA1558Q	17	DIL	plastic	SOT243R

2 x 22 W or 4 x 11 W single-ended car radio power amplifier

TDA1558Q

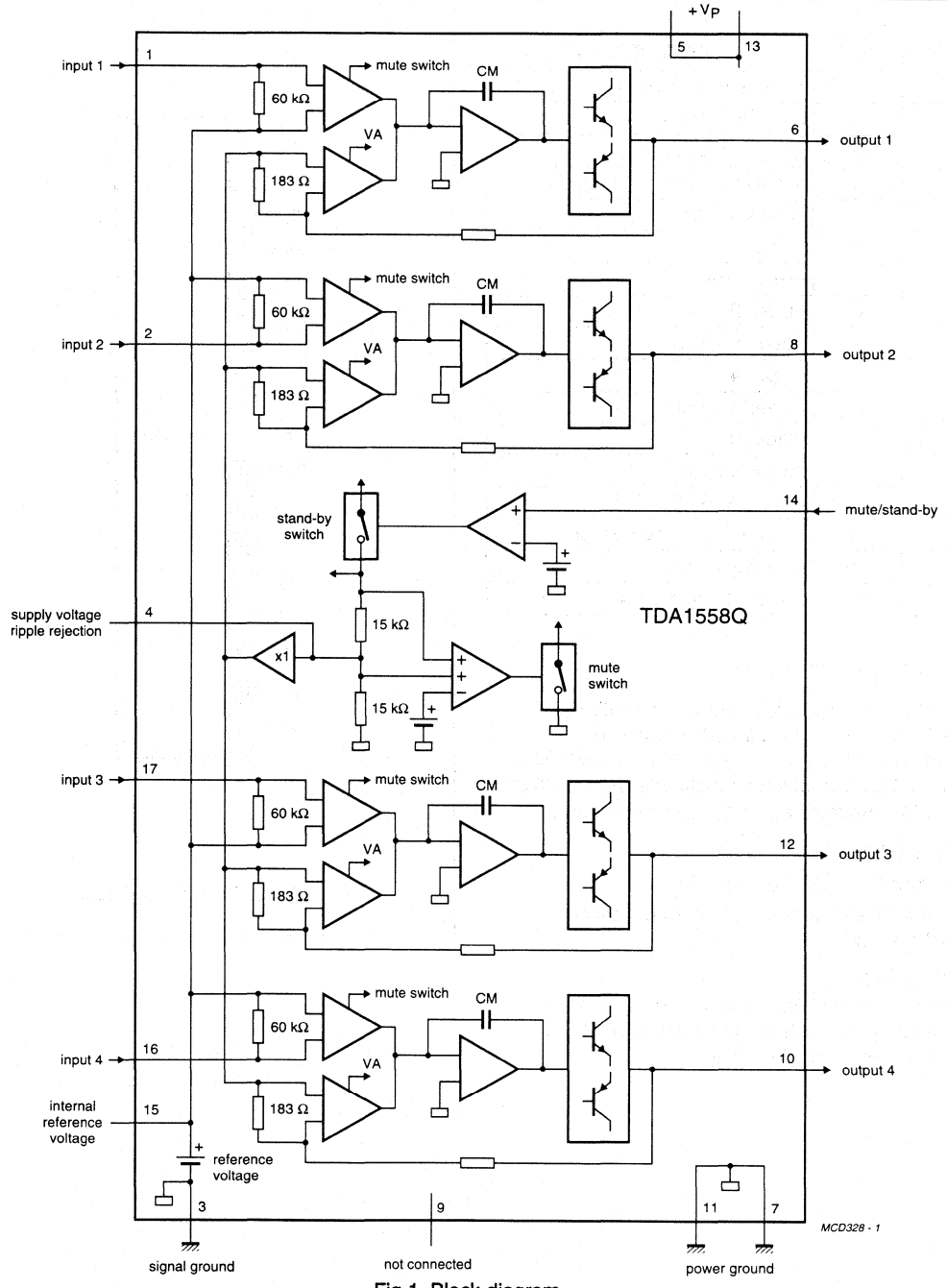


Fig.1 Block diagram.

2 x 22 W or 4 x 11 W single-ended car radio power amplifier

TDA1558Q

PINNING

SYMBOL	PIN	DESCRIPTION
–INV1	1	non-inverting input 1
INV2	2	inverting input 2
GND	3	ground (signal)
SVRR	4	supply voltage ripple rejection
V_{P1}	5	supply voltage
OUT1	6	output 1
GND1	7	power ground 1
OUT2	8	output 2
n.c.	9	not connected
OUT4	10	output 4
GND2	11	power ground 2
OUT3	12	output 3
V_{P2}	13	supply voltage
M/SS	14	mute/stand-by switch
V_{ref}	15	internal reference voltage
INV3	16	inverting input 3
–INV4	17	non-inverting input 4

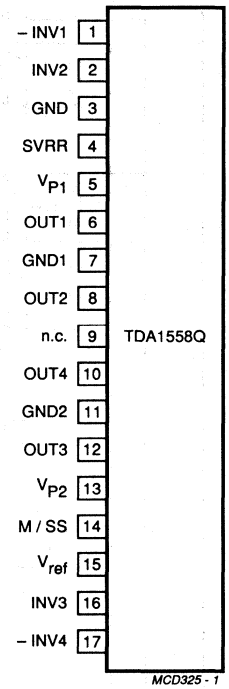


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The TDA1558Q contains four identical amplifiers with differential input stages (two inverting and two non-inverting), and can be used for single-ended or BTL applications. The gain of each amplifier is fixed at 40 dB (46 dB in BTL). Special features of this device are:

a. mute/stand-by switch

   low stand-by current (< 100 μA)

   low mute/stand-by switching current (low cost supply switch)

   mute facility.

b. the harmonic distortion at low frequencies can be decreased by connecting two diodes at pin 15 to ground or a zener diode of 1.5 V.

LIMITING VALUES

In accordance with the Absolute maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_P	positive supply voltage				
		operating	–	18	V
		non-operating	–	30	V
		load dump protected; during 50 ms; rise time ≥ 2.5 ms	–	45	V
V_{PSC}	AC and DC short-circuit safe voltage		–	18	V
V_{PR}	reverse polarity		–	6	V
	energy handling capability at outputs	$V_P = 0$	–	200	mJ
I_{OSM}	non-repetitive peak output current		–	6	A
I_{ORM}	repetitive peak output current		–	4	A
P_{tot}	total power dissipation		–	60	W
T_{stg}	storage temperature range		–55	+150	°C
T_j	junction temperature		–	+150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ vj\text{-}a}$	from virtual junction to ambient in free air	40 K/W
$R_{th\ vj\text{-}c}$	from virtual junction to case (see Fig.3)	1.5 K/W

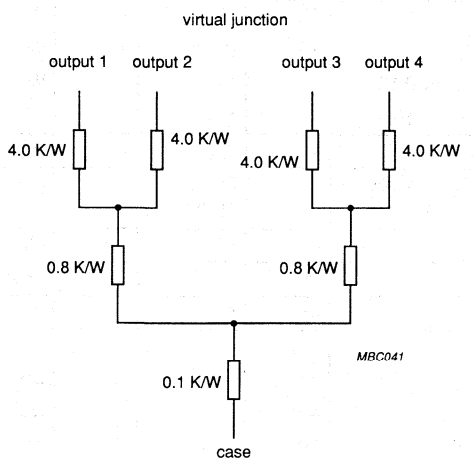


Fig.3 Equivalent thermal resistance network.

DC CHARACTERISTICS

V_P = 14.4 V, T_{amb} = 25 °C, unless otherwise specified. See note 1.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_P	positive supply voltage range	note 2	6.0	14.4	18	V
I_P	quiescent current		–	80	160	mA
V_O	DC output voltage	note 3	–	6.9	–	V
$\lvert\Delta V_{os}\rvert$	DC output offset voltage		–	–	250	mV
Mute/stand-by switch						
V_{ON}	switch-on voltage level		8.5	–	–	V
MUTE CONDITION						
V_{mute}	mute voltage		3.3	–	6.4	V
V_O	output signal in mute position	V_I = 1 V (max); f = 1 kHz	–	–	20	mV
$\lvert\Delta V_{os}\rvert$	DC output offset voltage	between pins 6-8 and pins 10-12	–	–	250	mV
STAND-BY CONDITION						
V_{sb}	stand-by voltage		0	–	2	V
I_{sb}	DC current in stand-by condition		–	–	100	µA
I_{sw}	switch-on current		–	12	40	µA

AC CHARACTERISTICS

V_P = 14.4 V, R_L = 4 Ω, f = 1 kHz, T_{amb} = 25 °C, unless otherwise specified. See note 1.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
P_O	output power	THD = 0.5%	15	17	–	W
		THD = 10%	20	22	–	W
		V_P = 13.2 V; THD = 0.5%	–	12	–	W
		V_P = 13.2 V; THD = 10%	–	17	–	W
THD	total harmonic distortion	P_O = 1 W	–	0.1	–	%
B	power bandwidth	THD = 0.5%; P_O = −1 dB with respect to 15 W	–	20 to 15 000	–	Hz
f_{low}	low frequency roll-off	−1 dB; note 4	–	45	–	Hz
f_{high}	high frequency roll-off	−1 dB	20	–	–	kHz
G_v	closed loop voltage gain		45	46	47	dB
SVRR	supply voltage ripple rejection					
		ON; note 5	45	–	–	dB
		MUTE; note 5	45	–	–	dB
		stand-by; note 5	80	–	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$\|Z_I\|$	input impedance		25	30	38	kΩ
V_{no}	noise output voltage					
		ON; R_S = 0; note 6	–	200	300	μV
		R_S = 10 kΩ; note 6	–	350	–	μV
		MUTE; notes 6 and 7	–	180	–	μV
α	channel separation	R_S = 10 kΩ	40	–	–	dB
$\|\Delta G_v\|$	channel unbalance		–	–	1	dB
Quad single-ended application (see Fig.5)						
P_O	output power	note 8				
		THD = 0.5%	4	5	–	W
		THD = 10%	5.5	6	–	W
		R_L = 2 Ω; THD = 0.5%	7.5	8.5	–	W
		R_L = 2 Ω; THD = 10%	10	11	–	W
THD	total harmonic distortion	P_O = 1 W	–	0.1	–	%
f_{low}	low frequency roll-off	–3 dB; note 4	–	45	–	Hz
f_{high}	high frequency roll-off	–1 dB	20	–	–	kHz
G_v	closed loop voltage gain		39	40	41	dB
SVRR	supply voltage ripple rejection	note 5				
		ON	44	–	–	dB
		MUTE	44	–	–	dB
		stand-by	80	–	–	dB
$\|Z_I\|$	input impedance		50	60	75	kΩ
V_{no}	noise output voltage					
		ON; R_S = 0; note 6	–	150	230	μV
		R_S = 10 kΩ; note 6	–	250	–	μV
		MUTE; notes 6 and 7	–	120	–	μV
α	channel separation	R_S = 10 kΩ	40	–	–	dB
$\|\Delta G_v\|$	channel unbalance		–	–	1	dB

Notes to the characteristics

1. All characteristics are measured using the circuit shown in Fig.4
2. The circuit is DC adjusted at V_P = 6 to 18 V and AC operating at V_P = 8.5 to 18 V.
3. At 18 V < V_P < 30 V, the DC output voltage ≤ V_P/2.
4. Frequency response externally fixed.
5. Ripple rejection measured at the output with a source-impedance of 0 Ω (max. ripple amplitude of 2 V) and a frequency between 100 Hz and 10 kHz.
6. Noise voltage measured in a bandwidth of 20 Hz to 20 kHz.
7. Noise output voltage independent of R_S (V_{in} = 0).
8. Output power is measured directly at the output pins of the IC.

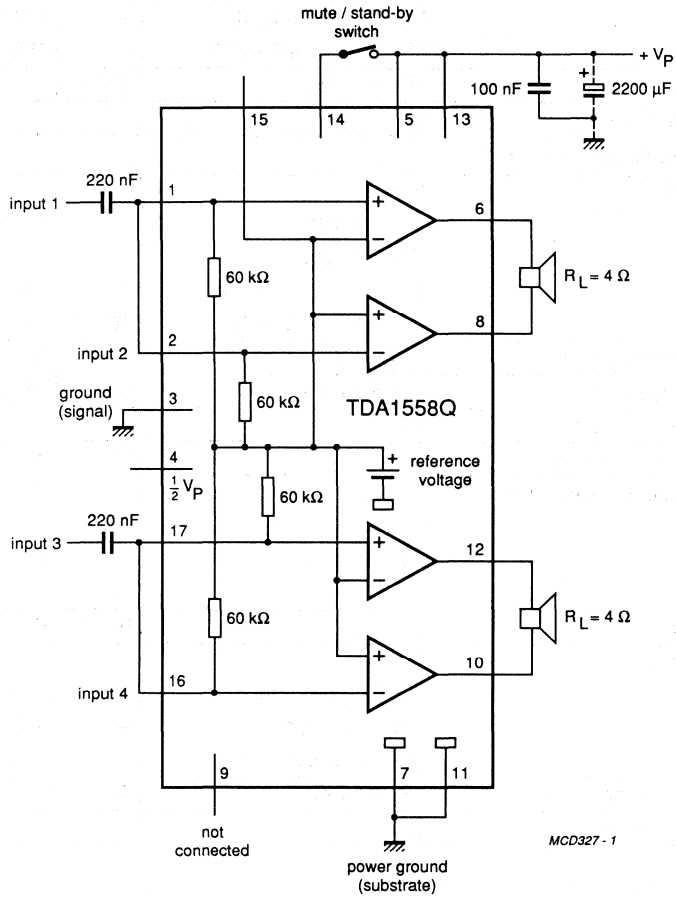


Fig.4 Stereo BTL application.

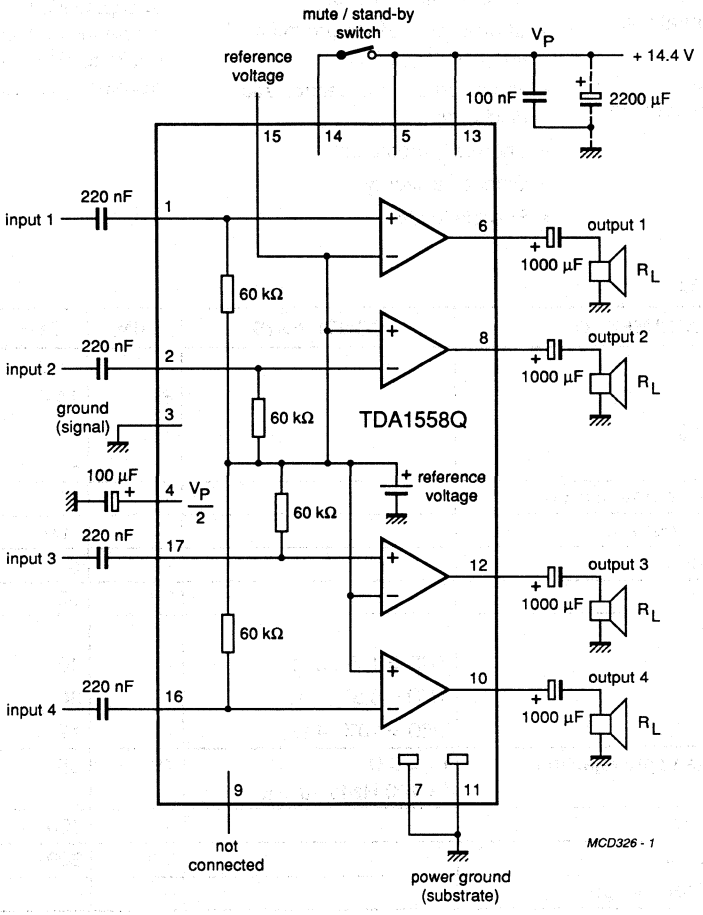


Fig.5 Quad single-ended application.

40 W car radio high power amplifier TDA1560Q

FEATURES

- Very high output power
- Low power dissipation when used for music signals
- Switches to low output power in the event of excessive heatsink temperatures
- Output power and power dissipation limited in the event of small load resistances
- Requires few external components
- Fixed gain
- Low cross-over distortion
- No switch-on/switch-off plops
- Mode select switch
- Low offset voltage at the output
- Load dump protection
- Short-circuit safe to ground or V_P and across the load
- Protected against electrostatic discharge
- Thermally protected
- Diagnostic facility
- Flexible leads.

GENERAL DESCRIPTION

The TDA1560Q is an integrated BTL class-H high power amplifier. In a load of 8 Ω, the output power is 40 W typical at a THD of 10%. The encapsulation is a 17-lead single-in-line (SIL) plastic power package. The device is primarily developed for car radio applications.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage					
	operating		8	14.4	18	V
	non-operating		–	–	30	V
	load dump		–	–	45	V
I_{ORM}	repetitive peak output current		–	–	4	A
I_P	total quiescent current		–	100	160	mA
I_{sb}	standby current		–	5	50	μA
G_v	voltage gain		29	30	31	dB
P_o	output power					
		THD = 10%; 8 Ω	–	40	–	W
		THD = 0.5%; 8 Ω	–	30	–	W
		THD = 10%; 4 Ω	–	17	–	W
SVRR	supply voltage ripple rejection	R_S = 0 Ω; f = 100 Hz to 10 kHz	48	55	–	dB
V_{no}	noise output voltage		–	100	300	μV
$\|Z_I\|$	input impedance		180	300	–	kΩ
$\|\Delta V_o\|$	DC output offset voltage		–	–	150	mV

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA1560Q	17	DBS	plastic	SOT243R

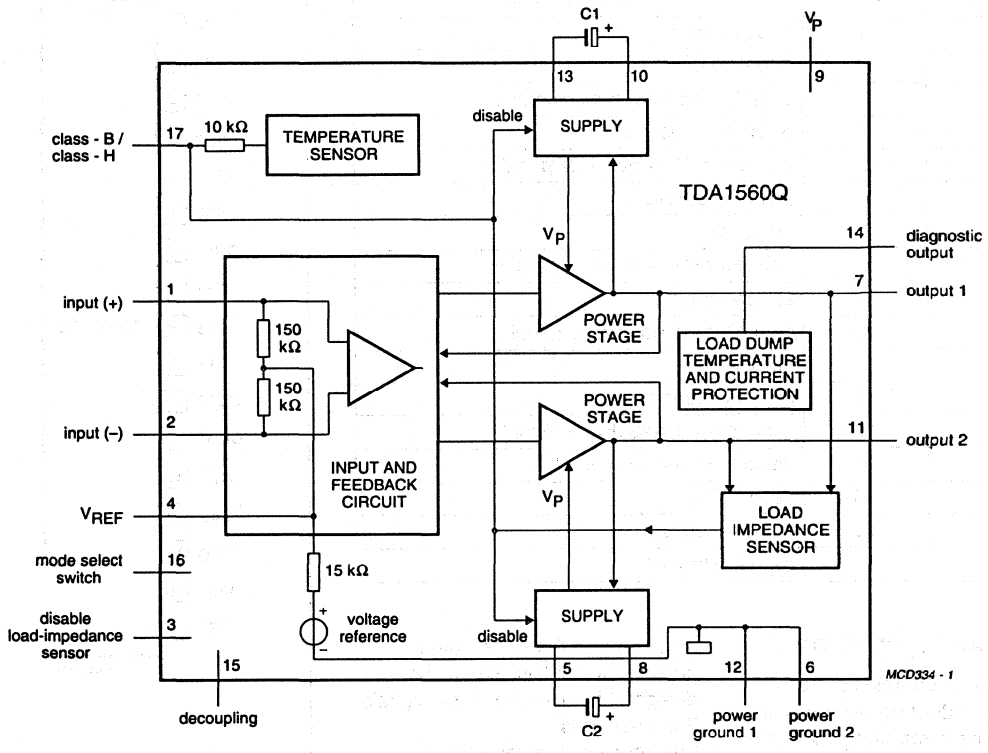


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
+INP	1	positive input
–INP	2	negative input
DLS	3	disable load-impedance sensor
V_{REF}	4	reference voltage
C2–	5	capacitor C2 negative terminal
GND2	6	power ground 2
OUT1	7	output 1
C2+	8	capacitor C2 positive terminal
V_P	9	supply voltage
C1+	10	capacitor C1 positive terminal
OUT2	11	output 2
GND1	12	power ground 1
C1–	13	capacitor C1 negative terminal
V_{DIAG}	14	diagnostic voltage output
C_{DEC}	15	decoupling
MSS	16	mode select switch
S1	17	class-B/class-H

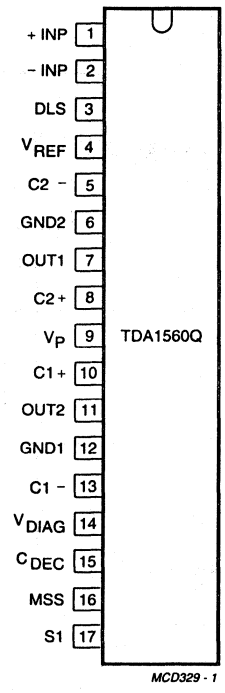


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The TDA1560Q contains a mono class-H BTL output power amplifier. At low output power, up to 10 W, the device operates as a normal BTL amplifier. When a larger output voltage swing is required, the internal supply voltage is lifted to approximately twice the external supply voltage. This extra supply voltage is obtained from the charge in the external electrolytic capacitors. Due to this momentarily higher supply voltage, the maximum output power is 40 W typical at a THD of 10%.

In normal use, when the output is driven with music-like signals, the high output power is only required for a small percentage of the time. Assuming a music signal has a normal (Gaussian) amplitude distribution, the reduction in dissipation is approximately 50% when compared to a class-B output amplifier with the same output power. The heatsink should be designed for use with music signals. If the device is **continuous sinewave** driven, instead of driven with music signals and at a high output power (class-H operation), the case temperature can rise above 120 °C with such a practical heatsink. In this event, the thermal protection disables the high power supply voltage and limits the output power to 10 W and the maximum dissipation to 5 W.

The gain of the amplifier is internally fixed at 30 dB. With the mode select switch pin, the device can be switched to the following modes:

- low standby current (< 50 μA)
- mute condition, DC adjusted
- on, operation in class-B, limited output power
- on, operation in class-H, high output power.

The mode select switch pin can be directly switched from standby to class-H without plops or clicks. A delay in mute condition is not necessary. (This is valid only if in the application capacitor C5 at pin 4 is connected and the load-impedance sensor is enabled, see Fig.6.

The device can be used as a normal BTL class-AB amplifier if the electrolytic capacitors C1 and C2 are omitted; see Fig.6. If the case temperature exceeds 120 °C, the device will switch back from class-H to class-B operation. The high power supply voltage is then disabled and the output power is

limited to 10 W. By measuring the voltage on the class-B/class-H pin, the actual crystal temperature can be detected. The open voltage on the class-B/class-H pin is related to the global temperature of the crystal. By measuring this voltage, external actions can be taken to reduce an excessive temperature (e.g. by cutting off low frequencies or externally switching to class-B). For the relationship between the crystal temperature and the voltage on this pin, see Fig.3.

By forcing a high voltage level on the class-B/class-H pin, thereby simulating a high temperature, the device can be externally switched to class-B operation. Similarly, by forcing a low voltage level on the class-B/class-H pin, thereby simulating a low temperature, the device can be forced into class-H operation, even if the case temperature exceeds 120 °C.

The device is fully protected against short-circuiting the outputs to ground or V_P and across the load, high crystal temperature and electrostatic discharge at all input and output pins. In the event of a continuing short-circuit to ground or V_P, excessive dissipation is prevented because the output stages will be switched off. The output stages will be switched on again within 20 ms after the short-circuit is removed.

Furthermore a load-impedance sensor is available. When a 4 Ω loudspeaker is connected instead of the normal 8 Ω, the power in the loudspeaker is limited, to prevent damage to it.

Each time the device is switched from standby condition to mute condition, the DC resistance between the output terminals is measured. If this load is 4 Ω (DC), the high voltage supply is disabled and only class-B operation is possible. If the DC load is more than 6 Ω, class-H operation is possible. If the load is less than 0.5 Ω (a short-circuited load), the output stages remain disabled and high dissipation is prevented.

The load-impedance sensor can be disabled by connecting pin 3 to ground. In that event the class-H operation is always possible (up to case temperature of 120 °C) and a short-circuited load is not detected before switching on. The load-impedance sensor is active if pin 3 is floating.

The load-impedance sensor can only operate reliably if any interference voltage at the moment of switching from standby to mute, due to external causes, is less than 1 mV between the pins 7 and 11.

A diagnostic facility is available at pin 14. In normal conditions the voltage at this pin will be the supply voltage (V_P). In the event of the following conditions:

- junction temperature exceeds 150 °C
- short-circuit of one of the outputs to ground or to V_P
- load dump; $V_P > 20$ V

The voltage level at pin 14 will be at a constant level of approximately $V_P/2$ during the fault condition. At a short-circuit over the load, pin 14 will be at $V_P/2$ for approximately 20 ms and V_P for approximately 50 µs.

Heatsink design

There are two parameters that determine the size of the heatsink. The first is the rating for the case temperature, the second the ambient temperature at which the amplifier must still deliver its full power in the class-H mode.

Example 1.

With an 8 Ω load and driven with a **music signal**, the maximum power dissipation is approximately 6.5 W. If the amplifier is to deliver its full power at ambient temperatures up to 50 °C the case temperature should not be higher than 120 °C for class-H operation.
The $R_{th\ case\_hs}$ = 1 K/W, thus the external heatsink should be:

$$\frac{(120 - 50)}{6.5} - 1 = 10 \text{ K/W}.$$

In this example and with an 8 Ω load, the size of the heatsink is determined by the rating for the maximum full power ambient temperature. If the case temperature of the device exceeds 120 °C then the device switches back to class-B, see Example 2.

Example 2.

With disabled class-H mode, an 8 Ω load and driven with a **sinewave signal** the maximum power dissipation is approximately 5 W. At a virtual junction temperature of 150 °C and T_{amb_max} = 60 °C, $R_{th\ vj\text{-}case}$ = 3 K/W and $R_{th\ case\_hs}$ = 1 K/W, the thermal resistance of the heatsink should be:

$$\frac{(150 - 60)}{5} - 3 - 1 = 14 \text{ K/W}.$$

In this example the size of the heatsink is determined by the virtual junction temperature.

Example 3.

With disabled class-H mode, a 4 Ω load and driven with a **sinewave signal** the maximum power dissipation is approximately 10 W. At a virtual junction temperature of 150 °C and T_{amb_max} = 60 °C, $R_{th\ vj\text{-}case}$ = 3 K/W and $R_{th\ case\_hs}$ = 1 K/W, the thermal resistance of the heatsink should be:

$$\frac{(150 - 60)}{10} - 3 - 1 = 5 \text{ K/W}.$$

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_P	supply voltage				
	operating		–	18	V
	non-operating		–	30	V
	load dump protected	during 50 ms; t_r > 2.5 ms	–	45	V
I_{OSM}	non-repetitive peak output current		–	6	A
I_{ORM}	repetitive peak output current		–	4	A
V_{PSC}	AC and DC short-circuit safe voltage		–	18	V
	energy handling capability at outputs	V_P = 0	–	200	mJ
I_{17}	current in pin 17	$V_{17} < V_P - 1$	–	5	mA
P_{tot}	total power dissipation		–	60	W
T_{stg}	storage temperature		–55	+150	°C
T_{amb}	operating ambient temperature		–40	–	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient in free air	40 K/W
$R_{th\ j\text{-}c}$	from junction to case (note 1)	3 K/W

Note

1. Measured in Fig.6.

DC CHARACTERISTICS

V_P = 14.4 V; R_L = 8 Ω; T_{amb} = 25 °C and using heatsink 4 K/W; measured in Fig.6 unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_P	supply voltage	note 1	8	14.4	18	V
I_P	quiescent current		–	100	160	mA
V_O	DC output voltage	note 2	–	6.5	–	V
$\lvert\Delta V_o\rvert$	DC output offset voltage		–	–	150	mV
V_{14}	diagnostic output voltage	note 3	6	–	8	V
Mode select switch (see Fig.4)						
V_{16}	standby condition	note 4	0	–	1.2	V
V_{16}	mute condition		2.6	–	3.5	V
V_{16}	class-B operation		4.5	–	7.0	V
V_{16}	class-H operation		8.5	–	V_P	V
I_{sw}	maximum switch current		–	–	20	μA
I_{sb}	DC current in standby condition		–	5	50	μA
$\lvert\Delta V_o\rvert$	DC output offset voltage	in mute position	–	–	150	mV

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Mode select switch (see Fig.4)						
$\lvert\Delta V_o\rvert$	DC output offset voltage mute-on step	note 5	–	–	150	mV
V_O	output signal in mute position	V_I = 1 V (max); f = 20 Hz to 15 kHz	–	–	2	mV
Class-B/class-H operation (see Fig.3 and note 6)						
V_{17}	input switch level for class-B operation		2.5	–	V_P – 1	V
V_{17}	input switch level for class-H operation		0	–	1.0	V
I_{17}	switch current	note 7	–	–	2	mA
T_{vj}	case temperature for switching to class-B		–	120	–	°C
R_L	DC load impedance for					
	class-B or class-H operation		6.4	–	–	Ω
	class-B operation		–	4	–	Ω
	disabled output stages		–	–	0.5	Ω
V_3	load impedance sensor active		–	2.1	–	V

Notes

1. The circuit is DC adjusted at V_P = 8 to 18 V and AC operating at V_P = 8.5 to 18 V.
2. The DC output voltage, or the common mode voltage on the loudspeaker terminals with respect to ground, is 6.3 V at output powers up to 8.5 W. At higher output powers, the common mode voltage will be higher.
3. V_{14} is approximately $V_P/2$ in the event of a short-circuit, load dump or temperature protection. Any circuit connected to pin 14 should have an input resistance of more than 2 MΩ and an input capacity of less than 5 nF.
4. If the load impedance sensor is active (pin 3 floating) then for a reliable start-up the steepness of the voltage at the mode select input (pin 16) should not be slower than 10 V/s and not faster than 10 V/μs.
5. The DC output offset voltage step is the difference in output offset voltage in the mute condition and the on condition. The absolute value of this voltage step is given as: $\lvert\Delta V_{o\_mute} - \Delta V_{o\_on}\rvert < 150$ mV.
6. Fig.3 shows the relationship between the global crystal temperature and the open voltage at the class-B/class-H pin.
7. The maximum voltage on pin 17 is V_P – 1, ($V_P \leq 18$ V).

AC CHARACTERISTICS

V_P = 14.4 V; R_L = 8 Ω; f = 1 kHz; T_{amb} = 25 °C and using 4 K/W heatsink; measured in Fig.6 unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
P_o	output power	class-H				
		THD = 0.5%	27	30	–	W
		THD = 10%; continuously driven	36	39	–	W
		THD = 10%; with burst signals; note 1	–	40	–	W

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
P_o	output power	class-B				
		THD = 10%; R_L = 4 Ω	–	17	–	W
		THD = 10%	7	10	–	W
THD	total harmonic distortion					
		P_o = 1 W	–	0.05	–	%
		P_o = 10 W	–	0.1	–	%
BW	power bandwidth	THD = 0.5%; P_o = −1 dB with respect to 30 W; note 2	–	40 to 15 000	–	Hz
f_L	low frequency roll-off	−3 dB; note 3	–	40	–	Hz
f_H	high frequency roll-off	−1 dB	20	–	–	kHz
G_v	voltage gain		29	30	31	dB
SVRR	supply voltage ripple rejection	note 4				
	on		48	55	–	dB
	mute		48	65	–	dB
	standby		80	–	–	dB
CMRR	common mode rejection ratio on	note 5	64	–	–	dB
$\|Z_i\|$	input impedance	note 8	180	300	–	kΩ
V_i	maximum input voltage		–	1.2	–	V
V_{no}	noise output voltage					
	on	R_S = 0; note 6	–	100	300	μV
	on	R_S = 10 kΩ; note 6	–	150	–	μV
	mute	notes 6 and 7	–	100	–	μV

Notes

1. With a continuous sinewave input signal the output power is approximately 1 W less than driven with a bursted signal; also depending on the equivalent series resistance of the capacitors C1 and C2 (see Fig.6) and the resistance of the connections between pins 5, 8, 10 and 13 and C1, C2.
2. The power bandwidth is limited by the value of the electrolytic capacitors C1 and C2.
3. Frequency response is externally fixed by the input coupling capacitor.
4. Ripple rejection measured at the output, across R_L, with a source-impedance of 0 Ω and a frequency between 100 Hz and 10 kHz, and an amplitude of 2 V (p-p). The maximum supply voltage ripple is 2.5 V (RMS).
5. The common mode rejection ratio is measured at the output, across R_L, with a voltage source (500 mV RMS) between both short-circuited inputs and signal ground (see Fig.5). Frequencies are between 100 Hz and 10 kHz.
6. Noise output voltage measured in a bandwidth of 20 Hz to 20 kHz.
7. Noise output voltage is independent of source impedance.
8. Input impedance without external resistor (R_{ex}).

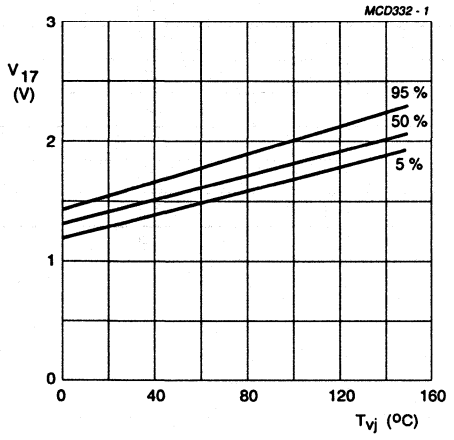


Fig.3 Class-B/class-H pin voltage level.

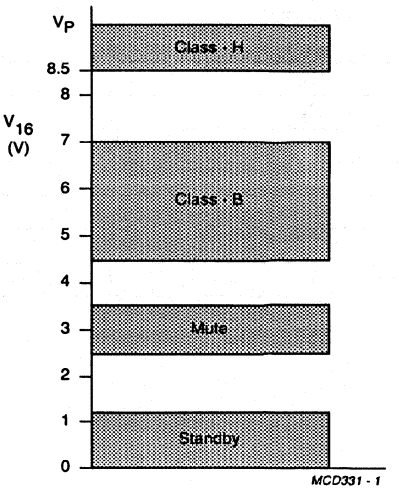


Fig.4 Standby/mute/class-B/class-H switch levels.

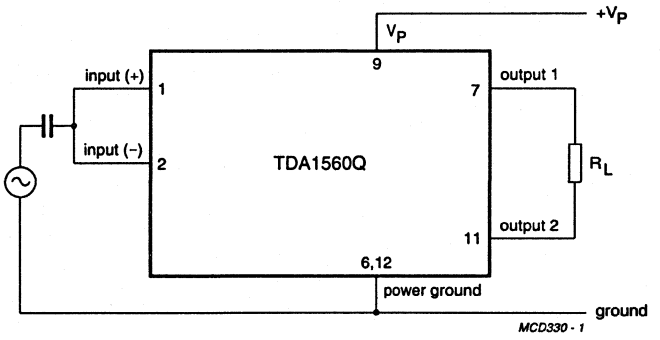
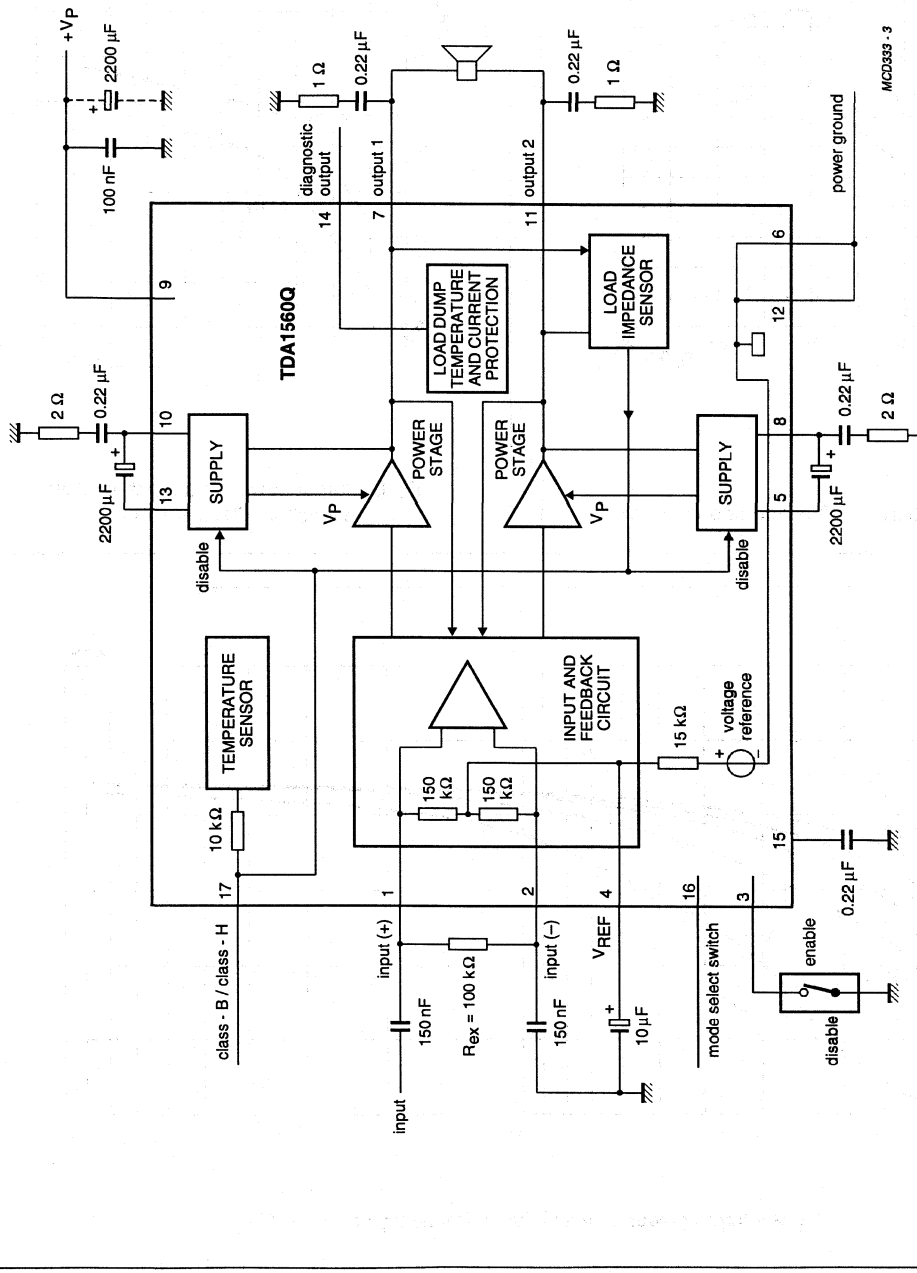


Fig.5 Common mode rejection ratio measurements.

Table 1 Values of C1, C2 and C_k as a function of frequency roll-off.

f (–3 dB) (Hz)	C1, C2 (μF)	C_k (nF)
10	4700	560
20	3300	270
30	2200	180
40	2200	150
50	1500	100
60	1500	82
70	1000	68



The values for C_k and R_{ex} are given for a low frequency roll-off (−3 dB) of 40 Hz; see also Table 1. In this application circuit the device is driven on input pin 1. If pin 2 is used the output power will be lower.

Fig.6 Test and application circuit.

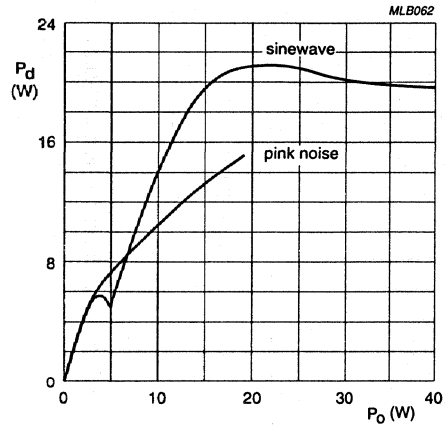


Fig.7 Dissipation as a function of output power.

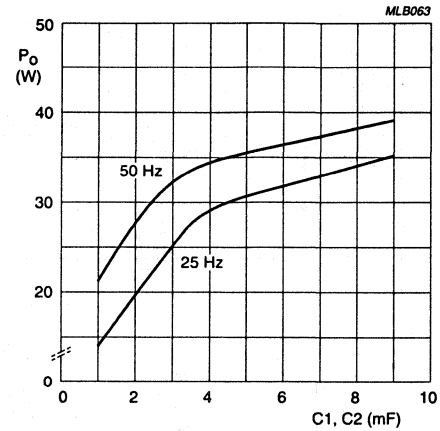


Fig.8 Output power as a function of lift capacitors (THD = 10%).

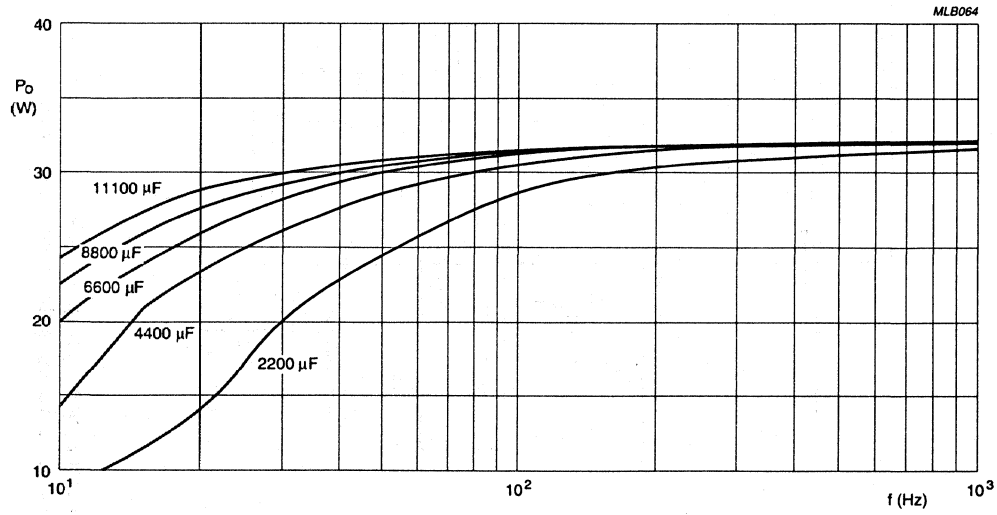


Fig.9 Output power as a function of frequency at THD = 1%.

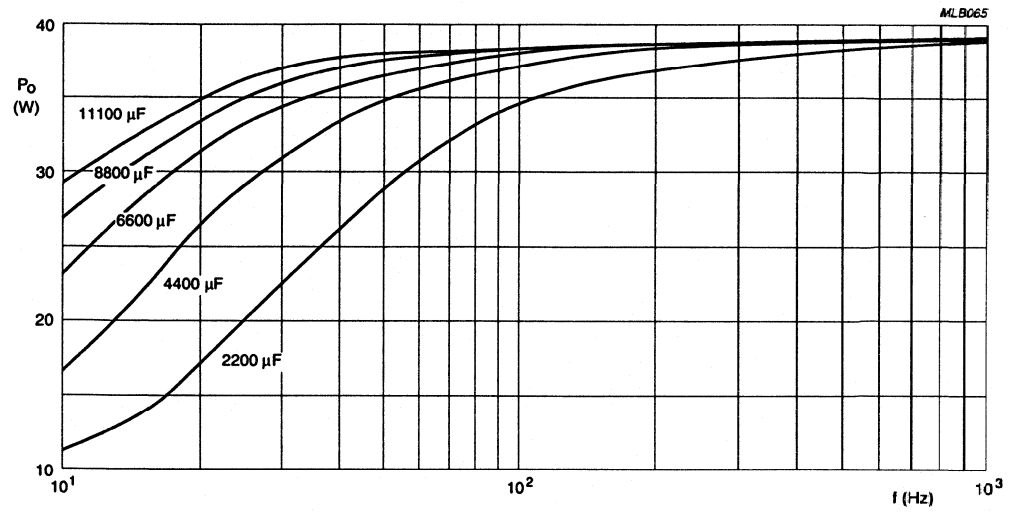


Fig.10 Output power as a function of frequency at THD = 10%.

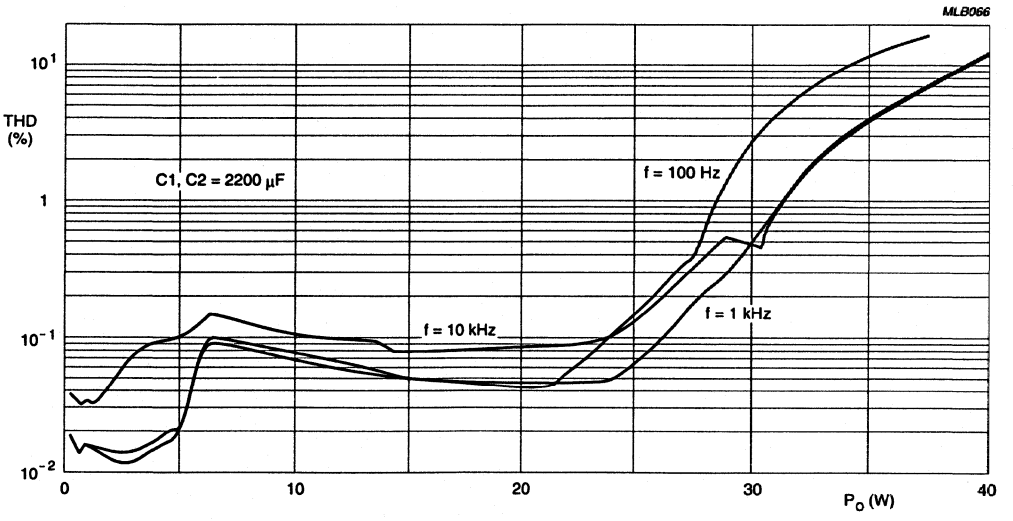


Fig.11 Total harmonic distortion as a function of output power.

AM RECEIVER CIRCUIT

GENERAL DESCRIPTION

The TDA1572 integrated AM receiver circuit performs all the active functions and part of the filtering required of an AM radio receiver. It is intended for use in mains-fed home receivers and car radios. The circuit can be used for oscillator frequencies up to 50 MHz and can handle RF signals up to 500 mV.

RF radiation and sensitivity to interference are minimized by an almost symmetrical design. The controlled-voltage oscillator provides signals with extremely low distortion and high spectral purity over the whole frequency range, even when tuning with variable capacitance diodes. If required, band switching diodes can easily be applied. Selectivity is obtained using a block filter before the IF amplifier.

Features

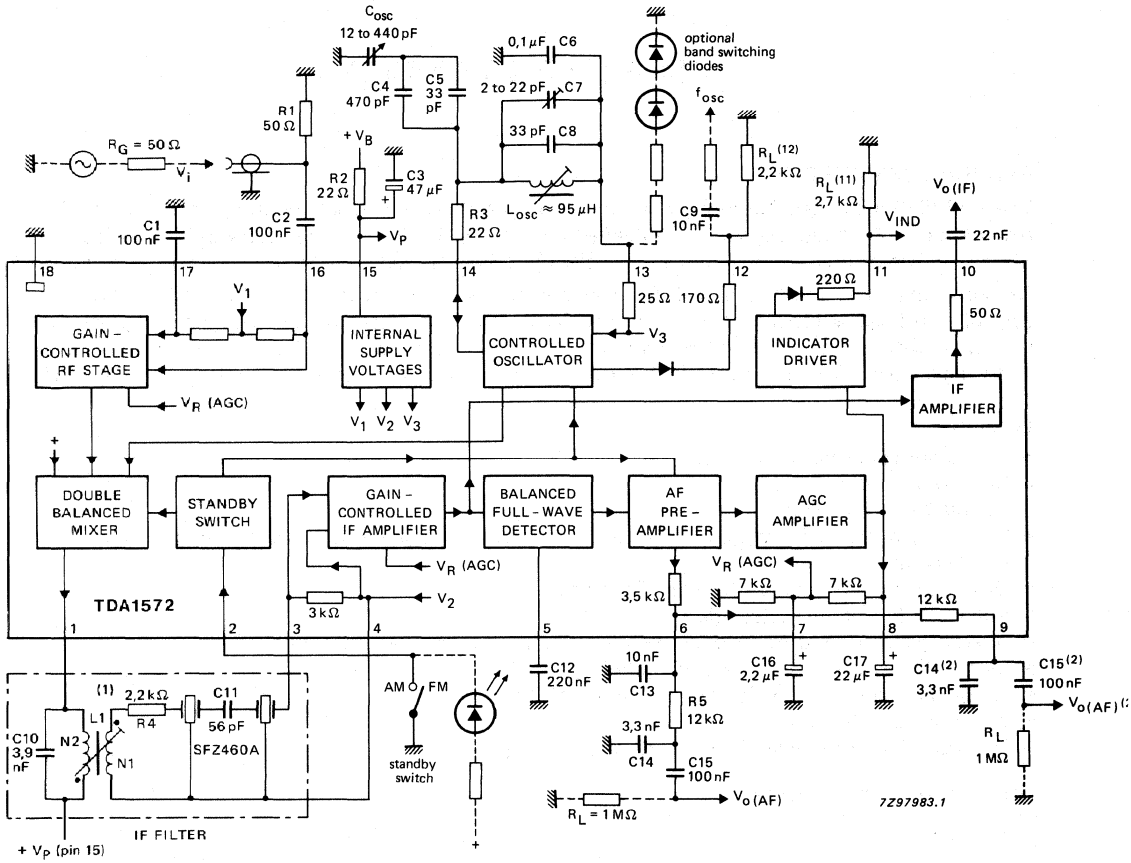
- Inputs protected against damage by static discharge
- Gain-controlled RF stage
- Double balanced mixer
- Separately buffered, voltage-controlled and temperature-compensated oscillator, designed for simple coils
- Gain-controlled IF stage with wide AGC range
- Full-wave, balanced envelope detector
- Internal generation of AGC voltage with possibility of second-order filtering
- Buffered field strength indicator driver with short-circuit protection
- AF preamplifier with possibilities for simple AF filtering
- Electronic standby switch
- IF output for stereo demodulator and search tuning

QUICK REFERENCE DATA

parameter	symbol	min.	typ.	max.	unit
Supply voltage range	V_P	7,5	–	18,0	V
Supply current range	I_P	15	–	30	mA
RF input voltage for (S+N)/N = 6 dB at m = 30%	$V_{i(RF)}$	–	1,5	–	μV
RF input voltage for 3% total harmonic distortion (THD) at m = 80%	$V_{i(RF)}$	–	500	–	mV
IF output voltage with V_i = 2 mV	$V_{o(IF)}$	–	230	–	mV
AF output voltage with V_i = 2 mV; f_i = 1 MHz; m = 30%; f_m = 400 Hz	$V_{o(AF)}$	–	310	–	mV
AGC range: change of V_i for 1 dB change of $V_{o(AF)}$		–	86	–	dB
Field strength indicator voltage at V_i = 500 mV; $R_{L(11)}$ = 2,7 kΩ	V_{IND}	–	2,8	–	V

PACKAGE OUTLINE

18-lead DIL; plastic (SOT102).



(1) Coil data: TOKO sample no. 7XNS-A7523DY; L1 : N1/N2 = 12/32; Q_o = 65; Q_B = 57.
Filter data: Z_F = 700 Ω at R_{3-4} = 3 kΩ; Z_I = 4,8 kΩ.

(2) AF output is pin 6 is not used.

Fig. 1 Block diagram and test circuit (connections shown in broken lines are not part of the test circuit).

FUNCTIONAL DESCRIPTION

Gain-controlled RF stage and mixer

The differential amplifier in the RF stage employs an AGC negative feedback network to provide a wide dynamic range. Very good cross-modulation behaviour is achieved by AGC delays at the various signal stages. Large signals are handled with low distortion and the (S+N)/N ratio of small signals is improved. Low noise working is achieved in the differential amplifier by using transistors with low base resistance.

A double balanced mixer provides the IF output signal to pin 1.

Oscillator

The differential amplifier oscillator is temperature compensated and is suitable for simple coil connection. The oscillator is voltage-controlled and has little distortion or spurious radiation. It is specially suitable for electronic tuning using variable capacitance diodes. Band switching diodes can easily be applied using the stabilized voltage $V_{13\text{-}18}$. An extra buffered oscillator putput (pin 12) is available for driving a synthesizer. If this is not needed, resistor $R_{L(12)}$ can be omitted.

Gain-controlled IF amplifier

This amplifier comprises two cascaded, variable-gain differential amplifier stages coupled by a band-pass filter. Both stages are gain-controlled by the AGC negative feedback network. The IF output is available at pin 10.

Detector

The full-wave, balanced envelope detector has very low distortion over a wide dynamic range. Residual IF carrier is blocked from the signal path by an internal low-pass filter.

AF preamplifier

This stage preamplifies the audio frequency output signal. The amplifier output has an emitter follower with a series resistor which, together with an external capacitor, yields the required low-pass for AF filtering.

AGC amplifier

The AGC amplifier provides a control voltage which is proportional to the carrier amplitude. Second-order filtering of the AGC voltage achieves signals with very little distortion, even at low audio frequencies. This method of filtering also gives fast AGC settling time which is advantageous for electronic search tuning. The AGC settling time can be further reduced by using capacitors of smaller value in the external filter (C16 and C17). The AGC voltage is fed to the RF and IF stages via suitable AGC delays. The capacitor at pin 7 can be omitted for low-cost applications.

Field strength indicator output

A buffered voltage source provides a high-level field strength output signal which has good linearity for logarithmic input signals over the whole dynamic range. If the field strength information is not needed, $R_{L(11)}$ can be omitted.

Standby switch

This switch is primarily intended for AM/FM band switching. During standby mode the oscillator, mixer and AF preamplifier are switched off.

Short-circuit protection

All pins have short-circuit protection to ground.

RATINGS

Limiting values in accordance with the Absolute Maximum Rating System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage	$V_P = V_{15-18}$	–	20	V
Total power dissipation	P_{tot}	–	875	mW
Input voltage	$\|V_{16-17}\|$	–	12	V
	$-V_{16-18}$, $-V_{17-18}$	–	0,6	V
	V_{16-18}, V_{17-18}	–	V_P	V
Input current	$\|I_{16}\|$, $\|I_{18}\|$	–	200	mA
Operating ambient temperature range	T_{amb}	–40	+ 85	°C
Storage temperature range	T_{stg}	–55	+ 150	°C
Junction temperature	T_j	–	+ 125	°C

THERMAL RESISTANCE

From junction to ambient	$R_{th\ j-a}$		80	K/W

CHARACTERISTICS

$V_P = V_{15-18} = 8{,}5$ V; $T_{amb} = 25\ ^oC$; $f_i = 1$ MHz; $f_m = 400$ Hz; m = 30%; $f_{IF} = 460$ kHz; measured in test circuit of Fig. 1; all voltages referenced to ground; unless otherwise specified.

parameter	symbol	min.	typ.	max.	unit
Supply					
Supply voltage (pin 15)	V_P	7,5	8,5	18,0	V
Supply current (pin 15)	I_P	15	23	30	mA
RF stage and mixer (pins 16 and 17)					
DC input voltage	V_I	–	$V_P/2$	–	V
RF input impedance at $V_I < 300\ \mu V$	Z_i	–	5,5	–	kΩ
RF input capacitance	C_i	–	25	–	pF
RF input impedance at $V_I > 10$ mV	Z_i	–	8	–	kΩ
RF input capacitance	C_i	–	22	–	pF
IF output impedance (pin 1)	Z_o	200	–	–	kΩ
IF output capacitance	C_o	–	6	–	pF
Conversion transconductance before start of AGC	I_1/V_i	–	6,5	–	mA/V
Maximum IF output voltage, inductive coupling to pin 1 (peak-to-peak value)	$V_{1-15(p-p)}$	–	5	–	V
DC value of output current; at $V_I = 0$ V (pin 1)	I_O	–	1,2	–	mA
AGC range of input stage		–	30	–	dB
RF signal handling capability: (r.m.s. value): input voltage for THD = 3% at m = 80%	$V_{i(rms)}$	–	500	–	mV

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Oscillator					
Frequency range	f_{osc}	0,1	–	60	MHz
Oscillator amplitude (pins 13 to 14)	V	–	130	150	mV
External load impedance (pins 14 to 13)	$R_{(ext)}$	0,5	–	200	kΩ
External load impedance for no oscillation (pins 14 to 13)	$R_{(ext)}$	–	–	60	Ω
Ripple rejection at $V_{P(rms)}$ = 100 mV; f_p = 100 Hz ($SVRR = 20 \log [V_{15}/V_{13}]$)	RR	–	55	–	dB
Source voltage for switching diodes (6 x V_{BE}) (pin 13)	V	–	4,2	–	V
DC output current (for switching diodes) (pin 13)	$-I_O$	0	–	20	mA
Change of output voltage at ΔI_{13} = 20 mA (switch to maximum load) (pin 13)	ΔV_I	–	0,3	–	V
Buffered oscillator output (pin 12)					
DC output voltage	V_O	–	0,8	–	V
Output signal amplitude (peak-to-peak value)	$V_{o(p-p)}$	–	320	–	mV
Output impedance	Z_O	–	170	–	Ω
Output current	$-I_{O(peak)}$	–	–	3	mA
IF, AGC and AF stages					
DC input voltage (pins 3 and 4)	V_I	–	2,0	–	V
IF input impedance (pins 3 to 4)	Z_i	2,4	3,0	3,9	kΩ
IF input capacitance	C_i	–	7	–	pF
IF input voltage for THD = 3% at m = 80% (pins 3 and 4)	V_i	–	90	–	mV
IF output impedance (pin 10)	Z_o	–	50	–	Ω
Unloaded IF output voltage at V_i = 10 mV (pin 10)	V_o	180	230	290	mV
Voltage gain before start of AGC (pins 3 to 4; 6 to 18)	G_v	–	68	–	dB
AGC range of IF stages: change of $V_{3\text{-}4}$ for 1 dB change of $V_{o(AF)}$; $V_{3\text{-}4(ref)}$ = 75 mV	ΔV_v	–	55	–	dB
AF output voltage at $V_{3\text{-}4(IF)}$ = 50 μV	$V_{o(AF)}$	–	130	–	mV
AF output voltage at $V_{3\text{-}4(IF)}$ = 1 mV	$V_{o(AF)}$	–	310	–	mV
AF output impedance (pin 6)	$\|Z_o\|$	2,8	3,5	4,2	kΩ

parameter	symbol	min.	typ.	max.	unit
Indicator driver (pin 11)					
Output voltage at V_i = 0 mV; R_L = 2,7 kΩ	V_o	–	–	140	mV
Output voltage at V_i = 500 mV; R_L = 2,7 kΩ	V_o	2,5	2,8	3,1	V
Load resistance	R_L	1,5	–	–	kΩ
Standby switch					
Switching threshold at; V_P = 7,5 to 18 V; T_{amb} = −40 to +80 °C					
ON-voltage	V_{2-1}	0	–	2,0	V
OFF-voltage	V_{2-1}	3,5	–	20,0	V
ON-current at V_{2-1} = 0 V	$-I_2$	–	100	200	μA
OFF-current at V_{2-1} = 20 V	$\|I_2\|$	–	–	10	μA

OPERATING CHARACTERISTICS

V_P = 8,5 V; f_i = 1 MHz; m = 30%; f_m = 400 Hz; T_{amb} = 25 °C; measured in Fig. 1; unless otherwise specified

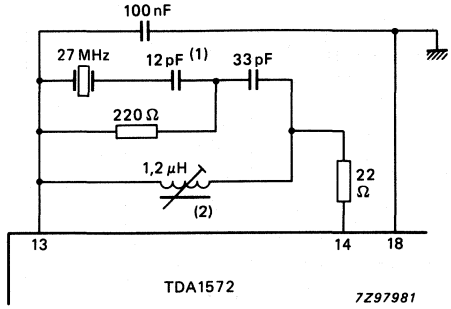
parameter	symbol	min.	typ.	max.	unit
RF sensitivity					
RF input required for (S+N)/N = 6 dB	V_i	–	1,5	–	μV
RF input required for (S+N)/N = 26 dB	V_i	–	15	–	μV
RF input required for (S+N)/N = 46 dB	V_i	–	150	–	μV
RF input at start of AGC	V_i	–	30	–	μV
RF large signal handling					
RF input at THD = 3%; m = 80%	V_i	–	500	–	mV
RF input at THD = 3%; m = 30%	V_i	–	700	–	mV
RF input at THD = 10%; m = 30%	V_i	–	900	–	mV
AGC range					
Change of V_i for 1 dB change of $V_{o(AF)}$; $V_{i(ref)}$ = 500 mV	ΔV_i	–	86	–	dB
Change of V_i for 6 dB change of $V_{o(AF)}$; $V_{i(ref)}$ = 500 mV	ΔV_i	–	91	–	dB
Output signal					
IF output voltage at V_i = 2 mV	$V_{o(IF)}$	180	230	290	mV
AF output voltage at V_i = 4 μV; m = 80%	$V_{o(AF)}$	–	130	–	mV
AF output voltage at V_i = 2 mV	$V_{o(AF)}$	240	310	390	mV
THD at V_i = 1 mV	d_{tot}	–	0,5	–	%
THD at V_i = 500 mV	d_{tot}	–	1	–	%
Signal plus noise-to-noise ratio at V_i = 100 mV	(S+N)/N	–	58	–	dB
Ripple rejection at V_i = 2 mV; $V_{P(rms)}$ = 100 mV; f_p = 100 Hz ($SVRR = 20 \log [V_P/V_{o(AF)}]$)	RR	–	38	–	dB
a) additional AF signal at IF output	RR	–	0*	–	dB
b) add modulation at IF output (m_{ref} = 30%)	RR	–	40	–	dB

* AF signals at the IF output will be suppressed by a coupling capacitor to the demodulator and by full wave-detection in the demodulator.

parameter	symbol	min.	typ.	max.	unit
Unwanted signals					
Suppression of IF whistles at V_i = 15 μV; m = 0% related to AF signal of m = 30%					
at $f_i \approx 2 \times f_{IF}$	α_{2IF}	–	*	–	dB
at $f_i \approx 3 \times f_{IF}$	α_{3IF}	–	*	–	dB
IF suppression at RF input;					
for symmetrical input	α_{IF}	–	40	–	dB
for asymmetrical input	α_{IF}	–	40	–	dB
Residual oscillator signal at mixer output;					
at f_{osc}	$I_{1(osc)}$	–	1	–	μA
at 2 x f_{osc}	$I_{1(2osc)}$	–	1,1	–	μA

* Value to be fixed.

APPLICATION INFORMATION



(1) Capacitor values depend on crystal type.
(2) Coil data: 9 windings of 0,1 mm dia laminated Cu wire on TOKO coil set 7K 199CN; $Q_o = 80$.

Fig. 2 Oscillator circuit using quartz crystal; centre frequency = 27 MHz.

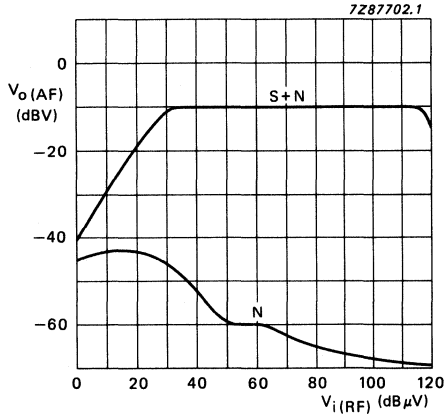


Fig. 3 AF output as a function of RF input in the circuit of Fig. 1; f_i = 1 MHz; f_m = 400 Hz; m = 30%.

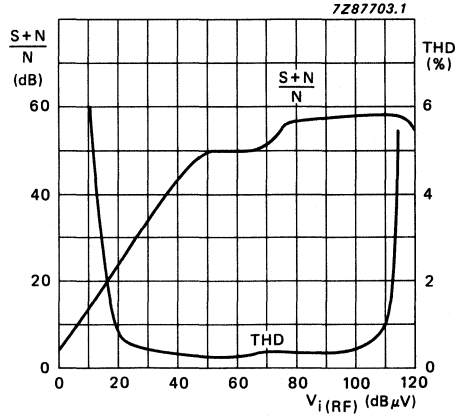


Fig. 4 Total harmonic distortion and (S + N)/N as functions of RF input in the circuit of Fig. 1; m = 30% for (S + N)/N curve and m = 80% for THD curve.

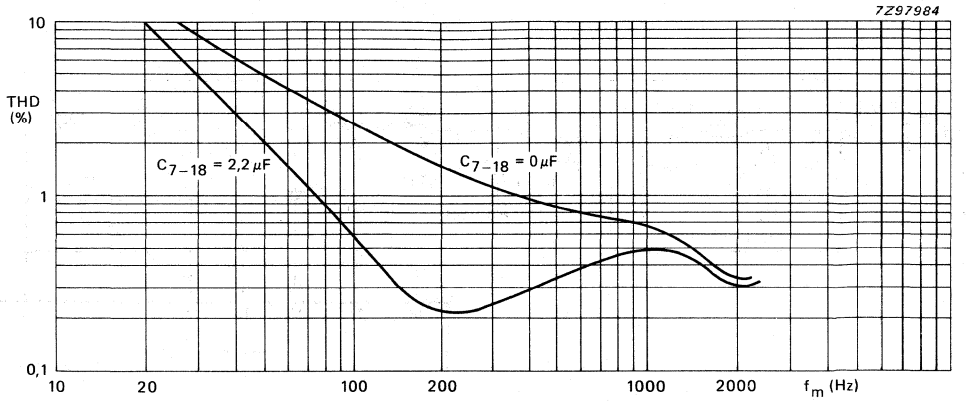


Fig. 5 Total harmonic distortion as a function of modulation frequency at V_i = 5 mV; m = 80%; measured in the circuit of Fig. 1 with $C_{7\text{-}18(ext)}$ = 0 μF and 2,2 μF.

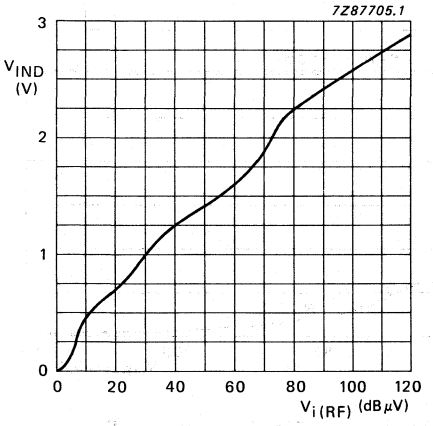


Fig. 6 Indicator driver voltage as a function of RF input in the circuit of Fig. 1.

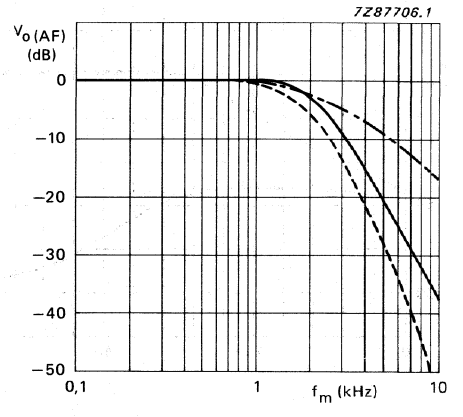


Fig. 7 Typical frequency response curves from Fig. 1 showing the effect of filtering as follows:

——— with IF filter;
—·—·— with AF filter;
– – – – – – with IF and AF filters.

APPLICATION INFORMATION (continued)

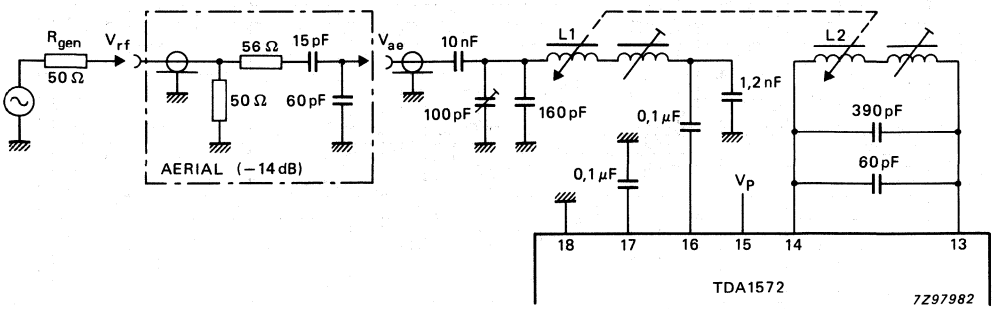


Fig. 8 Car radio application with inductive tuning.

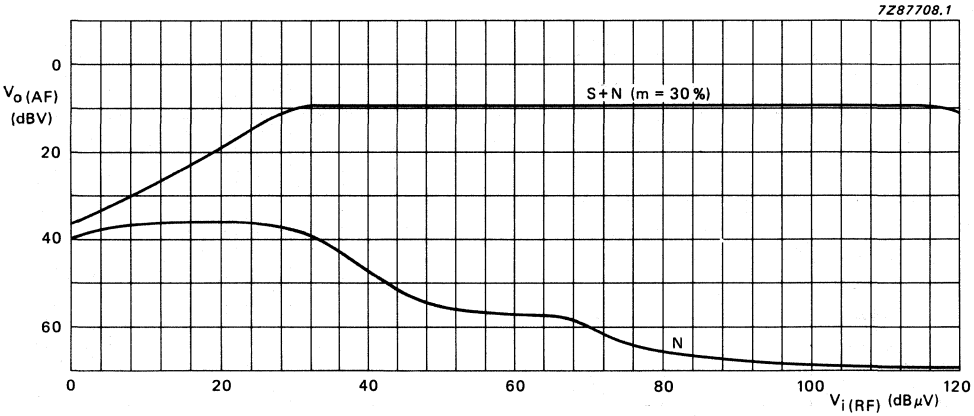


Fig. 9 AF output as a function of RF input using the circuit of Fig. 8 with that of Fig. 1.

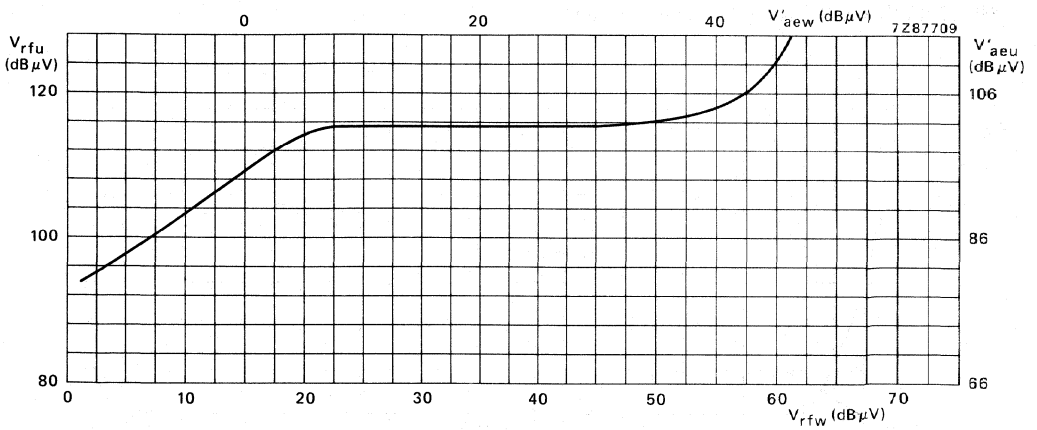


Fig. 10 Suppression of cross-modulation as a function of input signal, measured in the circuit of Fig. 8 with the input circuit as shown in Fig. 11. Curve is for Wanted $V_{O(AF)}$/Unwanted $V_{O(AF)}$ = 20 dB; V_{rfw}, V_{rfu} are signals at the aerial input, V'_{aew}, V'_{aeu} are signals at the unloaded output of the aerial.

Wanted signal (V'_{aew}, V_{rfw}): f_i = 1 MHz; f_m = 400 Hz; m = 30%.

Unwanted signal (V'_{aeu}, V_{rfu}): f_i = 900 kHz; f_m = 400 Hz; m = 30%.

Effective selectivity of input tuned circuit = 21 dB.

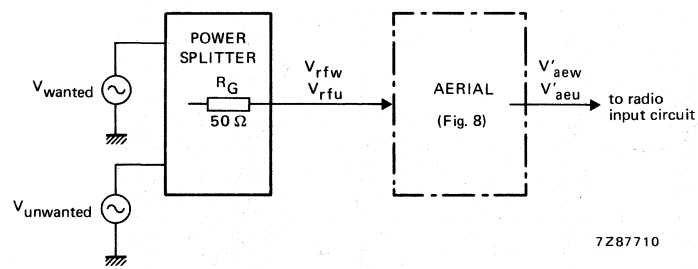


Fig. 11 Input circuit to show cross-modulation suppression (see Fig. 10).

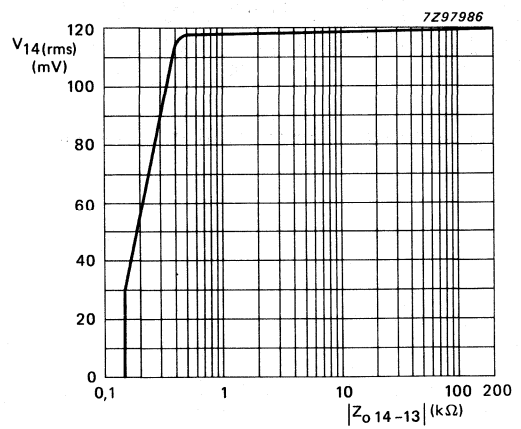


Fig. 12 Oscillator amplitude as a function of pin 13, 14 impedance in the circuit of Fig. 8.

APPLICATION INFORMATION (continued)

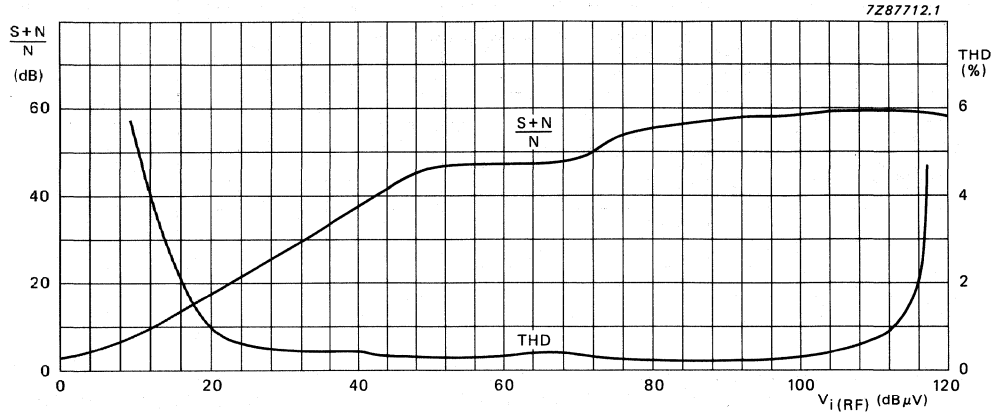


Fig. 13 Total harmonic distortion and (S + N)/N as functions of RF input using the circuit of Fig. 8 with that of Fig. 1.

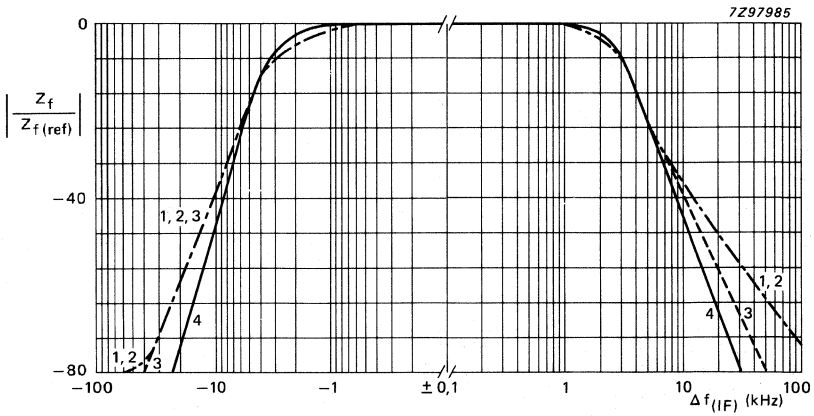


Fig. 14 Forward transfer impedance as a function of intermediate frequency for filters 1 to 4 shown in Fig. 15; centre frequency = 455 kHz.

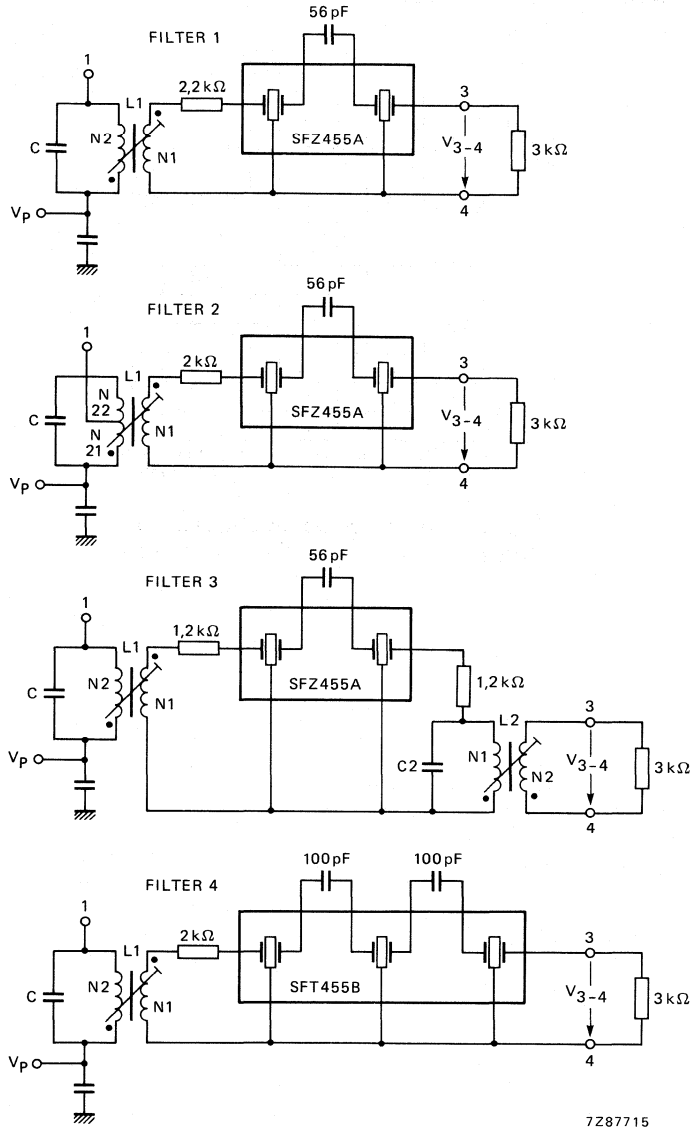


Fig. 15 IF filter variants applied to the circuit of Fig. 1. For filter data, refer to Table 1.

APPLICATION INFORMATION (continued)

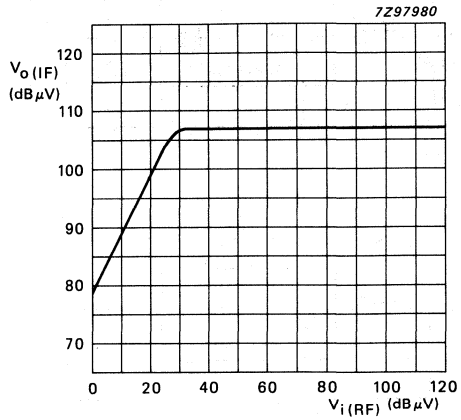
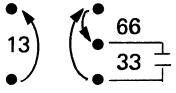
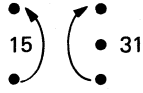
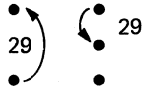
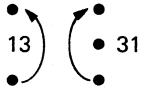


Fig. 16 IF output voltage as a function of RF input in the circuit of Fig. 1; f_i = 1 MHz.

Table 1 Data for IF filters shown in Fig. 15. Criteria for adjustment is Z_F = maximum (optimum selectivity curve at centre frequency f_0 = 455 kHz). See also Fig. 14.

filter no.	1	2	3		4	unit
Coil data	L1	L1	L1	L2	L1	
Value of C	3900	430	3900	4700	3900	pF
N1: N2	12 : 32	13 : (33 + 66)	15 : 31	29 : 29	13 : 31	
Diameter of Cu laminated wire	0,09	0,08	0,09	0,08	0,09	mm
Q_o	65 (typ.)	50	75	60	75	
Schematic* of windings						
Toko order no.	7XNS-A7523DY	L7PES-A0060BTG	7XNS-A7518DY	7XNS-A7521AIH	7XNS-A7519DY	
Resonators						
Murata type	SFZ455A	SFZ455A	SFZ455A		SFT455B	
D (typical value)	4	4	4		6	dB
R_G, R_L	3	3	3		3	kΩ
Bandwidth (−3 dB)	4,2	4,2	4,2		4,5	kHz
S_{9kHz}	24	24	24		38	dB
Filter data						
Z_I	4,8	3,8	4,2		4,8	kΩ
Q_B	57	40	52 (L1)	18 (L2)	55	
Z_F	0,70	0,67	0,68		0,68	kΩ
Bandwidth (−3 dB)	3,6	3,8	3,6		4,0	kHz
S_{9kHz}	35	31	36		42	dB
S_{18kHz}	52	49	54		64	dB
S_{27kHz}	63	58	66		74	dB

* The beginning of an arrow indicates the beginning of a winding; N1 is always the inner winding, N2 the outer winding.

AM RECEIVER

GENERAL DESCRIPTION

The TDA1572T integrated AM receiver circuit performs all the active functions and part of the filtering required of an AM radio receiver. It is intended for use in mains-fed home receivers and car radios. The circuit can be used for oscillator frequencies up to 50 MHz and can handle RF signals up to 500 mV.

RF radiation and sensitivity to interference are minimized by an almost symmetrical design. The controlled-voltage oscillator provides signals with extremely low distortion and high spectral purity over the whole frequency range, even when tuning with variable capacitance diodes. If required, band switching diodes can easily be applied. Selectivity is obtained using a block filter before the IF amplifier.

Features

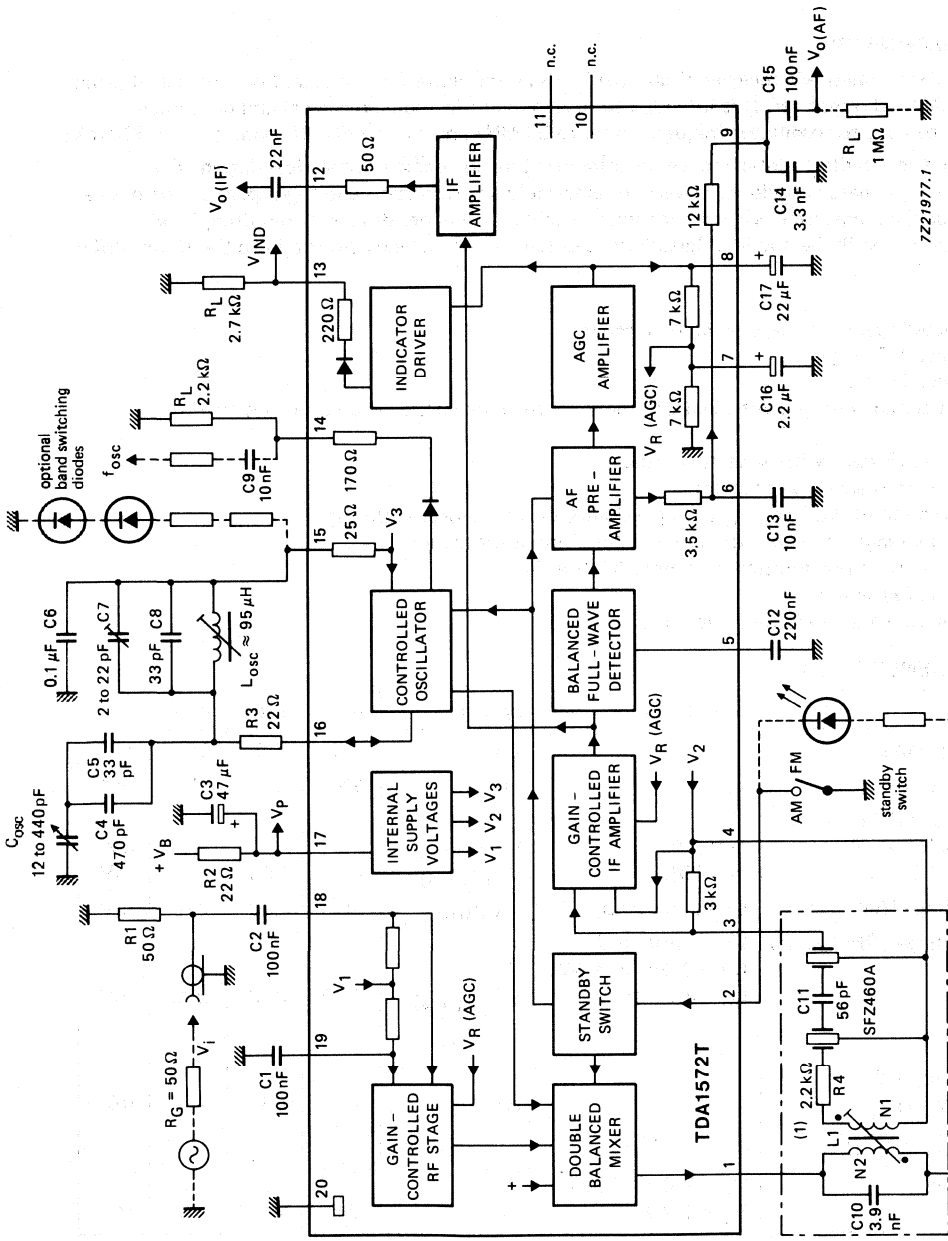
- Inputs protected against damage by static discharge
- Gain-controlled RF stage
- Double balanced mixer
- Separately buffered, voltage-controlled and temperature-compensated oscillator, designed for simple coils
- Gain-controlled IF stage with wide AGC range
- Full-wave, balanced envelope detector
- Internal generation of AGC voltage with possibility of second-order filtering
- Buffered field strength indicator driver with short-circuit protection
- AF preamplifier with possibilities for simple AF filtering
- Electronic standby switch
- IF output for stereo demodulator and search tuning

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage range		V_P	7.5	8.5	14.0	V
Supply current range	V_P = 8.5 V	I_P	15	25	28	mA
RF input voltage (RMS value)						
for (S + N)/N = 6 dB	m = 30%	$V_{iFR(rms)}$	–	1.5	–	μV
for THD = 3%	m = 80%	$V_{iRF(rms)}$	–	500	–	mV
IF output voltage (RMS value)	V_i = 2 mV(rms)	$V_{oIF(rms)}$	180	230	290	mV
AF output voltage (RMS value)	V_i = 2 mV(rms); f_i = 1 MHz; m = 30%; f_m = 400 Hz	$V_{oAF(rms)}$	240	310	390	mV
AGC range						
Change of V_i for 1 dB change of V_{oAF}		ΔV_i	–	86	–	dB
Indicator driver (pin 13)						
Output voltage	V_i = 500 mV(rms); R_L = 2.7 kΩ	V_o	2.5	2.8	3.1	V

PACKAGE OUTLINE

20-lead mini-pack; plastic (SO20; SOT163A).



(1) Coil data: TOKO sample no. 7XNS-A7523DY; L1 : N1/N2 = 12/32; Q_O = 65; Q_B = 57.
Filter data: Z_F = 700 Ω at $R_{3\text{-}4}$ = 3 kΩ; Z_I = 4.8 kΩ.

Fig. 1 Block diagram and test circuits (connections shown in broken lines are not part of the test circuits).

PINNING

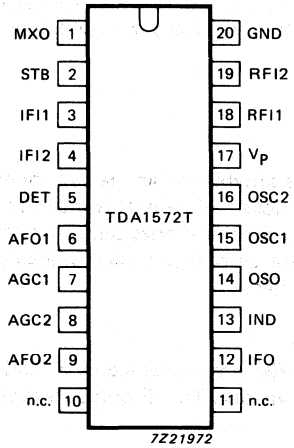


Fig.2 Pinning diagram.

1	MXO	mixer output
2	STB	standby switch
3	IFI1	IF input 1
4	IFI2	IF input 2
5	DET	detector
6	AFO1	AF output 1
7	AGC1	AGC stage 1
8	AGC2	AGC stage 2
9	AFO2	AF output 2
10	n.c.	not connected
11	n.c.	not connected
12	IFO	IF output
13	IND	indicator output
14	OSO	buffered oscillator output
15	OSC1	oscillator 1
16	OSC2	oscillator 2
17	V_P	supply voltage
18	RFI1	RF input 1
19	RFI2	RF input 2
20	GND	ground

FUNCTIONAL DESCRIPTION

Gain-controlled RF stage and mixer

The differential amplifier in the RF stage employs an AGC negative feedback network to provide a wide dynamic range. Very good cross-modulation behaviour is achieved by AGC delays at the various signal stages. Large signals are handled with low distortion and the (S + N)/N ratio of small signals is improved. Low noise working is achieved in the differential amplifier by using transistors with low base resistance.

A double balanced mixer provides the IF output signal to pin 1.

Oscillator

The differential amplifier oscillator is temperature compensated and is suitable for simple coil connection. The oscillator is voltage-controlled and has little distortion or spurious radiation. It is specially suitable for electronic tuning using variable capacitance diodes. Band switching diodes can easily be applied using the stabilized voltage $V_{15\text{-}20}$. An extra buffered oscillator putput (pin 14) is available for driving a synthesizer. If this is not needed, resistor $R_{L(14)}$ can be omitted.

Gain-controlled IF amplifier

This amplifier comprises two cascaded, variable-gain differential amplifier stages coupled by a band-pass filter. Both stages are gain-controlled by the AGC negative feedback network. The IF output is available at pin 12.

Detector

The full-wave, balanced envelope detector has very low distortion over a wide dynamic range. Residual IF carrier is blocked from the signal path by an internal low-pass filter.

AF preamplifier

This stage preamplifies the audio frequency output signal. The amplifier output has an emitter follower with a series resistor which, together with an external capacitor, yields the required low-pass for AF filtering.

AGC amplifier

The AGC amplifier provides a control voltage which is proportional to the carrier amplitude. Second-order filtering of the AGC voltage achieves signals with very little distortion, even at low audio frequencies. This method of filtering also gives fast AGC settling time which is advantageous for electronic search tuning. The AGC settling time can be further reduced by using capacitors of smaller value in the external filter (C16 and C17). The AGC voltage is fed to the RF and IF stages via suitable AGC delays. The capacitor at pin 7 can be omitted for low-cost applications.

Field strength indicator output

A buffered voltage source provides a high-level field strength output signal which has good linearity for logarithmic input signals over the whole dynamic range. If the field strength information is not needed, $R_{L(13)}$ can be omitted.

Standby switch

This switch is primarily intended for AM/FM band switching. During standby mode the oscillator, mixer and AF preamplifier are switched off.

Short-circuit protection

All pins have short-circuit protection to ground.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage (pin 17)	$V_P = V_{17-20}$	–	16	V
Input voltage	$\|V_{18-19}\|$	–	12	V
	$-V_{18-19}$; $-V_{19-20}$	–	0.6	V
	V_{18-19}; V_{19-20}	–	V_P	V
Input current (pins 18 and 20)	$\|I_{18}\|$; $\|I_{20}\|$	–	200	mA
Total power dissipation	P_{tot}	–	500	mW
Storage temperature range	T_{stg}	−55	+150	°C
Operating ambient temperature range	T_{amb}	−40	+85	°C
Junction temperature	T_j	–	+125	°C
Electrostatic handling*				
all pins except pins 3, 6, 9, 14	V_{es}	−2000	+2000	V
pins 3, 6, 14	V_{es}	−1500	+2000	V
pin 9	V_{es}	−1000	+2000	V

THERMAL RESISTANCE

From junction to ambient (in free air) $R_{th\ j\text{-}a\ (max.)} = 95$ K/W

* Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor; (5 pulses, both polarities).

CHARACTERISTICS

$V_P = V_{17-20} = 8.5$ V; $T_{amb} = 25$ °C; $f_i = 1$ MHz; $f_m = 400$ Hz; m = 30%; $f_{IF} = 460$ kHz; measured in test circuit of Fig. 1; all voltages referenced to ground; unless otherwise specified.

parameter	symbol	min.	typ.	max.	unit
Supply					
Supply voltage (pin 17)	V_P	7.5	8.5	14.0	V
Supply current (pin 17)	I_P	15	25	28	mA
RF stage and mixer (pins 18 and 19)					
DC input voltage	V_I	–	$V_P/2$	–	V
RF input impedance at $V_I < 300\ \mu V$ (rms)	Z_i	–	5.5	–	kΩ
RF input capacitance	C_i	–	25	–	pF
RF input impedance at $V_I > 10$ mV (rms)	Z_i	–	8	–	kΩ
RF input capacitance	C_i	–	22	–	pF
IF output impedance (pin 1)	Z_o	200	–	–	kΩ
IF output capacitance	C_o	–	6	–	pF
Conversion transconductance before start of AGC	I_1/V_i	–	6.5	–	mA/V
Maximum IF output voltage, inductive coupling to pin 1 (peak-to-peak value)	$V_{1-17(p-p)}$	–	5	–	V
DC value of output current; at $V_I = 0$ V (pin 1)	I_O	–	1.2	–	mA
AGC range of input stage		–	30	–	dB
RF signal handling capability					
Input voltage (RMS value) for THD = 3% at m = 80%	$V_{i(rms)}$	–	500	–	mV

parameter	symbol	min.	typ.	max.	unit
Oscillator					
Frequency range	f_{osc}	0.1	–	60	MHz
Voltage amplitude (pins 15 to 16) (RMS value)	$V_{(rms)}$	80	130	150	mV
External load impedance (pins 16 to 15)	$R_{(ext)}$	0.5	–	200	kΩ
External load impedance for no oscillation (pins 16 to 15)	$R_{(ext)}$	–	–	60	Ω
Supply voltage ripple rejection at V_P = 100 mV(rms); f_p = 100 Hz ($SVRR = 20 \log [V_{17}/V_{15}]$)	SVRR	–	55	–	dB
Source voltage for switching diodes (6 x V_{BE}) (pin 15)	$V_{15\text{-}20}$	–	4.2	–	V
DC output current (for switching diodes) (pin 15)	$-I_O$	0	–	20	mA
Change of output voltage at ΔI_{15} = 20 mA (switch to maximum load) (pin 15)	ΔV_I	–	0.3	–	V
Buffered oscillator output (pin 14)					
DC output voltage	V_O	–	0.8	–	V
Output signal amplitude (peak-to-peak value)	$V_{o(p\text{-}p)}$	–	320	–	mV
Output impedance	Z_O	–	170	–	Ω
Output current (peak value)	$-I_{O(peak)}$	–	–	3	mA
IF, AGC and AF stages					
DC input voltage (pins 3 and 4)	V_I	–	2.0	–	V
IF input impedance (pins 3 to 4)	Z_i	2.4	3.0	3.9	kΩ
IF input capacitance	C_i	–	7	–	pF
IF input voltage for THD = 3% at m = 80% (pins 3 and 4) (RMS value)	$V_{iIF(rms)}$	–	90	–	mV
IF output impedance (pin 12)	Z_o	–	50	–	Ω
Unloaded IF output voltage at V_i = 10 mV (pin 12) (RMS value)	$V_{oIF(rms)}$	180	230	290	mV
Voltage gain before start of AGC (pins 3 to 4; 6 to 20)	G_v	–	68	–	dB
AGC range of IF stages: change of $V_{3\text{-}4}$ for 1 dB change of $V_{o(AF)}$; $V_{3\text{-}4(ref)}$ = 75 mV(rms)	ΔV_v	–	55	–	dB

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
IF, AGC and AF stages (continued)					
AF output voltage (RMS value)					
at $V_{3\text{-}4(IF)}$ = 50 μV(rms)	$V_{oAF(rms)}$	–	130	–	mV
at $V_{3\text{-}4(IF)}$ = 1 mV(rms)	$V_{oAF(rms)}$	–	310	–	mV
AF output impedance (pin 6)	$\|Z_o\|$	2.8	3.5	4.2	kΩ
AF output impedance (pin 9)	$\|Z_o\|$	12.4	15.5	18.6	kΩ
Indicator driver (pin 13)					
Output voltage at V_i = 0 mV(rms); R_L = 2.7 kΩ	V_o	–	–	140	mV
Output voltage at V_i = 500 mV(rms); R_L = 2.7 kΩ	V_o	2.5	2.8	3.1	V
Load resistance	R_L	1.5	–	–	kΩ
Output current at V_i = 500 mV(rms)	$-I_o$	–	–	2.0	mA
Output impedance at $-I_o$ = 0.5 mA	Z_o	–	220	–	Ω
Reverse output voltage at AM off	V_o	–	6	–	V
Standby switch					
Switching threshold at; V_P = 7.5 to 14 V; T_{amb} = −40 to +80 °C					
ON-voltage	$V_{2\text{-}20}$	0	–	2.0	V
OFF-voltage	$V_{2\text{-}20}$	3.5	–	20.0	V
ON-current at $V_{2\text{-}20}$ = 0 V	$-I_2$	–	100	200	μA
OFF-current at $V_{2\text{-}20}$ = 14 V	$\|I_2\|$	–	–	10	μA

OPERATING CHARACTERISTICS

V_P = 8.5 V; f_i = 1 MHz; m = 30%; f_m = 400 Hz; T_{amb} = 25 °C; measured in Fig.1; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
RF sensitivity					
RF input voltage (RMS value)					
for (S + N)/N = 6 dB	$V_{iRF(rms)}$	–	1.5	–	μV
for (S + N)/N = 26 dB	$V_{iRF(rms)}$	–	15	–	μV
for (S + N)/N = 46 dB	$V_{iRF(rms)}$	–	150	–	μV
at start of AGC	$V_{iRF(rms)}$	–	30	–	μV
RF large signal handling					
RF input voltage (RMS value)					
at THD = 3%; m = 80%	$V_{iRF(rms)}$	–	500	–	mV
at THD = 3%; m = 30%	$V_{iRF(rms)}$	–	700	–	mV
at THD = 10%; m = 30%	$V_{iRF(rms)}$	–	900	–	mV
AGC range					
Change of V_i for 1 dB change of V_{oAF}; $V_{i(ref)}$ = 500 mV(rms)	ΔV_i	–	86	–	dB
Change of V_i for 6 dB change of V_{oAF}; $V_{i(ref)}$ = 500 mV(rms)	ΔV_i	–	91	–	dB
Output signal (RMS value)					
IF output voltage at V_i = 2 mV(rms)	$V_{oIF(rms)}$	180	230	290	mV
AF output voltage					
at V_i = 4 μV(rms); m = 80%	$V_{oAF(rms)}$	–	130	–	mV
at V_i = 2 mV(rms)	$V_{oAF(rms)}$	240	310	390	mV
Total harmonic distortion					
at V_i = 2 mV(rms); m = 30%	THD	–	0.5	–	%
at V_i = 2 mV(rms); m = 80%	THD	–	1.0	–	%
at V_i = 500 mV(rms); m = 30%	THD	–	1.0	–	%
Signal-to-noise ratio at V_i = 100 mV(rms)	(S + N)/N	–	58	–	dB
Supply voltage ripple rejection at V_i = 2 mV(rms) V_P = 100 mV(rms); f_p = 100 Hz ($SVRR = 20 \log[V_P/V_{oAF}]$)	SVRR	–	38	–	dB
(a) additional AF signal at IF output	SVRR	–	0*	–	dB
(b) add modulation at IF output (m_{ref} = 30%)	SVRR	–	40	–	dB

* AF signals at the IF output will be suppressed by a coupling capacitor to the demodulator and by full wave-detection in the demodulator.

OPERATING CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Unwanted signals					
Suppression of IF whistles at V_i = 15 μV; m = 0% related to AF signal of m = 30%					
at $f_i \approx 2 \times f_{IF}$	α_{2IF}	–	37	–	dB
at $f_i \approx 3 \times f_{IF}$	α_{3IF}	–	44	–	dB
IF suppression at RF input;					
for symmetrical input	α_{IF}	–	40	–	dB
for asymmetrical input	α_{IF}	–	40	–	dB
Residual oscillator signal at mixer output;					
at f_{osc}	$I_{1(osc)}$	–	1	–	μA
at 2 x f_{osc}	$I_{1(2osc)}$	–	1.1	–	μA

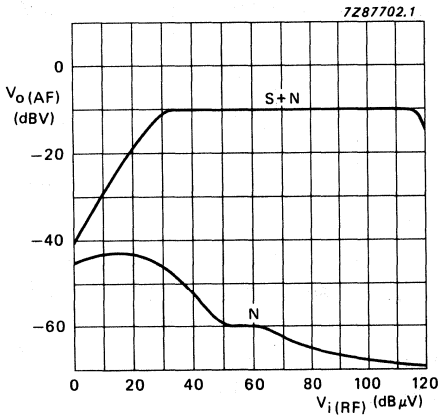


Fig. 3 AF output as a function of RF input in the circuit of Fig. 1; f_i = 1 MHz; f_m = 400 Hz; m = 30%.

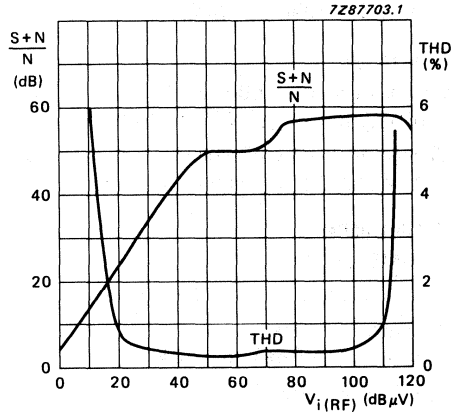


Fig. 4 Total harmonic distortion and (S + N)/N as functions of RF input in the circuit of Fig. 1; m = 30% for (S + N)/N curve and m = 80% for THD curve.

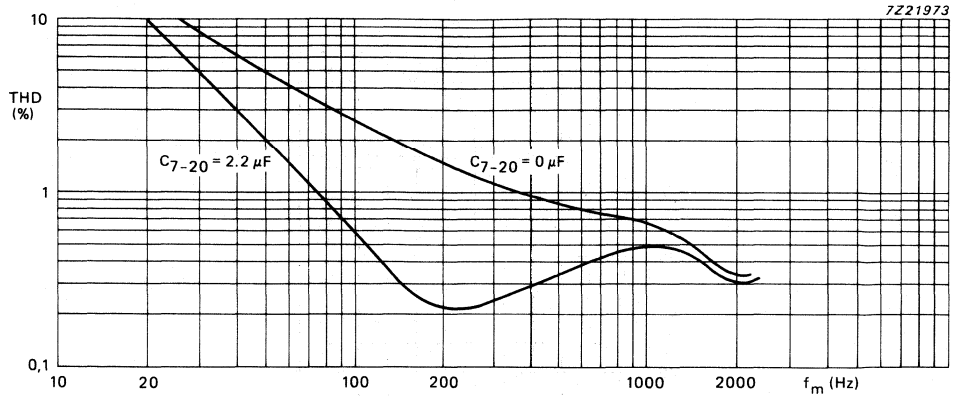


Fig. 5 Total harmonic distortion as a function of modulation frequency at V_i = 5 mV; m = 80%; measured in the circuit of Fig. 1 with $C_{7-20(ext)}$ = 0 μF and 2.2 μF.

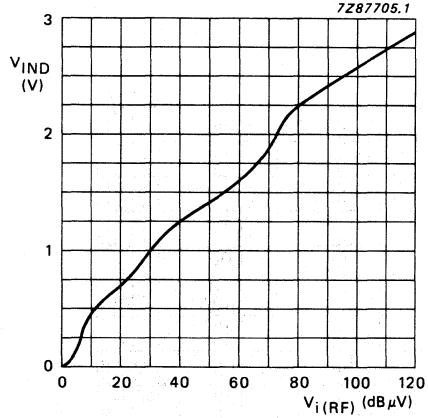
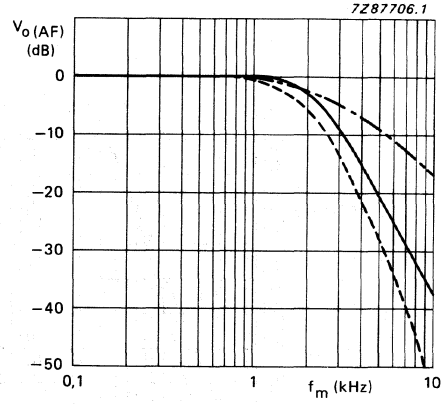


Fig. 6 Indicator driver voltage as a function of RF input in the circuit of Fig. 1.



——— with IF filter;
—·—·— with AF filter;
– – – – – – with IF and AF filters.

Fig.7 Typical frequency response curves from Fig.1 showing the effect of filtering.

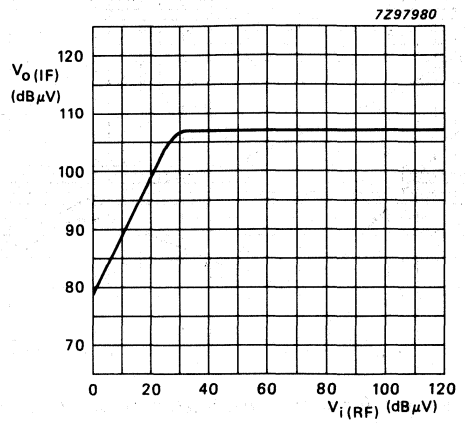


Fig.8 IF output voltage as a function of RF input in the circuit of Fig.1; f_i = 1 MHz.

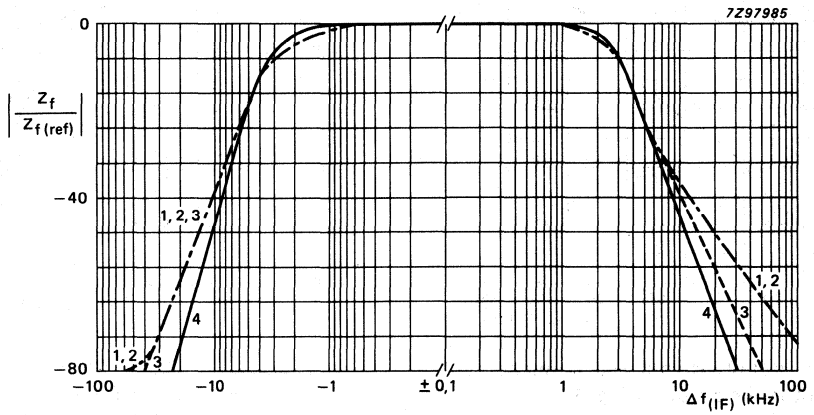


Fig.9 Forward transfer impedance as a function of intermediate frequency for filters 1 to 4 shown in Fig.10; centre frequency = 455 kHz.

APPLICATION INFORMATION

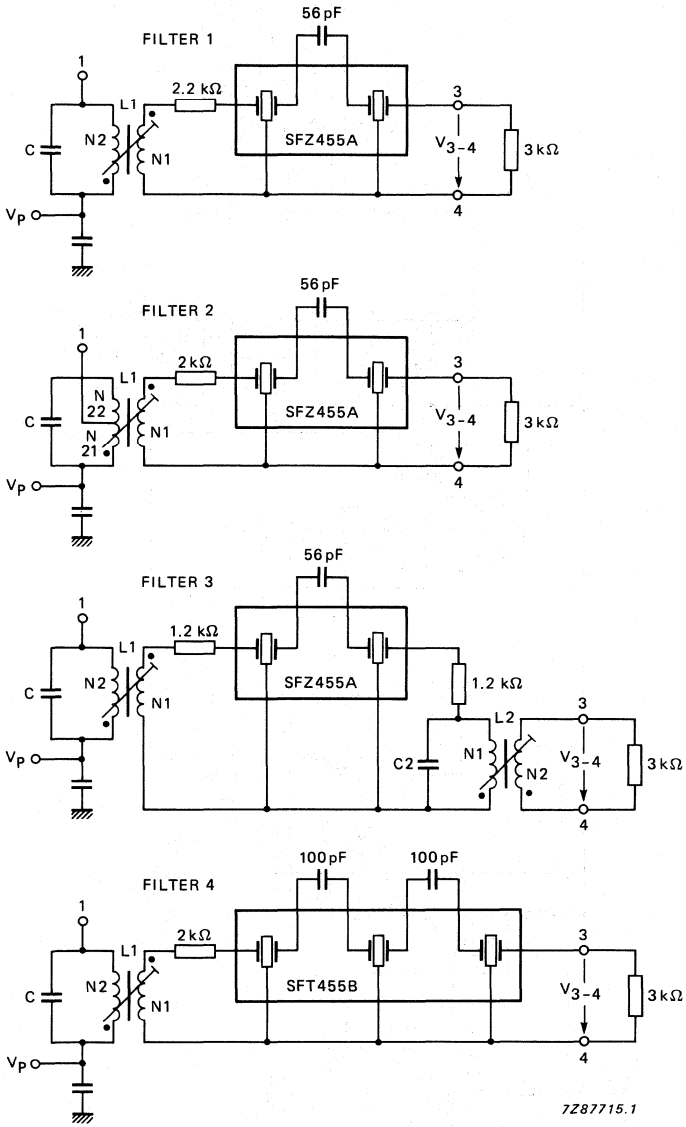


Fig. 10 IF filter variants applied to the circuit of Fig. 1. For filter data, refer to Table 1.

APPLICATION INFORMATION (continued)

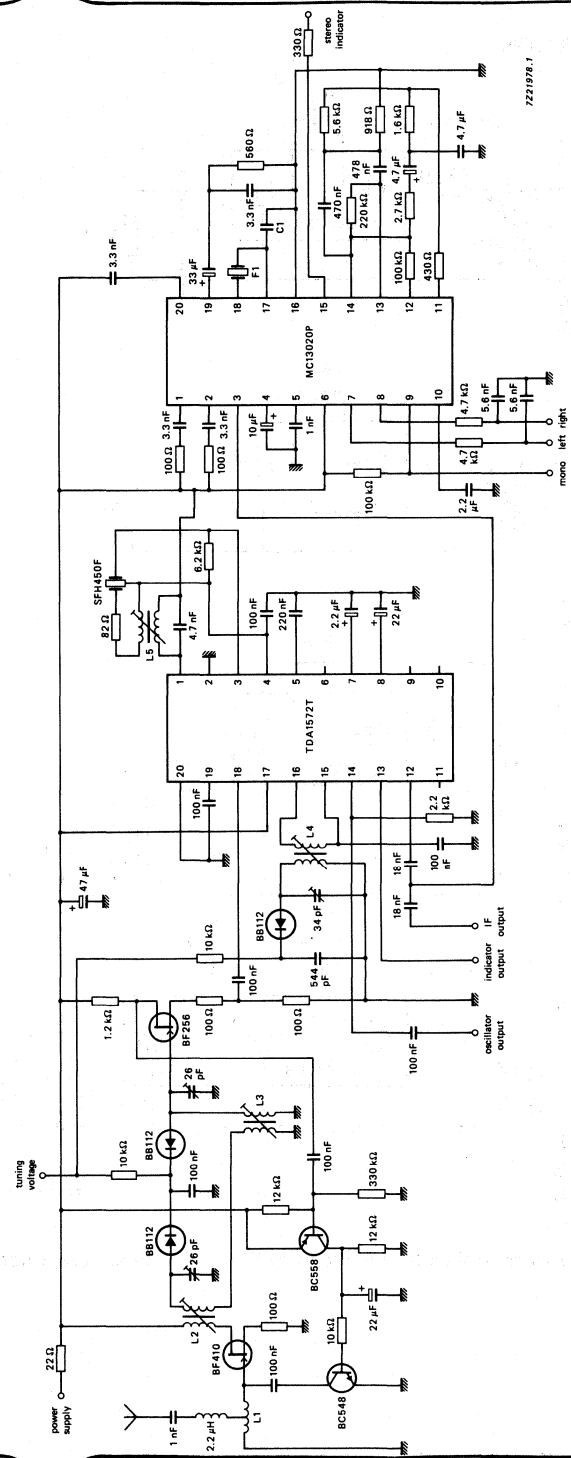


Fig.11 Application diagram.

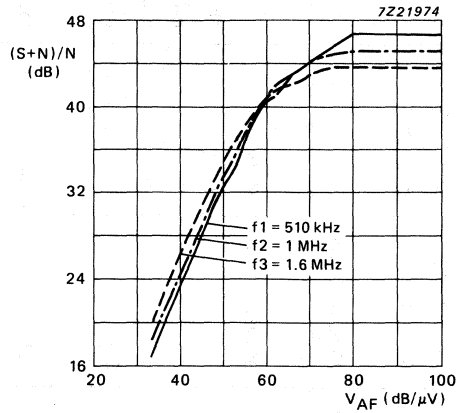


Fig.12 (S + N)/N as a function of input voltage; measured in the circuit of Fig.11 for AM stereo.

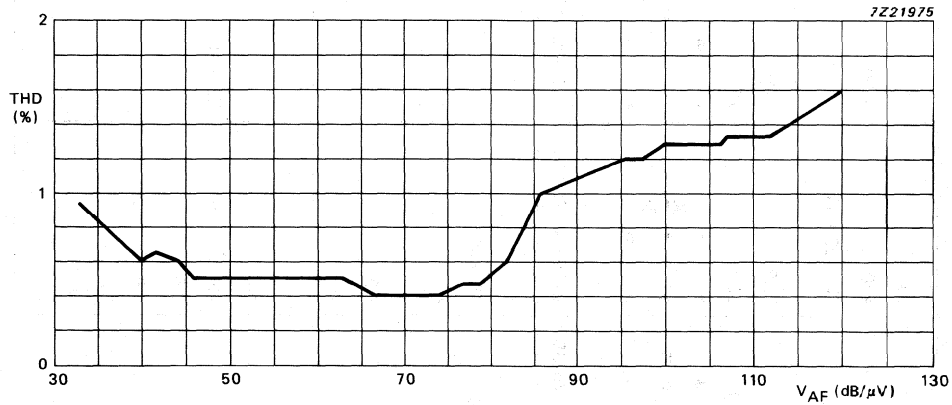


Fig.13 Total harmonic distortion (THD) as a function of input voltage; measured in the circuit of Fig.11 for AM stereo.

filter no.	1	2	3		4	5	unit
Coil data	L1	L1	L1	L2	L1	L1	
Value of C	3900	430	3900	4700	3900	4700	pF
N1 : N2	12 : 32	13 : (33 + 66)	15 : 31	29 : 29	13 : 31	26 : 32	
Diameter of CU laminated wire	0.09	0.08	0.09	0.08	0.09	0.07	mm
Q_o	65 (typ.)	50	75	60	75	50	
Schematic* of windings							
Toko order no.	7XNS-A7523DY	L7PES-A0060BTG	7XNS-A7518DY	7XNS-A7521AIH	7XNS-A7519DY		
Resonators							
Murata type	SFZ455A	SFZ455A	SFZ455A		SFT455B	SFH450F	
D (typical value)	4	4	4		6	6	dB
R_G, R_L	3	3	3		3	2	kΩ
Bandwidth (−3 dB)	4.2	4.2	4.2		4.5	10	kHz
S_{9kHz}	24	24	24		38		dB
Filter data							
Z_I	4.8	3.8	4.2		4.8	1.8	kΩ
Q_B	57	40	52 (L1)	18 (L2)	55	20	
Z_F	0.70	0.67	0.68		0.68	0.70	kΩ
Bandwidth (−3 dB)	3.6	3.8	3.6		4.0	10	kHz
S_{9kHz}	35	31	36		42		dB
S_{18kHz}	52	49	54		64		dB
S_{27kHz}	63	58	66		74		dB

* The beginning of an arrow indicates the beginning of a winding; N1 is always the inner winding, N2 the outer winding.

Table 1 Data for IF filters shown in Fig.10 (Filter 1 to 4) and Fig.11 (Filter 5). Criteria for adjustment is IF = maximum (optimum selectivity curve at centre frequency f_O = 455 kHz). Filter 5 is used for AM stereo application with centre frequency f_O = 450 kHz.

INTEGRATED FM TUNER FOR RADIO RECEIVERS

GENERAL DESCRIPTION

The TDA1574 is a monolithic integrated FM tuner circuit designed for use in the r.f./i.f. section of car radios and home-receivers. The circuit comprises a mixer, oscillator and a linear i.f. amplifier for signal processing, plus the following additional features.

Features

- Keyed automatic gain control (a.g.c.)
- Regulated reference voltage
- Buffered oscillator output
- Electronic standby switch
- Internal buffered mixer driving

QUICK REFERENCE DATA

Supply voltage range (pin 15)	V_P		7 to 16 V
Mixer input bias voltage (pins 1 and 2)	$V_{1,2-4}$	typ.	1 V
noise figure	NF	typ.	9 dB
Oscillator output voltage (pin 6)	V_{6-4}	typ.	2 V
output admittance at pin 6 for f = 108,7 MHz	Y22	typ.	1,5 + j2 mS
Oscillator output buffer			
D.C. output voltage (pin 9)	V_{9-4}	typ.	6 V
Total harmonic distortion	THD	typ.	−15 dBC
Linear i.f. amplifier output voltage (pin 10)	V_{10-4}	typ.	4,5 V
noise figure at R_S = 300 Ω	NF	typ.	6,5 dB
Keyed a.g.c. output voltage range (pin 18)	V_{18-4}	+ 0,5 to V_P−0,3	V

PACKAGE OUTLINE

18-lead DIL; plastic (SOT102).

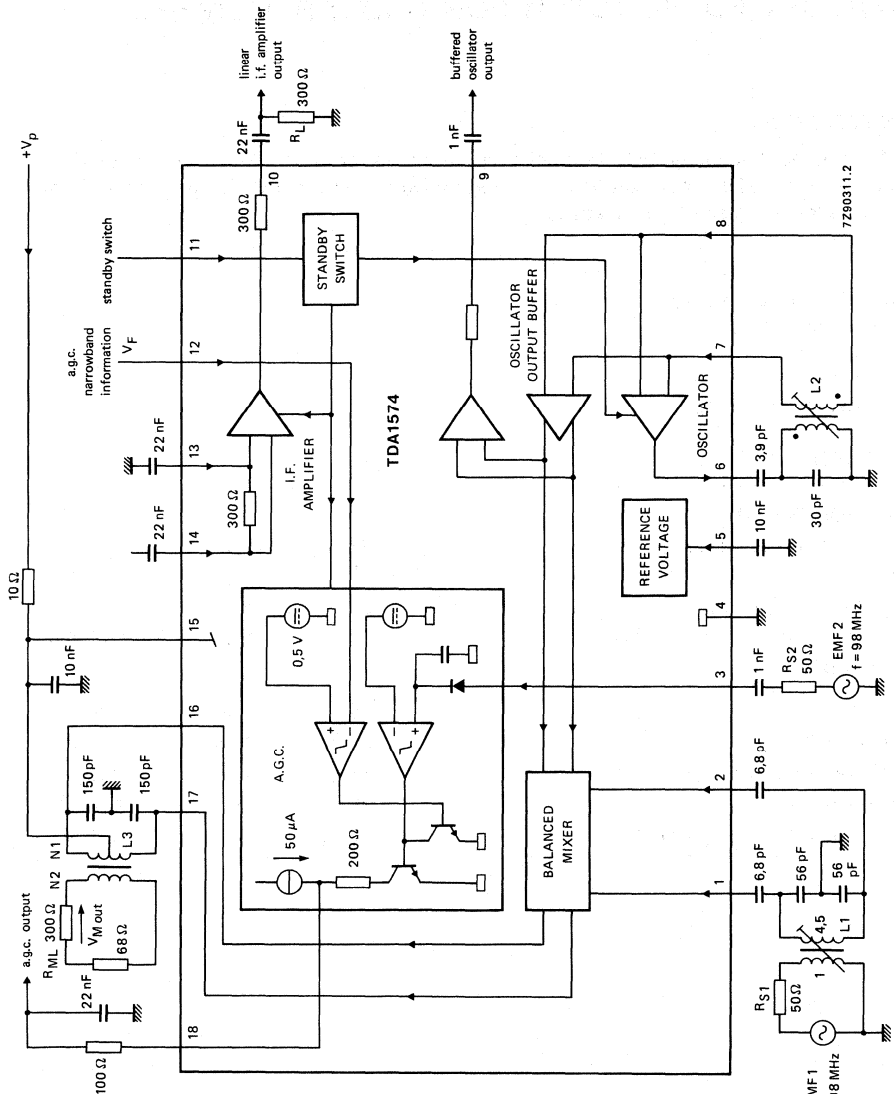


Fig. 1 Block diagram and test circuit.

Coil data

L1: TOKO MC 108, 514HNE 150014S14; L = 0,078 µH
L2: TOKO MC 111, E516HNS 200057; L = 0,08 µH
L3: TOKO coil set 7P, N1 = 5,5 + 5,5 turns, N2 = 4 turns

FUNCTIONAL DESCRIPTION

Mixer

The mixer circuit is a double balanced multiplier with a preamplifier (common base input) to obtain a large signal handling range and a low oscillator radiation.

Oscillator

The oscillator circuit is an amplifier with a differential input. Voltage regulation is achieved by utilizing the symmetrical tanh-transfer-function to obtain low order 2nd harmonics.

Linear IF amplifier

The IF amplifier is a one stage, differential input, wideband amplifier with an output buffer.

Keyed AGC

The AGC processor combines narrow- and wideband information via an RF level detector, a comparator and an ANDing stage. The level dependent, current sinking output has an active load, which sets the AGC threshold.
The AGC function can either be controlled by a combination of wideband and narrowband information (keyed AGC), or by a wideband information only, or by narrowband information only. If only narrowband AGC is wanted pin 3 should be connected to pin 5. If only wideband AGC is wanted pin 12 should be connected to pin 13.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 15)	$V_P = V_{15-4}$	max.	18	V
Mixer output voltage (pins 16 and 17)	$V_{16,\ 17-4}$	max.	35	V
Standby switch input voltage (pin 11)	V_{11-4}	max.	23	V
Reference voltage (pin 5)	V_{5-4}	max.	7	V
Field strength input voltage (pin 12)	V_{12-4}	max.	7	V
Total power dissipation	P_{tot}	max.	800	mW
Storage temperature range	T_{stg}	−55 to +	150	°C
Operating ambient temperature range	T_{amb}	−40 to +	85	°C

THERMAL RESISTANCE

From junction to ambient (in free air)	$R_{th\ j\text{-}amb}$	=	80	K/W

Note

All pins are short-circuit protected to ground.

CHARACTERISTICS

$V_P = V_{15-4} = 8{,}5$ V; $T_{amb} = 25$ °C; measured in test circuit Fig. 1; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply (pin 15)					
Supply voltage	$V_P = V_{15-4}$	7	–	16	V
Supply current (except mixer)	$I_P = I_{15}$	16	23	30	mA
Reference voltage (pin 5)	V_{5-4}	3,9	4,1	4,4	V
Mixer					
D.C. characteristics					
Input bias voltage (pins 1 and 2)	$V_{1,2-4}$	–	1	–	V
Output voltage (pins 16 and 17)	$V_{16,17-4}$	4	–	35	V
Output current (pin 16 + pin 17)	$I_{16} + I_{17}$	–	4,0	–	mA
A.C. characteristics (f_i = 98 MHz)					
Noise figure	NF	–	9	–	dB
Noise figure including transforming network	NF	–	11	–	dB
3rd order intercept point	$EMF1_{IP3}$	–	115	–	dBμV
Conversion power gain $10 \log \frac{4\ (V_{M(out)}\ 10{,}7\ MHz)^2}{(EMF1\ 98\ MHz)^2} \times \frac{R_{S1}}{R_{ML}}$	G_P	–	14	–	dB
Input resistance (pins 1 and 2)	$R_{1,2-4}$	–	14	–	Ω
Output capacitance (pins 16 and 17)	$C_{16,17}$	–	13	–	pF
Oscillator					
D.C. characteristics					
Input voltage (pins 7 and 8)	$V_{7,8-4}$	–	1,3	–	V
Output voltage (pin 6)	V_{6-4}	–	2	–	V
A.C. characteristics (f_{osc} = 108,7 MHz)					
Residual FM (Bandwidth 300 Hz to 15 kHz); de-emphasis = 50 μs	Δf	–	2,2	–	Hz

parameter	symbol	min.	typ.	max.	unit
Linear i.f. amplifier					
D.C. characteristics					
Input bias voltage (pin 13)	V_{13-4}	–	1,2	–	V
Output voltage (pin 10)	V_{10-4}	–	4,5	–	V
A.C. characteristics (f_i = 10,7 MHz)					
Input impedance					
	R_{14-13}	240	300	360	Ω
	C_{14-13}	–	13	–	pF
Output impedance					
	R_{10-4}	240	300	360	Ω
	C_{10-4}	–	3	–	pF
Voltage gain					
$20 \log \frac{V_{10-4}}{V_{14-13}}$	G_{VIF}	27	30	–	dB
T_{amb} = −40 to + 85 °C	ΔG_{VIF}	–	0	–	dB
1 dB compression point (r.m.s. value)					
at V_P = 8,5 V	$V_{10-4rms}$	–	750	–	mV
at V_P = 7,5 V	$V_{10-4rms}$	–	550	–	mV
Noise figure					
at R_S = 300 Ω	NF	–	6,5	–	dB
Keyed a.g.c.					
D.C. characteristics					
Output voltage range (pin 18)	V_{18-4}	0,5	–	V_P−0,3	V
A.G.C. output current					
at I_3 = ϕ or					
V_{12-4} = 450 mV; $V_{18-4} = V_P/2$	$-I_{18}$	25	50	100	μA
at V_{3-4} = 2 V and					
V_{12-4} = 1 V; $V_{18-4} = V_{15-4}$	I_{18}	2	–	5	mA

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Narrowband threshold					
at V_{3-4} = 2 V; V_{12-4} = 550 mV	V_{18-4}	–	–	1	V
at V_{3-4} = 2 V; V_{12-4} = 450 mV	V_{18-4}	V_P–0,3	–	–	V
A.C. characteristics (f_i = 98 MHz)					
Input impedance					
	R_{3-4}	–	4	–	kΩ
	C_{3-4}	–	3	–	pF
Wideband threshold (r.m.s. value) (see figures 2, 3, 4 and 5)					
at V_{12-4} = 0,7 V; $V_{18-4} = V_P/2$; I_{18} = 0	$EMF2_{rms}$	–	17	–	mV
Oscillator output buffer (pin 9)					
D.C. output voltage	V_{9-4}	–	6,0	–	V
Oscillator output voltage (r.m.s. value)					
at $R_L = \infty$; C_L = 2 pF	$V_{9-4(rms)}$	–	110	–	mV
at R_L = 75 Ω	$V_{9-4(rms)}$	30	50	–	mV
D.C. output impedance	R_{9-15}	–	2,5	–	kΩ
Signal purity					
Total harmonic distortion	THD	–	–15	–	dBC
Spurious frequencies					
at EMF1 = 0,2 V; R_{S1} = 50 Ω	f_S	–	–35	–	dBC
Electronic standby switch (pin 11)					
Oscillator; linear i.f. amplifier; a.g.c.					
at T_{amb} = –40 to + 85 °C					
Input switching voltage					
for threshold ON; $V_{18-4} = \geqslant V_P$–3 V	V_{11-4}	0	–	2,3	V
for threshold OFF; $V_{18-4} = \leqslant$ 0,5 V	V_{11-4}	3,3	–	23	V
Input current					
at ON condition; V_{11-4} = 0 V	$-I_{11}$	–	–	150	μA
at OFF condition; V_{11-4} = 23 V	I_{11}	–	–	10	μA
Input voltage					
at $I_{11} = \phi$	V_{11-4}	–	–	4,4	V

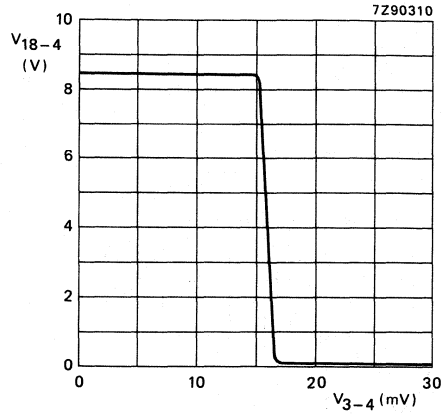


Fig. 2 Keyed a.g.c. output voltage V_{18-4} as a function of r.m.s. input voltage V_{3-4}. Measured in test circuit Fig. 1 at $V_{12-4} = 0{,}7$ V; $I_{18} = \phi$.

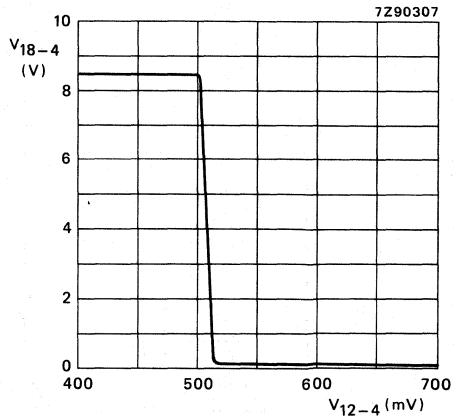


Fig. 3 Keyed a.g.c. output voltage V_{18-4} as a function of input voltage V_{12-4}. Measured in test circuit Fig. 1 at $V_{3-4} = 2$ V; $I_{18} = \phi$.

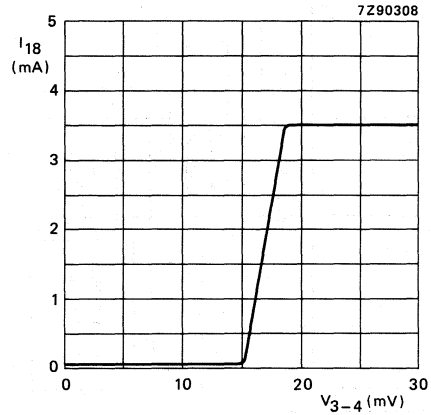


Fig. 4 Keyed a.g.c. output current I_{18} as a function of r.m.s. input voltage V_{3-4}. Measured in test circuit Fig. 1 at $V_{12-4} = 0{,}7$ V; $V_{18-4} = 8{,}5$ V.

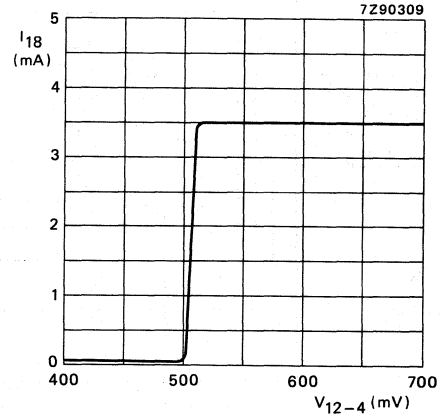


Fig. 5 Keyed a.g.c. output current I_{18} as a function of input voltage V_{12-4}. Measured in test circuit Fig. 1 at $V_{3-4} = 2$ V; $V_{18-4} = 8{,}5$ V.

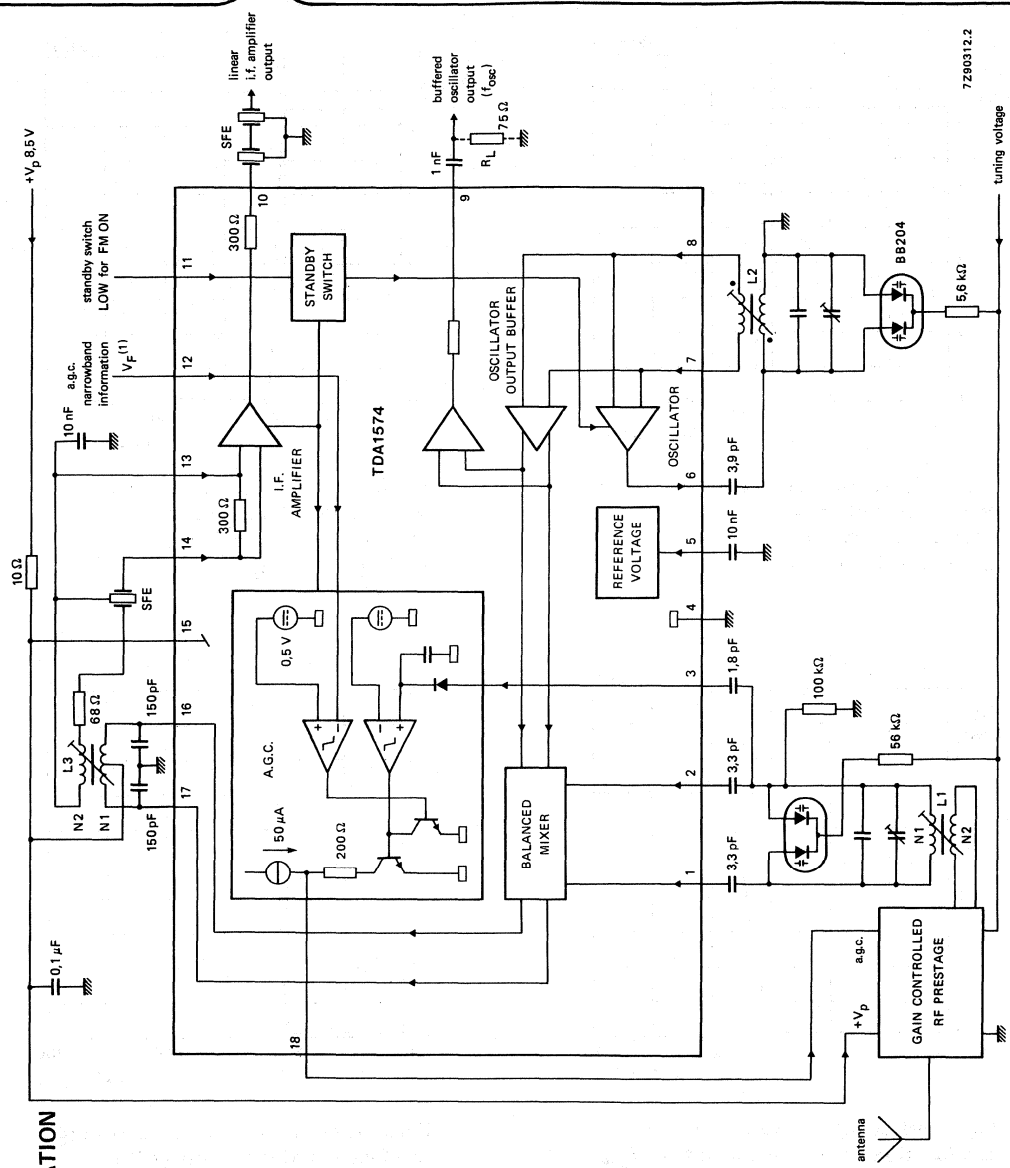


Fig. 6 TDA1574 application diagram.

APPLICATION INFORMATION

Coil data

L1: TOKO MC-108,
514HNE-15023S15,
N1 = 5,5 turns, N2 = 1 turn

L2: see Fig. 1
L3:

(1) Field strength indication of main i.f. amplifier.

INTEGRATED FM TUNER FOR RADIO RECEIVERS

GENERAL DESCRIPTION

The TDA1574T is an integrated FM tuner circuit designed for use in the RF/IF section of car radios and home-receivers. The circuit contains a mixer and an oscillator and a linear IF amplifier for signal processing. The circuit also incorporates the following features.

Features

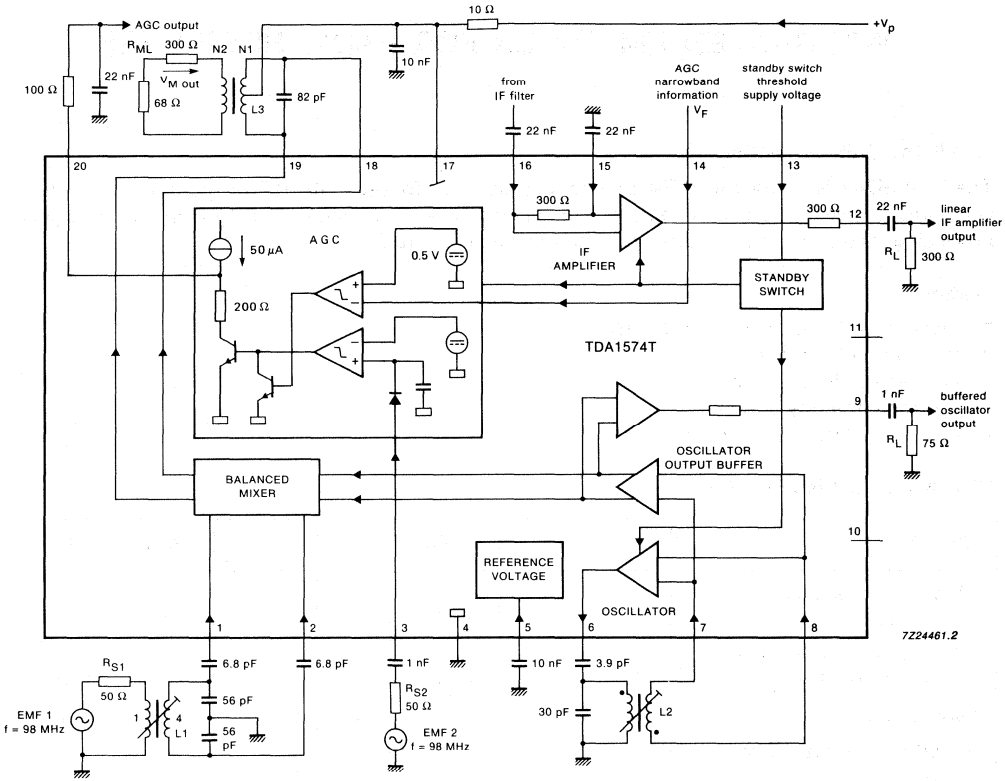
- Keyed Automatic Gain Control (AGC)
- Regulated reference voltage
- Buffered oscillator output
- Electronic standby switch
- Internal buffered mixer driving

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage range (pin 17)		V_P	7	–	14	V
Mixer input bias voltage (pins 1 and 2)		$V_{1,2-4}$	–	1	–	V
Noise factor		NF	–	9	–	dB
Oscillator output voltage (pin 6)		V_{6-4}	–	2	–	V
Output admittance at pin 6	f = 108.7 MHz	Y22	–	1.5 + j2		ms
Oscillator output buffer DC output voltage (pin 9)		V_{9-4}	–	6	–	V
Total harmonic distortion		THD	–	–15	–	dB
Linear IF amplifier output voltage (pin 12)		V_{12-4}	–	4.5	–	V
Noise factor	R_S = 300 Ω	NF	–	6.5	–	dB
Keyed AGC output voltage range (pin 20)		V_{20-4}	0.5	–	V_P–0.3	V

PACKAGE OUTLINE

20-lead mini-pack; plastic (SO20; SOT163A).



Coil data

L1: TOKO MC-108, 514HNE-150023S14; L = 0.078 μH
L2: TOKO MC-111, E516HNS-200057; L = 0.08 μH
L3: TOKO Coil set 7P, N1 = 5.5 + 5.5 turns, N2 = 4 turns

Fig.1 Block diagram and test circuit.

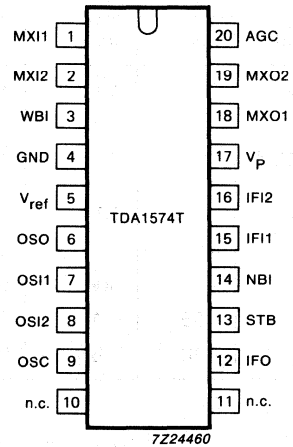


Fig.2 Pinning diagram.

PINNING

1. Mixer input 1
2. Mixer input 2
3. Wideband information input
4. Ground
5. Voltage reference
6. Oscillator output
7. Oscillator input 1
8. Oscillator input 2
9. Buffered oscillator output
10. Not connected
11. Not connected
12. IF output
13. Standby switch
14. Narrowband information input
15. IF input 1
16. IF input 2
17. Supply voltage
18. Mixer output 1
19. Mixer output 2
20. AGC output

FUNCTIONAL DESCRIPTION

Mixer

The mixer circuit uses a double balanced multiplier with a preamplifier (common base input) in order to obtain a large signal handling range and low oscillator radiation.

Oscillator

The oscillator circuit uses an amplifier with a differential input. Voltage regulation is achieved by utilizing the symmetrical tan h-transfer-function to obtain low order 2nd harmonics.

Linear IF amplifier

The IF amplifier is a one stage, differential input, wideband amplifier with an output buffer.

Keyed AGC

The AGC processor combines narrow and wideband information via an RF level detector, a comparator and an ANDing stage. The level dependent current sinking output has an active load which sets the AGC threshold.
The AGC function can either be controlled by a combination of wideband and narrowband information (keyed AGC) or by a wideband/narrowband information only. If narrowband AGC is required pin 3 should be connected to pin 5. If wideband AGC is required pin 14 should be connected to pin 15.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage (pin 17)		V_{17-4}	–	14	V
Mixer output voltage (pins 18 and 19)		$V_{18,19-4}$	–	35	V
Standby switch input voltage (pin 13)		V_{13-4}	–	23	V
Reference voltage (pin 5)		V_{5-4}	–	7	V
Total power dissipation		P_{tot}	–	500	mW
Storage temperature range		T_{stg}	–55	+ 150	°C
Operating ambient temperature range		T_{amb}	–40	+ 85	°C

THERMAL RESISTANCE

From junction to ambient (in free air) $R_{th\ j-a}$ = 95 K/W

Note to the ratings

All pins are short-circuit protected to ground.

CHARACTERISTICS

$V_P = V_{17-4} = 8.5$ V; $T_{amb} = 25$ °C; measured in test circuit Fig.1;
All measurements are with respect to ground (pin 4); unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply (pin 17)						
Supply voltage	$V_P = V_{17}$	V_{17}	7	–	14	V
Supply current (except mixer)	$I_P = I_{17}$	I_{17}	16	23	30	mA
Reference voltage (pin 5)		V_5	4.0	4.2	4.4	V
Mixer						
DC characteristics						
Input bias voltage (pins 1 and 2)		$V_{1,2}$	–	1	–	V
Output voltage (pins 18 and 19)		$V_{18,19}$	4	–	35	V
Output current (pins 18 and 19)		I_{18+19}	–	4.5	–	mA
AC characteristics	$f_i = 98$ MHz					
Noise figure		NF	–	9	–	dB
Noise figure including transforming network		NF	–	11	–	dB
3rd order intercept point		$EMF1_{IP3}$	–	115	–	dB/μV
Conversion power gain	note 1	G_{CP}	–	14	–	dB
Input resistance (pins 1 and 2)		$R_{1,2}$	–	14	–	Ω
Output capacitance (pins 18 and 19)		$C_{18,19}$	–	13	–	pF
Oscillator						
DC characteristics						
Input voltage (pins 7 and 8)		$V_{7,8}$	–	1.3	–	V
Output voltage (pin 6)		V_6	–	2	–	V
AC characteristics						
Residual FM (bandwidth = 300 Hz to 15 kHz)	de-emphasis = 50 μs	Δf	–	2.2	–	Hz
Linear IF amplifier						
DC characteristics						
Input bias voltage (pin 15)		V_{15}	–	1.2	–	V

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Output voltage (pin 12)		V_{12}	–	4.5	–	V
AC characteristics	f_i = 10.7 MHz					
Input impedance		$R_{16\text{-}15}$	240	300	360	Ω
		$C_{16\text{-}15}$	–	13	–	pF
Output impedance		R_{12}	240	300	360	Ω
		C_{12}	–	3	–	pF
Voltage gain	note 2	G_v	27	30	–	dB
Voltage gain with variation of temperature	T_{amb} = −40 to + 85 °C	ΔG_T	–	0	–	dB
1 dB compression point (RMS value)						
at V_P = 8.5 V		$V_{12(rms)}$	–	750	–	mV
at V_P = 7.5 V		$V_{12(rms)}$	–	550	–	mV
Signal-to-noise ratio	R_S = 300 Ω	S/N	–	6.5	–	dB
Keyed AGC						
DC characteristics						
Output voltage range (pin 20)		ΔV_{20}	0.5	–	V_P−0.3	V
AGC output current at I_3 = 0 or V_{14} = 450 mV; V_{20} = V_P/2		$-I_{20}$	25	50	100	μA
at V_3 = 2 V and V_{14} = 1 V; V_{20} = V_{15}		I_{20}	2	–	5	mA
Narrowband threshold						
at V_3 = 2 V; V_{14} = 550 mV		V_{20}	–	–	1	V
at V_3 = 2 V; V_{14} = 450 mV		V_{20}	V_P−0.3	–	–	V
AC characteristics	f_i = 98 MHz					
Input impedance		R_3	–	4	–	kΩ
		C_3	–	3	–	pF

parameter	conditions	symbol	min.	typ.	max.	unit
Wideband threshold (RMS value) (see Figs 3, 4, 5 and 6) at V_{14} = 0.7 V; $V_{20} = V_P/2$; $I_{20} = 0$		$EMF_{2(rms)}$	–	17	–	mV
Oscillator output buffer (pin 9)						
DC output voltage		V_9	–	6	–	V
Oscillator output voltage (RMS value)						
at R_L = oo; C_L = 2 pF		$V_{9(rms)}$	–	110	–	mV
at R_L = 75 Ω		$V_{9(rms)}$	30	50	–	mV
DC output resistance		$R_{9\text{-}17}$	–	2.5	–	kΩ
Signal purity						
Total harmonic distortion		THD	–	–15	–	dB
Spurious frequencies at EMF1 = 1 V; R_{S1} = 50 Ω		f_S	–	–35	–	dB
Electronic standby switch (pin 11)						
Oscillator; linear IF amplifier; AGC	T_{amb} = –40 to + 85 °C					
Input switching voltage						
for threshold ON	$V_{20} => V_P$–3 V	V_{13}	0	–	2.3	V
for threshold OFF	$V_{20} =< 0.5$ V	V_{13}	3.3	–	23	V
Input current						
at ON condition	V_{13} = 0 V	$-I_{13}$	–	–	150	μA
at OFF condition	V_{13} = 23 V	$-I_{13}$	–	–	10	μA
Input voltage	I_{13} = 0	V_{13}	–	–	4.4	V

Notes to the characteristics

1. Power gain conversion is equated by the following equation:

$$10 \log \frac{4\,(V_{M(out)}\ 10.7\ MHz)^2}{(EMF1\ 98\ MHz)^2} \times \frac{R_{S1}}{R_{ML}}$$

2. Voltage gain is equated by the following equation:

$$20 \log \frac{V_{12}}{V_{16\text{-}15}}$$

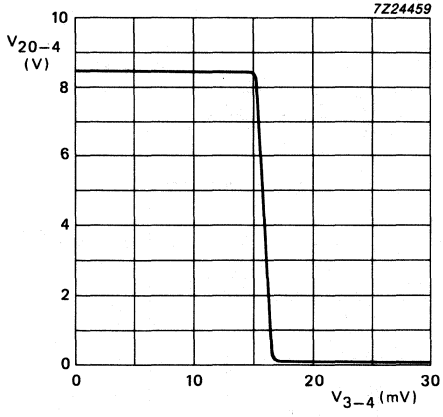


Fig.3 Keyed AGC output voltage V_{20} as a function of RMS input voltage V_3. Measured in test circuit Fig.1 at V_{14} = 0.7 V; I_{20} = 0.

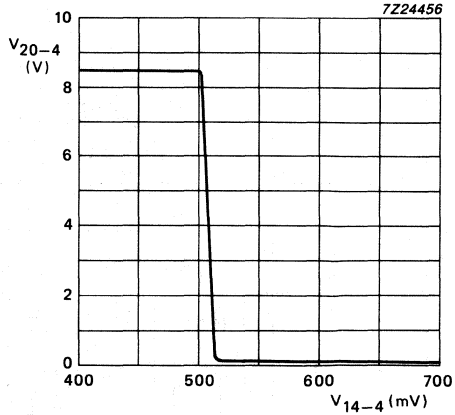


Fig.4 Keyed AGC output voltage V_{20} as a function of input voltage V_{14}. Measured in test circuit Fig.1 at V_3 = 2 V; I_{20} = 0.

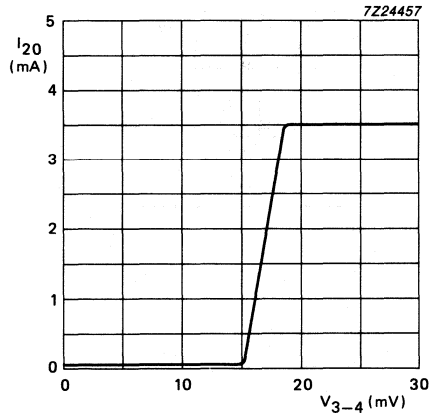


Fig.5 Keyed AGC output current I_{20} as a function of RMS input voltage V_3. Measured in test circuit Fig.1 at V_{14} = 0.7 V; V_{20} = 8.5 V.

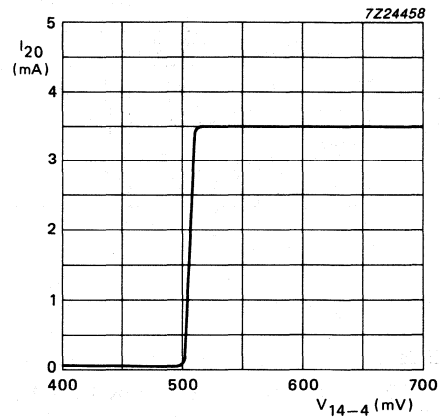
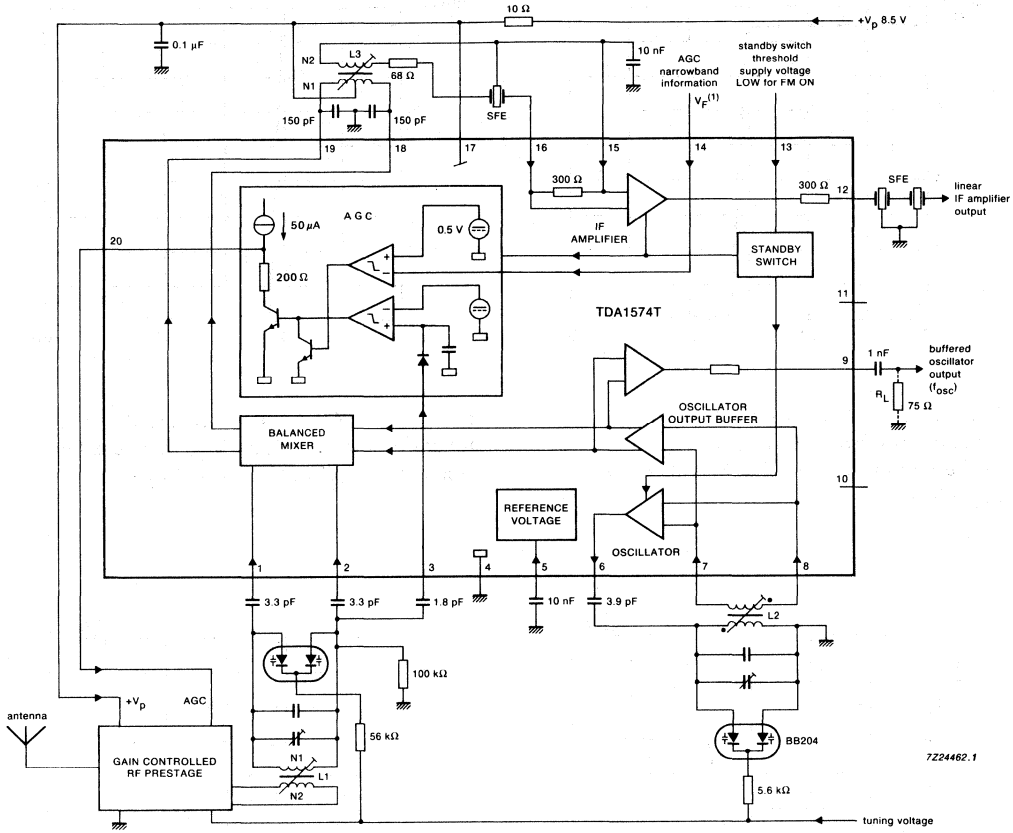


Fig.6 Keyed AGC output voltage I_{20} as a function of input voltage V_{14}. Measured in test circuit Fig.1 at V_3 = 2 V; V_{20} = 8.5 V.



Coil data

L1: TOKO MC-108, N1 = 5.5 turns, N2 = 1 turn

L2: } see Fig.1
L3: }

(1) Field strength indication of main IF amplifier.

Fig.7 TDA1574T application diagram.

FM front end circuit for CENELEC EN 55020 applications

TDA1575T

FEATURES

- Bipolar integrated FM front end circuit, designed for use in car radios and home receivers
- Fulfills CENELEC EN 55020 requirements
- Radio frequency range of 76 to 90 MHz (Japan) or 87.5 to 108 MHz (Europe, USA)
- Low noise oscillator, buffered oscillator output
- Double balanced mixer
- Internal buffered mixer driving
- Linear IF amplifier, suitable for ceramic IF filters
- Regulated reference voltage

QUICK REFERENCE DATA

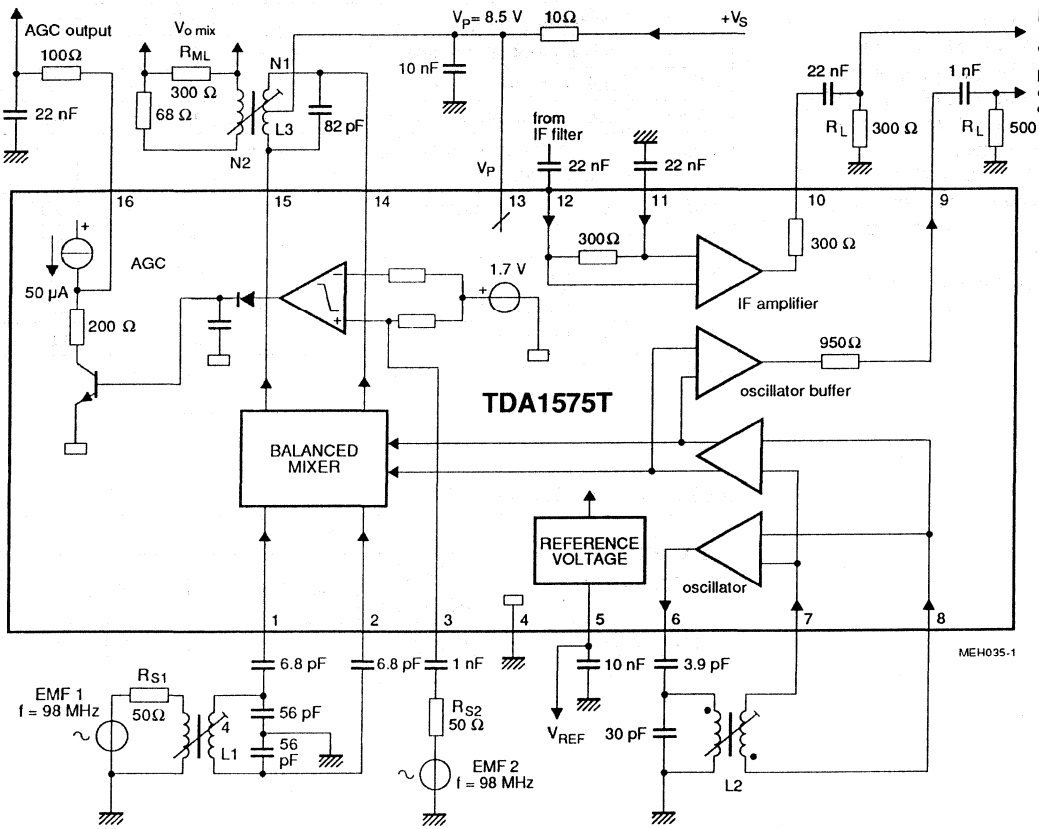
SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage	7	8.5	10	V
I_P	supply current, without mixer	–	23	–	mA
V_{REF}	reference voltage output	–	4.2	–	V
Z_I	mixer input impedance	–	14	–	Ω
NF	noise figure of mixer	–	9	–	dB
EMF1	3rd order intermodulation	–	115	–	dBμV
V_{OSC}	oscillator buffer output signal (RMS value)	75	–	–	mV
THD	total harmonic distortion	–	–15	–	dBC
G_V	IF gain	–	30	–	dB
NF	IF noise figure	–	6.5	–	dB
Z_I	IF input impedance	–	300	–	Ω
Z_O	IF output impedance	–	300	–	Ω
EMF2	AGC wideband threshold (RMS value)	–	17	–	mV

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA1575T	16	mini-pack	plastic	SOT109A

FM front end circuit for CENELEC EN 55020 applications

TDA1575T



Coils TOKO
L1: MC-108 514 HNE-150023S14; L = 78 nH, N = 4 turns
L2: MC-111 E516 HNS-200057; L = 80 nH
L3: A119 ACS-17114 FTT

Fig.1 Block diagram and test circuit.

FM front end circuit for CENELEC EN 55020 applications

TDA1575T

PINNING

SYMBOL	PIN	DESCRIPTION
MIXI1	1	RF input 1 to mixer
MIXI2	2	RF input 2 to mixer
AGCI	3	HF input to automatic gain control
GND	4	ground (0 V)
V_{REF}	5	reference voltage output
OSCO	6	oscillator output
OSCI1	7	oscillator input 1
OSCI2	8	oscillator input 2
LO	9	buffered oscillator output
IFO	10	linear FM IF output
IFI1	11	FM IF input 1
IFI2	12	FM IF input 2
V_P	13	supply voltage (+8.5 V)
MIXO1	14	mixer output 1
MIXO2	15	mixer output 2
AGCO	16	automatic gain control output

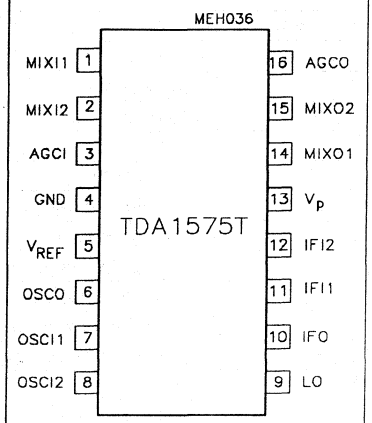


Fig.2 Pin configuration.

LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_P	supply voltage (pin 13)	0	12	V
$V_{14, 15}$	voltage at mixer output	0	V_P	V
P_{tot}	total power dissipation	0	380	mW
T_{stg}	storage temperature range	−55	+150	°C
T_{amb}	operating ambient temperature range	−40	+85	°C
V_{ESD}	electrostatic handling (see note 1)			
	all pins except 3 and 10	−	±2000	V
	pin 3	−	+2000	V
		−	−1000	V
	pin 10	−	+1500	V
		−	−2000	V

Note to the limiting values

1. Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

CHARACTERISTICS

V_P = 8.5 V and T_{amb} = +25 °C, measurements taken in Fig.1 with f_0 = 98 MHz (EMF1) unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage (pin 13)		7	8.5	10	V
I_P	supply current	without mixer	16	23	30	mA
V_{REF}	reference voltage (pin 5)	$I_5 \leq 3$ mA	3.9	4.2	4.4	V
Mixer		EMF1 = 98 MHz				
I_{14+15}	mixer supply current (pins 14 and 15)		–	4	–	mA
$V_{1,2}$	DC voltage input (pins 1 and 2)		–	1	–	V
$Z_{1,2}$	input impedance		–	14	–	Ω
$V_{14,15}$	DC output voltage (pins 14 and 15)		4	–	10	V
$C_{14,15}$	output capacitance		–	13	–	pF
G_P	conversion power gain	note 1	–	14	–	dB
$EMF1_{IP3}$	3rd order intercept point		–	115	–	dBμV
NF	noise figure		–	9	–	dB
	total noise figure	including transforming network	–	11	–	dB
Oscillator		f_{OSC} = 108.7 MHz				
$V_{7,8}$	DC input voltage (pins 7 and 8)		–	1.3	–	V
V_6	DC output voltage (pin 6)		–	2.0	–	V
Δf	residual FM at pin 6	f = 300 to 15000 Hz; de-emphasis 50 μs	–	2.2	–	Hz
Oscillator buffered output (pin 9)						
V_O	output signal (RMS value)	R_L = 500 Ω; C_L = 2 pF	75	–	–	mV
V_9	DC output voltage		–	6	–	V
R_9	DC output resistor		–	950	–	Ω
THD	total harmonic distortion		–	–15	–	dBC
f_S	spurious frequencies	EMF1 = 2 V; R_S = 50 Ω; f_{OSC} = 108.7 MHz	–	–37	–	dBC
Automatic gain control (AGC)		f_i = 98 MHz				
R_3	input resistance (pin 3)		–	4	–	kΩ
C_3	input capacitance		–	3	–	pF
V_{16}	AGC output swing (DC)	Figs 3 and 4	0.5	–	V_P – 0.3	V
I_{16}	output current at I_3 = 0	V_{16} = 1/2 V_P	–25	–50	–150	μA
	output current at U_3 = 2 V	V_{16} = 7 to 10 V	2	–	5	mA
EMF2	threshold (RMS value)	I_{16} = 0; V_{16} = 1/2 V_P; Figs 4 and 5	–	17	–	mV

FM front end circuit for CENELEC EN 55020 applications

TDA1575T

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Linear IF amplifier		IF = 10.7 MHz				
$V_{11,12}$	DC input voltage (pins 11 and 12)		–	1.25	–	V
Z_{12-11}	input impedance		240	300	360	Ω
C_{12-11}	input capacitance		–	13	–	pF
V_{10}	DC output voltage (pin 10)		–	4.4	–	V
Z_{10}	output impedance		240	300	360	Ω
C_{10}	output capacitance		–	3	–	pF
V_O	output signal (RMS value)	–1 dB compression	–	–	650	mV
G_v	IF voltage gain (20 log (V_{10-4} / V_{12-11}))		27	30	–	dB
ΔG_v	IF voltage gain deviation	T_{amb} = –40 to +85 °C	–	0	–	dB
NF	noise figure	R_S = 300 Ω	–	6.5	–	dB

Note to the characteristics

1. G_P = 10 log (4$V_{o\,mix}$ x 10.7 MHz) / (EMF2 x 98 MHz)^2 x (R_{S1} / R_{ML}).

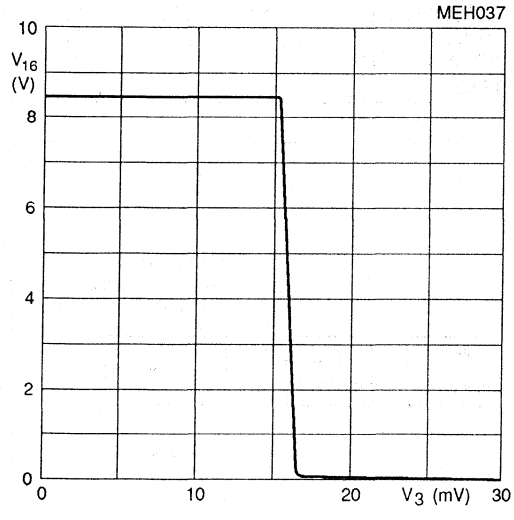


Fig.3 AGC output voltage V_{16} as a function of V_{i3} RMS at I_{16} = 0, measured in test circuit Fig.1.

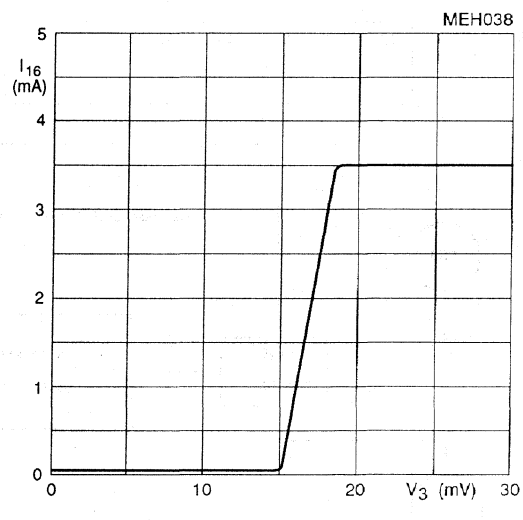


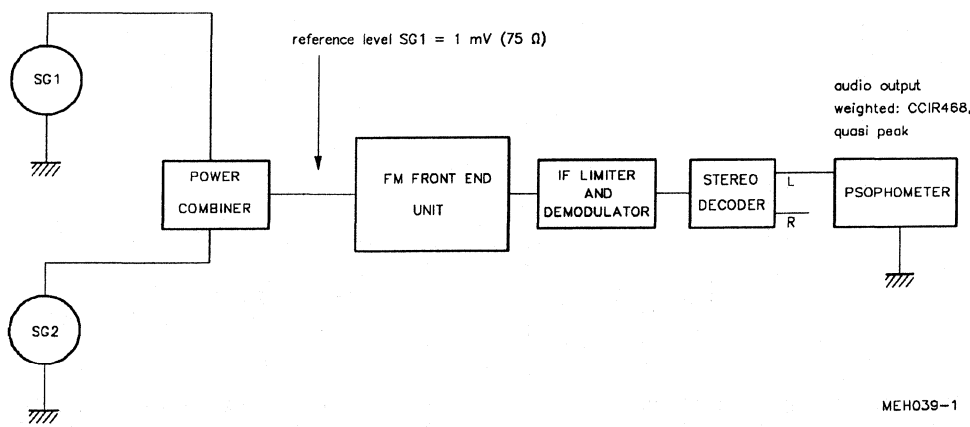
Fig.4 AGC output current I_{16} as a function of V_{i3} RMS at V_{16} = 8.5 V, measured in test circuit Fig.1.

APPLICATION INFORMATION

Operating characteristics

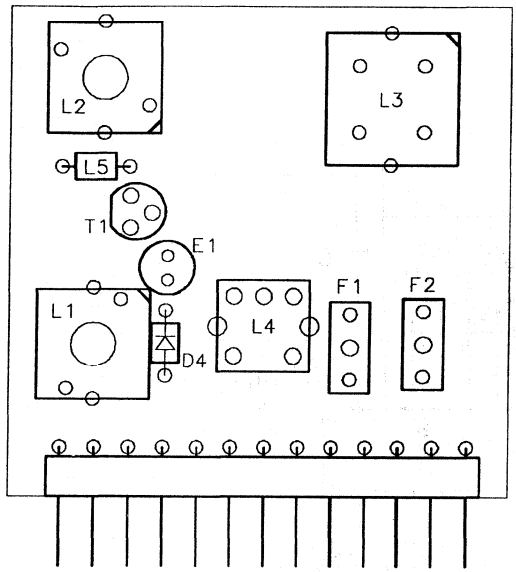
Measured in application circuit Fig.7, according to CENELEC EN 55020, Chapter 4.1 (passive interference suppression). Measurements are shown in Figs 8 and 9.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_S	supply voltage		7	8.5	10	V
I_S	total supply current		–	37	–	mA
f_{RF}	tuning range of RF input		87.5	–	108	MHz
V_{tune}	tuning voltage of RF input		1	–	7	V
G	gain (20 log $V_{O\,IF}$ / V_{ant})		–	43	–	dB
$V_{i\,ant}$	input sensitivity	S/N = 26 dB; R_{ant} = 150 Ω	–	2	–	μV
IR	image rejection	f = 98 MHz	–	64	–	dB
RSS	repeat spot suppression	f = 98 MHz; $V_{i\,ant}$ = 10 μV	–	89	–	dB
DBS	double beat suppression	f1 = 93 MHz; f2 = 98 MHz				
	DBS1	f_{tune} = 88 MHz	–	81	–	dB
	DBS2	f_{tune} = 103 MHz	–	80	–	dB
	DBS3	f_{tune} = 90.15 MHz	–	85	–	dB
CBS	continuous beat suppression	f1 = 90 MHz; f2 = 100.7 MHz f_{tune} = 95 MHz	–	90	–	dB

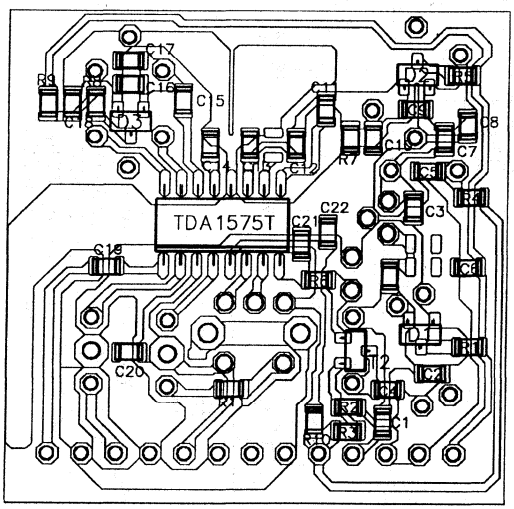


SG1: Wanted carrier; modulated with f = 1 kHz, Δf = ±40 kHz (for audio reference)
SG2: Unwanted carrier; modulated with f = 1 kHz, FM: Δf = ±40 kHz (in band) or AM: m = 80% (out of band) increase level of SG2 until S/N = 26 dB w.r.t. wanted modulation (for car radio, home radio S/N = 40 dB)

Fig.5 Set-up for CENELEC EN 55020 passive interference measurements.



Component Side



MEH040

SMD and Track Side

Fig.6 PCB layout of FM front end unit.

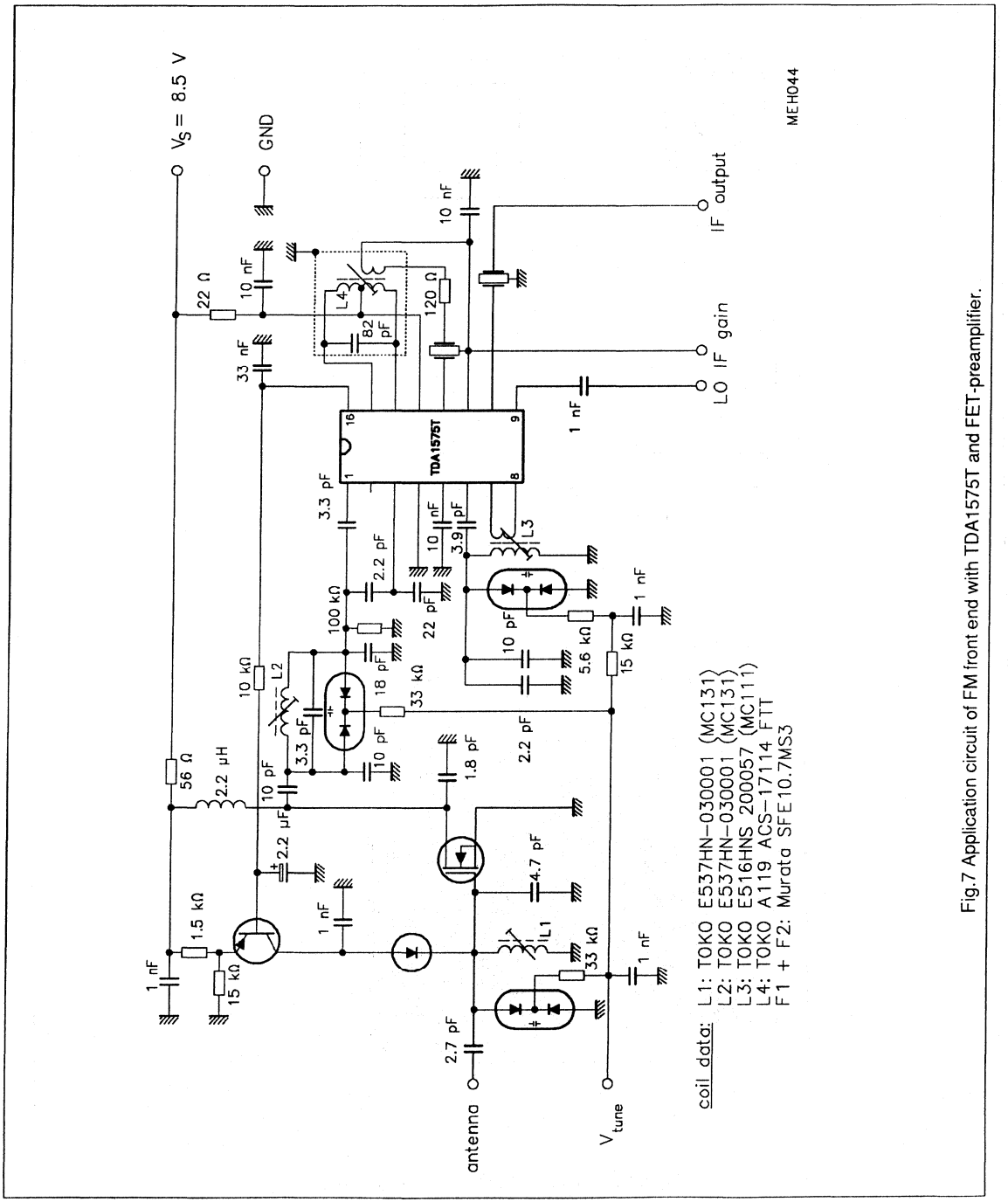


Fig.7 Application circuit of FM front end with TDA1575T and FET-preamplifier.

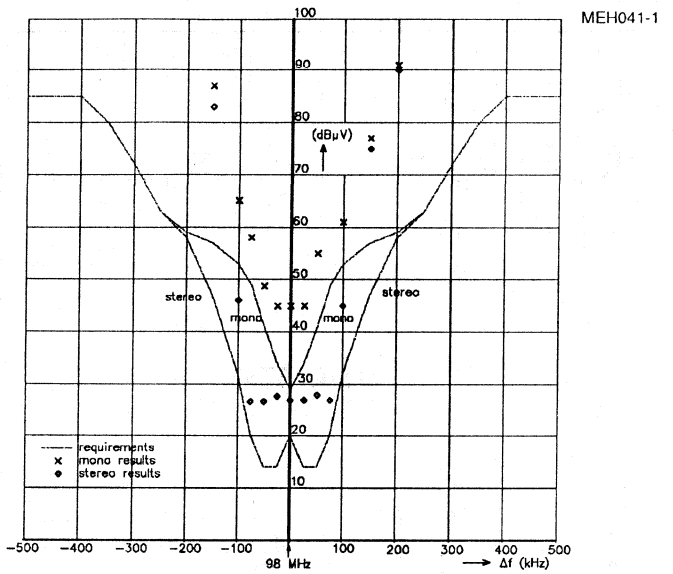


Fig.8 Interference level as a function of detuning for S/N = 26 dB; IN-BAND passive interference (CENELEC EN 55020).

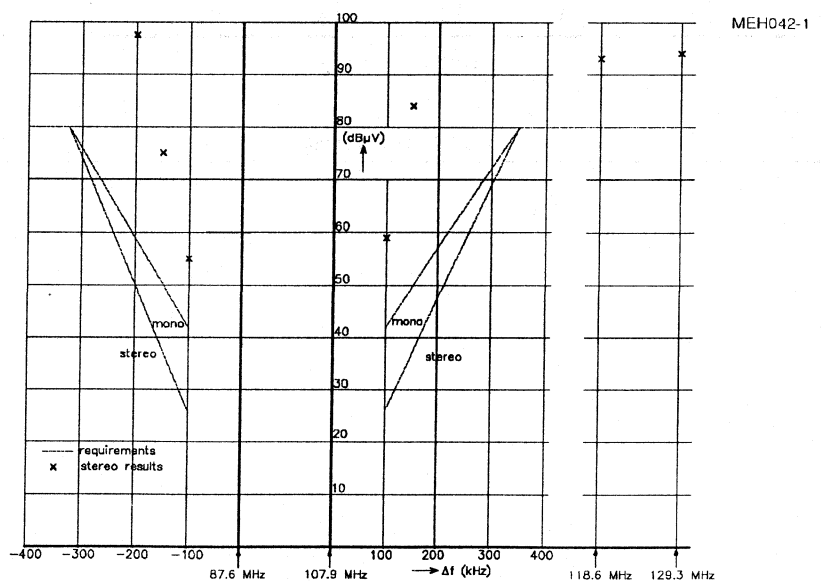


Fig.9 Interference level as a function of detuning for S/N = 26 dB; OUT-OF-BAND passive interference (CENELEC EN 55020).

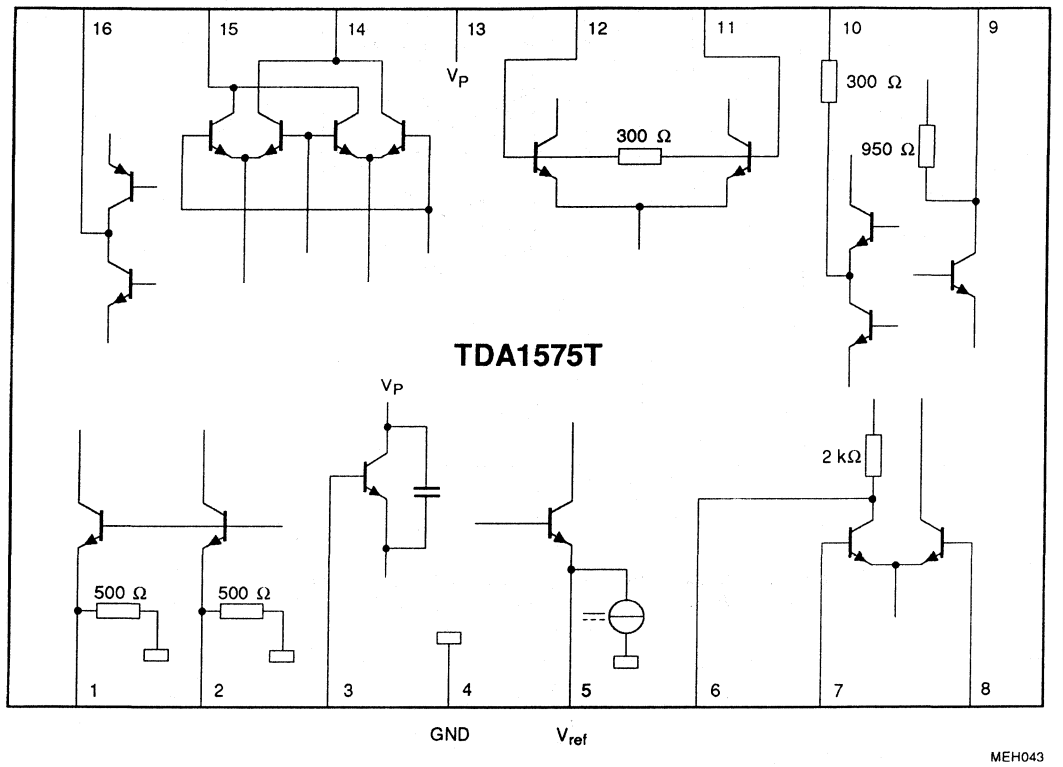


Fig.10 Internal circuits.

Philips Semiconductors

Data sheet	
status	Preliminary specification
date of issue	February 1991

TDA1576T
FM-IF amplifier/demodulator circuit

FEATURES

- Fully balanced 4-stage limiting IF amplifier
- Symmetrical quadrature demodulator
- Field-strengh indication output for 1 mA ammeter
- Detune detector for side response and noise attenuation
- Detune voltage output
- Internal muting circuit
- 0° and 180° AF output signals
- Reference voltage output
- Electronic smoothing of the supply voltage

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage range (pin 1)	7.5	8.5	15	V
I_P	supply current	10	16	23	mA
V_{iIF}	input sensivity (RMS value)				
	–3 dB before limiting	14	22	35	μV
	S/N = 26 dB	-	10	-	μV
	S/N = 46 dB	-	55	-	μV
V_{oAF}	AF output signal (RMS value)	-	67	-	mV
THD	total harmonic distortion with double resonant circuits	-	0.02	-	%
S/N	signal-to-noise ratio (V_i > 1 mV)	-	72	-	dB
α_{AM}	AM suppression	-	50	-	dB
RR	ripple rejection (f = 100 Hz)	43	48	-	dB
I_{15}	maximum indicator output current	-	-	2	mA
T_{amb}	operating ambient temperature	–30	-	+80	°C

GENERAL DESCRIPTION

The TDA1576T is a monolithic integrated FM-IF amplifier circuit for use in mono and stereo FM-receivers of car radios or home sets.

ORDERING AND PACKAGE INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA1576T	20	mini-pack	plastic	SOT163A

FM-IF amplifier/demodulator circuit TDA1576T

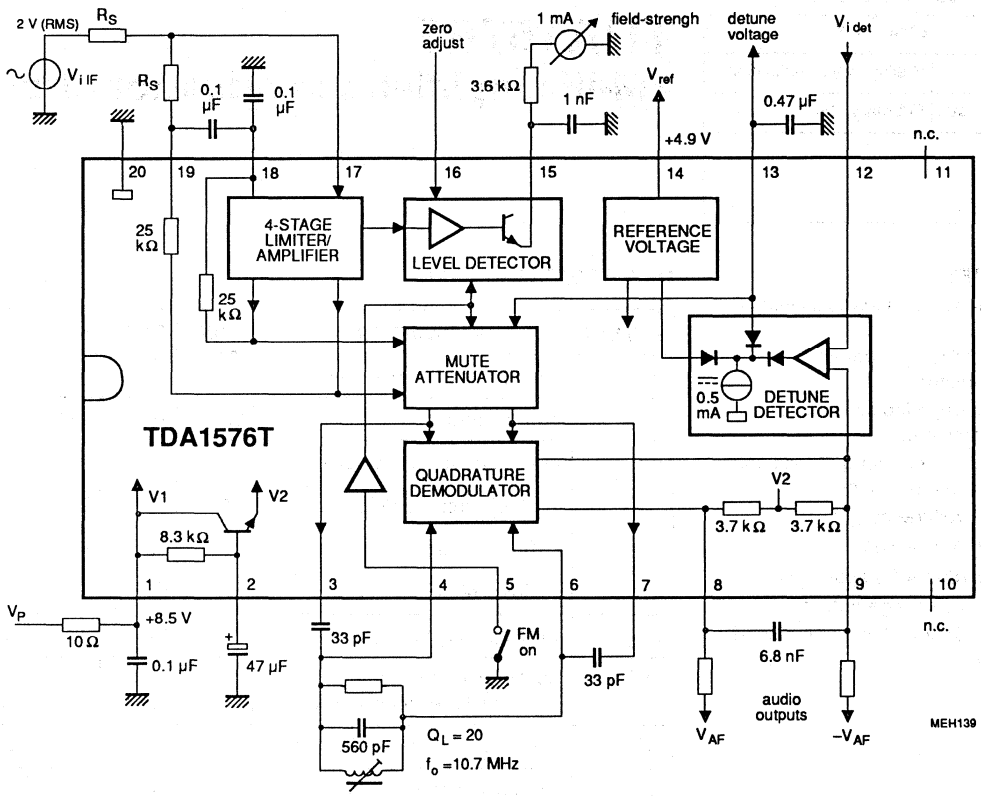


Fig.1 Block diagram and application circuit.

FM-IF amplifier/demodulator circuit TDA1576T

PINNING

SYMBOL	PIN	DESCRIPTION
V_P	1	positive supply voltage
C_{PS}	2	smoothing capacitor of power supply
IF1	3	IF signal to resonant circuit
RES1	4	resonant circuit
FMON	5	FM-ON, standby switch
RES2	6	resonant circuit
IF2	7	IF signal to resonant circuit
$V_{o\ AF1}$	8	AF output voltage (0° phase)
$V_{o\ AF2}$	9	AF output voltage (180° phase)
n.c.	10	not connected
n.c.	11	not connected
$V_{i\ det}$	12	detune detector input for external audio reference
$V_{o\ det}$	13	detune detector output voltage
V_{ref}	14	reference voltage output
V_F	15	level output for field-strengh
$V_{F\ o}$	16	zero adjust for field-strengh
$V_{i\ IF}$	17	FM-IF input signal
IN2	18	input 2 of differential IF amplifier
IFLV	19	IF input level
GND	20	ground (0 V)

PIN CONFIGURATION

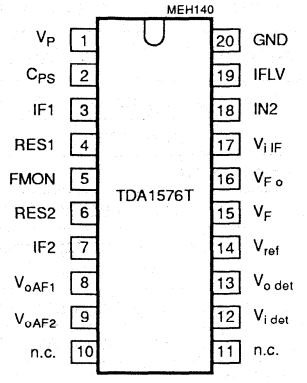


Fig.2 Pin configuration.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_P	supply voltage (pin 1)	0	15	V
$V_{2, 5, 16}$	voltage on pins 2, 5 and 16	0	V_P	V
P_{tot}	total power dissipation	0	450	mW
T_{stg}	storage temperature range	–55	150	°C
T_{amb}	operating ambient temperature range	–30	+85	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
$R_{th\ j\text{-}a}$	from junction to ambient in free air	-	85	K/W

CHARACTERISTICS

V_P = 8.5 V; $f_{i\,ZF}$ = 10.7 MHz; R_S = 60 Ω; f_m = 400 Hz with Δf = ±22.5 kHz; 50 µs de-emphasis ($C_{8\text{-}9}$ = 6.8 nF); T_{amb} = 25 °C and measurements taken in Fig.1, unless otherwise specified. The demodulator circuit is adjusted at minimum second harmonic distortion for $V_{i\,ZF}$ = 1 mV and a deviation Δf = ±75 kHz.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage range (pin 1)		7.5	8.5	15	V
I_P	supply current	$V_5 = V_9 = V_{13} = 0$	10	16	23	mA
Reference voltage						
V_{ref}	reference voltage (pin 14)	I_{14} = −1 mA	-	4.9	-	V
ΔV_{ref}	reference voltage dependence on temperature	$\Delta V_{14} / V_{14} * \Delta T$	-	0.3	-	%/K
I_{14}	maximum output current	short-circuit current	4	6	7.5	mA
R_{14}	output resistor ($\Delta V_{14} / \Delta I_{14}$)	I_{14} < 1.2 mA	-	60	150	Ω
IF amplifier						
$V_{i\,IF}$	input sensivity (RMS value, pin 17)	−3 dB before limiting	14	22	35	µV
$R_{17\text{-}18}$	input resistance	$V_{i\,IF}$ = 200 mV (RMS)	10	-	-	kΩ
$C_{17\text{-}18}$	input capacitance	$V_{i\,IF}$ = 200 mV (RMS)	-	5	-	pF
$V_{o\,IF}$	output signal at pins 3 and 7 (peak-to-peak value)	$Z_{3,7}$ = 10 pF // 1MΩ	610	680	750	mV
$R_{3\text{-}7}$	output impedance		200	250	300	Ω
Demodulator						
$R_{4\text{-}6}$	input resistance		20	30	40	kΩ
$C_{4\text{-}6}$	input capacitance		-	1	2.5	pF
$R_{8,9}$	output impedance		2.9	3.7	4.5	kΩ
$V_{8,9}$	DC offset voltage on output pins at $V_{4\text{-}6}$ = 0	V_5 > 3 V or $V_{3\text{-}7}$ = 0 or V_{13} < 0.3 V	-	0	±100	mV
$\Delta V/\Delta\varphi$	demodulator efficiency	$\Delta V_{8\text{-}9}/\Delta\varphi$	-	40	-	mV/°
	demodulator efficiency dependent on supply voltage (note 1)	K	-	6.2	-	mV/°
V/V	DC voltage ratio	$V_{8+}V_9 / 2*V_2$	0.653	0.667	0.680	V/V
$\Delta V/\Delta T$	dependence on temperature	$\Delta(V_8+V_9 / 2*V_2)/\Delta T$	-	10^{-5}	-	1/K
Field-strengh output						
V_{15}	output voltage (Fig.4)	$V_{i\,IF}$ = 0	0	0.1	0.25	V
		$V_{i\,IF}$ = 1 mV (RMS)	1.1	1.5	1.9	V
		$V_{i\,IF}$ = 250 mV (RMS)	3.2	3.6	4.1	V
S	control steepness	Fig.4	-	0.85	-	V/dec
R_{15}	output resistance		-	150	200	Ω
$\Delta V/\Delta T$	dependence on temperature	$V_{i\,IF} = \Delta V_{15} / (\Delta T * V_{15})$	-	0.3	-	%/K
I_{15}	stand-by operational cut-off current	$V_5 \geq 3$ V; V_{15} = 0 to 5 V	-	-	10	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero level adjustment						
V_{16}	internal bias voltage		-	260	-	mV
R_{16}	input resistance		-	19	-	kΩ
S	control steepness	$V_{i\ IF}$ = 100 mV; $A = \Delta V_{15}/\Delta V_{16}$	0.87	1.0	1.2	V/V
Detuning detector						
I_{12}	input bias current		-	20	100	nA
R_{12}	input resistance (Fig.5)	$5\ V/\Delta I_{12}$	6	30	-	MΩ
V_{13}/V_{14}	output voltage ratio for $\Delta\varphi = \varphi$ (pins 3-7) – φ (pins 4-6) –90°; (Fig.6)	$V_1 = V_2 = 7.5$ V; R_{13-14} = 10 kΩ; pins 9 and 12 short-circuit				
	$\Delta\varphi$ = 9.2° (43 kHz), Q = 20	$V_{9,12}$ = 334 mV	0.45	0.5	0.55	V/V
	$\Delta\varphi$ = 3.5° (16 kHz), Q = 20	$V_{9,12}$ = 138 mV	0.75	0.8	0.85	V/V
	$\Delta\varphi$ = 14° (65 kHz), Q = 20	$V_{9,12}$ = 501 mV	0.335	0.345	0.355	V/V
I_{13}	maximum output current (Fig.7)	V_{13} = 6 V	0.4	0.5	0.6	mA
	cut-off current	V_{13} = 2.5 V; $V_{9,12}$ = 0	-	-	–100	nA
Internal audio attenuation						
V_{13}/V_{14}	output voltage ratio (Fig.8)	α = attenuation factor				
	for α = 1 dB		0.11	0.12	0.13	
	for α = 7.2 dB		0.095	0.1	0.105	
	for α ≥ 40 dB		-	0.06	-	
I_{13}	input current	$V_{13} / V_{13} \leq 0.1$	-	-	–225	nA
Stand-by switch						
V_5	input voltage for FM-on	$V_{3,7} / V_{3,7(max)}$ = 0.9	2.4	2.5	-	V
	input voltage for FM-off	V_{19} = 0.3 V	-	2.9	3	V
	linear range (Fig 9)		-	350	-	mV
I_5	input current	V_5 = 0 to 2 V	-	-	–100	μA
		V_5 = 3.5 to 15 V	-	-	1	μA
$V_5/\Delta T$	temperature dependence	FM-on ($3.5V_{BE}$)	-	7	-	mV/K
		FM-off ($5V_{BE}$)	-	10	-	mV/K
Supply voltage smoothing						
V_{1-2}	internal voltage drop	proportional to $V_1 - 3V_{BE}$	80	210	400	mV
R_{1-2}	internal resistor		5.8	8.3	10.8	kΩ

OPERATING CHARACTERISTICS

V_P = 8.5 V; $f_{i\,ZF}$ = 10.7 MHz; R_S = 60 Ω; f_m = 400 Hz with Δf = ±22.5 kHz; 50 µs de-emphasis (C_{8-9} = 6.8 nF); T_{amb} = 25 °C and measurements taken in Fig.1, unless otherwise specified. The demodulator circuit is adjusted at minimum second harmonic distortion with $V_{i\,ZF}$ = 1 mV.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
IF amplifier and demodulator						
$V_{i\,IF}$	input sensivity (RMS value, pin 17)	–3 dB before AF limiting	14	22	35	µV
	input signal for S/N = 26 dB	f = 250 to 15000 Hz	-	10	-	µV
	input signal for S/N = 46 dB	f = 250 to 15000 Hz	-	55	-	µV
$V_{o\,AF}$	output signal at (RMS value, pins 8 and 9)		60	67	75	mV
$V_{o\,N}$	noise voltage for $V_{i\,IF}$ = 0 (RMS value, pins 8 and 9)	R_S = 300 Ω f = 250 to 15000 Hz	-	900	-	µV
	weighted noise voltage according to	DIN 45405	-	2	-	mV
S/N	signal-to-noise ratio Fig.3 (pin 8 and 9)	$V_{i\,IF}$ = 1 mV (RMS)	-	72	-	dB
α_{AM}	AM suppression	$V_{i\,IF}$ = 0.5 to 200 mV FM: 70 Hz, ±15 kHz AM: 1 kHz, m = 30%	-	50	-	dB
α_{FM}	FM rejection for FM-off	$V_{i\,IF}$ = 500 mV; V_5 = 3V	80	-	-	dB
$\Delta V_{8,9}$	AFC shift in relation to minimum second harmonic distortion α_{2H}	$V_{i\,IF}$ = 0.03 to 500 mV	-	25	-	mV
	DC offset at second harmonic distortion	operating	-	0	±100	mV
		mute or FM-off	-	0	±50	mV
α_{3H}	distortion for third harmonic		-	0.65	-	%
RR	ripple rejection V_{ripple} = 200 mV on V_P	f = 100 Hz	43	48	-	dB

Note to the characteristics

1. $V_{8\text{-}9} / \Delta\varphi = K(V_P - 3\,V_{BE})$

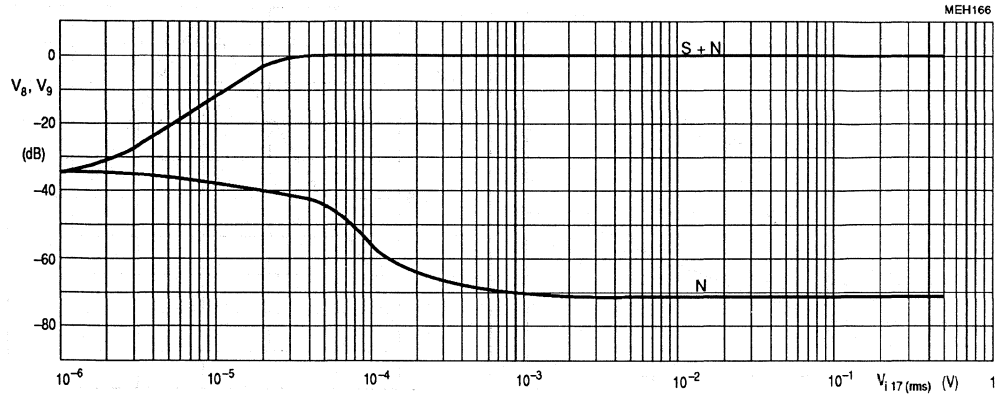


Fig.3 AF output voltage level on pins 8 and 9 as a function of $V_{i\,IF}$ at V_P = 8.5 V; f_m = 1 kHz; Q_L = 20 and with de-emphasis. S = signal; N = noise.

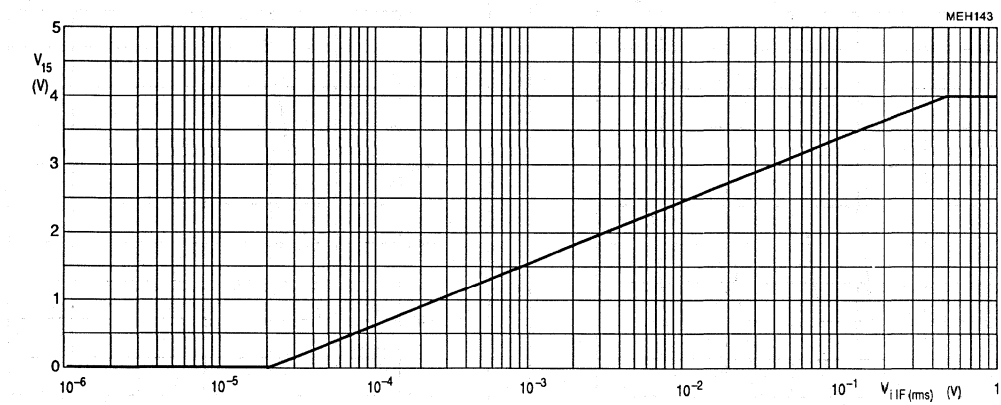


Fig.4 Field-strengh output (I_{16} = 0).

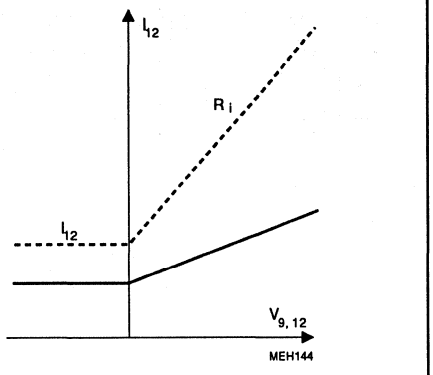


Fig.5 Detuning input impedance.

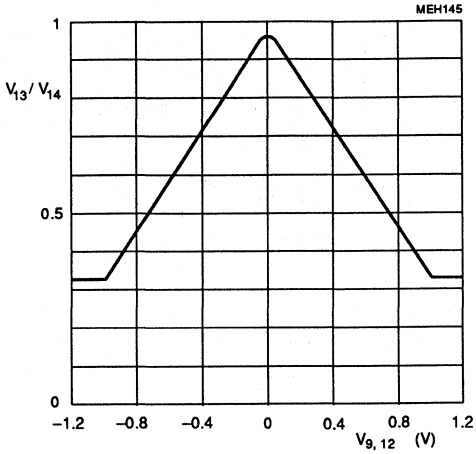


Fig.6 Detuning curve.

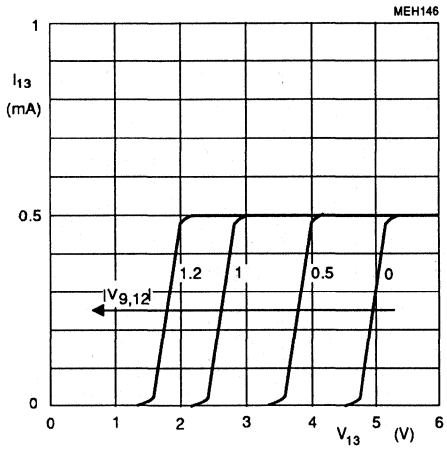


Fig.7 Detuning output.

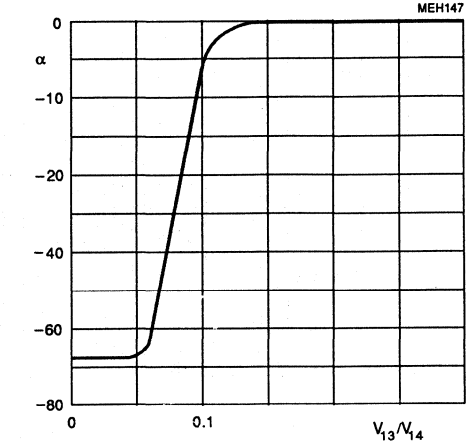


Fig.8 Internal audio attenuation.

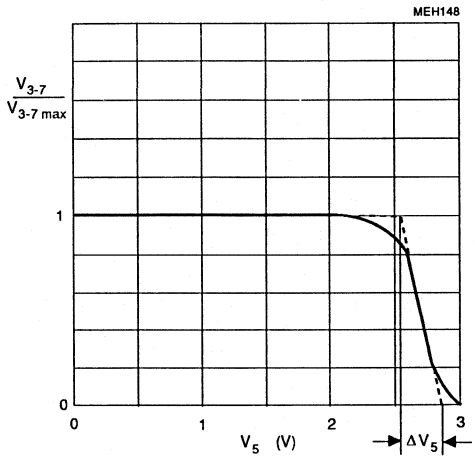


Fig.9 Stand-by switch.

TIME MULTIPLEX PLL STEREO DECODER

GENERAL DESCRIPTION

The TDA1578A is a PLL stereo decoder based on the time-division multiplex principle.

Features

- adjustable input and output voltage levels
- automatic mono/stereo switching with hysteresis, controlled by both pilot signal and field strength level
- analogue control of mono/stereo change over
- pilot indicator driver
- analogue muting control
- muting indicator driver
- oscillator with decoupled frequency measurement output
- electronic smoothing of the supply voltage

QUICK REFERENCE DATA

Measured with a frequency deviation $\Delta f = \pm 75$ kHz without pilot; $f_m = 1$ kHz						
Supply voltage (pin 8)		$V_P = V_{8-7}$	typ.	8,5	15	V
Supply current (pin 8)		$I_P = I_8$	typ.	21	30	mA
Multiplex input signal (adjustable)		$V_{MUX(p-p)}$	typ.	0,5	1	V
Input resistance (adjustable)		R_i	typ.	47		kΩ
A.F. output voltage (R = 15 kΩ)		V_o	typ.	0,75	1,5	V
Output resistance		R_o		low-ohmic		
Spread in gain		ΔG_v	⩽	1		dB
Channel separation		α	typ.	50		dB
Total harmonic distortion		THD	⩽	0,3	0,1	%
Signal-to-noise ratio		S/N	typ.	90		dB
Carrier and harmonic suppression						
pilot signal;	f = 19 kHz	α_{19}	typ.	32		dB
subcarrier;	f = 38 kHz	α_{38}	typ.	50		dB
	f = 57 kHz	α_{57}	typ.	46		dB
	f = 76 kHz	α_{76}	typ.	60		dB
traffic radio (V.W.F.);	f = 57 kHz	$\alpha_{57(VWF)}$	typ.	70		dB
SCA (Subsidiary Communications Authorization);	f = 67 kHz	α_{67}	typ.	70		dB
ACI (Adjacent Channel Interference);	f = 114 kHz	α_{114}	typ.	80		dB
intermodulation;	f = 10/13 kHz	α_2, α_3	typ.	70		dB
Supply voltage range (pin 8)		$V_P = V_{8-7}$		7,5 to 18		V
Operating ambient temperature range		T_{amb}		−30 to + 80		°C

PACKAGE OUTLINE

18-lead DIL; plastic (SOT102).

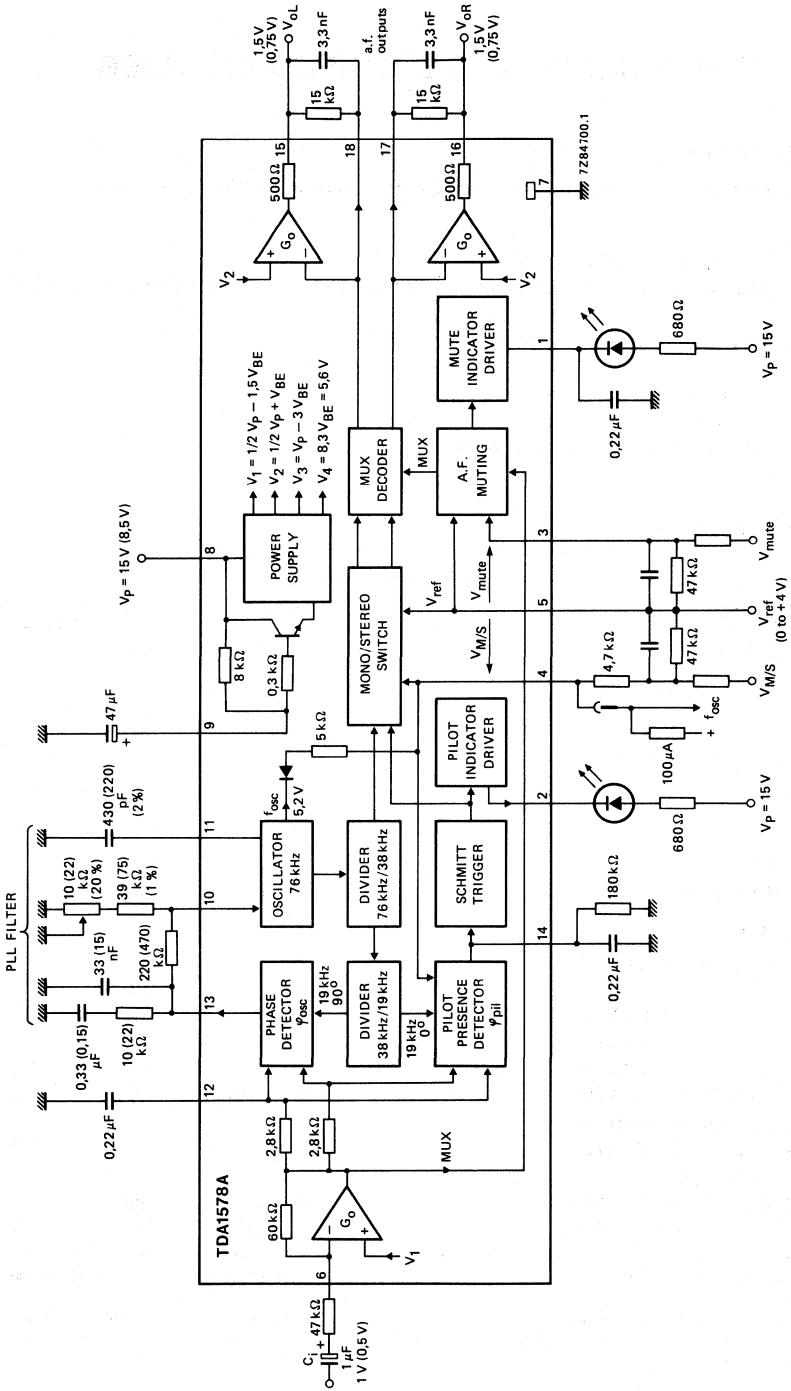


Fig. 1 Block diagram with external components; used as test circuit. Values given in parentheses are for Vp = 8,5 V.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 8)	$V_P = V_{8-7}$	max.	20	V
Input voltages (pins 3, 4 and 5)	$V_{3;4;5-7}$		0 to 12	V
Indicator driver output voltage	$V_{1;2-7}$	max.	24	V
Indicator driver output current	$I_1; I_2$	max.	30	mA
Total power dissipation at T_{amb} = 25 °C	P_{tot}	max.	1,2	W
Storage temperature range	T_{stg}		−55 to + 150	°C
Operating ambient temperature range	T_{amb}		−30 to + 80	°C

THERMAL RESISTANCE

From crystal to ambient	$R_{th\ c-a}$	=	80	K/W

CHARACTERISTICS (measured in Fig. 1)

Input signal: m = 100% ($\Delta f = \pm 75$ kHz); pilot signal: m = 9% ($\Delta f = \pm 6{,}75$ kHz);
modulation frequency: 1 kHz; $V_{3\text{-}5} = V_{4\text{-}5} = 0$ V;
de-emphasizing time: T = 50 μs; oscillator adjusted to f_{osc} at a pilot voltage $V_i = 0$ V;
$T_{amb} = 25\ ^{o}C$; unless otherwise specified

parameter	V_P (V)	symbol	min.	typ.	max.	unit
Supply voltage range (pin 8)	–	V_P	7,5	–	18	V
Supply current (except output and indicator) pin 8	8,5	I_P	–	21	–	mA
	15	I_P	–	30	40	mA
Nominal multiplex input voltage (peak-to-peak value)	8,5	$V_{MUX(p\text{-}p)}$	–	0,5	–	V
$R_i = 47$ kΩ	15	$V_{MUX(p\text{-}p)}$	–	1,0	–	V
Overdrive reserve of input						
at THD = 1 %	8,5		3	6	–	dB
at THD = 0,3 %	15		3	6	–	dB
A.F. output voltage (r.m.s. value; mono without pilot)						
$R_{15\text{-}18} = R_{16\text{-}17} = 15$ kΩ	8,5	$V_{o(rms)}$	–	0,75	–	V
	15	$V_{o(rms)}$	–	1,5	–	V
$R_{15\text{-}18} = R_{16\text{-}17} = 24$ kΩ	8,5	$V_{o(rms)}$	–	1,2	–	V
	15	$V_{o(rms)}$	–	2,4	–	V
Overdrive reserve of output $R_{15\text{-}18} = R_{16\text{-}17} = 24$ kΩ	*		3	–	–	dB
Spread in output voltage levels	*	$\pm \Delta V_o/V_o$	–	–	1	dB
Difference of output voltage levels	*	$\pm \Delta V_{15\text{-}16}/V_o$	–	–	1	dB
Output resistance	*	R_o	low-ohmic			
Available output current pins 15 and 16	*	$\pm I_o$	–	–	–	mA
Modulation range at output (unloaded)	*	$V_{15;16\text{-}7}$	–	1 to $V_{9\text{-}7} - 1$	–	V
Internal current limiting	*	I_o	–	15	–	mA
D.C. output voltage	8,5	$V_{15;16\text{-}7}$	3,6	4,1	4,6	V
$R_{15\text{-}18} = R_{16\text{-}17} = 24$ kΩ	15	$V_{15;16\text{-}7}$	7,0	7,7	8,4	V
D.C. current	8,5	$-I_{17;18}$	–	33	–	μA
(pins 17 and 18)	15	$-I_{17;18}$	–	23	–	μA

* $V_P = 8{,}5$ or 15 V.

parameter	V_P (V)	symbol	min.	typ.	max.	unit
Channel separation	8,5	α	32	50	–	dB
at V_{4-5} = 0 V	15	α	39	50	–	dB
Total harmonic distortion	8,5	THD	–	0,1	0,3	%
	15	THD	–	0,04	0,1	%
Signal-to-noise ratio	8,5	S/N	–	87	–	dB
f = 20 Hz to 16 kHz	15	S/N	–	90	–	dB
Carrier and harmonic suppression at the output						
pilot signal; f = 19 kHz	*	α_{19}	–	32	–	dB
subcarrier; f = 38 kHz	*	α_{38}	40	50	–	dB
f = 57 kHz	*	α_{57}	–	46	–	dB
f = 76 kHz	*	α_{76}	–	60	–	dB
intermodulation (note 1) f_m = 10 kHz; spurious signal f_s = 1 kHz						
PLL-filter Fig. 1	*	α_2	–	50	–	dB
PLL-filter Fig. 2	*	α_2	–	70	–	dB
f_m = 13 kHz; spurious signal f_s = 1 kHz	*	α_3	–	75	–	dB
traffic radio (V.W.F.); f = 57 kHz (note 2)	*	$\alpha_{57(VWF)}$	–	70	–	dB
SCA (Subsidiary Communications Authorization); f = 67 kHz (note 4)	*	α_{67}	–	70	–	dB
ACI (Adjacent Channel Interference) (note 3);						
f = 114 kHz	*	α_{114}	–	80	–	dB
f = 190 kHz	*	α_{190}	–	52	–	dB
Ripple rejection at the output; f = 100 Hz; $V_{P(rms)}$ = 100 mV (pin 8)	*	RR_{100}	40	43	–	dB
Voltage on filter capacitor without external load	*	V_{9-7}	–	V_P–0,25	–	V
Source resistance	*	R_{9-8}	6	8	10	kΩ

* V_P = 8,5 or 15 V.

CHARACTERISTICS (continued)

parameter	V_P (V)	symbol	min.	typ.	max.	unit
Mono/stereo control						
Pilot threshold voltages (peak-to-peak values)						
for stereo 'ON'	8,5	$V_{i(p-p)}$	–	21	30	mV
	15	$V_{i(p-p)}$	–	43	61	mV
for mono 'ON'	8,5	$V_{i(p-p)}$	6	15	–	mV
	15	$V_{i(p-p)}$	12	30	–	mV
Switch hysteresis						
$V_{i\,ON}/V_{i\,OFF}$	*	ΔV_i	–	3	–	dB
Switching time at $C_{14-7} = 0{,}22\ \mu F$						
for stereo 'ON'	*	$t_{st\,ON}$	–	15	–	ms
for mono 'ON'	*	$t_{m\,ON}$	–	27	–	ms
External mono/stereo control (see Fig. 12 and note 5)						
Switching voltage for external mono control	8,5	V_{14-7}	–	–	0,7	V
	15	V_{14-7}	–	–	1,4	V
	*	or: $-V_{4-5}$	315	–	–	mV
Control voltage for channel separation: α = 6 dB	8,5	$-V_{4-5}$	–	120	–	mV
	15	$-V_{4-5}$	–	130	–	mV
	*	ΔV_{4-5}	–	–	± 20	mV
α = 26 dB	8,5	$-V_{4-5}$	–	70	–	mV
	15	$-V_{4-5}$	–	80	–	mV
Control voltage						
for mono 'ON'	8,5	$-V_{4-5}$	–	240	–	mV
	15	$-V_{4-5}$	–	270	–	mV
for stereo 'ON'	8,5	$-V_{4-5}$	–	220	–	mV
	15	$-V_{4-5}$	–	250	–	mV
Control voltage difference						
for α = 6 dB; stereo 'ON'	8,5	ΔV_{4-7}	80	100	120	mV

* V_P = 8,5 or 15 V.

parameter	V_P (V)	symbol	min.	typ.	max.	unit
Muting circuit (see Fig. 13 and note 5)						
Control voltage for an attenuation: α = 3 dB	8,5	$-V_{3-5}$	–	140	–	mV
	15	$-V_{3-5}$	–	145	–	mV
	*	ΔV_{3-5}	–	± 20	–	mV
α = 26 dB	8,5	$-V_{3-5}$	–	255	–	mV
	15	$-V_{3-5}$	–	270	–	mV
Attenuation						
with V_{3-5} = 0 V	*	α	–	–	0,2	dB
with $-V_{3-5}$ = 450 mV	*	α	–	80	–	dB
LED driver output current at an attenuation: α = 3 dB	*	I_1	1,2	1,7	2,2	mA
Control voltage for I_1 = 200 μA	8,5	$-V_{3-5}$	–	150	–	mV
	15	$-V_{3-5}$	–	160	–	mV
Control inputs						
Recommended voltage range	*	$V_{3;4;5-7}$	0	–	4	V
Input bias current	*	$I_{3;4;5}$	–	10	100	nA
Indicator driver						
Output saturation voltages at I_1 = 20 mA; V_{3-5} = 0 V	*	V_{1-7sat}	–	1,2	1,8	V
at I_2 = 20 mA	*	V_{2-7sat}	–	0,5	1,0	V
Output leakage current at $V_{1;2-7}$ = 24 V	*	$I_{1;2}$	–	20	–	μA

* V_P = 8,5 or 15 V.

CHARACTERISTICS (continued)

parameter	V_P (V)	symbol	min.	typ.	max.	unit
VCO						
Oscillator frequency adjustable with R_{10-7}	*	f_{osc}	–	76	–	kHz
Spread of free-running frequency at nominal external circuitry	*	f_{osc}	71	–	82	kHz
Free-running frequency dependency (note 6)						
with temperature	*	TC	–	1×10^{-4}	–	K^{-1}
with supply voltage	*	$\Delta f_{osc}/\Delta V_P$	–	–	400	Hz/V
Capture and holding range for a pilot input voltage $V_{pil} = 0{,}5 \times V_{pil\,nom}$	*	$\Delta f/f$	± 2	–	–	%
PLL control slope (total)	*	S_{tot}	–	4,5	–	kHz/μs
D.C. voltage at pin 10	*	V_{10-7}	–	2,1	–	V
		or:	–	$3{,}2\ V_{BE}$	–	V
Frequency measuring point; internal switching threshold	*	V_{4-7}	–	6	–	V
		or:	–	$9\ V_{BE}$	–	V
Output voltage (peak-to-peak value) at pin 4; R = 4,7 kΩ	*	$V_{4-7(p-p)}$	–	350	–	mV
Output resistance	*	R_{4-7}	–	5	–	kΩ

* V_P = 8,5 or 15 V.

Notes to the characteristics

1. Intermodulation suppression (BFC: Beat-Frequency Components)

$$\alpha_2 = \frac{V_{o(signal)}\ (\text{at } 1\text{ kHz})}{V_{o(spurious)}\ (\text{at } 1\text{ kHz})};\ f_s = (2 \times 10\text{ kHz}) - 19\text{ kHz}$$

$$\alpha_3 = \frac{V_{o(signal)}\ (\text{at } 1\text{ kHz})}{V_{o(spurious)}\ (\text{at } 1\text{ kHz})};\ f_s = (3 \times 13\text{ kHz}) - 38\text{ kHz}$$

measured with: 91% mono signal; f_m = 10 or 13 kHz; 9% pilot signal.

2. Traffic radio (V.W.F.) suppression

$$\alpha_{57(VWF)} = \frac{V_{o(signal)}\ (\text{at } 1\text{ kHz})}{V_{o(spurious)}\ (\text{at } 1\text{ kHz} \pm 23\text{ kHz})}$$

measured with: 91% stereo signal; f_m = 1 kHz; 9% pilot signal; 5% traffic subcarrier (f = 57 kHz, f_m = 23 Hz AM, m = 60%).

3. ACI (Adjacent Channel Interference)

$$\alpha_{114} = \frac{V_{o\ (signal)}\ (\text{at } 1\text{ kHz})}{V_{o(spurious)}\ (\text{at } 4\text{ kHz})};\ f_s = 110\text{ kHz} - (3 \times 38\text{ kHz})$$

$$\alpha_{190} = \frac{V_{o(signal)}\ (\text{at } 1\text{ kHz})}{V_{o(spurious)}\ (\text{at } 4\text{ kHz})};\ f_s = 186\text{ kHz} - (5 \times 38\text{ kHz})$$

measured with: 90% mono signal; f_m = 1 kHz; 9% pilot signal; 1% spurious signal (f_s = 110 or 186 kHz, unmodulated).

4. SCA (Subsidiary Communications Authorization)

$$\alpha_{67} = \frac{V_{o(signal)}\ (\text{at } 1\text{ kHz})}{V_{o(spurious)}\ (\text{at } 9\text{ kHz})};\ f_s = (2 \times 38\text{ kHz}) - 67\text{ kHz}$$

measured with: 81% mono signal; f_m = 1 kHz; 9% pilot signal; 10% SCA-subcarrier (f_s = 67 kHz, unmodulated).

5. Assuming $V_T = \frac{k \times T}{q}$ = 28,6 mV at T_j = 330 K.

6. The effects of external components are not taken into account.

APPLICATION NOTES

1. When mono/stereo control and muting control are not used, pins 3, 4 and 5 have to be grounded.
2. In a receiver, channel separation adjustment can be obtained by:
   a. A capacitor at pin 12 (C_{12-7}): phasing 19/38 kHz
   b. RC or LCR filter at the input: frequency response compensation ($V_G = f(\omega)$)
   c. Feeding the output signals of the output amplifier to the inputs of the other channel.
3. PLL-filter for reduced intermodulation (α_2); see Fig. 2.
4. External mono 'ON' switch; see Fig. 3.
5. Switching 'OFF' the oscillator; see Fig. 4.

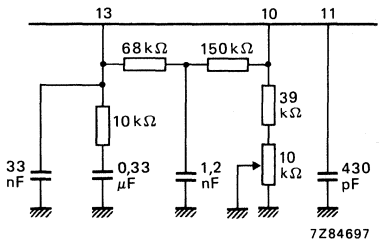


Fig. 2 PLL-filter for α_2 = 70 dB at V_P = 15 V (see also Fig. 1).

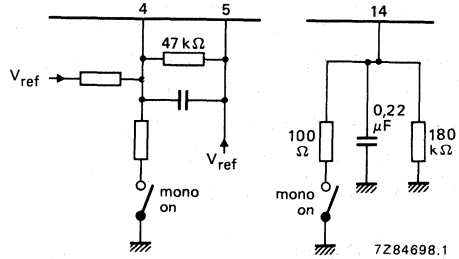


Fig. 3 (a) At pin 4; $-V_{4-5} > 300$ mV; (b) at pin 14.

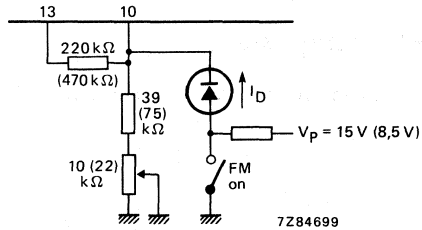


Fig. 4 The oscillator is switched-off when: $I_D > 100$ µA (> 50 µA for V_P = 8,5 V) and $I_D < 1$ mA.

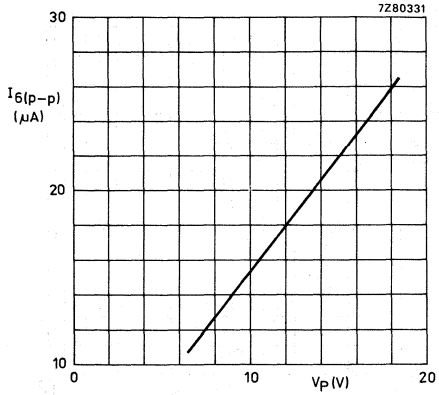


Fig. 5 Signal handling range at the input for I_{6nom} (± 75 kHz); $V_{9-7} = V_P$.

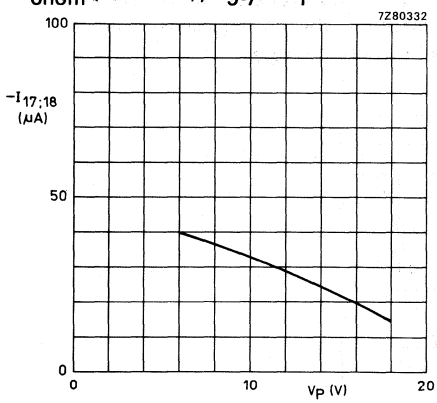
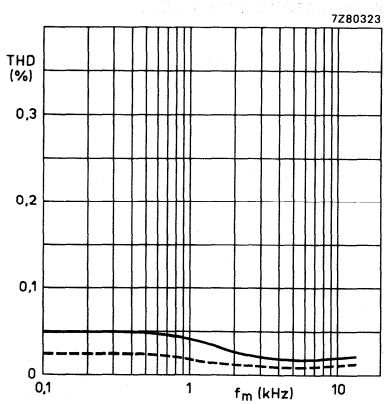


Fig. 7 D.C. current in the feedback loop of the output amplifier.



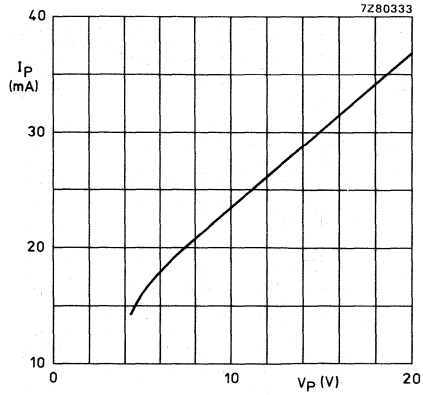


Fig. 6 Supply current comsumption at $V_{9-7} = V_P$.

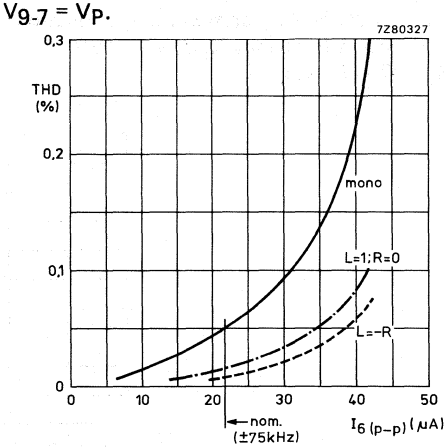


Fig. 8 Total harmonic distortion (THD) as a function of the peak-to-peak input current at pin 6; V_P = 15 V; f_m = 1 kHz; $V_{3-5} = V_{4-5}$ = 0 V.

Fig. 9 Total harmonic distortion (THD) as a function of the modulation frequency (f_m); V_P = 15 V; $I_{6(p-p)}$ = 21,5 μA.

——— mono

– – – – stereo; L = –R; 91% + 9% pilot signal.

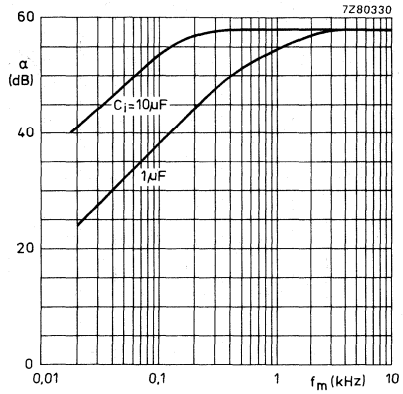


Fig. 10 Channel separation (α) as a function of the modulation frequency (f_m); V_P = 15 V; R_i = 47 kΩ; V_{4-5} = 0 V.

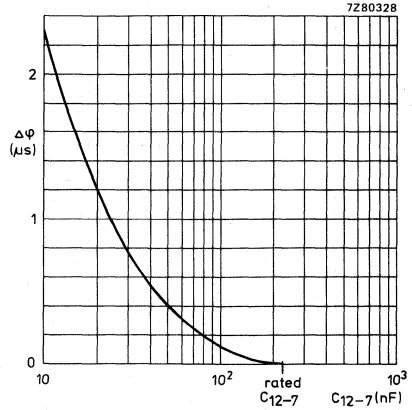


Fig. 11 Phase shift between pilot signal at the input and the internal carrier processing as a function of C_{12-7}.

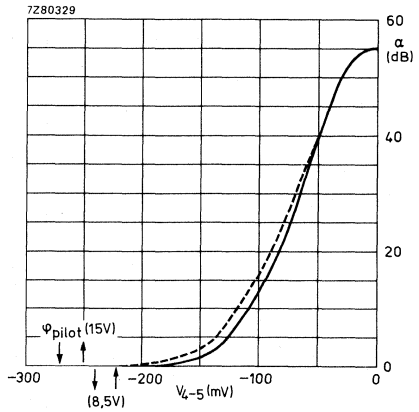


Fig. 12 Mono/stereo control at f_m = 1 kHz; α is the channel separation.
——— V_P = 8,5 V
– – – – V_P = 15 V

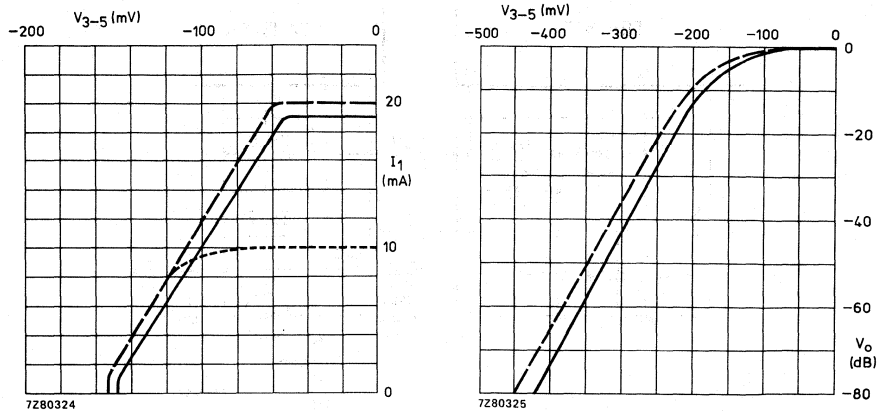


Fig. 13 Muting (V_o) and muting indicator current (I_1) as a function of V_{3-5}.

V_o in dB curves; ——— V_P = 8,5 V
– – – – V_P = 15 V

I_1 in mA curves for V_{PL}/R_{bias1} (pin 1); – – – – 22 V/1 kΩ
——— 14 V/680 Ω
- - - - - - - 10 V/680 Ω

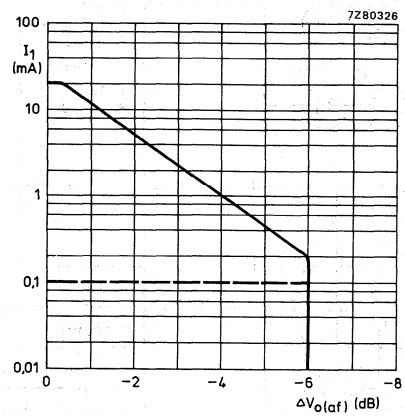


Fig. 14 Muting indicator current; V_P = 8,5 to 15 V; V_{PL} = 14 V.

——— R_{bias1} = 680 Ω
– – – – R_{bias1} = matched

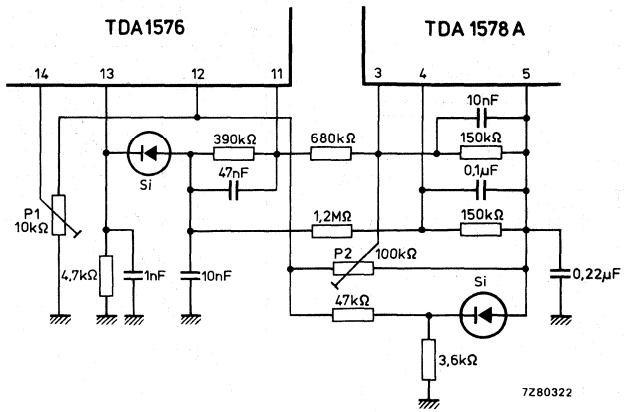


Fig. 15 Application information for external circuitry to provide external mono/stereo and muting control.

Adjustment recommendations:

at $V_{i(hf)}$ = 100 μV with P1 to α = 6 dB (channel separation),
at $V_{i(hf)}$ = 15 μV with P2 to $V_{o(af)}$ = −3 dB.

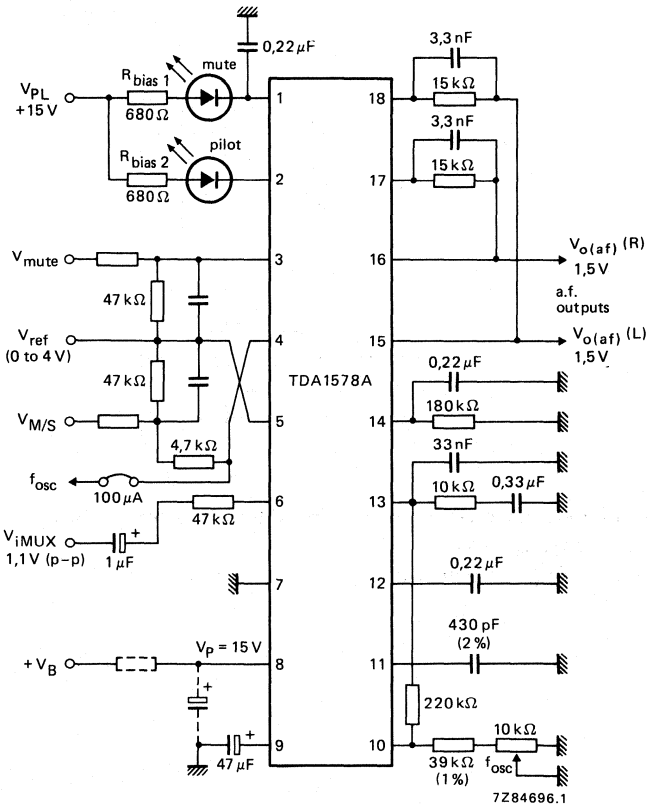


Fig. 16 Typical application circuit using TDA1578A for V_P = 15 V.

DECODER FOR TRAFFIC WARNING (VWF) RADIO TRANSMISSIONS

GENERAL DESCRIPTION

The TDA1579 decoder is for radio transmissions having 57 kHz amplitude-modulated subcarriers as used in the German 'Verkehrs Warnfunk' (VWF) traffic warning system.

Features

- Selective subcarrier amplifier (57 kHz) with gain control
- Transmitter identification signal (SK) decoder
- Area identification signal (BK) and announcement identification signal (DK) active filtering
- BK and DK decoders (Schmitt trigger with switched hysteresis)
- BK and DK switch-on/switch-off delay circuits
- Driver output for SK indicator (LED)
- SK and BK control outputs

QUICK REFERENCE DATA

Measured in Fig. 1 at V_{iSK} = 8 mV; f = 57 kHz amplitude modulated with f_m = 34.95 Hz and m = 60% for 'BK-traffic area C' signal; or with f_m = 125 Hz and m = 30% for DK signal

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage		V_P	7.5	8.5	12	V
Supply current		I_P	–	6	–	mA
Nominal input voltage	at f = 57 kHz	V_{iSK}	–	8	–	mV
Input impedance	at f ⩽ 57 kHz	$\|Z_i\|$	100	–	–	kΩ
Control level	−3 dB	V_{iSK}	–	2.4	–	mV
Input voltage	peak-to-peak value	$V_{i(p-p)}$	2	–	–	V
SK switch-on threshold level		m_{BKon}	–	42	–	%
SK switch hysteresis		Δm_{BK}	–	3.5	–	dB
SK switch-on delay		t_{dSKon}	–	150	–	ms
SK switch-off delay		t_{dSKoff}	–	750	–	ms
DK switch-on threshold level		m_{DKon}	–	13	–	%
DK switch hysteresis		Δm_{DK}	–	3.6	–	dB
DK switch-on delay		t_{dDKon}	–	750	–	ms
DK switch-off delay		t_{dDKoff}	–	750	–	ms
Ambient operating temperature range		T_{amb}	−30	–	+ 80	°C

PACKAGE OUTLINES

TDA1579: 18-lead DIL; plastic (SOT102).
TDA1579T: 20-lead mini-pack; plastic (SO20; SOT163A).

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134).
All pin numbers in this table apply to TDA1579; for TDA1579T refer to Fig. 1.

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage	pin 7	$V_P = V_{7-18}$	–	–	15	V
Switch output voltage	pin 1	V_{1-18}	–	–	23	V
	pins 2 or 3	$V_{2;3-18}$	–	–	15	V
	pins 1, 2 or 3	$-V_{1;2;3-18}$	–	–	0.5	V
Switch output current	pin 1	I_1	–	–	50	mA
	pins 2 or 3	$I_{2;3}$	–	–	5	mA
	pins 1, 2 or 3	$-I_{1;2;3}$	–	–	10	mA
Signal input voltage	pin 13	V_{13-18}	–	–	V_P	
	pin 13	$-V_{13-18}$	–	–	0.5	V
Signal input current	pin 13	$-I_{13}$	–	–	10	mA
Total power dissipation		P_{tot}	–	–	800	mW
Storage temperature range		T_{stg}	−55	–	+ 150	°C
Operating ambient temperature range		T_{amb}	−30	–	+ 80	°C

CHARACTERISTICS

V_P = 8.5 V; T_{amb} = 25 °C; measured at nominal input signal: V_{iSK} = 8 mV, f = 57 kHz amplitude modulated with f_m = 34.95 Hz and m = 60% for 'BK-traffic area C' signal; or with f_m = 125 Hz and m = 30% for DK signal.
All pin numbers in this table apply to TDA1579, for TDA1579T refer to Fig. 1.

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage	pin 7	V_P	7.5	–	12	V
Supply current	pin 7	I_P	–	6	10	mA
SK amplifier/decoder						
Input impedance	f ⩽ 57 kHz	$\|Z_i\|$	100	–	–	kΩ
Input voltage (peak-to-peak value)		$V_{i(p-p)}$	2	–	–	V
Input voltage at start of gain control	V_{o9BK} = −3 dB	V_{iSK}	–	2.4*	–	mV
Voltage gain	V_{9BK}/V_{13SK}	G_{v9-13}	–	44*	–	dB

* Selectable by R_{12-8} or Z_{10-8}.

parameter	conditions	symbol	min.	typ.	max.	unit
SK amplifier/decoder (continued)						
Gain spread		$\pm \Delta G_{v9\text{-}13}$	–	–	2	dB
Gain control range		ΔG_v	40	–	–	dB
Controlled output voltage		V_{o9BK}	–	440	–	mV
		V_{o9DK}	–	220	–	mV
BK circuit						
Switch-on threshold level	pin 3 high-Z	V_{o5BKon}	600	670	750	mV
Switch hysteresis		$\frac{V_{o5BKon}}{V_{o5BKoff}}$	3	3.5	4	dB
BK switch threshold level for BK-off (SK-off) (typ. value = $0.21V_{8\text{-}18}$)	pin 3 conducting	$V_{4\text{-}18off}$	0.8	0.88	0.97	V
SK output (pin 3)						
allowable load current		I_3	–	–	1.5	mA
saturation voltage	I_3 = 1.5 mA	$V_{3\text{-}18sat}$	–	–	0.35	V
rejection voltage	$I_3 < 5\ \mu A$	$V_{3\text{-}18}$	18	–	–	V
Indicator driver (pin 1)						
allowable load current		I_1	–	–	40	mA
saturation voltage	I_1 = 20 mA	$V_{1\text{-}18sat}$	–	–	0.8	V
rejection voltage	$I_1 < 10\ \mu A$	$V_{1\text{-}18}$	23	–	–	V
DK circuit						
Switch-on threshold level	pin 2 high-Z	V_{15DKon}	600	670	750	mV
Switch hysteresis		$\frac{V_{15DKon}}{V_{15DKoff}}$	3.1	3.6	4.1	dB
DK switch threshold level for DK-off (Schmitt trigger output) (typ. value = 1 x V_{BE})	pin 2 conducting	$V_{16\text{-}18off}$	–	0.6	–	V
DK output (pin 2)						
allowable load current		I_2	–	–	1.5	mA
saturation voltage	I_2 = 1.5 mA	$V_{2\text{-}18sat}$	–	–	0.35	V
rejection voltage	$I_2 < 5\ \mu A$	$V_{2\text{-}18}$	18	–	–	V
BK and DK filter amplifiers						
Open loop gain	f = 100 Hz	G_o	84	–	–	dB
Current gain		G_i	120	–	–	dB
Input bias current		$\pm I_i$	–	–	50	nA
Output offset voltage	$R_{5\text{-}6} = R_{14\text{-}15}$ = 680 kΩ	$\pm V_{o5\text{-}8}$ $\pm V_{15\text{-}8}$	–	–	50	mV

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
BK and DK filter amplifiers (continued)						
Available output current		$\pm I_o$	1	–	–	mA
Output resistance		R_o	–	2	3.5	kΩ
Allowable load capacitance		C_L	–	–	50	pF
Internal reference voltage						
Output voltage (typ. value = 0.5 V_P)		$V_{8\text{-}18}$	4.0	4.25	4.5	V
Internal resistance of voltage source		R_8	–	–	5	Ω
Available output current		$-I_8$	2	–	–	mA
		$+I_8$	0.6	–	–	mA
Output short-circuit current (typ. value = V_P/1 kΩ)		$-I_{8sc}$	–	8	–	mA
Reference current source						
Reference voltage (typ. value = $V_{8\text{-}18}-V_{BE}$)		$V_{17\text{-}18}$	–	3.6	–	V
Internal biasing resistor		R_{i17}	–	5	–	kΩ
Allowable range of external reference resistor		$R_{17\text{-}18}$	180	–	270	kΩ

APPLICATION INFORMATION (Fig. 1)

parameter	symbol		application	unit
SK switch-on threshold level at m_{BK} = 60%	V_{iSKon}	typ.	1.8	mV
SK switch-on threshold level at V_{iSK} = 8 mV	m_{BKon}	typ.	32	%
SK switch hysteresis	$\frac{m_{BKon}}{m_{BKoff}}$	>	3.0	dB
		typ.	3.5	dB
		<	4.0	dB
SK switch-on delay (note 1)	t_{dSKon}	typ.	95	ms
		<	130	ms
SK switch-off delay (note 2)	t_{dSKoff}	>	380	ms
		typ.	500	ms
		<	620	ms
DK switch-on threshold level at m_{DK} = 30%	V_{iDKon}	typ.	1.5	mV
DK switch-on threshold level at V_{iDK} = 8 mV	m_{DKon}	typ.	13	%
DK switch hysteresis	$\frac{m_{DKon}}{m_{DKoff}}$	>	3.1	dB
		typ.	3.6	dB
		<	4.1	dB
DK switch-on delay (note 1)	t_{dDKon}	typ.	750	ms
		<	1000	ms
DK switch-off delay (note 2)	t_{dDKoff}	>	600	ms
		typ.	750	ms
		<	1000	ms

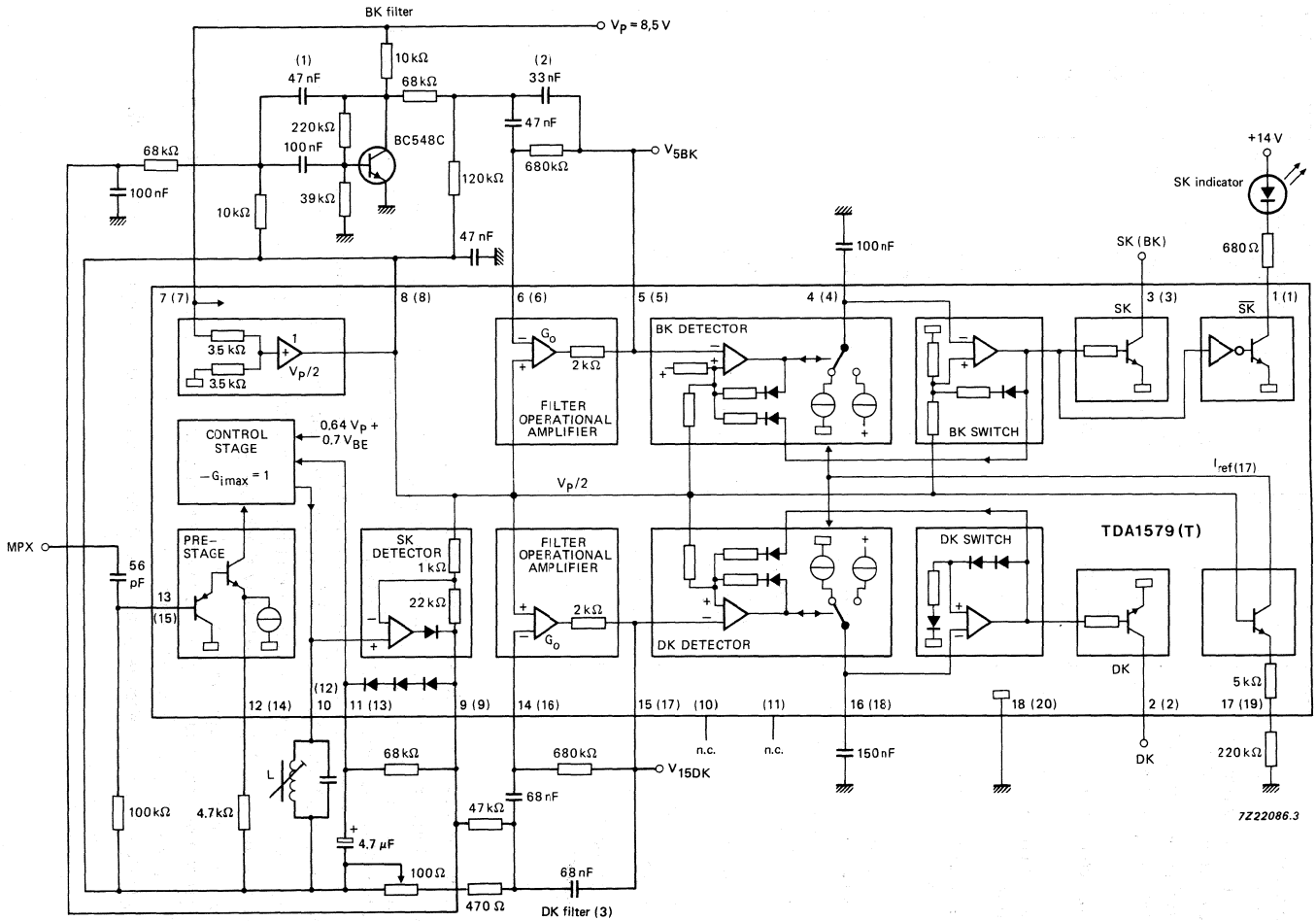
Notes

1. **Sequence for measuring switch-on delay times** (t_{don})
   a) Nominal BK or DK input signal at pin 13: $V_{i(p-p)}$ = 8 mV; f = 57 kHz; modulation-on.
   b) Pin 4 of the BK detector (pin 16 of the DK detector) is switched to ground to cause a low signal at the SK output at pin 3 (DK output at pin 2).
   c) t_{don} commences when the ground connection is removed from pin 4 (pin 16) as the positive-going V_{oBK} signal at pin 5 (V_{oDK} signal at pin 15) crosses zero.

   t_{don} ends when the positive-going edge of the SK output arrives at pin 13 (DK at pin 2).
2. **Sequence for measuring switch-off delay times** (t_{doff})
   a) Nominal operating conditions as in note 1.
   b) t_{doff} commences when the input is switched off as the negative-going V_{oBK} signal at pin 5 (V_{oDK} signal at pin 15) crosses zero.

   t_{doff} ends when the negative-going edge of the SK output arrives at pin 3 (DK at pin 2).

APPLICATION INFORMATION (continued)



(1) f_o = 55 Hz; Q = 1.9
(2) f_o = 24 Hz; Q = 1.9
(3) f_o = 125 Hz

Fig. 1 Application diagram.

L = 2.36 mH; Q_L = 70; C = 3.3 nF; f_o = 57 kHz.
Pin numbers in parentheses are for TDA1579T, other pin numbers are for TDA1579.

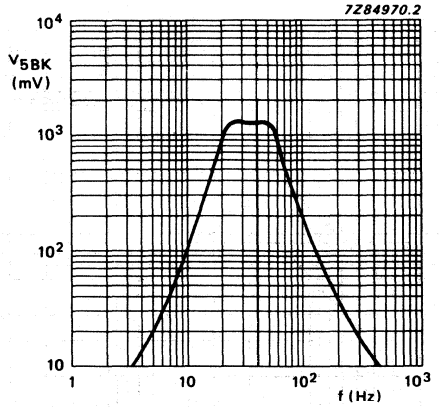


Fig. 2 BK signal voltage at pin 5 as a function of frequency.

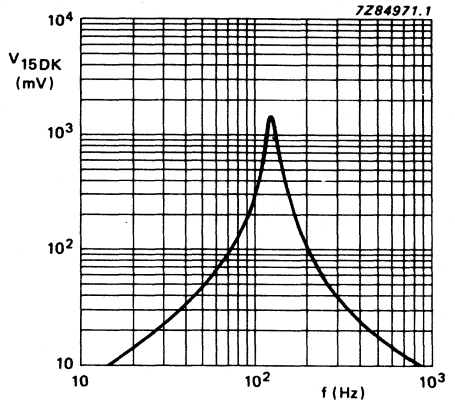


Fig. 3 DK signal voltage at pin 15 as a function of frequency: f_o = 125 Hz; Q ≈ 18.

APPLICATION INFORMATION (continued)

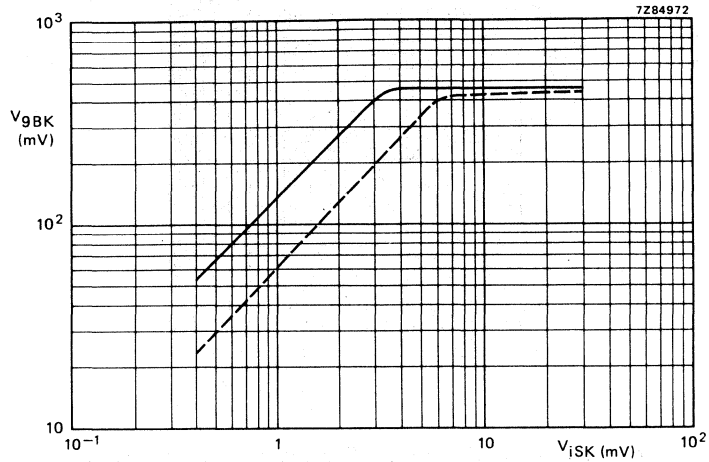


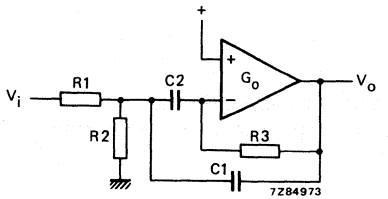
Fig. 4 Control characteristic of the SK amplifier at V_P = 8.5 V, m_{BK} = 60% and Q_L = 70.

FILTER INFORMATION

Gain

Amplifier conditions: $G_o >> G_v$ and $G_o >> 2 \cdot Q^2$

$$G_v = - \frac{\frac{p}{R1 \cdot C1}}{p^2 + p\,\frac{C1 + C2}{R3 \cdot C1 \cdot C2} + \frac{R1 + R2}{R1 \cdot R2 \cdot R3 \cdot C1 \cdot C2}}$$, in which $p = j\omega$ and $G_v = \frac{V_o}{V_i}$.



	general equation	C1 = C2 = C	C1 = C2 = C R2 << R1
Resonance frequency $\omega_r =$	$\frac{1}{\sqrt{\frac{R1 \cdot R2}{R1 + R2} \cdot R3 \cdot C1 \cdot C2}}$	$\frac{1}{C\sqrt{\frac{R1 \cdot R2}{R1 + R2} \cdot R3}}$	$\frac{1}{C\sqrt{R2 \cdot R3}}$
Gain at $\omega = \omega_r$ $-G_{vr} =$	$\frac{C2}{C1 + C2} \cdot \frac{R3}{R1}$	$\frac{1}{2} \cdot \frac{R3}{R1}$	$\frac{1}{2} \cdot \frac{R3}{R1}$
Quality $Q =$	$\sqrt{\frac{C1 \cdot C2}{C1 + C2}} \cdot \sqrt{\frac{R3\,(R1 + R2)}{R1 \cdot R2}}$	$\frac{1}{2}\sqrt{\frac{R3\,(R1 + R2)}{R1 \cdot R2}}$	$\frac{1}{2} \cdot \frac{R3}{R2}$

Recommended components

C1, C2 and R1, R2, R3	metallized polycarbonate film (MKC) capacitors; ± 5% metal film (MR) resistors; ± 2%
or	
C1, C2 and R1, R2, R3	metallized polyester film (MKT) capacitors; ± 5% carbon film (CR) resistors; ± 2%

Decoder for traffic warning (VWF) radio transmissions

TDA1581T

FEATURES

- Selective subcarrier amplifier (57 kHz) with gain control
- Transmitter identification signal (SK) decoder
- Area identification signal (BK) and announcement identification signal (DK) active filtering
- BK and DK decoders (Schmitt trigger with switched hysteresis)
- BK and DK switch-on/switch-off delay circuits
- SK and BK control outputs

GENERAL DESCRIPTION

The TDA1581T decoder is for radio transmissions having 57 kHz amplitude-modulated subcarriers as used in the german 'Verkehrs Warnfunk' (VWF) traffic warning system.

QUICK REFERENCE DATA

Measured in Fig.3 at V_{iSK} = 8 mV; f = 57 kHz amplitude modulated with f_m = 34.95 Hz and m = 60 % for 'BK-traffic area C' signal; or with f_m = 125 Hz and m = 30 % for DK signal

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage range		7.5	8.5	10	V
I_P	supply current		–	6	–	mA
V_{iSK}	nominal input voltage	f = 57 kHz	–	8	–	mV
Z_i	input impedance	f ≤ 57 kHz	100	–	–	kΩ
V_{iSK}	control level	-3 dB	–	2.4	–	mV
$V_{i(p-p)}$	input voltage peak-to-peak value		2	–	–	V
m_{BKon}	SK switch-on threshold level		–	42	–	%
Δm_{BK}	SK switch hysteresis		–	3.5	–	dB
t_{dSKon}	SK switch-on delay		–	150	–	ms
t_{dSKoff}	SK switch-off delay		–	750	–	ms
m_{DKon}	DK switch-on threshold level		–	13	–	%
Δm_{DK}	DK switch hysteresis		–	3.6	–	dB
t_{dDKon}	DK switch-on delay		–	750	–	ms
t_{dDKoff}	DK switch-off delay		–	750	–	ms
T_{amb}	operating ambient temperature range		-30	–	+80	°C

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA1581T	20	SO	plastic	SOT163A

Decoder for traffic warning (VWF) radio transmissions

TDA1581T

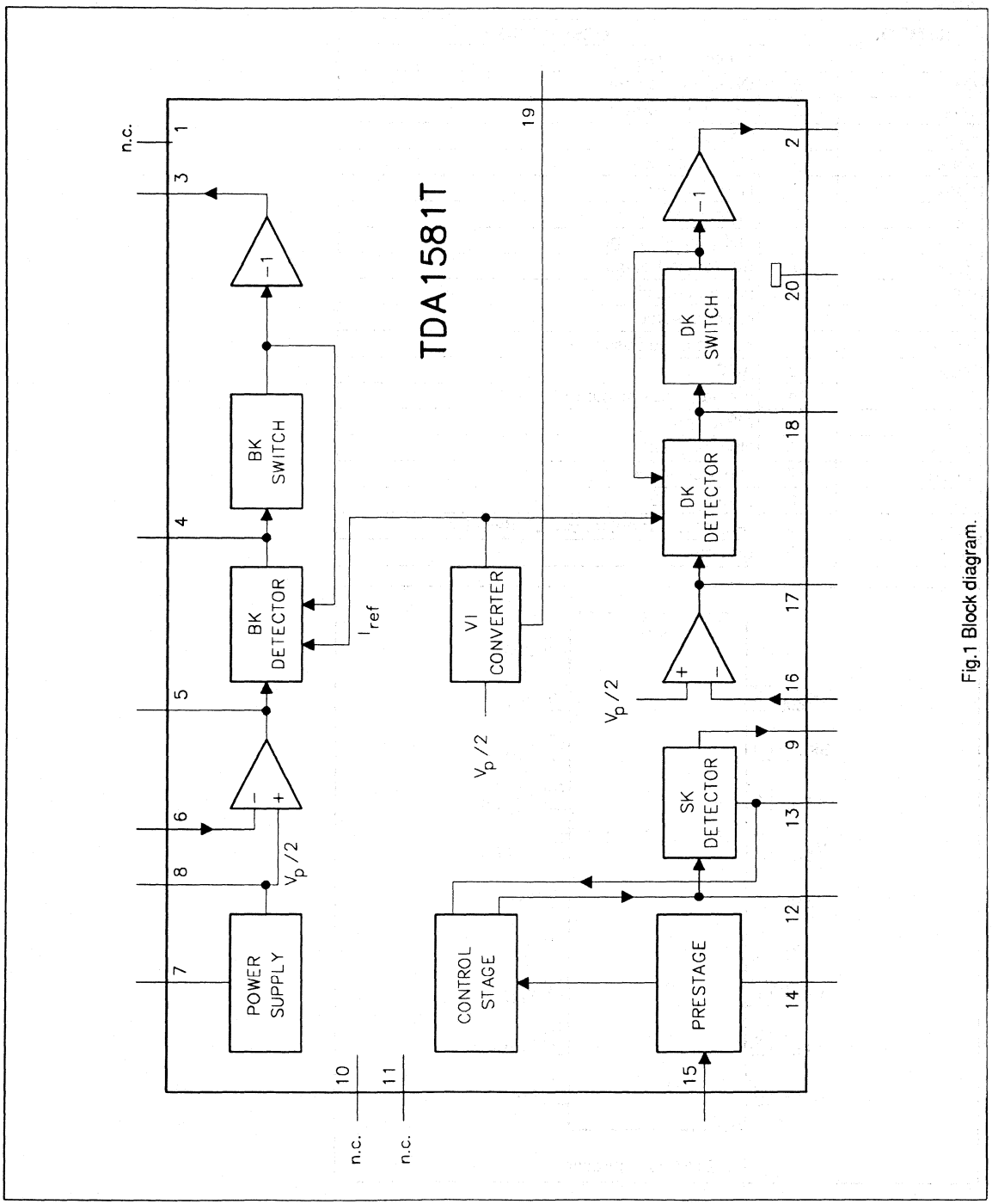


Fig.1 Block diagram.

Decoder for traffic warning (VWF) radio transmissions

TDA1581T

PINNING

SYMBOL	PIN	DESCRIPTION
n.c.	1	not connected
DK_{out}	2	DK output current
SK_{out}	3	SK output current
τ_{BK}	4	time delay BK
V_{5BK}	5	filter output BK
V_{6BK}	6	filter input BK
V_p	7	supply voltage
$V_p / 2$	8	half supply voltage
V_{9SK}	9	SK detector output
n.c.	10	not connected
n.c.	11	not connected
V_{12SK}	12	57 kHz band pass filter
V_{AGC}	13	AGC
I_{14}	14	prestage biasing current
V_{MPX}	15	MPX input
V_{16DK}	16	filter input DK
V_{17DK}	17	filter output DK
τ_{DK}	18	time delay DK
I_{19}	19	reference current for BK, DK detector
GND	20	ground

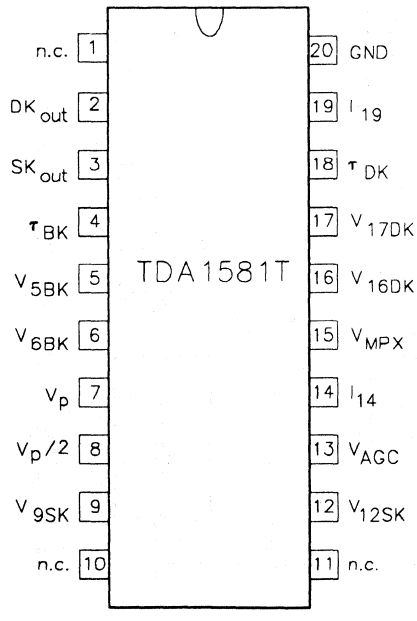


Fig.2 Pin configuration.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_P = V_{7-20}$	supply voltage	pin 7	–	–	15	V
$V_{2;3-20}$	switch output voltage	pins 2 or 3	-0.5	–	15	V
$I_{2;3}$	switch output current	pins 2 or 3	-10	–	5	mA
V_{15-20}	signal input voltage	pin 15	-0.5	–	V_p	V
I_{15}	signal input current	pin 15	–	–	-10	mA
P_{tot}	total power dissipation		–	–	800	mW
T_{stg}	storage temperature range		-55	–	+150	°C
T_{amb}	operating ambient temperature range		-30	–	+80	°C

CHARACTERISTICS

V_p = 8.5 V; T_{amb} = +25 °C; measured at nominal input signal: V_{iSK} = 8 mV, f = 57 kHz amplitude modulated with f_m = 34.95 Hz and m = 60 % for 'BK-traffic area C' signal; or with f_m = 125 Hz and m = 30 % for DK signal.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_p	supply voltage	pin 7	7.5	–	10	V
I_p	supply current	pin 7	–	6	15	mA
SK amplifier/decoder						
Z_i	input impedance	f ≤ 57 kHz	60	–	–	kΩ
$V_{i(p-p)}$	input voltage (peak-to-peak value)		2	–	–	V
V_{iSK}	input voltage at start of gain control	V_{o9BK} = -3 dB	–	2.4 *	–	mV
G_{v9-15}	voltage gain	V_{9BK} / V_{15SK}	–	44 *	–	dB
ΔG_{v9-15}	gain spread		–	–	±2	dB
ΔG_v	gain control range		40	–	–	dB
V_{o9BK}	controlled output voltage		–	440	–	mV
V_{o9DK}			–	220	–	mV
BK circuit						
V_{o5BKon}	switch-on threshold level	pin 3 high-Z	600	670	750	mV
$\frac{V_{o5BKon}}{V_{o5BKoff}}$	switch hysteresis		3	3.5	4	dB
$V_{4-20off}$	BK switch threshold level for BK-off (SK-off) (typ. value = $0.21V_{8-20}$)	pin 3 conducting	0.8	0.88	0.97	V
	SK output (pin 3)					
I_3	permitted load current		–	–	0.5	mA
$V_{3-20sat}$	saturation voltage	I_3 = 1.5 mA	–	–	0.35	V
V_{3-20}	rejection voltage	I_3 < 5 µA	18	–	–	V
DK circuit						
V_{17DKon}	switch-on threshold level	pin 2 high-Z	600	670	750	mV
$\frac{V_{17DKon}}{V_{17DKoff}}$	switch hysteresis		3.1	3.6	4.1	dB
$V_{18-20off}$	DK switch threshold level for DK-off (Schmitt trigger output) (typ. value = 1 x V_{BE})	pin 2 conducting	–	0.6	–	V

* selectable by R_{14-8} or Z_{12-8}

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	DK output (pin 2)					
I_2	permitted load current		–	–	0.5	mA
$V_{2\text{-}20sat}$	saturation voltage	I_2 = 1.5 mA	–	–	0.35	V
$V_{2\text{-}20}$	rejection voltage	$I_2 < 5$ µA	18	–	–	V
BK and DK filter amplifiers						
G_o	open loop gain	f = 100 Hz	84	–	–	dB
G_i	current gain		120	–	–	dB
I_i	input bias current		–	–	±50	nA
$V_{o5\text{-}8}$	output offset voltage	$R_{5\text{-}6} = R_{16\text{-}17}$ = 680 kΩ	–	–	±50	mV
$V_{17\text{-}8}$						
I_o	available output current		±1	–	–	mA
R_o	output resistance		–	2	3.5	kΩ
C_L	permitted load capacitance		–	–	50	pF
Internal reference voltage						
$V_{8\text{-}20}$	output voltage (typ. value = $0.5V_p$)		4.0	4.25	4.5	V
R_8	internal resistance of voltage source		–	–	5	Ω
$I_{8\text{-}20}$	available output current		-2	–	–	mA
$I_{20\text{-}8}$			0.6	–	–	mA
I_{8sc}	output short-circuit current (typ. value = V_p / 1 kΩ)		–	-8	–	mA
Reference current source						
$V_{19\text{-}20}$	reference voltage (typ. value = $V_{8\text{-}20} - V_{BE}$)		–	3.6	–	V
R_{i19}	internal biasing resistor		–	5	–	kΩ
$R_{19\text{-}20}$	permitted range of external reference resistor		180	–	270	kΩ

APPLICATION INFORMATION (see Fig.3)

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{iSKon}	SK switch-on threshold level	m_{BK} = 60 %	–	1.8	–	mV
m_{BKon}	SK switch-on threshold level	V_{iSK} = 8 mV	–	32	–	%
$\frac{m_{BKon}}{m_{BKoff}}$	SK switch hysteresis		3.0	3.5	4.0	dB
t_{dSKon}	SK switch-on delay	note 1	–	95	200	ms
t_{dSKoff}	SK switch-off delay	note 2	380	500	700	ms
V_{iDKon}	DK switch-on threshold level	m_{DK} = 30 %	–	1.5	–	mV
m_{DKon}	DK switch-on threshold level	V_{iDK} = 8 mV	–	13	–	%
$\frac{m_{DKon}}{m_{DKoff}}$	DK switch hysteresis		3.1	3.6	4.1	dB
t_{dDKon}	DK switch-on delay	note 1	–	750	1000	ms
t_{dDKoff}	DK switch-off delay	note 2	600	750	1000	ms

Notes to the application information

1. Sequence for measuring switch-on delay times (t_{don})
   a) Nominal BK or DK input signal at pin 15: $V_{i(p-p)}$ = 8 mV; f = 57 kHz; modulation-on.
   b) Pin 4 of the BK detector (pin 18 of the DK detector) is switched to ground to cause a low signal at the SK output at pin 3 (DK output at pin 2).
   c) t_{don} commences when the ground connection is removed from pin 4 (pin 18) as the positive-going V_{oBK} signal at pin 5 (V_{oDK} signal at pin 17) crosses zero.
   t_{don} ends when the positive-going edge of the SK output arrives at pin 15 (DK at pin 2).
2. Sequence for measuring switch-off delay times (t_{doff})
   a) Nominal operating conditions as in note 1.
   b) t_{doff} commences when the input is switched off as the negative-going V_{oBK} signal at pin 5 (V_{oDK} signal at pin 17) crosses zero.
   t_{doff} ends when the negative-going edge of the SK output arrives at pin 3 (DK at pin 2).

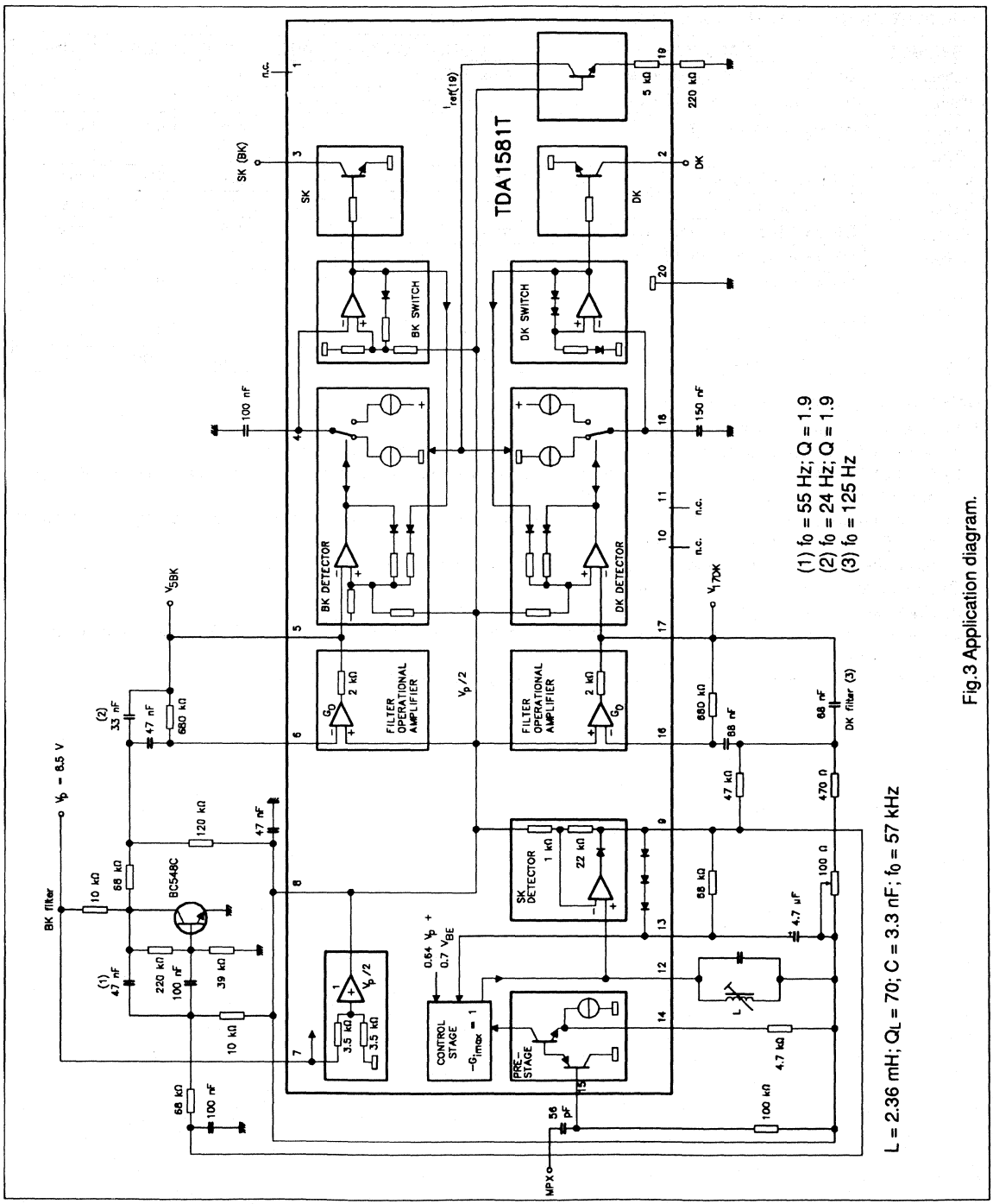


Fig.3 Application diagram.

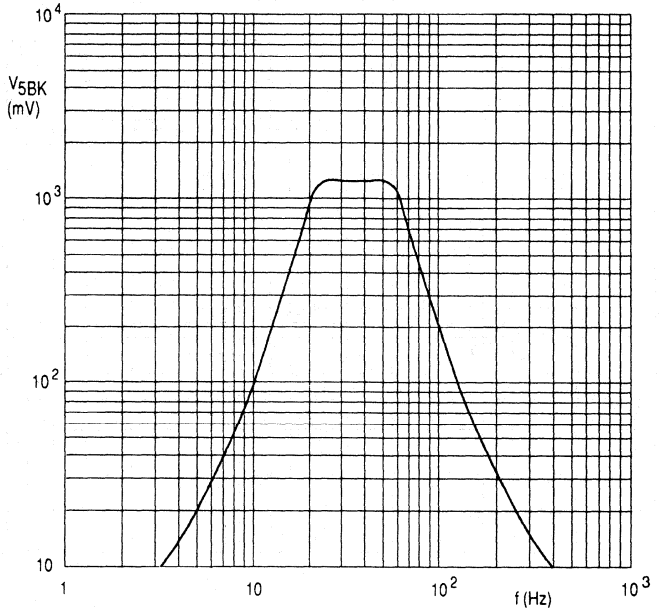


Fig.4 BK signal voltage at pin 5 as a function of frequency.

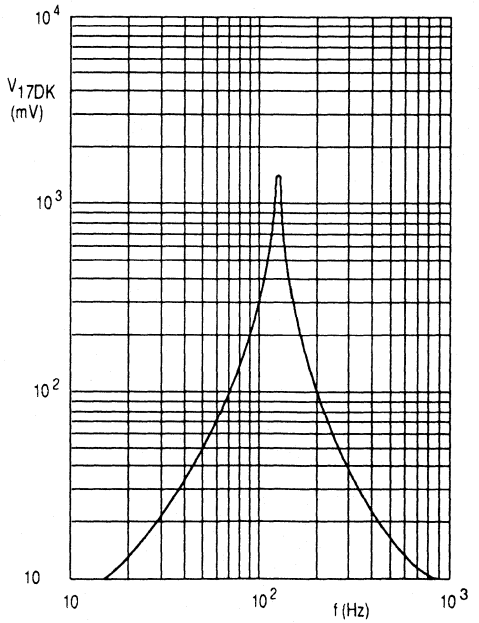


Fig.5 DK signal voltage at pin 17 as a function of frequency: f_0 = 125 Hz; Q ≈ 18.

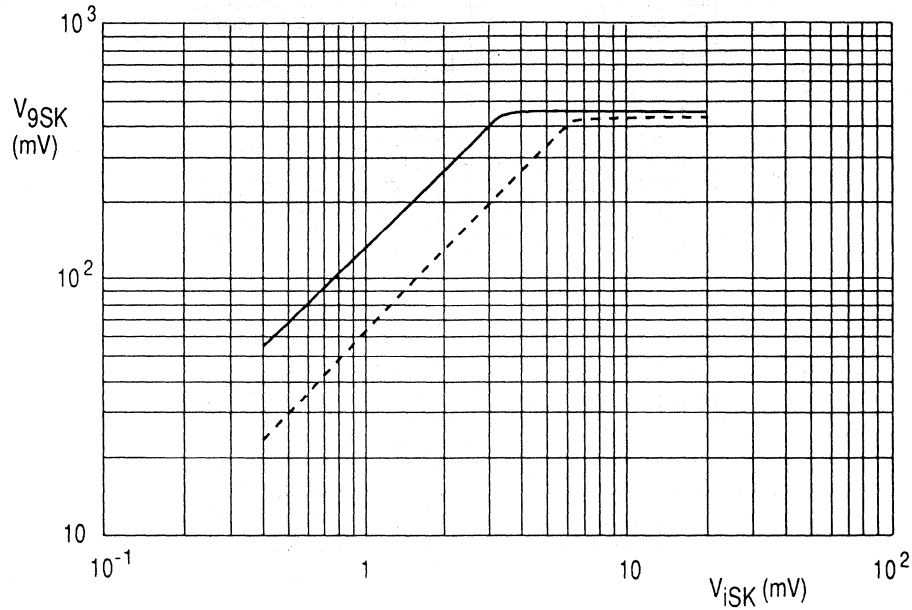


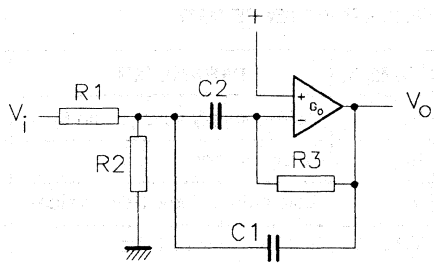
Fig.6 Control characteristic of the SK amplifier at V_p = 8.5 V, m_{BK} = 60 % and Q_L = 70.

FILTER INFORMATION

Gain

Amplifier conditions: $G_o >> G_v$ and $G_o >> 2 \times Q^2$

$$G_v = -\frac{\frac{p}{R1 \times C1}}{p^2 + p \times \frac{C1 + C2}{R3 \times C1 \times C2} + \frac{R1 + R2}{R1 \times R2 \times R3 \times C1 \times C2}}$$, in which $p = j\omega$ and $G_v = \frac{V_o}{V_i}$.



	GENERAL EQUATION	C1 = C2 = C	C1 = C2 = C R2 << R1
resonance frequency $\omega_r =$	$\frac{1}{\sqrt{\frac{R1 \times R2}{R1 + R2} \times R3 \times C1 \times C2}}$	$\frac{1}{C\sqrt{\frac{R1 \times R2}{R1 + R2} \times R3}}$	$\frac{1}{C\sqrt{R2 \times R3}}$
gain at $\omega = \omega_r$ $-G_{vr} =$	$\frac{C2}{C1 + C2} \times \frac{R3}{R1}$	$\frac{1}{2} \times \frac{R3}{R1}$	$\frac{1}{2} \times \frac{R3}{R1}$
quality $Q =$	$\sqrt{\frac{C1 \times C2}{C1 + C2}} \times \sqrt{\frac{R3\,(R1 + R2)}{R1 \times R2}}$	$\frac{1}{2}\sqrt{\frac{R3\,(R1 + R2)}{R1 \times R2}}$	$\frac{1}{2} \times \frac{R3}{R2}$

Recommended components

C1, C2	metallized polycarbonate film (MKC) capacitors; ±5 %
and	
R1, R2, R3	metal film (MR) resistors; ±2 %
or	
C1, C2	metallized polyester film (MKT) capacitors; ±5 %
and	
R1, R2, R3	carbon film (CR) resistors; ±2 %

Philips Semiconductors

Data sheet	
status	Preliminary specification
date of issue	March 1992

TDA1591/T
PLL stereo decoder and noise blanker

FEATURES

- Adjustment-free voltage controlled PLL oscillator for ceramic resonator (f = 456 kHz).
- Mono/stereo switching, dependent on pilot signal.
- Analog control of mono/stereo change over (stereo blend, SNC).
- Adjacent channel noise suppression (114 kHz).
- Pilot canceller
- Analog control of de-emphasis (High Cut Control input, HCC).
- Applicable as source selector for AM/FM/cassette switching
- Separate interference noise detector
- Integrated input low-pass filter for delayed noise blanking.
- Noise blanking at MPX-demodulator outputs
- Internal voltage stabilization

GENERAL DESCRIPTION

The TDA1591/T is a monolithic bipolar integrated circuit providing the stereo decoder function and noise blanking for FM car radio applications.
The device operates in a power supply range of 7.5 to 12 V.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_P	positive supply voltage (pin 5)	7.5	10	12	V
I_P	supply current	–	12	–	mA
V_o	audio output signal (RMS value)	–	900	–	mV
THD	total harmonic distortion	–	0.1	0.3	%
S/N	signal-to-noise ratio	–	76	–	dB
α	channel separation	–	40	–	dB
V_{trigg}	interference voltage trigger level	–	10	–	mV

ORDERING AND PACKAGE INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA1591	20	DIL	plastic	SOT146
TDA1591T	20	mini-pack	plastic	SOT163A

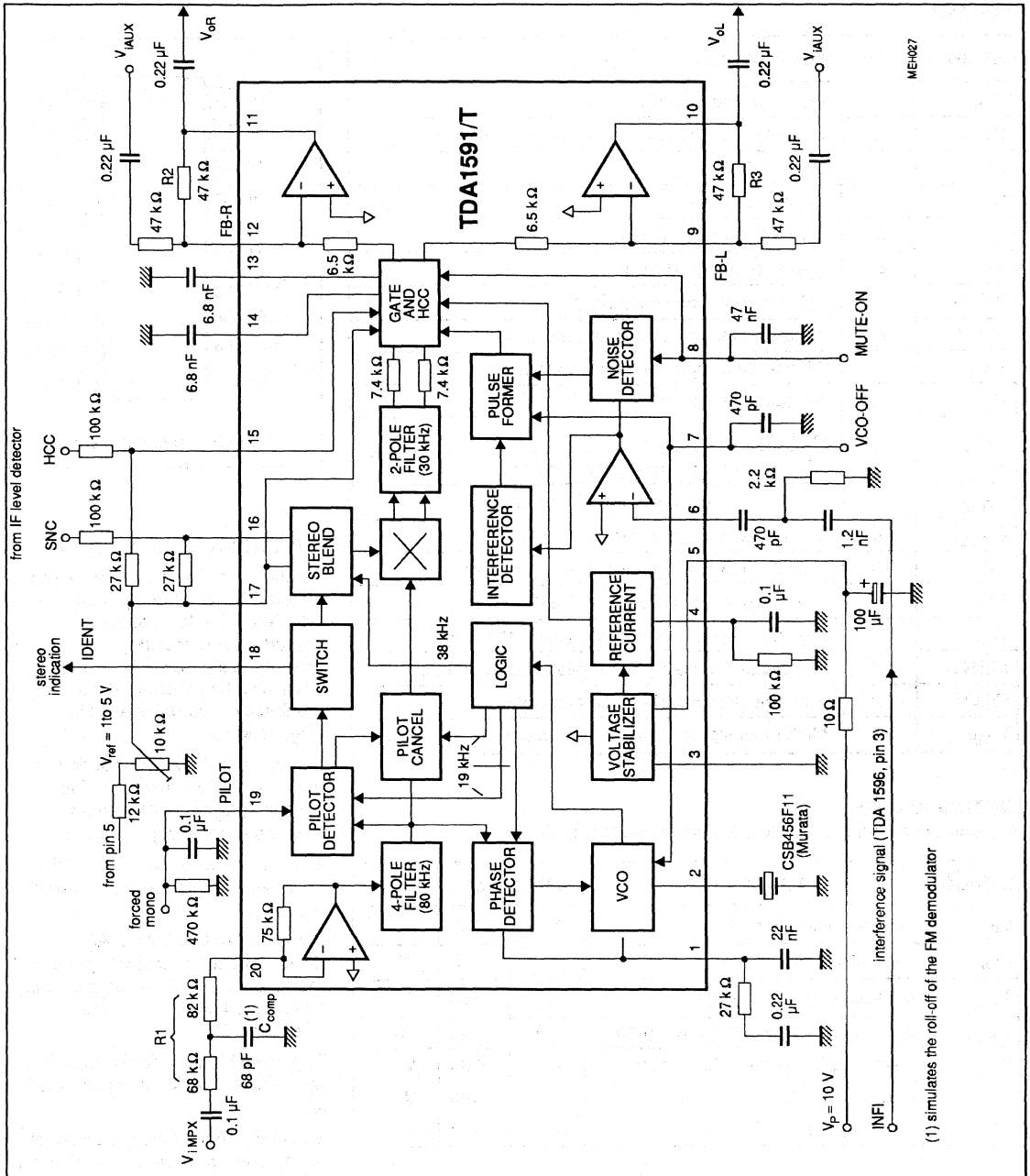


Fig.1 Block diagram, test and application circuit.

PLL stereo decoder and noise blanker

TDA1591/T

PINNING

SYMBOL	PIN	DESCRIPTION
PLL	1	phase locked loop filter
OSC	2	oscillator input/output pin for ceramic resonator
GND	3	ground (0 V)
I_{ref}	4	reference current
V_P	5	supply voltage (+10 V)
INFI	6	interference signal input
PUFO	7	pulse former time constant, VCO off
NDET	8	noise detector time constant, mute on
FB-L	9	AF feedback input for left audio signal
V_{oL}	10	AF output signal left
V_{oR}	11	AF output signal right
FB-R	12	AF feedback input for right audio signal
C_{DEEL}	13	de-emphasis capacitor for left channel
C_{DEER}	14	de-emphasis capacitor for right channel
HCC	15	High Cut Control input for de-emphasis control
SNC	16	stereo blend input (Stereo Noise Controller)
V_{ref}	17	externally-applied reference voltage of 1 to 5 V
IDENT	18	identification output (High = pilot existing, stereo)
PILOT	19	pilot detector level (forced mono input)
V_{iMPX}	20	MPX input signal from IF demodulator

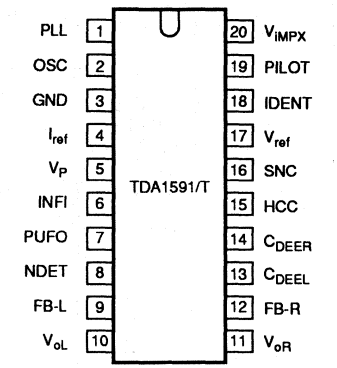


Fig.2 Pin configuration.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_P	supply voltage (pin 5)	0	13.2	V
P_{tot}	total power dissipation	0	0.25	W
T_{stg}	storage temperatur range	−55	+150	°C
T_{amb}	operating ambient temperatur range	−40	+85	°C
V_{ESD}	electrostatic handling* for all pins	−	±600	V
	except pin 1, 16	−	±400	V
	pin 5	−	±300	V

* Equivalent to discharging a 200 pF capacitor through a 0 Ω series resistor.

FUNCTIONAL DESCRIPTION

By changing the value of the input resistor R1 the MPX input can be adapted to the level of the FM demodulator output (Fig.3). The total gain of the stereo decoder is applicable by variation of the feedback resistors R2 and R3 (Fig.1 and 4).

In mute and VCO-OFF position the output amplifier can be used for cassette playback, AM-stereo purpose or other signal sources.

The Stereo Noise Controller SNC provides a smooth mono to stereo take over (Fig.5).

For High Cut Control (HCC), dependent on an analog input signal, the de-emphasis time constant can be changed to higher values (Fig.7 and 8).

The noise blanking facility is achieved by gating the stereo decoder output signal.

The interference detector generates a gating pulse preferable forced by the level detector voltage of the IF part.

CHARACTERISTICS

V_P = 10 V, T_{amb} = +25 °C, input signal $V_{i\ MPX\ (p-p)}$ = 1.7 V; m = 100% (deviation Δf = ±75 kHz, f_{mod} = 1 kHz), de-emphasis 50 µs and serial resistor at input R1 = 150 kΩ; measurements taken in Fig.1 unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	positive supply voltage (pin 5)		7.5	10	12	V
I_P	supply current		–	12	–	mA
Stereo decoder						
V_i	MPX input signal on pin 20 (peak-to-peak value)		–	1.7	–	V
ΔV_i	overdrive margin of MPX input signal	THD = 1%	3	–	–	dB
V_o	AF mono output signal at pins 10 and 11 (RMS value)	without pilot	–	900	–	mV
ΔV_o	overdrive margin of output signal	THD = 1%	3	–	–	dB
V_{10-11}/V_o	difference of output voltage levels		–	–	1	dB
$V_{10,11}$	DC output voltage (pins 10 and 11)		3.3	3.8	4.3	V
$R_{10,11}$	output resistance		–	130	–	Ω
α	channel separation, see Fig.6	pin 16 open-circuit	–	40	–	dB
THD	total harmonic distortion		–	0.1	0.3	%
S/N	signal-to-noise ratio	f = 20 to 16000 Hz	–	76	–	dB
α_{19}	pilot signal suppression	f = 19 kHz	–	50	–	dB
α_{38}	subcarrier suppression	f = 38 kHz	–	50	–	dB
α_{57}		f = 57 kHz	–	46	–	dB
α_{76}		f = 76 kHz	–	60	–	dB
α_2	intermodulation for f_{spur} = 1 kHz	f_{mod} = 10 kHz, note 1	–	60	–	dB
α_3		f_{mod} = 13 kHz	–	58	–	dB
$\alpha_{57\ VF}$	traffic radio (VWF)	f = 57 kHz, note 2	–	70	–	dB
α_{67}	SCA (subsidiary communications authorization)	f = 67 kHz, note 3	70	–	–	dB
α_{114}	ACI (adjacent channel interference)	f = 114 kHz, note 4	–	80	–	dB
α_{190}		f = 190 kHz	–	70	–	dB
RR	ripple rejection with ripple on V_P	f = 100 Hz; $V_{ripple\ (rms)}$ = 100 mV	–	35	–	dB
VCO (pin 2)						
f_{osc}	oscillator frequency (ceramic resonator)		–	456	–	kHz
f_{osc}	frequency range of free running oscillator		452	–	460	kHz
$\Delta f/f$	capture and holding range		–	1	–	%
V_7	VCO-OFF voltage (pin 7)		0	–	0.6	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Mono/stereo control (pins 16, 17 and 19)						
$V_{i\ pil}$	pilot threshold voltage for automatic switching by pilot input voltage (RMS value)					
	for stereo on		–	24	30	mV
	for stereo off		8	20	–	mV
H	hysteresis of pilot threshold voltage		–	2	–	dB
V_{19}	switching voltage for external mono control (pin 19)		0	–	1	V
V_{ref}	reference input voltage range (pin 17)		1	–	5	V
V_{16-17}	control voltage for channel separation due to pin 17 (V_{ref}), see Fig.5	α = 6 dB	–	–85	–	mV
		α = 26 dB	–	–32	–	mV
	pilot indicator logic level output					
V_{18}	LOW voltage (pin 18)	I_{18} = –500 µA	–	250	400	mV
I_{18}	HIGH current	V_{18} = 10 V	–	–	1	µA
Muting (pin 8)						
V_8	mute attenuation (pin 8)	V_8 < 0.4 V	–	80	–	dB
		V_8 > 4 V	–	–	0.2	dB
$V_{10, 11}$	DC offset voltage	after muting	–	–	±400	mV
High Cut Control HCC (pin 15)						
t_{deem}	control range of de-emphasis	(Fig.7 and 8)				
	for European standard	C_{deem} = 6.8 nF	50	–	150	µs
	for US standard	C_{deem} = 10 nF	75	–	225	µs
V_{15-17}	control voltage (pin 15 due to pin 17) in both standards	lower value t_{deem}	–	0	–	mV
		upper value t_{deem}	–	–300	–	mV
Noise interference detector						
V_{trigg}	trigger threshold (pin 6)	f_{int} = 120 kHz				
		$V_{8\ (DC)}$ = 7.7 V	–	10	–	mV
		$V_{8\ (DC)}$ = 6.7 V	–	100	–	mV
ΔV_8	voltage offset as a function of V_{trigg}	$V_{6\ trigg}$ = 10 mV	–	200	–	mV
		$V_{6\ trigg}$ = 100 mV	–	2.3	–	V
t_{suppr}	AF suppression time, pulse width		–	40	–	µs
$I_{13,14}$	input offset current (pins 13 and 14)	during AF suppression time	–	20	–	nA
V_{pulse}	trigger sensitivity (pin 6)	τ_{pulse} = 10 µs	–	10	–	mV

Notes to the characteristics

1. Intermodulation suppression (BFC: Beat Frequency Components)

$$\alpha_2 = \frac{V_{o(signal)}\ (\text{at } 1\ \text{kHz})}{V_{o(spurious)}\ (\text{at } 1\ \text{kHz})} \quad ; \quad f_s = (2 \times 10\ \text{kHz}) - 19\ \text{kHz}$$

$$\alpha_3 = \frac{V_{o(signal)}\ (\text{at } 1\ \text{kHz})}{V_{o(spurious)}\ (\text{at } 1\ \text{kHz})} \quad ; \quad f_s = (3 \times 13\ \text{kHz}) - 38\ \text{kHz}$$

measured with 91% mono signal; f_{mod}= 10 kHz or 13 kHz; 9% pilot signal

2. Traffic radio (V.F.) suppression

$$\alpha_{57}\ (\text{VF}) = \frac{V_{o(signal)}\ (\text{at } 1\ \text{kHz})}{V_{o(spurious)}\ (\text{at } 1\ \text{kHz} \pm 23\ \text{Hz})}$$

measured with 91% stereo signal; f_{mod}= 1 kHz; 9% pilot signal;
5% traffic subcarrier (f = 57 kHz; f_{mod}= 23 Hz AM, m = 0.6).

3. SCA (Subsidiary Communication Authorization)

$$\alpha_{67} = \frac{V_{o(signal)}\ (\text{at } 1\ \text{kHz})}{V_{o(spurious)}\ (\text{at } 9\ \text{kHz})} \quad ; \quad f_s = (2 \times 38\ \text{kHz}) - 67\ \text{kHz}$$

measured with 81% mono signal; f_{mod}= 1 kHz; 9% pilot signal;
10% SCA subcarrier (f_s = 67 kHz, unmodulated).

4. ACI (Adjacent Channel Interference)

$$\alpha_{114} = \frac{V_{o(signal)}\ (\text{at } 1\ \text{kHz})}{V_{o(spurious)}\ (\text{at } 4\ \text{kHz})} \quad ; \quad f_s = 110\ \text{kHz} - (3 \times 38\ \text{kHz})$$

$$\alpha_{190} = \frac{V_{o(signal)}\ (\text{at } 1\ \text{kHz})}{V_{o(spurious)}\ (\text{at } 4\ \text{kHz})} \quad ; \quad f_s = 186\ \text{kHz} - (5 \times 38\ \text{kHz})$$

measured with 90% mono signal; f_{mod}= 1 kHz; 9% pilot signal; 1% spurious signal
(f_s = 110 kHz or 186 kHz, unmodulated).

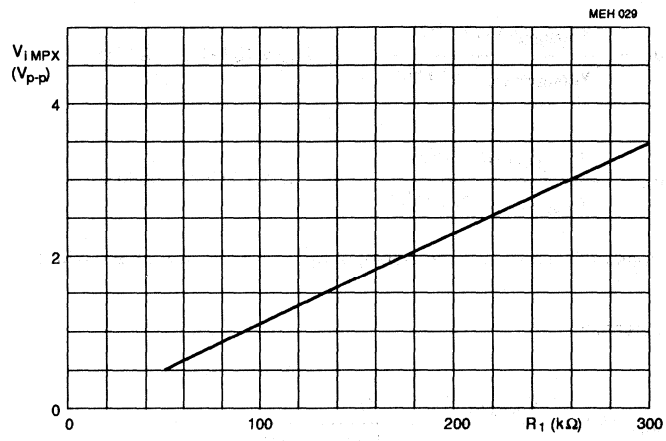


Fig.3 Input signal as a function of serial input resistor R1.

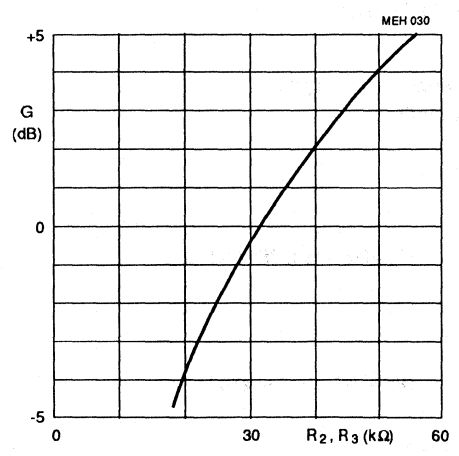


Fig.4 Over all signal gain as a function of feedback resistors R2 and R3 (R1 = 150 kΩ).

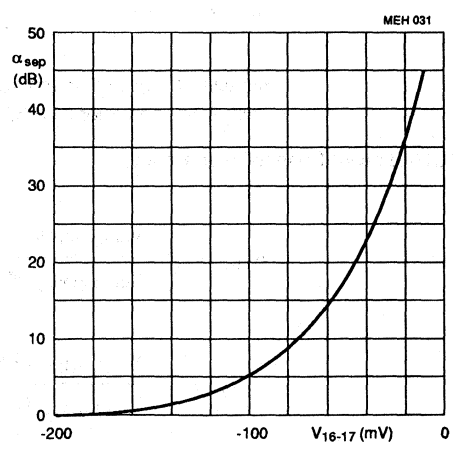


Fig.5 Stereo blend characteristic (SNC).

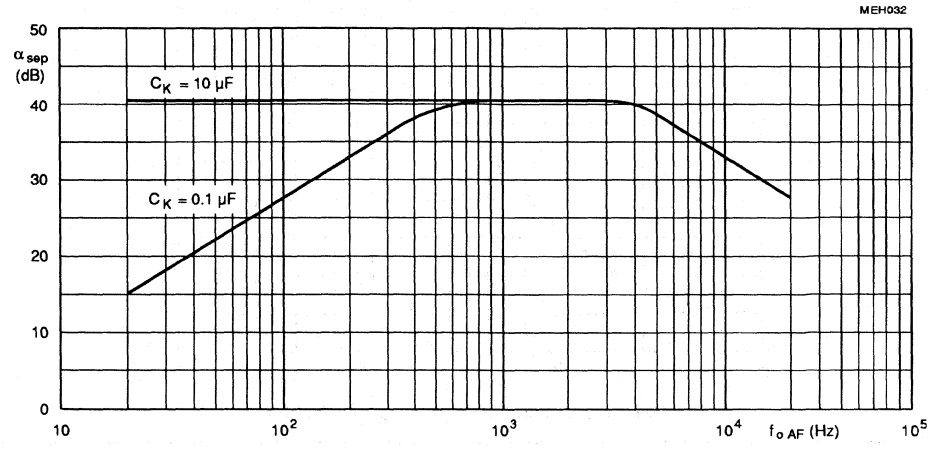


Fig.6 Channel separation as a function of audio frequency.

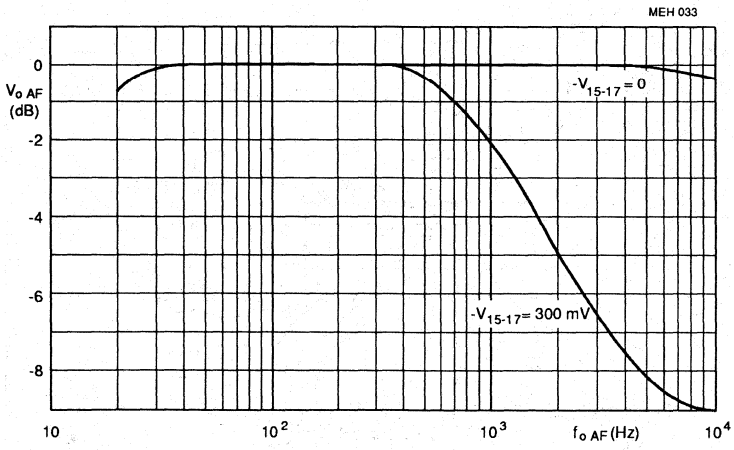


Fig.7 High Cut Control (HCC) as a function of audio frequency.

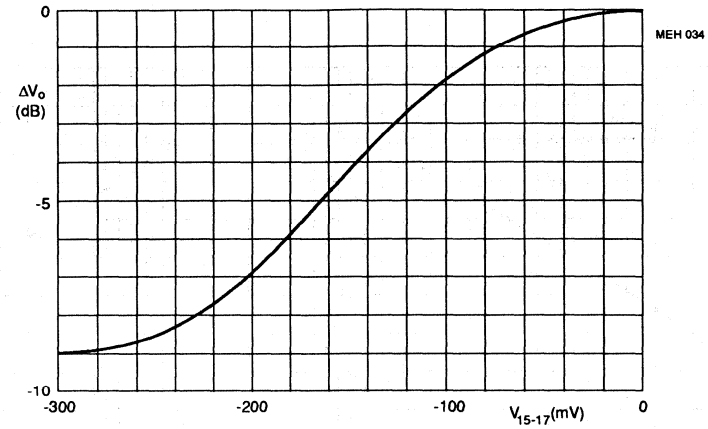


Fig.8 High Cut Control (HCC) with f_{mod} = 10 kHz.

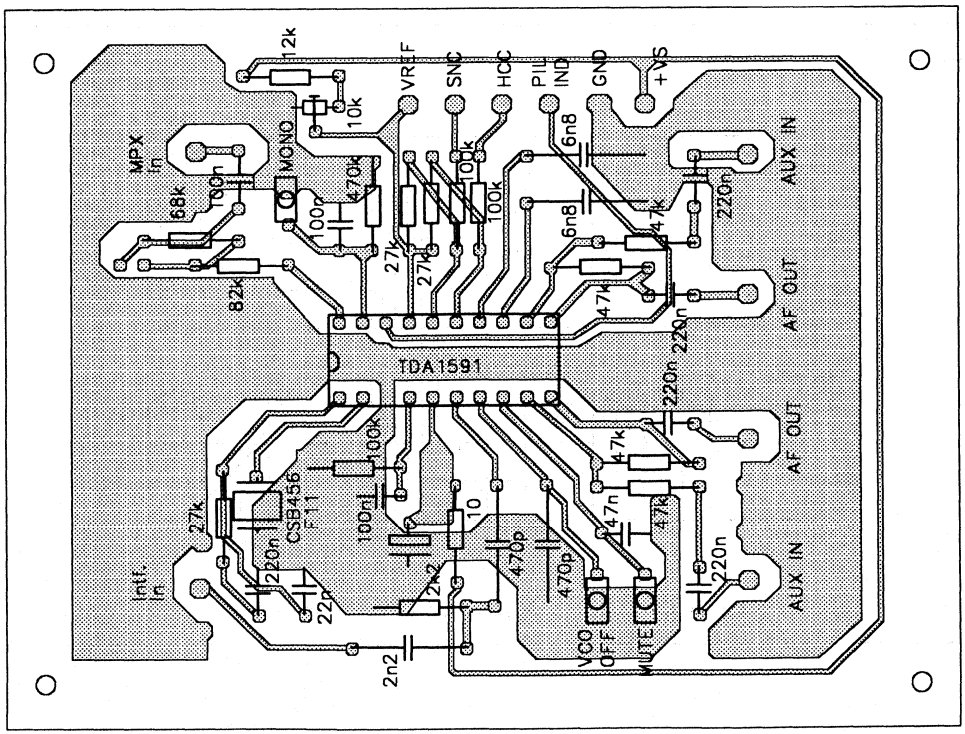


Fig.9 TDA1591 testboard (component side).

PLL stereo decoder and noise blanker — TDA1592

FEATURES

- Adjustment-free voltage controlled PLL oscillator for ceramic resonator (f = 456 kHz)
- Mono/stereo switching, dependent on pilot signal
- Analog control of mono/stereo change over (stereo blend, SNC)
- Adjacent channel noise suppression (114 kHz)
- Pilot canceller
- Analog control of de-emphasis (High Cut Control input, HCC)
- Reduced and controlled de-emphasis for AM operation (pin 7 to GND)
- Applicable as source selector for AM/FM/cassette switching
- Soft mute for silent tuning
- Separate interference noise detector
- Integrated input low-pass filter for delayed noise blanking
- Noise blanking at MPX-demodulator outputs.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_P	positive supply voltage (pin 5)	7.5	10	12	V
I_P	supply current	–	15	20	mA
V_o	audio output signal (RMS value)	800	900	1000	mV
THD	total harmonic distortion	–	0.1	0.3	%
S/N	signal to noise ratio	–	82	–	dB
α	channel separation	30	40	–	dB
V_{trigg}	interference voltage trigger level	–	10	–	mV

GENERAL DESCRIPTION

The TDA1592 is a monolithic bipolar integrated circuit providing the stereo decoder function and noise blanking for FM car radio applications.
The device operates in a power supply range of 7.5 to 12 V.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA1592	20	DIL	plastic	SOT146
TDA1592T	20	mini-pack	plastic	SOT163A

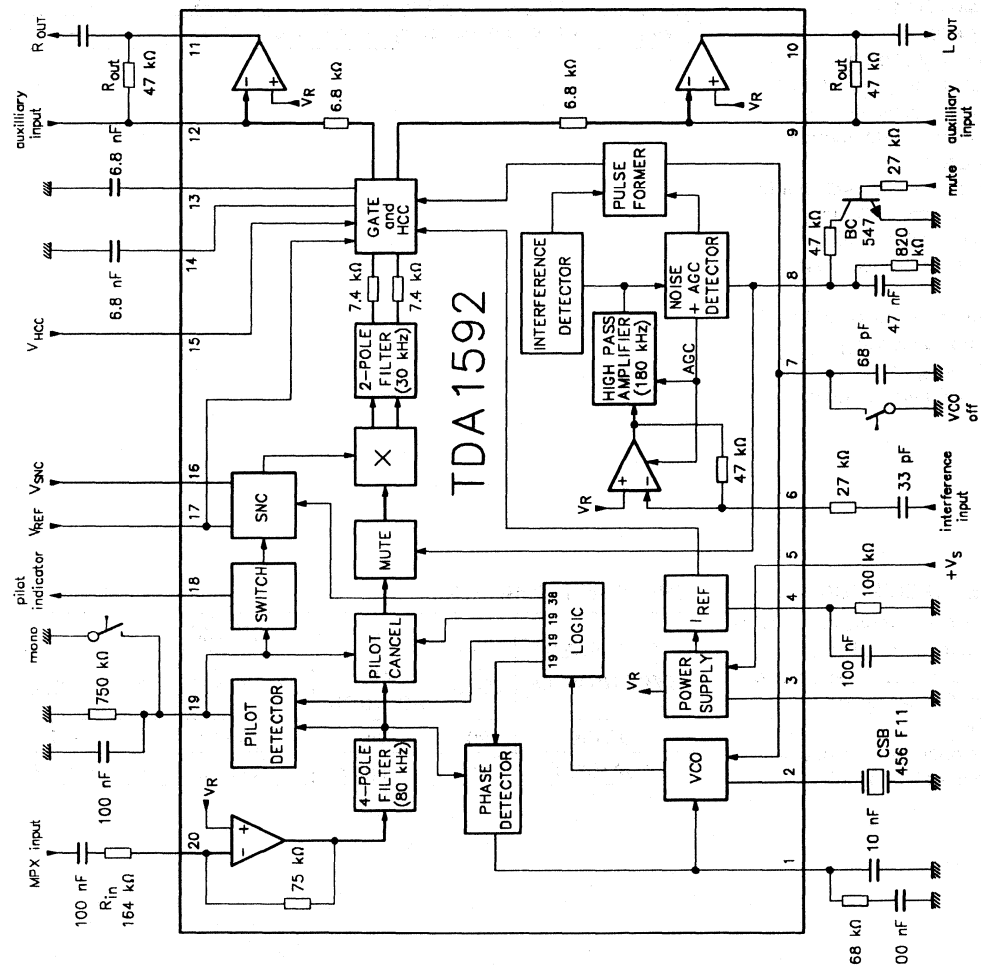


Fig.1 Block diagram, test and application circuit.

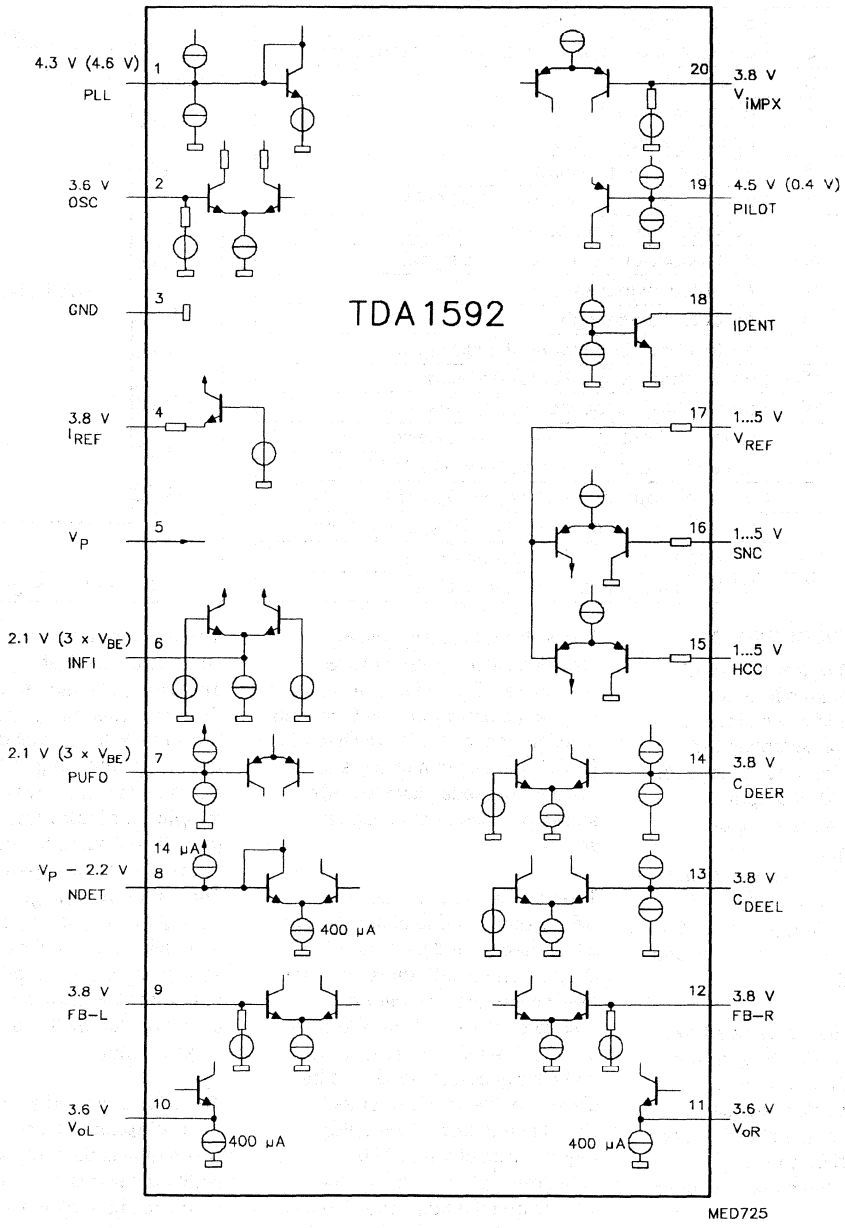


Fig.2 Internal circuits.

PINNING

SYMBOL	PIN	DESCRIPTION
PLL	1	phase locked loop filter
OSC	2	oscillator input/output pin for ceramic resonator
GND	3	ground (0 V)
I_{REF}	4	reference current
V_P	5	supply voltage (+10 V)
INFI	6	interference signal input
PUFO	7	pulse former time constant, VCO OFF
NDET	8	noise detector time constant, mute ON
FB-L	9	AF feedback input for left audio signal
V_{oL}	10	AF output signal left
V_{oR}	11	AF output signal right
FB-R	12	AF feedback input for right audio signal
C_{DEEL}	13	de-emphasis capacitor for left channel
C_{DEER}	14	de-emphasis capacitor for right channel
HCC	15	High Cut Control input for de-emphasis control
SNC	16	stereo blend input (Stereo Noise Controller)
V_{REF}	17	externally-applied reference voltage of 1 to 5 V
IDENT	18	identification output (HIGH = pilot existing, stereo)
PILOT	19	pilot detector level (forced mono input)
V_{iMPX}	20	MPX input signal from IF demodulator

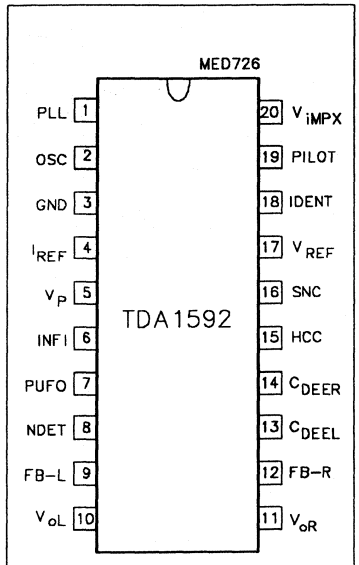


Fig.3 Pin configuration.

FUNCTIONAL DESCRIPTION

The **MPX input** of the TDA1592 (pin 20) is the null-node of an operational amplifier with internal feedback resistor. Adapting the stereo decoder input to the level of the FM demodulator output is realized by the value of input resistor R_{IN} (Fig.4).
The total gain of the stereo decoder is applicable by varying the feedback resistors R_{out} (pins 9, 10, 11 and 12) of the output operational amplifiers (Fig.5).

The input amplifier is followed by an **integrated 4th order Bessel low pass filter** with a cut-off frequency of 80 kHz. It provides necessary signal delay for noise blanking and damping of high frequency interferences at the stereo decoder input.

The **soft mute** facility (pin 8) provides silent tuning for RDS processing. The mute time constant may be adjusted from pin 8. In mute position and the VCO switched off (pin 7), the output amplifiers can be used for cassette playback, AM stereo purpose or other signal sources.

The voltage to current converted MPX signal is fed to phase detector, pilot detector, and pilot canceller circuits. The **oscillator** is alignment free with an external ceramic resonator at 456 kHz as reference (pin 2). The required 19 kHz and 38 kHz signals are generated by division of the oscillator output signal in a **logical circuit**. For regeneration of the 38 kHz subcarrier, a PLL is used. The 19 kHz quadrature phase signal is fed to the 19 kHz **phase detector**, where it is compared with the incoming pilot tone. The DC output signal of the phase detector (pin 1) controls the oscillator (PLL).
The **pilot presence detector** is driven by internally generated in phase 19 kHz. Its pilot dependant DC output voltage (pin 19) is fed to a threshold switch, which activates the **pilot indicator** logic output (pin 18) and turns the stereo decoder to stereo operation.
The same DC voltage is used to control the amplitude of an anti-phase internally generated 19 kHz signal. In the **pilot canceller**, the pilot tone is compensated by this anti-phase 19 kHz signal.

The pilot cancelled signal is fed to the **multiplex decoder**. There, the side signal is demodulated and combined with the main signal in a matrix to left and right audio channel.

Compensation for roll-off in the incoming MPX signal caused by IF filters and FM demodulator is realized by corresponding side signal amplification.
A smooth mono to stereo take over, which is controlled by the level detector voltage of the IF part, is achieved by the **Stereo Noise Controller, SNC** (pins 16 and 17; Fig.7).

From the output of the MPX demodulator the signals are fed to **2-pole low pass filters** with a cut-off frequency of 30 kHz to provide additional signal delay for noise blanking and attenuation of the subcarrier and its harmonics.

These filters are followed by the **noise suppression gates**, which are combined with **de-emphasis** and High Cut Control (HCC). The de-emphasis is defined by internal resistors (aligned by external current) and external capacitors (pins 13 and 14). For **High Cut Control**, the de-emphasis time constant can be changed to higher values (pins 15 and 17; Figs 8 to 10).

This function is controlled by an analog input signal, derived from the level detector voltage of the IF part. When the VCO is turned off (pin 7 to GND) de-emphasis is reduced to 20 µs for full frequency response when AM-AF is fed through the stereo decoder. De-emphasis remains controllable.

From the gate circuits audio is fed through internal series resistors to the inverting inputs of the **output operational amplifiers** (pins 9 and 12), which can also be used as signal inputs for cassette playback or other sources when the mute is activated. The gain of these amplifiers is defined by external feedback resistors R_{out} (pins 9, 10, 11 and 12).

Input of the **ignition noise blanker** is the null node of an operational amplifier (pin 6). It can be driven by the level detector output of the FM-IF limiter or/and the MPX signal. Its sensitivity is dependent on the value of the series input resistor at pin 6.

The operational amplifier output signal is fed through an **integrated 180 kHz high pass filter**, becomes amplified and then fed in parallel to the noise detector and the interference detector. The **noise detector** is a negative peak detector. Its output (pin 8) controls the trigger sensitivity (preventation to false triggering at noisy input signals) and the attenuation of the input operational amplifier. The output of the **interference detector**, when receiving a steep pulse, fires a monoflop, contained in the **pulse former** circuit. The time constant of the monoflop is defined by an external capacitor (pin 7) and its output activates the blanking gates in the audio.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_P	supply voltage (pin 5)	0	13.2	V
P_{tot}	total power dissipation	0	0.25	W
T_{stg}	storage temperature	−55	+150	°C
T_{amb}	operating ambient temperature	−40	+85	°C
V_{ESD}	electrostatic handling for all pins (note 1)	±500	−	V

Note to the limiting values

1. Equivalent to discharging a 200 pF capacitor through a 0 Ω series resistor.

CHARACTERISTICS

V_P = 10 V, T_{amb} = +25 °C, input signal $V_{i\,MPX(p\text{-}p)}$ = 1.7 V; m = 100% (deviation Δf = ±75 kHz, f_{mod} = 1 kHz), de-emphasis 50 µs and serial resistor at input R_1 = 164 kΩ; measurements taken in Fig.1 unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	positive supply voltage (pin 5)		7.5	10	12	V
I_P	supply current		–	15	20	mA
Stereo decoder						
V_i	MPX input signal (peak-to-peak value)		–	1.7	–	V
ΔV_i	overdrive margin of MPX input signal	THD = 1%	6	–	–	dB
V_o	AF mono output signal at pins 10 and 11 (RMS value)	without pilot	800	900	1000	mV
ΔV_o	overdrive margin of output signal	THD = 1%	6	–	–	dB
$V_{10\text{-}11}/V_o$	difference of output voltage levels		–	–	1	dB
V_{10}, V_{11}	DC output voltage (pins 10 and 11)		3.2	3.6	4.0	V
$R_{10\text{-}11}$	output resistance		–	150	–	Ω
I_O	output current		–	–	400	µA
R_2, R_3	maximum feedback resistor		–	–	68	kΩ
$V_{4\text{-}3}$	reference voltage		3.7	3.8	3.9	V
α	channel separation	pin 16 open-circuit; see Fig.7	30	40	–	dB
THD	total harmonic distortion		–	0.1	0.3	%
S/N	signal-to-noise ratio	f = 20 to 16000 Hz	79	82	–	dB
α_{19}	pilot signal suppression	f = 19 kHz	40	50	–	dB
α_{38}	subcarrier suppression	f = 38 kHz	35	50	–	dB
α_{57}		f = 57 kHz	46	–	–	dB
α_{76}		f = 76 kHz	–	60	–	dB
α_2	intermodulation for f_{spur} = 1 kHz	f_{mod} = 10 kHz, note 1	–	60	–	dB
α_3		f_{mod} = 13 kHz	–	58	–	dB
$\alpha_{57\,VF}$	traffic radio (VWF)	f = 57 kHz, note 2	–	70	–	dB
α_{67}	SCA (Subsidiary Communications Authorization)	f = 67 kHz, note 3	70	–	–	dB
α_{114}	ACI (Adjacent Channel Interference)	f = 114 kHz, note 4	–	80	–	dB
α_{190}		f = 190 kHz, note 4	–	70	–	dB
RR	power supply ripple rejection	f = 100 Hz $V_{ripple\,(RMS)}$ = 100 mV	–	35	–	dB
VCO (pin 2)						
f_{osc}	oscillator frequency (ceramic resonator)		–	456	–	kHz
	frequency range of free running oscillator		451	–	459	kHz
$\Delta f/f$	capture and holding range		–	±0.65	–	%
V_7	VCO-OFF voltage (pin 7)		0	–	0.6	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Mono/stereo control (pins 16, 17 and 19)						
$V_{i\,pil}$	pilot threshold voltage for automatic switching by pilot input voltage (RMS value)					
	for stereo ON		–	24	30	mV
	for stereo OFF		8	20	–	mV
H	hysteresis of pilot threshold voltage		–	2	–	dB
V_{19}	switching voltage for external mono control (pin 19)		–	–	0.7	V
V_{REF}	reference input voltage range (pin 17)		1	–	5	V
$V_{16\text{-}17}$	control voltage for channel separation due to pin 17 (V_{REF}), see Fig.6	α = 6 dB	–80	–100	–120	mV
		α = 20 dB	–40	–55	–70	mV
	pilot indicator logic level output					
V_{18}	LOW voltage (pin 18)	I_{18} = –500 µA	–	250	400	mV
I_{18}	HIGH current	V_{18} = 10 V	–	–	1	µA
Muting (pin 8)						
V_8	mute attenuation (pin 8)	V_8 < 0.7 V	80	–	–	dB
		V_8 > 4 V	–	–	0.2	dB
$V_{10,\,11}$	DC offset voltage	after muting	–	–	±50	mV
High Cut Control (HCC) (pin 15)						
t_{deem}	control range of de-emphasis	see Figs 8 and 9				
	for European standard	C_{deem} = 6.8 nF	50	–	150	µs
	for USA standard	C_{deem} = 10 nF	75	–	225	µs
$V_{15\text{-}17}$	control voltage (pin 15 due to pin 17) in both standards	lower value t_{deem}	–	0	–	mV
		upper value t_{deem}	–	–300	–	mV
High Cut Control (HCC) (pin 15, pin 7 to GND)						
t_{deem}	control range of de-emphasis	see Fig.10				
	for European standard	C_{deem} = 6.8 nF	15	–	90	µs
	for USA standard	C_{deem} = 10 nF	22	–	135	µs
$V_{15\text{-}17}$	control voltage (pin 15 due to pin 17) in both standards	lower value t_{deem}	–	0	–	mV
		upper value t_{deem}	–	–300	–	mV
ΔV_{10}, ΔV_{11}	DC offset voltage at AF outputs (AM on/off)		–	–	±200	mV
Noise interference detector						
V_{pulse}	trigger sensitivity	τ_{pulse} = 10 µs	–	10	–	mV
ΔV_8	trigger threshold voltage offset as a function of V_{trigg}	f_{int} = 120 kHz				
		$V_{interf.in}$ = 10 mV	80	135	190	mV
		$V_{interf.in}$ = 100 mV	470	570	670	mV
t_{suppr}	AF suppression time, pulse width		–	40	–	µs
$I_{13,\,14}$	input offset current (pins 13 and 14)	during AF suppression time	–	20	–	nA

Notes to the characteristics

1. Intermodulation suppression (BFC: Beat Frequency Components)

$$\alpha_2 = \frac{V_{o(signal)}\ (\text{at } 1\ \text{kHz})}{V_{o(spurious)}\ (\text{at } 1\ \text{kHz})}; \quad f_s = (2 \times 10\ \text{kHz}) - 19\ \text{kHz}$$

$$\alpha_3 = \frac{V_{o(signal)}\ (\text{at } 1\ \text{kHz})}{V_{o(spurious)}\ (\text{at } 1\ \text{kHz})}; \quad f_s = (3 \times 13\ \text{kHz}) - 38\ \text{kHz}$$

measured with 91% mono signal; f_{mod} = 10 kHz or 13 kHz; 9% pilot signal.

2. ARI suppression

$$\alpha_{57\ ARI} = \frac{V_{o(signal)}\ (\text{at } 1\ \text{kHz})}{V_{o(spurious)}\ (\text{at } 1\ \text{kHz} \pm 23\ \text{Hz})}$$

measured with 91% stereo signal; f_{mod} = 1 kHz; 9% pilot signal;
5% ARI subcarrier (f = 57 kHz; f_{mod} = 23 Hz AM, m = 0.6).

3. SCA (Subsidiary Communication Authorization)

$$\alpha_{67} = \frac{V_{o(signal)}\ (\text{at } 1\ \text{kHz})}{V_{o(spurious)}\ (\text{at } 9\ \text{kHz})}; \quad f_s = (2 \times 38\ \text{kHz}) - 67\ \text{kHz}$$

measured with 81% mono signal; f_{mod} = 1 kHz; 9% pilot signal;
10% SCA subcarrier (f_s = 67 kHz, unmodulated).

4. ACI (Adjacent Channel Interference)

$$\alpha_{114} = \frac{V_{o(signal)}\ (\text{at } 1\ \text{kHz})}{V_{o(spurious)}\ (\text{at } 4\ \text{kHz})}; \quad f_s = 110\ \text{kHz} - (3 \times 38\ \text{kHz})$$

$$\alpha_{190} = \frac{V_{o(signal)}\ (\text{at } 1\ \text{kHz})}{V_{o(spurious)}\ (\text{at } 4\ \text{kHz})}; \quad f_s = 186\ \text{kHz} - (5 \times 38\ \text{kHz})$$

measured with 90% mono signal; f_{mod} = 1 kHz; 9% pilot signal;
1% spurious signal (f_s = 110 kHz or 186 kHz, unmodulated).

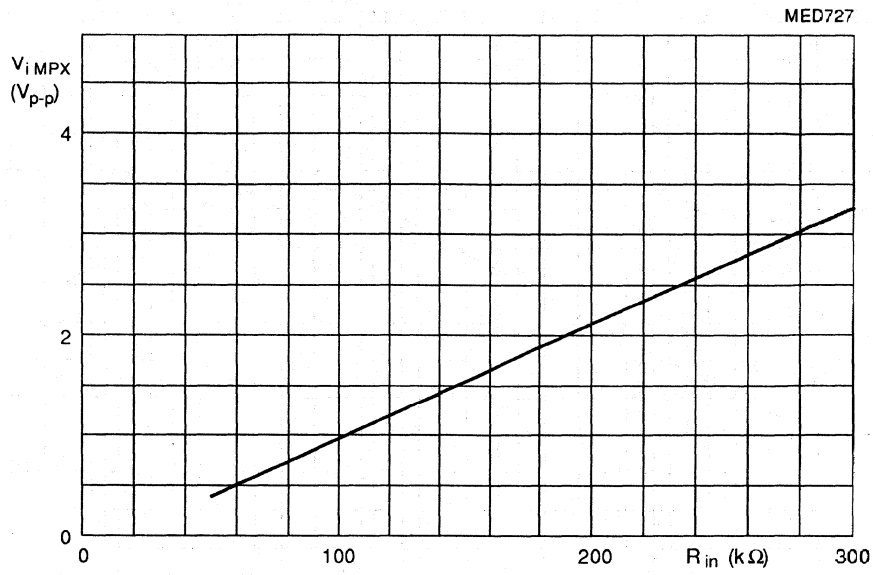


Fig.4 Input signal as a function of series input resistor R_{in}.

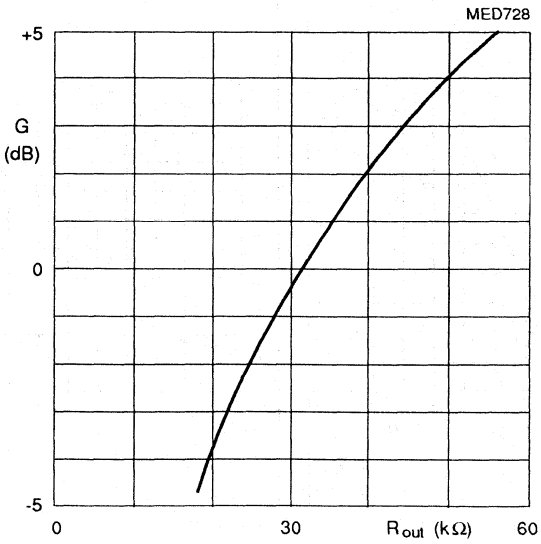


Fig.5 Overall signal gain as a function of feedback resistors R_{out} (R_{in} = 164 kΩ).

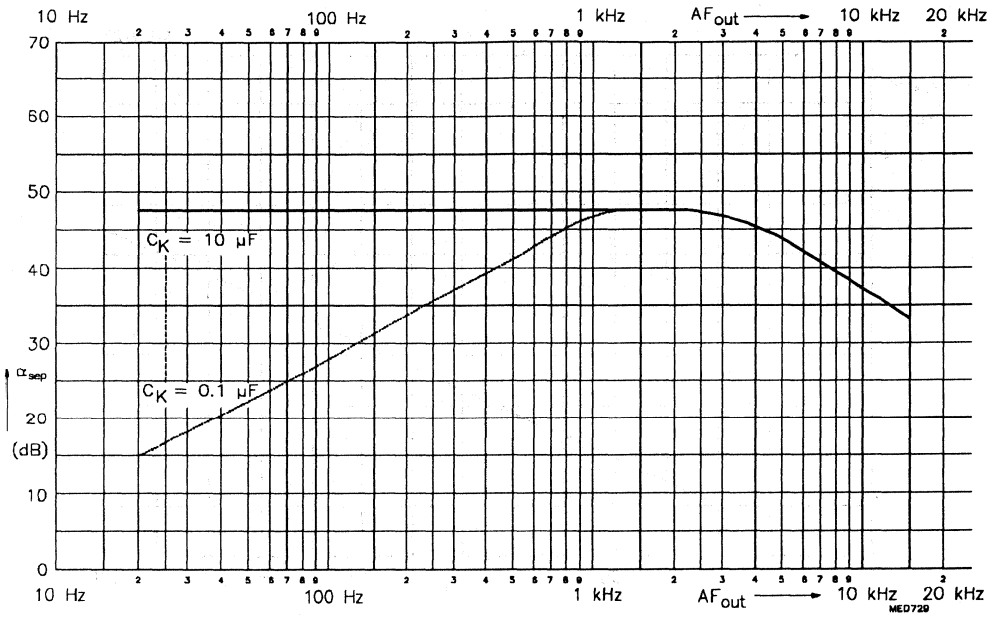


Fig.6 Channel separation as a function of audio frequency.

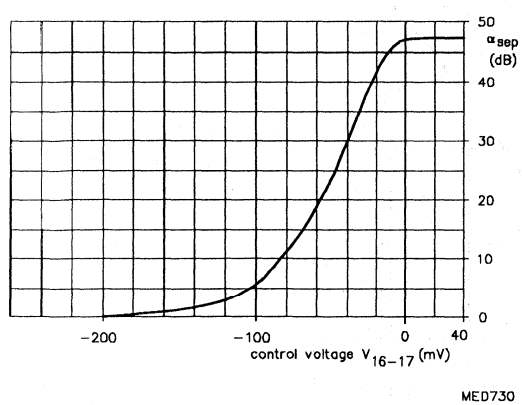


Fig.7 Stereo blend characteristic (SNC).

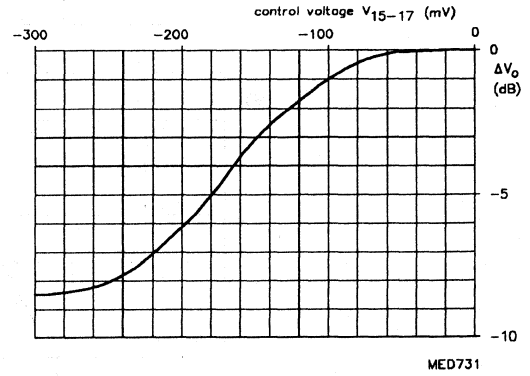


Fig.8 High Cut Control (HCC) with f_{mod} = 10 kHz.

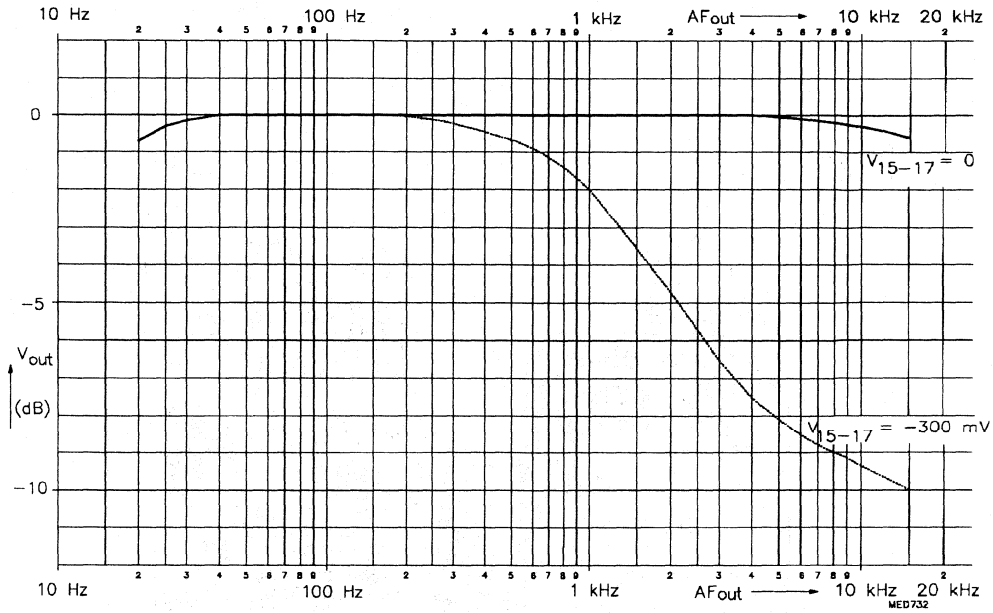


Fig.9 High Cut Control (HCC) with pre-emphasis as a function of audio frequency.

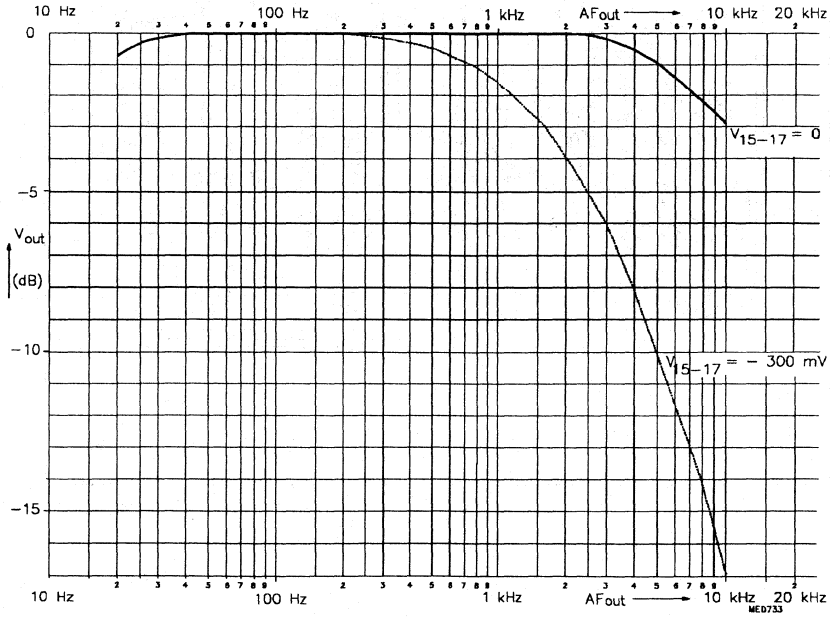


Fig.10 High Cut Control (HCC) as a function of audio frequency (pin 7 connected to GND, without pre-emphasis).

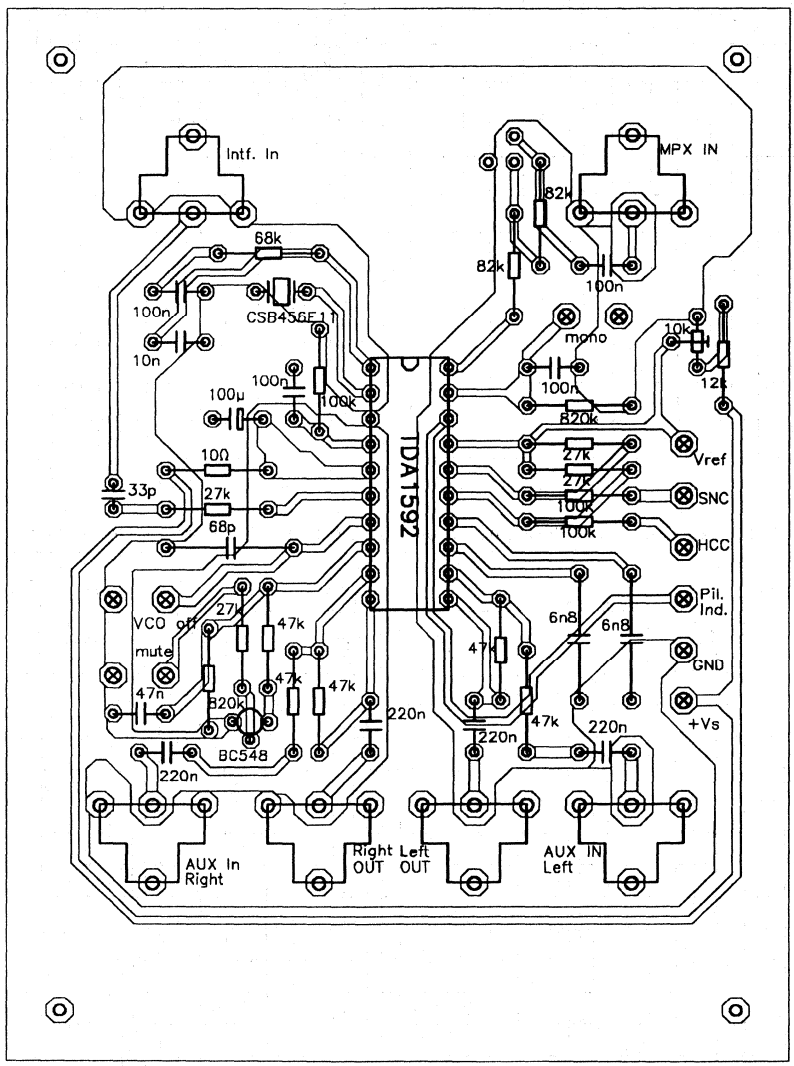


Fig.11 TDA1592 testboard (component side).

IF amplifier/demodulator for FM radio receivers TDA1593

FEATURES

- Balanced limiting amplifier
- Balanced coincidence demodulator
- Two open-collector stop pulse outputs for microcomputer tuning control
- Simulated behaviour of a ratio detector (internal field strength and detuning dependent voltage for dynamic AF signal muting)
- Mono/stereo blend field strength indication control voltage
- AFC output
- Internal compensation of AF signal total harmonic distortion (THD)
- Built-in hum and ripple rejection circuits.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_P	positive supply voltage (pin 1)	7.5	8.5	12	V
I_P	supply current ($I_2 = 0$)	–	20	26	mA
V_i	IF input sensitivity for limiting on pin 20 (RMS value)	14	22	35	μV
V_o	AF output signal on pin 4 (RMS value)	180	200	220	mV
S/N	signal-to-noise ratio (f_m = 400 Hz; Δf = ±75 kHz)	–	82	–	dB
THD	total harmonic distortion (f_m = 1 kHz; Δf = ±75 kHz)	–	0.2	0.6	%
T_{amb}	operating ambient temperature	–40	–	+85	°C

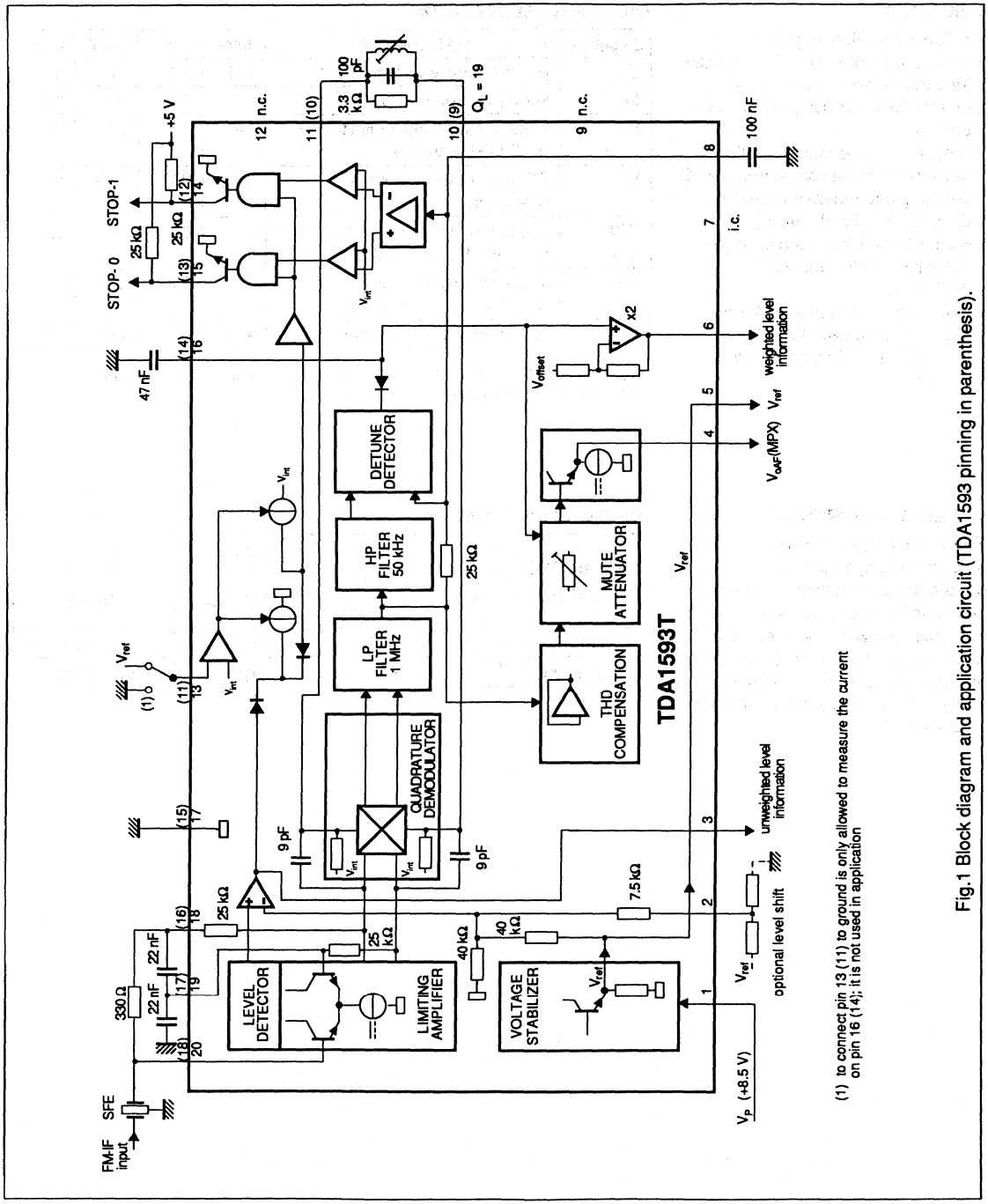
All pin numbers mentioned in this data sheet refer to the SO-version (TDA1593T) unless otherwise specified.

GENERAL DESCRIPTION

The TDA1593 provides IF amplification, symmetrical quadrature demodulation and level detection for quality home and car FM radio receivers and is suitable for mono and stereo reception. It may also be applied to common front ends, stereo decoders and AM receiver circuits.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA1593	18	DIL	plastic	SOT102
TDA1593T	20	mini-pack	plastic	SOT163A



(1) to connect pin 13 (11) to ground is only allowed to measure the current on pin 16 (14); it is not used in application

Fig.1 Block diagram and application circuit (TDA1593 pinning in parenthesis).

PINNING (SO-version TDA1593T; pinning for DIL-version in parenthesis)

SYMBOL	PIN	DESCRIPTION
V_P	1 (1)	supply voltage (+8.5 V)
LVA	2 (2)	level adjustment for stop condition
ULV	3 (3)	unweighted level output
V_{oAF}	4 (4)	audio frequency output (MPX signal)
V_{REF}	5 (5)	reference voltage output
WLV	6 (6)	weighted level output
i.c.	7 (7)	internal connected
DDV	8 (8)	detune detector voltage
n.c.	9 (–)	not connected
DEMI1	10 (9)	demodulator input 1
DEMI2	11 (10)	demodulator input 2
n.c.	12 (–)	not connected
TSW	13 (11)	tau switch input
ST1	14 (12)	STOP-1, stop pulse output 1
ST0	15 (13)	STOP-0, stop pulse output 0
MUTE	16 (14)	muting voltage
GND	17 (15)	ground (0 V)
LFB1	18 (16)	IF limiter feedback 1
LFB2	19 (17)	IF limiter feedback 2
V_{iIF}	20 (18)	IF signal input

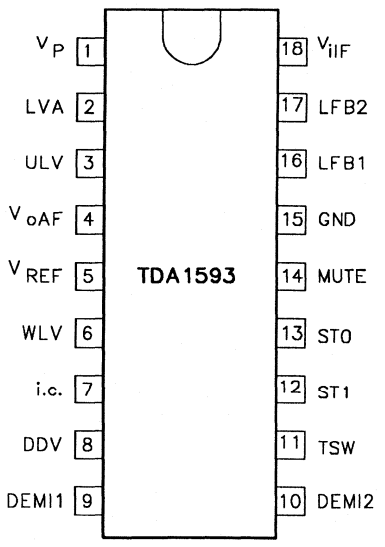


Fig.2 Pin configuration for DIL-version.

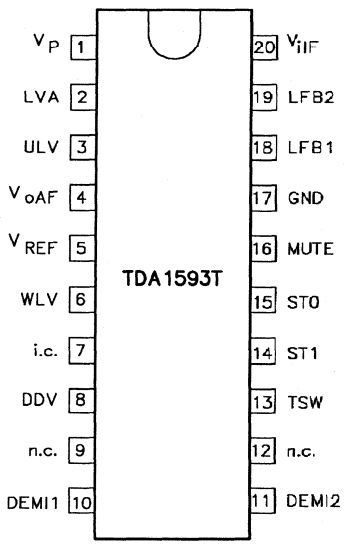


Fig.3 Pin configuration for SO-version.

FUNCTIONAL DESCRIPTION

The limiter amplifier has five stages of IF amplification using balanced differential limiter amplifiers with emitter follower coupling.
Decoupling of the stages from the supply voltage line and an internal high-ohmic DC feedback loop give a very stable IF performance. The amplifier gain is virtually independent of changes in temperature.
The FM demodulator is fully balanced and compromises two cross-coupled differential amplifiers. The quadrature detection of the FM signal is performed by direct feeding of one differential amplifier from the limiter amplifier output, and the other via an external 90 degrees phase shifting network. The demodulator has a good stability and a small zero-cross-over shift. The bandwidth on the demodulator output is restricted by an internal low-pass filter to approximately 1 MHz.

Non-linearities, which are introduced by demodulation, are compensated by the THD compensation circuit. For this reason, the demodulator resonance circuit (between pins 10 and 11) must have a loaded Q-factor of 19. Consequently, there is no need for the demodulator tuned circuit to be adjusted for minimum distortion. Adjustment criterion is a symmetrical stop pulse.
The control voltage for the mute attenuator (pin 16) is derived from the values of the level detector and the detuning detector output signals. The mute attenuator has a fast attack and a slow decay determined by the capacitor on pin 16. The AF signal is fed via the mute attenuator to the output (pin 4). A weighted control voltage (pin 6) is obtained from the mute attenuator control voltage via a buffer amplifier that introduces an additional voltage shift and gain.

The level detector generates a voltage output signal proportional to the amplitude of the input signal. The unweighted level detector output signal is available.
The open-collector tuning stop output voltages STOP-0 and STOP-1 (pins 15 and 14) are derived from the detuning and the input signal level. The pins 14 and 15 may be tied together, if only one tuning-stop output is required.

LIMITING VALUES (TDA1593T pinning)

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_P	supply voltage (pin 1)	−0.3	+13	V
V_{n1}	voltage at pins 2, 4, 5, 6, 10, 11 and 16	−0.3	+10	V
V_{n2}	voltage at pins 3, 8, 14, 15, 18, 19 and 20	−0.3	V_P	V
V_{13}	voltage on pin 13	–	6	V
$I_{14, 15}$	current at pins 14 and 15	–	2	mA
P_{tot}	total power dissipation	–	360	mW
T_{stg}	storage temperature	−55	+150	°C
T_{amb}	operating ambient temperature	−40	+85	°C
V_{ESD}	electrostatic handling; note 1			
	all pins except 5 and 7	–	±2000	V
	pin 5	–	+800	V
			−2000	V
	pin 7	–	+1000	V
			−2000	V

Note to the limiting values

1. Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient in free air	
	SOT102	80 K/W
	SOT163A	90 K/W

CHARACTERISTICS (TDA1593T pinning)

V_P = 8.5 V; T_{amb} = +25 °C; f_{IF} = 10.7 MHz; deviation ±22.5 kHz with f_m = 400 Hz; V_i = 10 mV RMS at pin 20; de-emphasis of 50 µs; tuned circuit at pins 10 and 11 aligned for symmetrical stop pulses; measurements taken in Fig.4 unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	positive supply voltage (pin 1)		7.5	8.5	12	V
I_P	supply current	I_2 = 0	–	20	26	mA
IF amplifier and demodulator						
Z_i	demodulator input impedance between pins 10 and 11		25	40	55	kΩ
C_i	demodulator input capacitance between pins 10 and 11		–	6	–	pF
AF output (pin 4)						
R_o	output resistance		–	400	–	Ω
V_4	DC output level	V_{iIF} ≤ 5 µV RMS on pin 20	2.75	3.1	3.45	V
RR_{1000}	power supply ripple rejection on pin 4	f = 1000 Hz; V_{ripple} = 50 mV RMS	33	36	–	dB
Tuning stop detector						
Δf	detuning frequency for STOP-0	on pin 15; Fig.9				
	for V_{15} ≥ 3.5 V		–	–	+14.0	kHz
	for V_{15} ≤ 0.3 V		+22.0	–	–	kHz
Δf	detuning frequency for STOP-1	on pin 14; Fig.8				
	for V_{14} ≥ 3.5 V		–	–	−14.0	kHz
	for V_{14} ≤ 0.3 V		−22.0	–	–	kHz
V_{20}	dependence on input voltage for STOP-0 and STOP-1 (RMS value)	Fig.7;				
		$V_{14, 15}$ ≥ 3.5 V	250	–	–	µV
		$V_{14, 15}$ ≤ 0.3 V	–	–	50	µV
$V_{14, 15}$	output voltage	$I_{14, 15}$ = 1 mA	–	–	0.3	V
Reference voltage source (pin 5)						
V_{REF}	reference output voltage	I_5 = −1 mA	3.3	3.7	4.1	V
R_5	output resistance	I_5 = −1 mA	–	40	80	Ω
TC	temperature coefficient		–	3.3	–	mV/VK
External muting						
V_{16}	muting voltage at I_2 = 0	V_{20} ≤ 5 µV RMS; Fig.10	1.45	1.75	2.05	V
		V_{20} = 1 mV RMS	3.0	3.45	3.9	V
S	steepness of control voltage (slope: 100 µV ≤ V_{20} ≤ 100 mV) 20 Δlog V_{20} = 20 dB (ΔV_{16} / Δlog V_{20})		–	0.85	–	V/dec

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Internal mute $\alpha = 20 \log (\Delta V_{4(FM\text{-}MUTE\text{-}OFF)} / \Delta V_{4(FM\text{-}MUTE\text{-}ON)})$						
α	mute voltage	$V_{16} \geq V_{REF}$	–	0	–	dB
		$V_{16} = 0.77V_{REF}$	1.5	–	4.5	dB
		$V_{16} = 0.55V_{REF}$	–	20	–	dB
I_{16}	current for capacitor (pin 16)					
	charge current	$V_{13} = 0$ V	–	–8	–	µA
	discharge current	$V_{13} = 0$ V	–	+120	–	µA
	charge current	$V_{13} = V_{REF}$	–	–100	–	µA
	discharge current	$V_{13} = V_{REF}$	–	+120	–	µA
Level detector						
R_6	output resistance		–	–	500	Ω
V_6	output voltage at $I_2 = 0$	$V_{20} \leq 5$ µV RMS; Fig.11	0.1	–	1.1	V
		$V_{20} = 1$ mV RMS	3.0	–	4.2	V
		±200 kHz detuning	1.2	1.5	1.8	V
ΔV_6	output voltage at detuning	±45 kHz detuning	–	–	0.2	V
TC	temperature coefficient		–	3.3	–	mV/VK
S	steepness of control voltage (slope: 50 µV ≤ V_{20} ≤ 50 mV) 20 Δlog V_{20} = 20 dB (ΔV_6 / Δlog V_{20})		1.4	1.7	2.0	V/dec
$\Delta V_6/\Delta f$	slope of output voltage at detuning	$\Delta f = 125 \pm 20$ kHz	–	35	–	mV/kHz
S	level shift adjustments					
	range by pin 2	$\pm\Delta V_6/V_{REF}$	0.42	0.5	–	V/V
	gain	$-\Delta V_6/\Delta V_2$	–	1.7	–	V/V
	range by pin 2	$\pm\Delta V_{16}/V_{REF}$	0.21	0.25	–	V/V
	gain	$-\Delta V_{16}/\Delta V_2$	–	0.85	–	V/V

OPERATING CHARACTERISTICS (TDA1593T pinning)

V_P = 7.5 to 12 V; T_{amb} = +25 °C; f_{IF} = 10.7 MHz; deviation ±22.5 kHz with f_m = 400 Hz; V_i = 10 mV RMS at pin 20; de-emphasis of 50 µs; tuned circuit at pins 10 and 11 aligned for symmetrical stop pulses; measurements taken in Fig.4 unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
IF amplifier and demodulator						
V_i	input signal for start of limiting (–3 dB) (RMS value; pin 20)	V_{16} = 4.5 V	14	22	35	µV
	input signal for signal-to-noise ratio (RMS value)	f = 250 to 15000 Hz				
	S/N = 26 dB	V_{16} = 4.5 V	–	15	–	µV
	S/N = 46 dB	V_{16} = 4.5 V	–	60	–	µV
S/N	signal-to-noise ratio	deviation ±75 kHz	–	82	–	dB
V_o	AF output signal (RMS value; pin 4)		180	200	220	mV
THD	total harmonic distortion	deviation ±75 kHz;				
	without de-emphasis	f_m = 1 kHz	–	0.2	0.6	%
	±25 kHz detuning		–	–	1.0	%
α_{AM}	AM suppression on pin 4	m = 30%; on pin 20				
	V_i = 0.3 to 1000 mV RMS		43	55	–	dB
	V_i = 1 to 300 mV RMS		57	65	–	dB
Tuning stop detector						
Δf	detuning frequency for STOP-0	on pin 15; Fig.9				
	for $V_{15} \geq 3.5$ V		–	–	+14.0	kHz
	for $V_{15} \leq 0.3$ V		+22.0	–	–	kHz
Δf	detuning frequency for STOP-1	on pin 14; Fig.8				
	for $V_{14} \geq 3.5$ V		–	–	–14.0	kHz
	for $V_{14} \leq 0.3$ V		–22.0	–	–	kHz
V_{20}	dependence on input voltage for STOP-0 and STOP-1 (RMS value)	Fig.7;				
		$V_{14, 15} \geq 3.5$ V	250	–	–	µV
		$V_{14, 15} \leq 0.3$ V	–	–	50	µV
R_8	internal low-pass resistance of detune detector		12	25	50	kΩ
V_8	voltage on capacitor	$V_i \leq 5$ µV RMS on input pin 20	–	2.2	–	V
Level detector (I_2 = 0)						
V_6	output voltage	$V_{20} \leq 5$ µV RMS	0.1	–	1.1	V
		V_{20} = 1 mV RMS	3.0	–	4.2	V
Reference voltage source (pin 5)						
V_{REF}	reference output voltage	I_5 = –1 mA	3.3	3.7	4.1	V

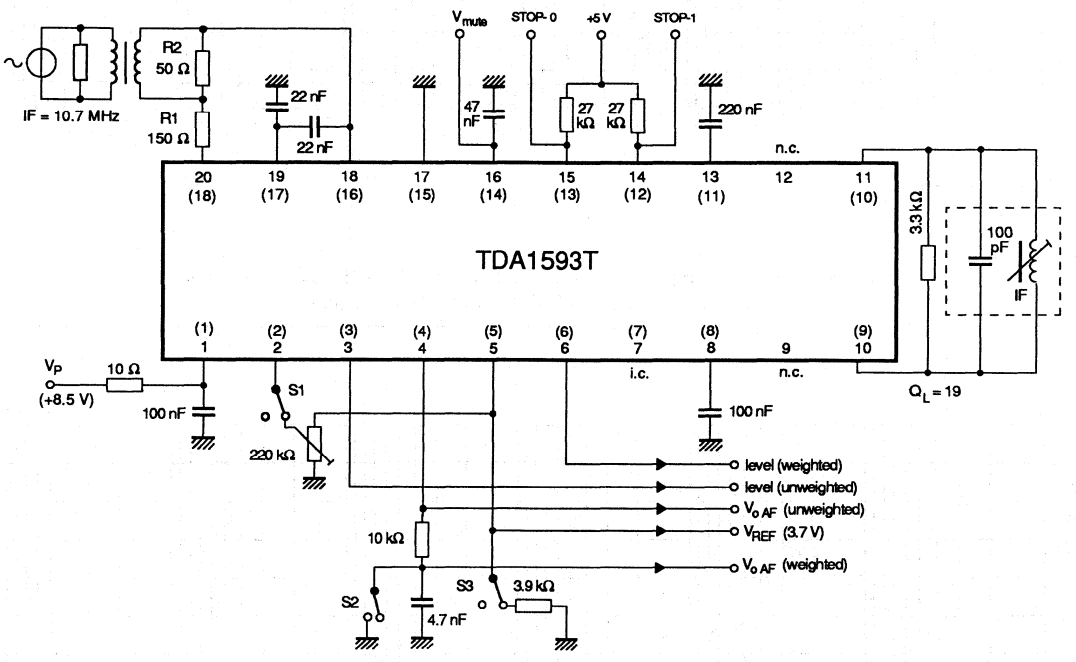
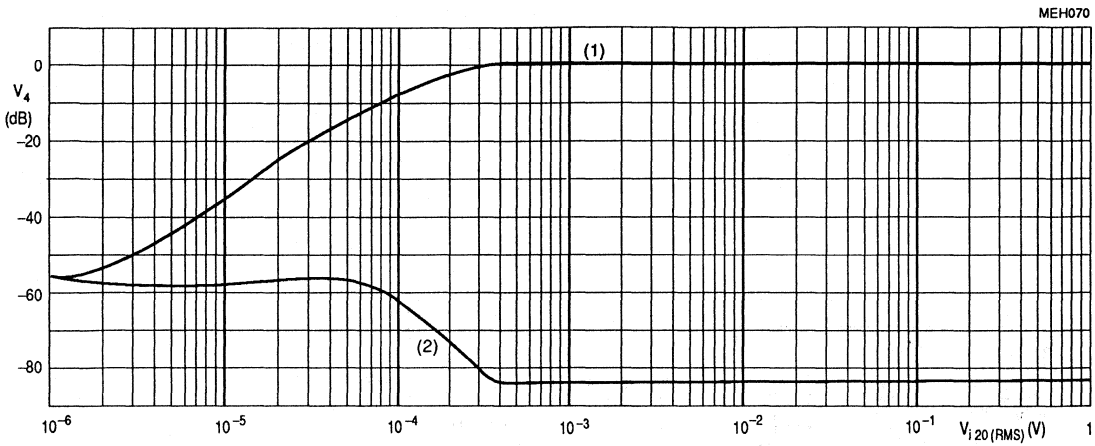
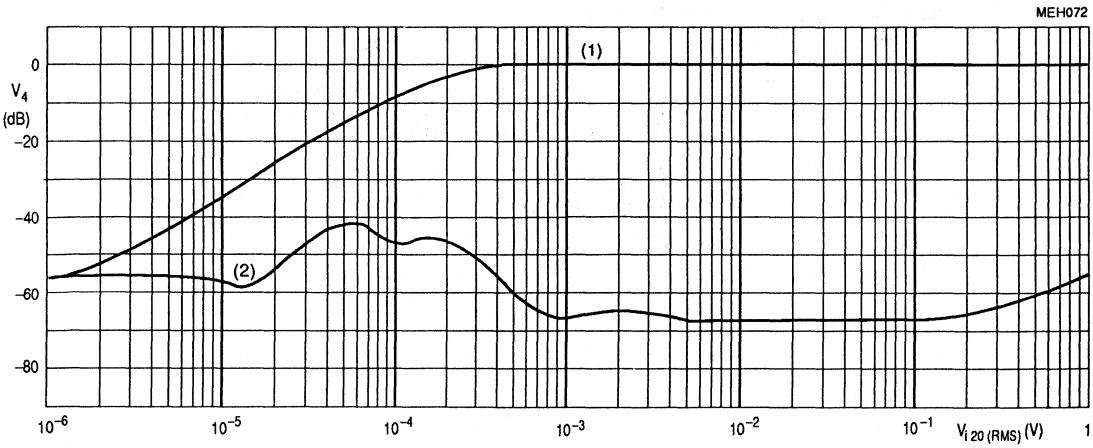


Fig.4 Test circuit (TDA1593 pinning in parenthesis).



(1) audio signal
(2) noise

Fig.5 Audio signal and noise as functions of the input signal V_{iIF} (pin 20) with $\Delta f = \pm 22.5$ kHz; $f_m = 1$ kHz; de-emphasis 50 µs.



(1) audio signal
(2) spurious AM signal

Fig.6 Typical AM suppression as a function of the input signal V_{iIF} (pin 20) with $\Delta f = \pm 22.5$ kHz; $f_m = 1$ kHz; AM with $f_m = 400$ Hz; m = 0.3 and 250 to 15000 Hz bandwidth.

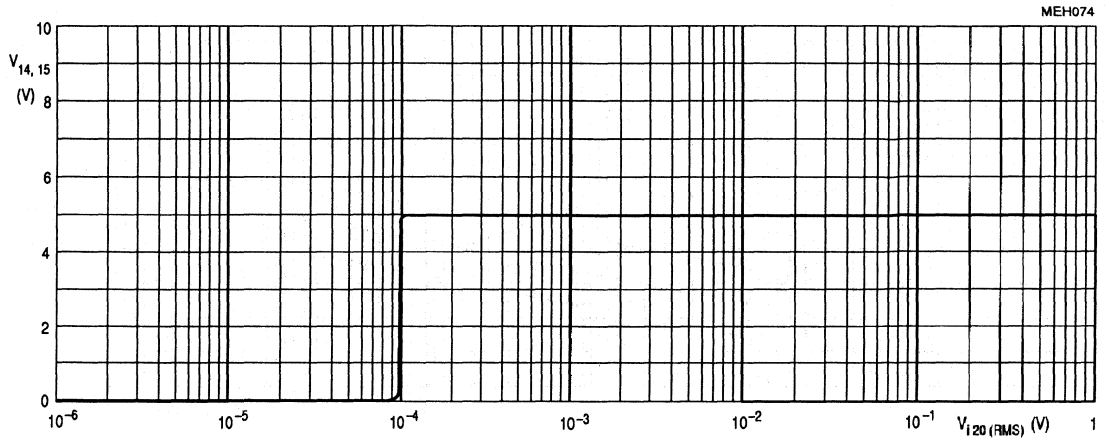


Fig.7 STOP-0 and STOP-1 output voltage dependent on input signal V_{iIF} (pin 20).

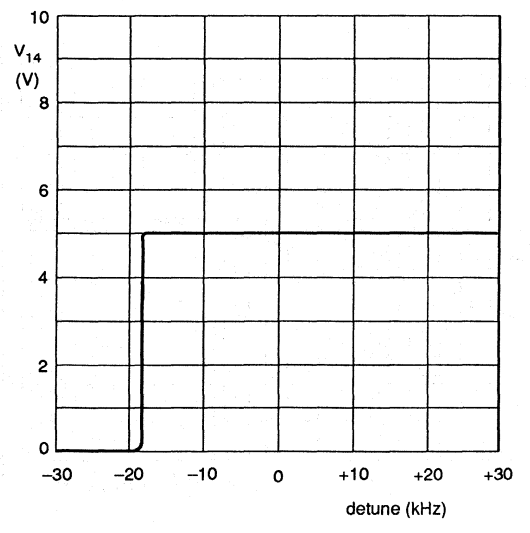


Fig.8 STOP-1 output voltage dependent on V_{iIF} = 10 mV RMS (pin 20).

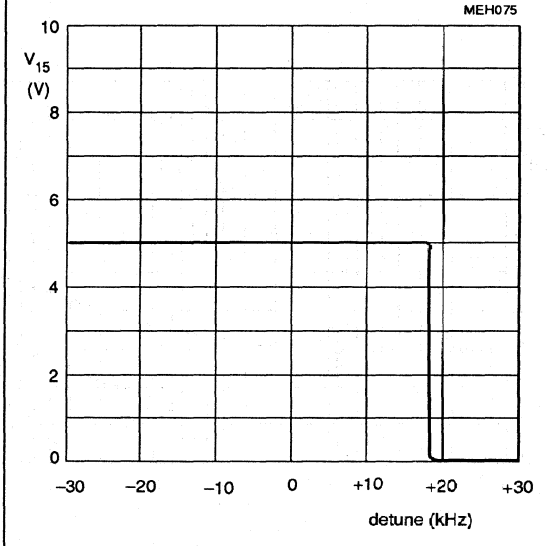


Fig.9 STOP-0 output voltage dependent on V_{iIF} = 10 mV RMS (pin 20).

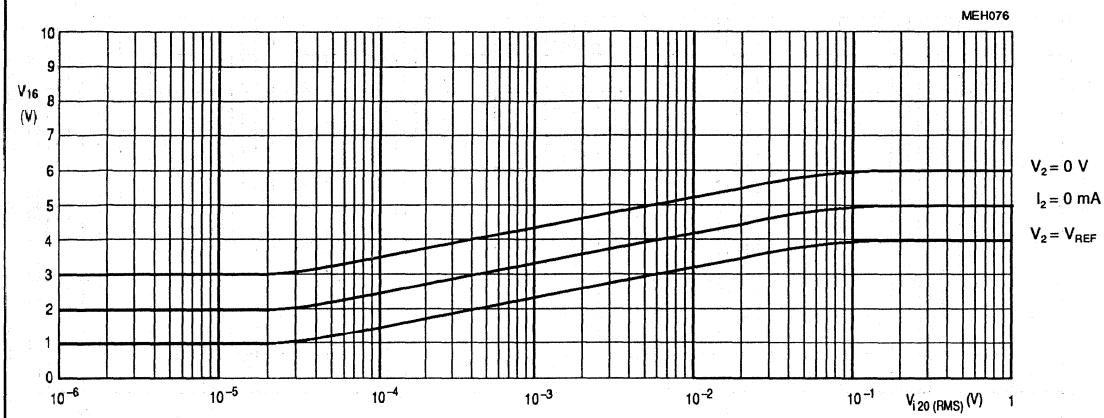


Fig.10 External mute voltage V_{16} dependent on input signal V_{iIF} (pin 20); typical adjusting range.

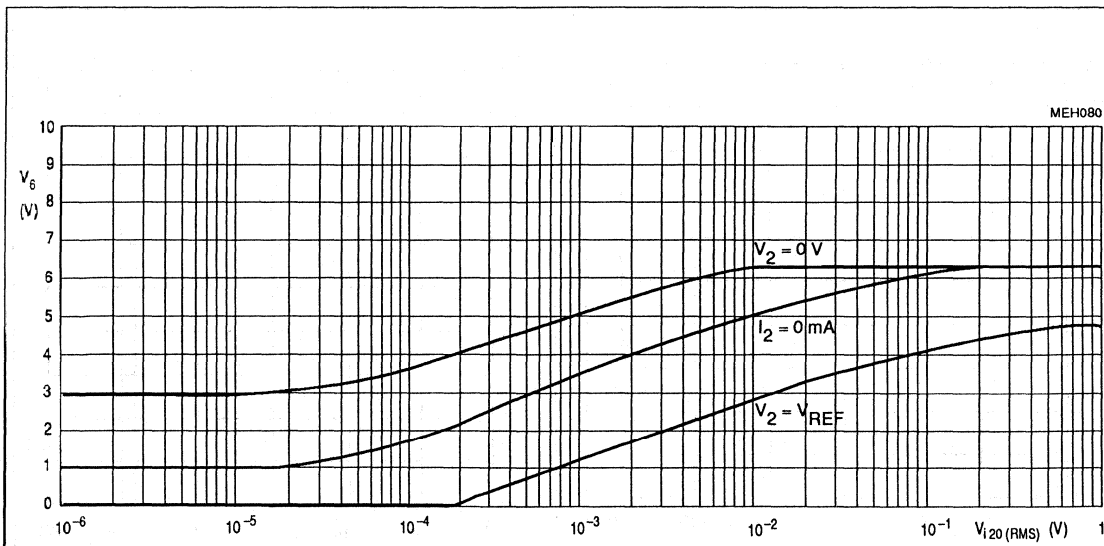


Fig.11 Control voltage V_6 dependent on input signal V_{iIF} (pin 20); typical adjusting range.

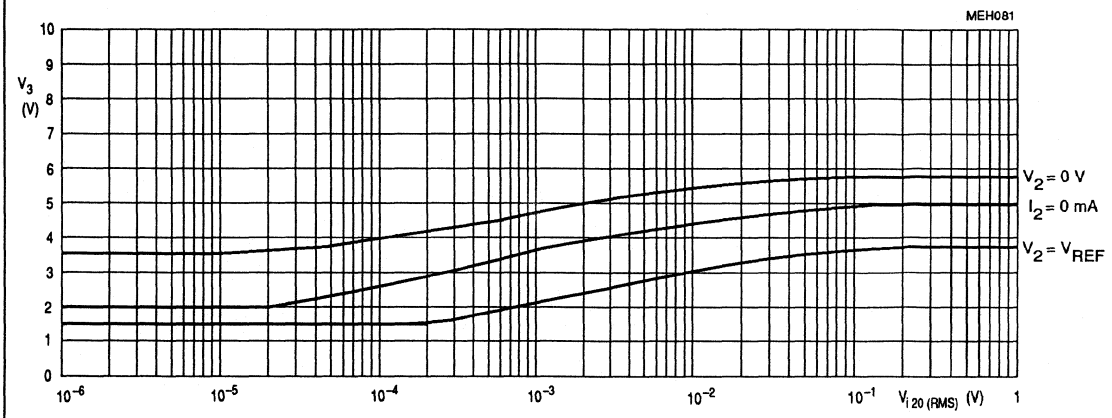


Fig.12 Level output voltage V_3 dependent on input signal V_{iIF} (pin 20); typical adjusting range.

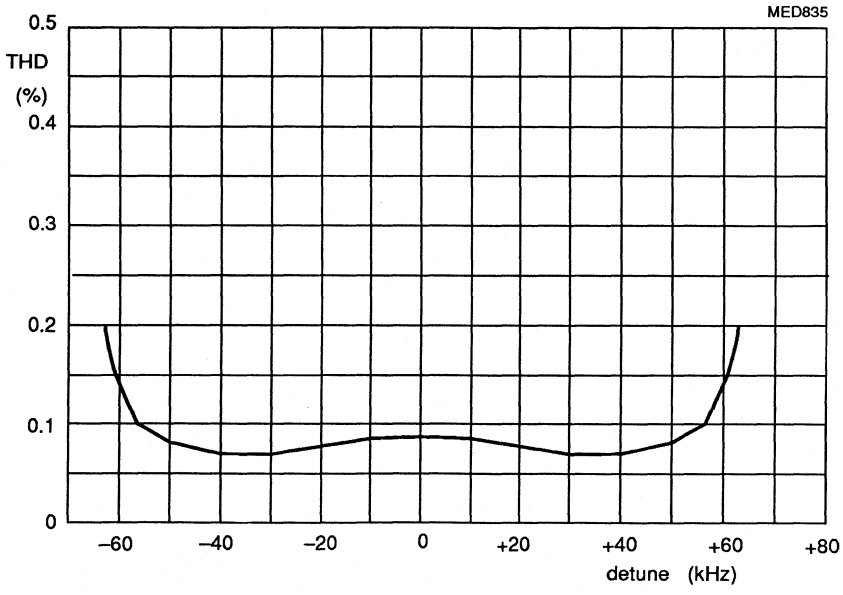


Fig.13 Total harmonic distortion dependent on detuning; deviation ±75 kHz; f_m = 1 kHz; V_{iIF} = 10 mV.

IF AMPLIFIER/DEMODULATOR FOR FM RADIO RECEIVERS

GENERAL DESCRIPTION

The TDA1596 provides IF amplification, symmetrical quadrature demodulation and level detection for quality home and car FM radio receivers and is suitable for both mono and stereo reception. It may also be applied to common front-ends, stereo decoders and AM receiver circuits.

Features

- Simulates behaviour of a ratio detector (internal field strength and detuning-dependent voltage for dynamic AF signal muting)
- Mono/stereo blend and field strength indication control voltage
- Three-state mode switch for FM, mute-on / FM, mute-off / FM-off
- Internal compensation of AF signal total harmonic distortion (THD)
- Two open collector stop pulse outputs for microcomputer tuning control (can be one stop pulse output by wired-ANDing)
- Internal reference voltage source
- Built-in hum and ripple rejection circuits

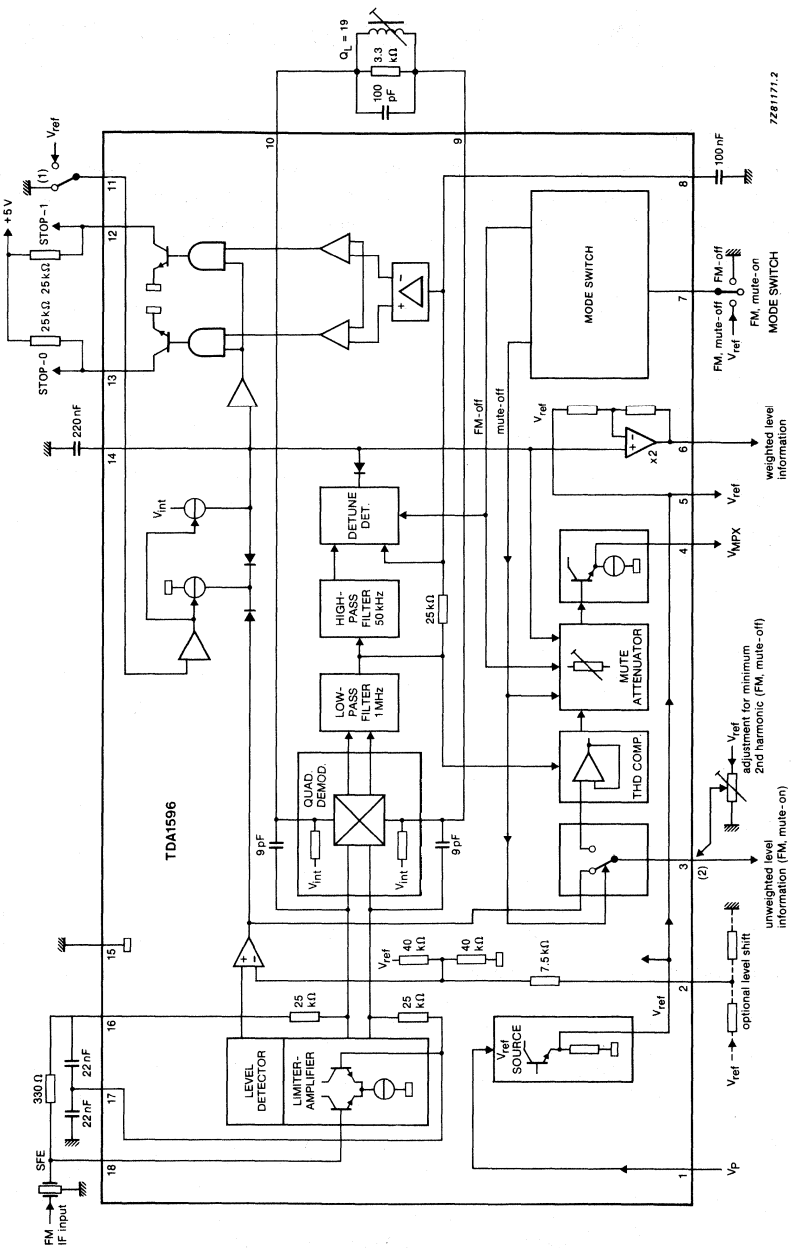
QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage (pin 1)		V_P	7.5	8.5	12.0	V
Supply current (pin 1)	V_P = 8.5 V; $I_2 = I_7$ = 0 mA	I_P	–	20	26	mA
AF output voltage (RMS value)	$V_{18(rms)}$ = 10 mV	$V_{4(rms)}$	180	200	220	mV
Signal-to-noise ratio	$V_{18(rms)}$ = 10 mV; f_m = 400 Hz; Δf = 75 kHz	S/N	–	82	–	dB
Total harmonic distortion	$V_{18(rms)}$ = 10 mV; f_m = 1 kHz; I_7 = 0 mA; Δf = 75 kHz; FM mute on; without de-emphasis; without detuning	THD	–	0.1	0.3	%
Operating ambient temperature range		T_{amb}	–40	–	+ 85	°C

SEE ALSO DATA SHEET FOR TDA1596T

PACKAGE OUTLINE

18-lead DIL; plastic (SOT102).



(1) Connecting pin 11 to ground is only allowed for measuring the current at pin 14. It is not for use in application.
(2) In the FM, mute-on condition the unweighted level detector output is available from pin 3. In the FM, mute-off condition the variable resistor at pin 3 can be adjusted for minimum 2nd harmonic distortion at pin 4.

Fig. 1 Block diagram and application circuit.

PINNING

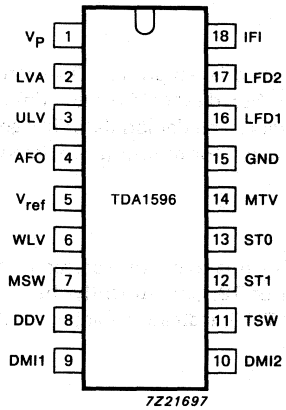


Fig. 2 Pinning diagram.

1	V_P	supply voltage
2	LVA	level voltage adjustment
3	ULV	unweighted level output/K2 adjustment
4	AF0	AF output
5	V_{ref}	reference voltage output
6	WLV	weighted level voltage output
7	MSW	mode switch
8	DDV	detune detector voltage
9	DMI1	demodulator input 1
10	DMI2	demodulator input 2
11	TSW	tau switch
12	ST1	stop pulse output 1
13	ST0	stop pulse output 0
14	MTV	mute voltage
15	GND	ground
16	LFD1	IF limiter feedback 1
17	LFD2	IF limiter feedback 2
18	IFI	IF input

FUNCTIONAL DESCRIPTION

Limiter-amplifier

This has five stages of IF amplification using balanced differential limiter-amplifiers with emitter-follower coupling. Decoupling of the stages from the voltage supply lines and an internal high-ohmic DC feed-back loop give a very stable IF performance. The amplifier gain is virtually independent from temperature changes.

FM demodulator

The demodulator is fully balanced and comprises two cross-coupled differential amplifiers. Quadrature detection of the FM signal is performed by feeding one differential amplifier directly from the limiter-amplifier output, and the other via an external 90° phase-shifting network. The demodulator has good stability and its zero cross-over shift is small. The bandwidth of the demodulator output is restricted to approximately 1 MHz by an internal low-pass filter.

THD compensation

This circuit compensates non-linearities introduced by demodulation. For this to operate correctly the demodulator circuit between pins 9 and 10 must have a loaded Q-factor of 19. Consequently there is no need for the demodulator tuned circuit to be adjusted for minimum THD, instead the adjustment criterium is for a symmetrical stop pulse.

Mute attenuator and AF output

The control voltage for the mute attenuator at pin 14 is generated from the values of the level detector and the detuning detector outputs. The mute attenuator has a fast attack and a slow decay which is determined by the capacitor at pin 14. The AF signal is passed via the mute attenuator to the output at pin 4.

A weighted control voltage, available from pin 6, is obtained from the mute attenuator control voltage via a buffer-amplifier which introduces an additional voltage shift and gain.

Level detector

The level detector generates a voltage output which is proportional to the field strength of the input signal. The unweighted level detector output is available when the mode switch is operating in the FM, mute-on condition.

Tuning-stop outputs

The open collector outputs STOP-0 and STOP-1 (from pins 13 and 12 respectively) are voltages derived from the detuning level and the field strength of the input signal. If only one tuning-stop output is required, pins 12 and 13 may be tied together.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage (pin 1)	$V_P = V_{1-15}$	−0.3	+ 16	V
Reference voltage range (pin 5)	V_{5-15}	−0.3	+ 10	V
Level adjustment range (pin 2)	V_{2-15}	−0.3	+ 10	V
Mode switch voltage range (pin 7)	V_{7-15}	−0.3	+ 16	V
Control input voltage range (pin 11)	V_{11-15}	−0.3	+ 6	V
THD compensation/unweighted field strength voltage range (pin 3)	V_{3-15}	−0.3	+ 16	V
Tuning-stop output voltage range				
STOP-0 (pin 13)	V_{13-15}	−0.3	+ 16	V
STOP-1 (pin 12)	V_{12-15}	−0.3	+ 16	V
Tuning-stop output current				
STOP-0 (pin 13)	I_{13}	−	2	mA
STOP-1 (pin 12)	I_{12}	−	2	mA
Storage temperature range	T_{stg}	−55	+ 150	°C
Operating ambient temperature range	T_{amb}	−40	+ 85	°C
Electrostatic handling*				
all pins except pins 5 and 6	V_{es}	−2000	+ 2000	V
pin 5	V_{es}	−2000	+ 900	V
pin 6	V_{es}	−2000	+ 1600	V

* Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

CHARACTERISTICS

$f = 10.7$ MHz; $V_P = V_{1-15} = 8.5$ V; $V_I = V_{18(rms)} = 1$ mV; $T_{amb} = 25$ °C; measured in the circuit of Fig. 3; tuned circuit at pins 9, 10 aligned for symmetrical stop pulses; all voltages are referred to ground (pin 15); unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supplies					
Supply voltage	$V_P = V_1$	7.5	8.5	12.0	V
Supply current at $I_2 = I_7 = 0$ mA	I_1	–	20	26	mA
FM demodulator					
Input impedance	R_{9-10}	25	40	55	kΩ
	C_{9-10}	–	6	–	pF
DC output voltage (no-signal condition) at $V_{9,\,10(p-p)} \leqslant 100\ \mu V$; $V_{18(rms)} \leqslant 5\ \mu V$	V_4	2.75	3.10	3.45	V
Output impedance	R_{4-15}	–	400	–	Ω
Mute attenuator control voltage					
Control voltage (pin 14)					
at $V_{18(rms)} \leqslant 5\ \mu V$	V_{14}	–	2.0	–	V
at $V_{18(rms)} = 1$ mV	V_{14}	–	3.45	–	V
Output impedance (pin 14)	R_{14-15}	–	–	2.0	MΩ
Level shift input (pin 2)					
internal bias voltage at $I_2 = 0$ mA	V_2	–	1.4	–	V
input impedance	R_{2-15}	15	–	–	kΩ
Internal muting (Fig. 4)					
Internal attenuation of signals ± 22.5 kHz ⩽ detuning ⩽ ± 80 kHz $A = 20\log[\Delta V_4(\text{FM mute-off})/\Delta V_4(\text{FM})]$					
at $V_{14} \geqslant 1\ V_5$	A	–	0	–	dB
at $V_{14} = 0.77\ V_5$	A	1.5	3.0	4.5	dB
at $V_{14} = 0.55\ V_5$	A	–	20	–	dB

parameter	symbol	min.	typ.	max.	unit
Attack and decay (pin 14)					
Pin 11 connected to ground *					
charge current	$+I_{14}$	–	8	–	μA
discharge current	$-I_{14}$	–	120	–	μA
Pin 11 connected to V_{ref}					
charge current	$+I_{14}$	–	100	–	μA
discharge current	$-I_{14}$	–	120	–	μA
Level detector					
Dependence of output voltage on temperature	$\frac{\Delta V_6}{V_6 \Delta T}$	–	3.3	–	mV/VK
Output impedance	R_6	–	–	500	Ω
Dependence of output voltage (pin 6) on input voltage (pin 18) (Fig. 5):					
$V_{18(rms)} \leqslant 5\ \mu V$; $I_2 = I_7 = 0$ mA	V_6	0.1	0.7	1.3	V
$V_{18(rms)} = 1$ mV; $I_2 = I_7 = 0$ mA	V_6	3.0	3.6	4.2	V
Slope of output voltage (pin 6) for input voltage range $V_{18(rms)} \geqslant 50\ \mu V$ to $V_{18(rms)} \leqslant 50$ mV	$\frac{\Delta V_6}{20 \Delta \log V_{18}}$	1.4	1.7	2.0	V/20 dB
Dependence of output voltage (pin 6) on detuning (Fig. 6) at input voltage $V_{18(rms)} = 10$ mV:					
detuning $\leqslant \pm 45$ kHz	ΔV_6	–	–	0.2	V
detuning = for $V_6 = 1.8$ V	$\pm \Delta f$	90	–	160	kHz
detuning = ± 200 kHz	V_6	0.5	0.7	0.9	V
Slope of output voltage with detuning = 125 ± 20 kHz at $V_{18(rms)} = 10$ mV	$\lvert \Delta V_6 / \Delta f \rvert$	–	35	–	mV/kHz
Level shift control (pin 2) (Fig. 7)					
adjustment range	$\pm \Delta V_6$	1.6	2.0	–	V
adjustment gain	$-(\Delta V_6 / \Delta V_2)$	–	1.7	–	V
output voltage at $V_2 = V_5$; $V_{18(rms)} \leqslant 5\ \mu V$	V_6	–	–	0.3	V
Low-pass filter at pin 8					
Output voltage at $I_7 = 0$ mA; $V_{18(rms)} \leqslant 5\ \mu V$	V_8	–	2.2	–	V
Internal resistance	$R_{8(int)}$	12	25	50	kΩ

* Connecting pin 11 to ground is only allowed for measuring the current at pin 14. It is not for use in application.

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Tuning-stop detector (Figs 8 and 9)					
Stop-0: detuning at $V_{18(rms)}$ = 10 mV					
for $V_{13} \geqslant 3.5$ V	$+\Delta f$	–	–	10	kHz
for $V_{13} \leqslant 0.3$ V	$+\Delta f$	18	–	–	kHz
Stop-1: detuning at $V_{18(rms)}$ = 10 mV					
for $V_{12} \geqslant 3.5$ V	$-\Delta f$	–	–	10	kHz
for $V_{12} \leqslant 0.3$ V	$-\Delta f$	18	–	–	kHz
Dependence of STOP-0, STOP-1 on input voltage (pin 18)					
input voltage (RMS value) for $V_{12} = V_{13} \geqslant 3.5$ V	$V_{18(rms)}$	250	–	–	μV
input voltage (RMS value) for $V_{12} = V_{13} \leqslant 0.3$ V	$V_{18(rms)}$	–	–	50	μV
Output voltage when $I_{12} = I_{13}$ = 1 mA	$V_{12, 13}$	–	–	0.3	V
Mode switch and pin 3 (Fig. 10)					
FM-off position					
Control voltage for 60 dB muting depth	V_7	–	–	1.4	V
FM, mute-on position (pin 3 = output)					
Internal bias voltage at $R_{7\text{-}15} \geqslant 10$ MΩ	V_7	–	2.8	–	V
Input current	$\lvert I_7 \rvert$	–	–	2.5	μA
Output voltage with $R_{3\text{-}15}$ = 10 kΩ; $C_{3\text{-}15} \geqslant 1$ nF*	V_3	–	2	–	V
Output impedance for $V_{18} = \leqslant 5\ \mu$V; I_3 = 500 μA	$R_{3\text{-}15}$	–	–	100	Ω
FM, mute-off position (pin 3 = input)					
Control voltage	V_7	0.9 V_5	–	–	V
Input current at $V_7 = V_5$	I_7	–	–	15	μA
Input resistance	$R_{3\text{-}15}$	1	–	–	MΩ
Reference voltage source					
Output voltage at $I_5 = -1$ mA	V_5	3.3	3.7	4.1	V
Output impedance at $I_5 = -1$ mA	$\Delta V_5/\Delta I_5$	–	40	80	Ω
Temperature coefficient	TC	–	3.3	–	mV/K

* Without input voltage.

OPERATING CHARACTERISTICS

f = 10.7 MHz; $V_{18(rms)}$ = 1 mV; deviation (Δf) = 22.5 kHz; modulation frequency (f_m) = 400 Hz; de-emphasis (pin 4) = 50 μs; test circuit as per Fig. 3; tuned circuit (Q_L = 19) aligned for symmetrical stop pulses; T_{amb} = + 25 °C; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
AF output voltage (RMS value) at $V_{18(rms)}$ = 10 mV	$V_{4(rms)}$	180	200	220	mV
Start of limiting (FM, mute-off); (RMS value) (Fig. 11)	$V_{18(rms)}$	14	22	35	μV
Dependence of signal-to-noise ratio (in noise frequency band 250 Hz to 15 kHz, unweighted) on input voltage					
for S/N = 26 dB	$V_{18(rms)}$	–	15	–	μV
for S/N = 46 dB	$V_{18(rms)}$	–	60	–	μV
at $V_{18(rms)}$ = 10 mV; Δf = 75 kHz	S/N	–	82	–	dB
THD (FM, mute-on) at $V_{18(rms)}$ = 10 mV; Δf = 75 kHz; f_m = 1 kHz; without detuning; without de-emphasis; I_7 = 0 mA	THD	–	0.1	0.3	%
Dynamic mute attenuation (Fig. 12) $\alpha_D = 20\log \frac{V_4 \text{ (FM mute-off)}}{V_4 \text{ (FM, mute-on)}}$ with f_m = 100 kHz; Δf = 75 kHz	α_D	–	16	–	dB
Slope of attenuation curve	$\alpha_D \Delta f$	–	0.8	–	dB/kHz
THD (FM, mute-on) at $V_{18(rms)}$ = 10 mV; Δf = 75 kHz; f_m = 1 kHz; detuning $\leqslant \pm$ 25 kHz without de-emphasis; I_7 = 0 mA (Fig. 13)	THD	–	–	0.6	%
THD (FM, mute-off and compensated via pin 3) at $V_{18(rms)}$ = 10 mV; Δf = 75 kHz; f_m = 1 kHz; $V_7 = V_5$	THD	–	0.07	0.25	%
Voltage range at pin 3 for THD compensation	V_3	0	–	V_5	V
AM suppression (FM, mute-off) with amplitude modulation at 30%; input voltage range V_{18} = 300 μV to 100 mV (Fig. 14)		–	65	–	dB
Power supply ripple rejection = $20\log [\Delta V_1/\Delta V_4]$		33	36	–	dB
Mute attenuation (FM-off) = $20\log [V_{4(FM\text{-}on)}/V_{4(FM\text{-}off)}]$		60	–	–	dB

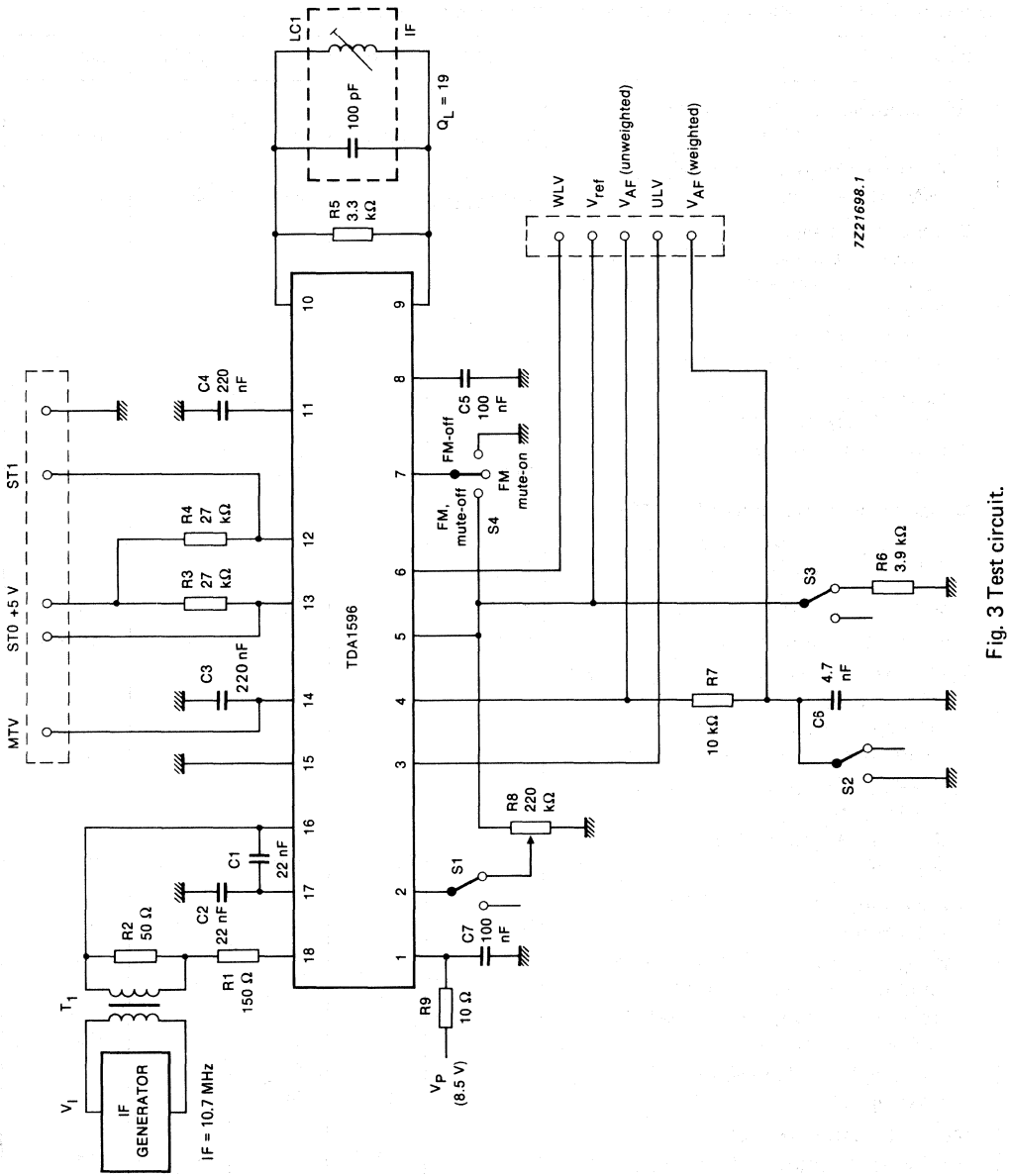


Fig. 3 Test circuit.

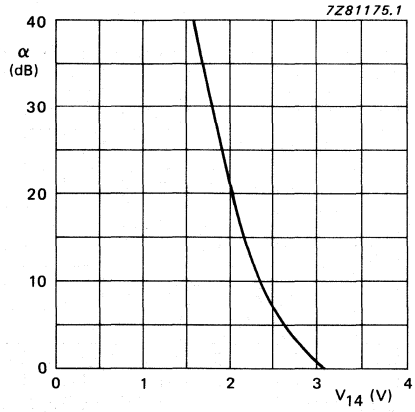


Fig. 4 Typical curve of internal attenuation showing the relationship between the mute attenuator control voltage (pin 14) and mute attenuation, $I_2 = I_7 = 0$ mA.

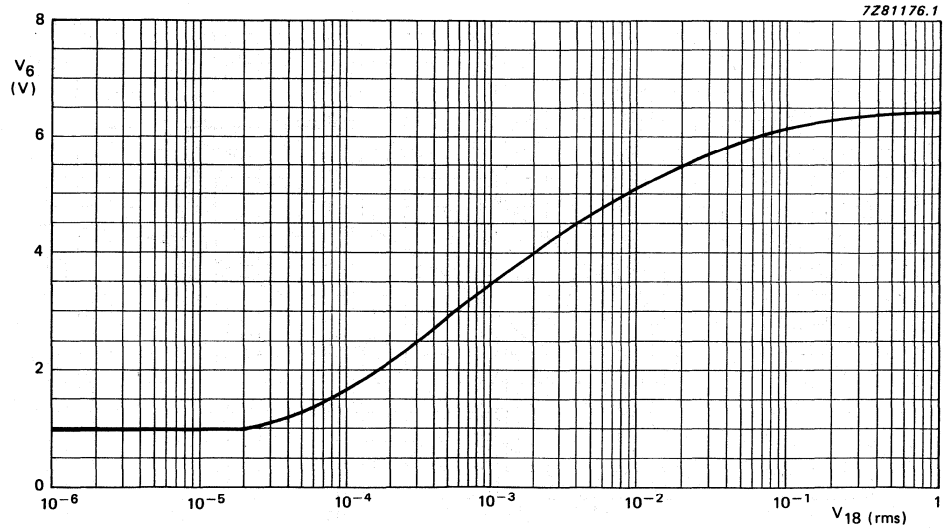


Fig. 5 Weighted field strength output voltage (pin 6) as a function of input voltage (pin 18); $R_{6\text{-}15} \geqslant 10$ kΩ; $I_2 = I_7 = 0$ mA.

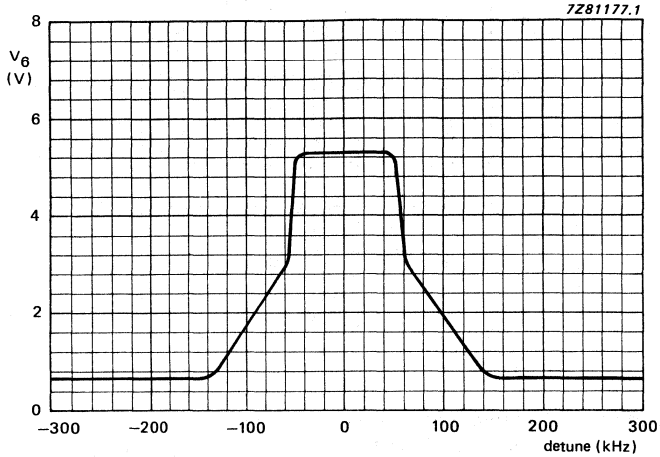


Fig. 6 Weighted field strength output voltage (pin 6) as a function of detuning; $R_{6\text{-}15} \geqslant 10$ kΩ; $I_2 = I_7 = 0$ mA; $V_{18} = 10$ mV.

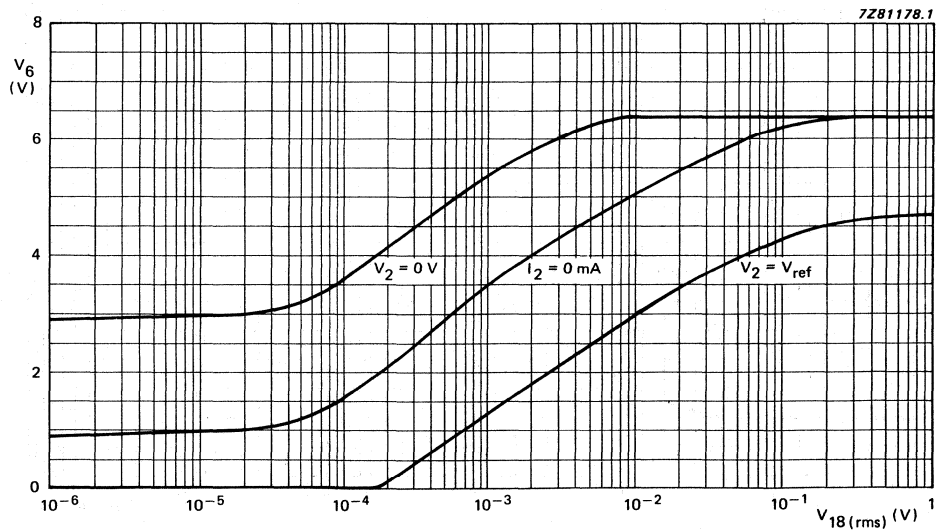
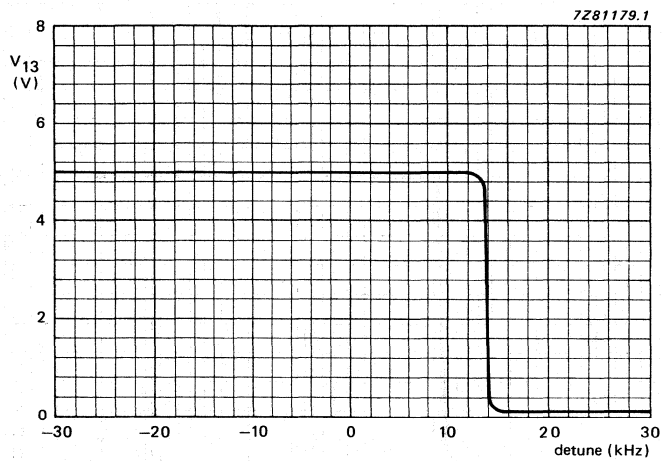
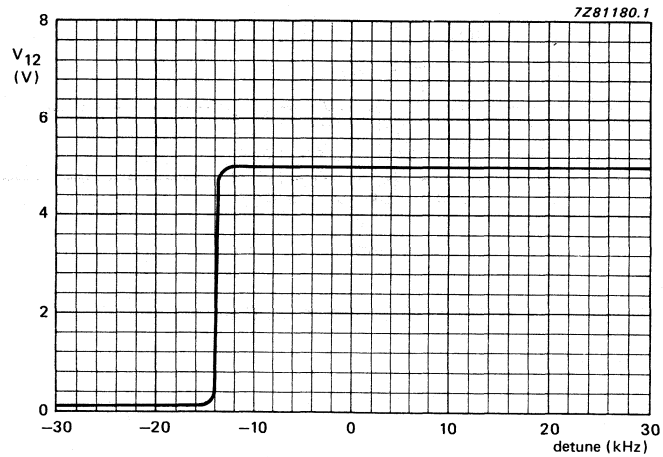


Fig. 7 Adjustment range of weighted field strength output voltage (pin 6) with level shift control (pin 2); $R_{6\text{-}15} \geqslant 10$ kΩ; $I_7 = 0$ mA.



(a) STOP-0.



(b) STOP-1

Fig. 8 STOP-0 and STOP-1 output voltages as a function of detuning, measured at V_{18} = 10 mV.

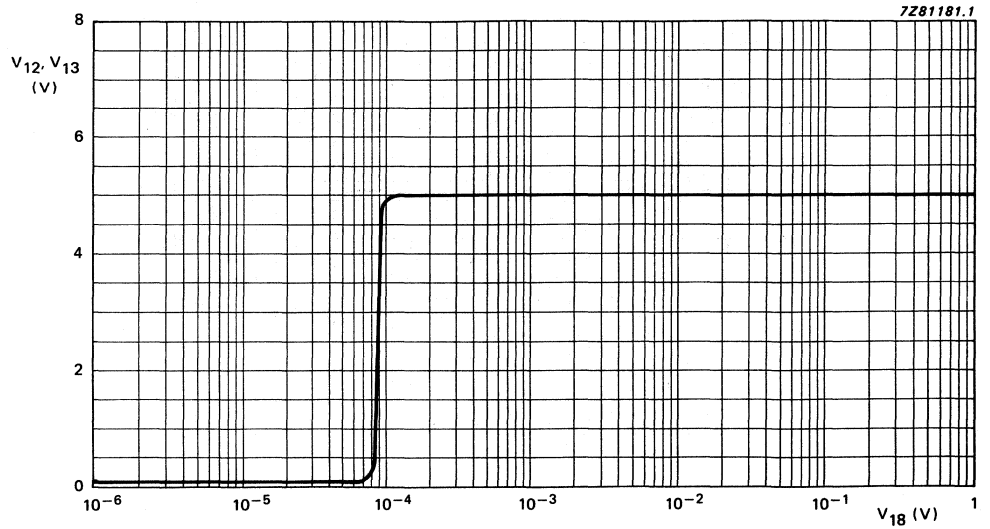


Fig. 9 STOP-0 or STOP-1 output voltages as a function of input voltage at pin 18.

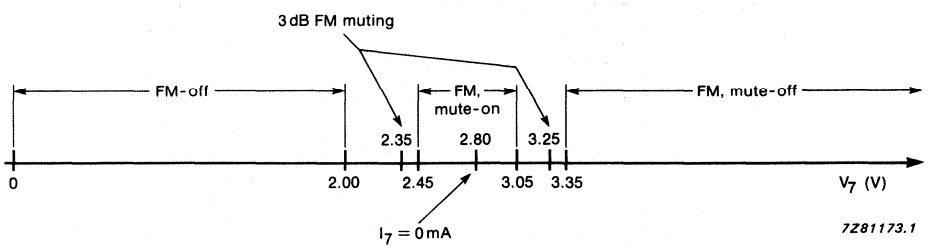
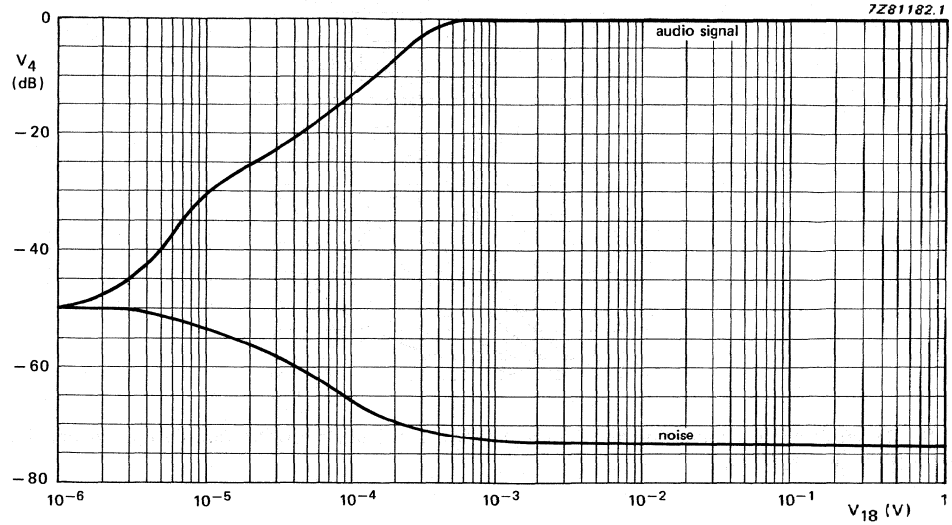
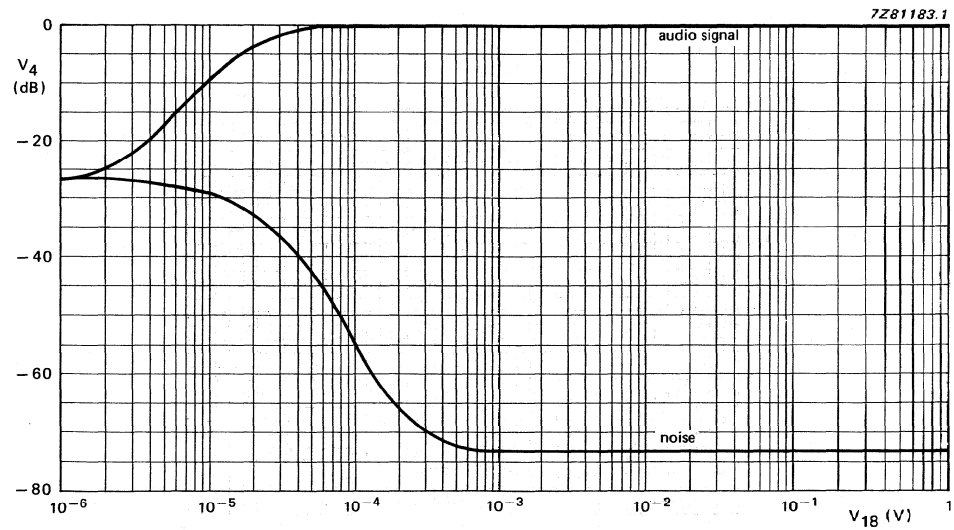


Fig. 10 Switch levels at pin 7.



(a) mode switch at FM, mute-on



(b) mode switch at FM, mute-off

Fig. 11 Audio signal (Δf = 22.5 kHz; f_m = 1 kHz) and noise as functions of input voltage at pin 18; measured with 50 μs de-emphasis.

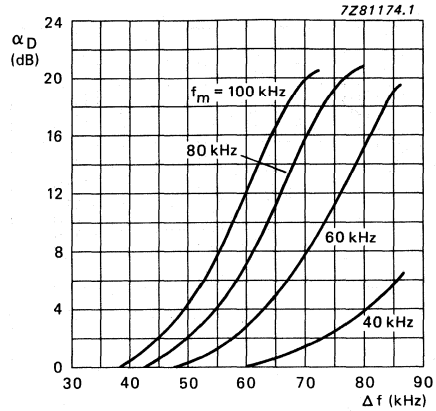


Fig. 12 Dynamic mute attenuation as a function of frequency deviation for modulation frequencies of 40, 60, 80 and 100 kHz.

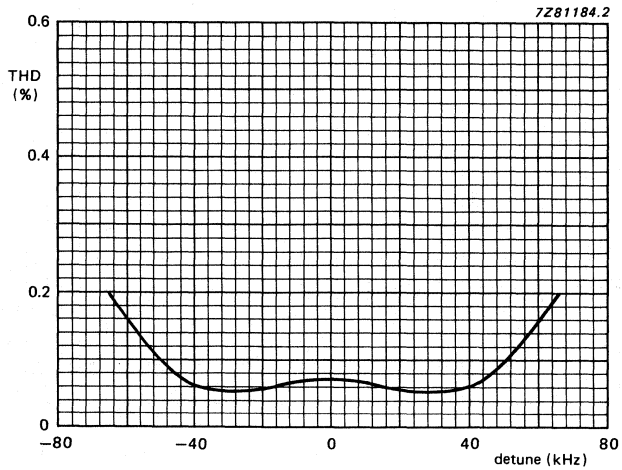
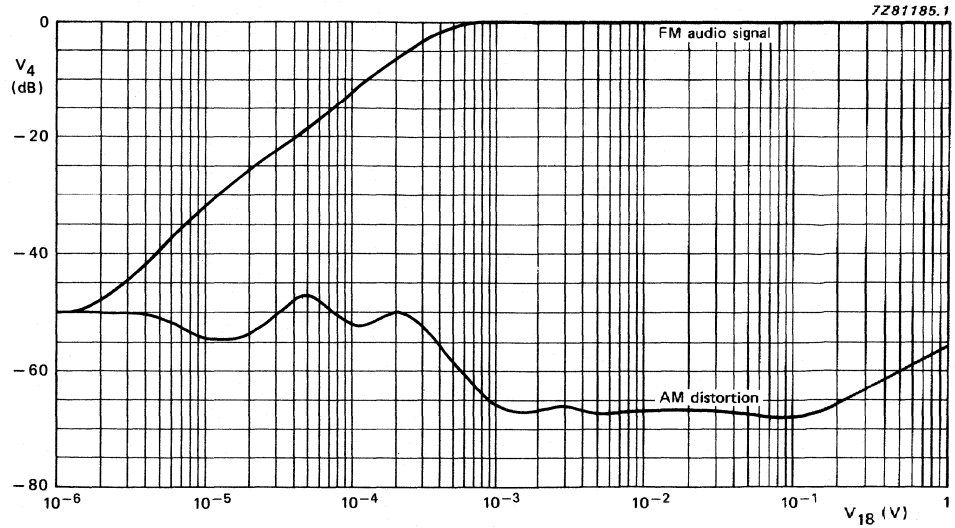
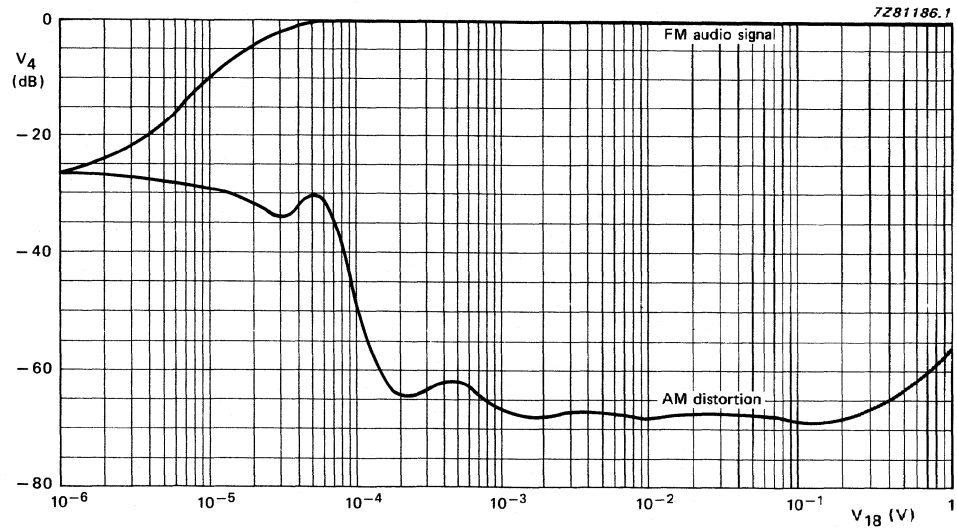


Fig. 13 THD as a function of detuning; mode switch at FM, mute-on position; Δf = 75 kHz; f_m = 1 kHz; $V_{18(rms)}$ = 10 mV.



(a) mode switch at FM, mute-on



(b) mode switch at FM, mute-off

Fig. 14 Typical curves showing AM suppression for an input signal having frequency modulation at Δf = 22.5 kHz and f_m = 1 kHz, and amplitude modulation of 30% at a frequency of 400 Hz; de-emphasis time = 50 μs and bandwidth = 250 Hz to 15 kHz.

IF AMPLIFIER/DEMODULATOR FOR FM RADIO RECEIVERS

GENERAL DESCRIPTION

The TDA1596T provides IF amplification, symmetrical quadrature demodulation and level detection for quality home and car FM radio receivers and is suitable for both mono and stereo reception. It may also be applied to common front-ends, stereo decoders and AM receiver circuits.

Features

- Simulates behaviour of a ratio detector (internal field strength and detuning-dependent voltage for dynamic AF signal muting)
- Mono/stereo blend and field strength indication control voltage
- Three-state mode switch for FM, mute-on / FM, mute-off / FM-off
- Internal compensation of AF signal total harmonic distortion (THD)
- Two open collector stop pulse outputs for microcomputer tuning control (can be one stop pulse output by wired-ANDing)
- Internal reference voltage source
- Built-in hum and ripple rejection circuits

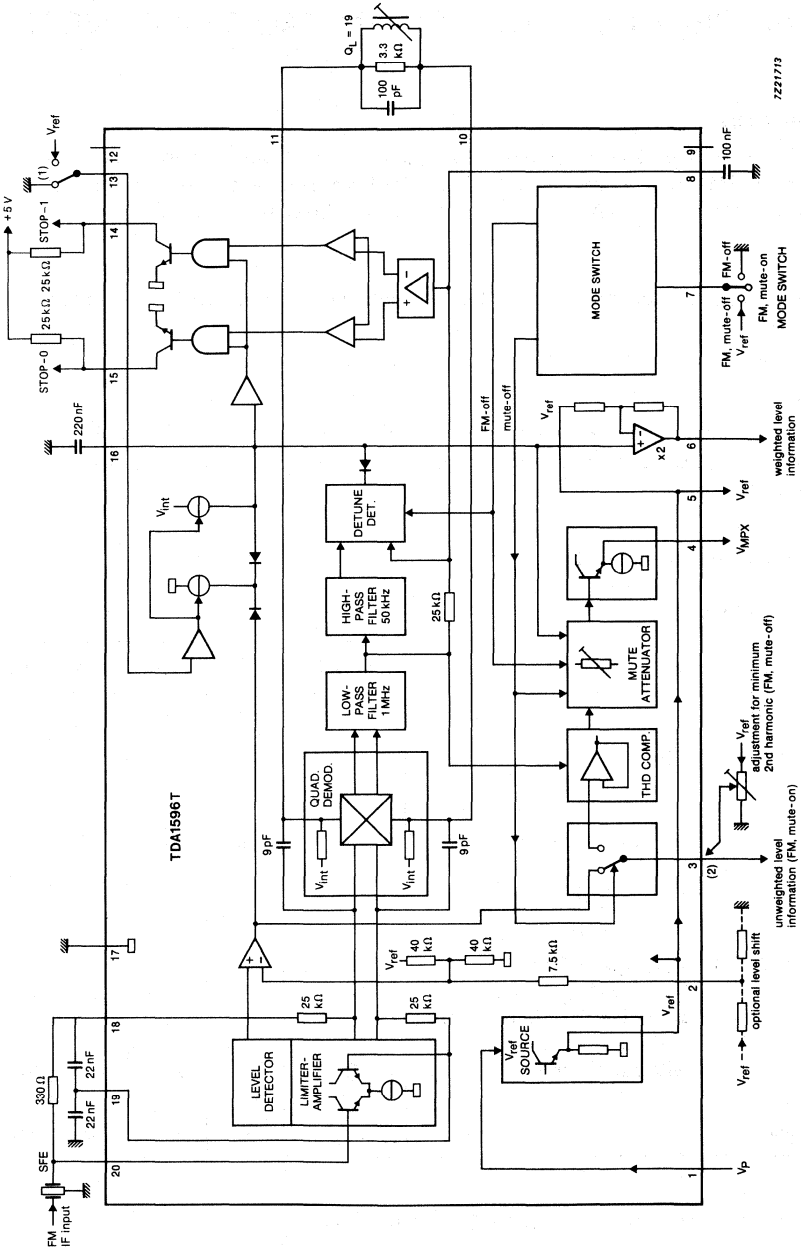
QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage (pin 1)		V_P	7.5	8.5	12.0	V
Supply current (pin 1)	V_P = 8.5 V; $I_2 = I_7$ = 0 mA	I_P	–	20	26	mA
AF output voltage (RMS value)	$V_{20(rms)}$ = 10 mV	$V_{4(rms)}$	180	200	220	mV
Signal-to-noise ratio	$V_{20(rms)}$ = 10 mV; f_m = 400 Hz; Δf = 75 kHz	S/N	–	82	–	dB
Total harmonic distortion	$V_{20(rms)}$ = 10 mV; f_m = 1 kHz; I_7 = 0 mA; Δf = 75 kHz; FM mute on; without de-emphasis; without detuning	THD	–	0.1	0.3	%
Operating ambient temperature range		T_{amb}	−40	–	+ 85	°C

SEE ALSO DATA SHEET FOR TDA1596

PACKAGE OUTLINE

20-lead mini-pack; plastic (SO20; SOT163A).



(1) Connecting pin 13 to ground is only allowed for measuring the current at pin 16. It is not for use in application.
(2) In the FM, mute-on condition the unweighted level detector output is available from pin 3. In the FM, mute-off condition the variable resistor at pin 3 can be adjusted for minimum 2nd harmonic distortion at pin 4.

Fig. 1 Block diagram and application circuit.

PINNING

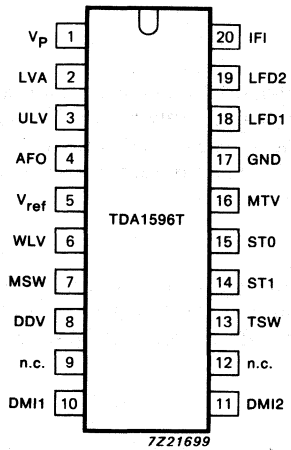


Fig. 2 Pinning diagram.

1	V_P	supply voltage
2	LVA	level voltage adjustment
3	ULV	unweighted level output/K2 adjustment
4	AF0	AF output
5	V_{ref}	reference voltage output
6	WLV	weighted level voltage output
7	MSW	mode switch
8	DDV	detune detector voltage
9	n.c.	not connected
10	DMI1	demodulator input 1
11	DMI2	demodulator input 2
12	n.c.	not connected
13	TSW	tau switch
14	ST1	stop pulse output 1
15	ST0	stop pulse output 0
16	MTV	mute voltage
17	GND	ground
18	LFD1	IF limiter feedback 1
19	LFD2	IF limiter feedback 2
20	IFI	IF input

FUNCTIONAL DESCRIPTION

Limiter-amplifier

This has five stages of IF amplification using balanced differential limiter-amplifiers with emitter-follower coupling. Decoupling of the stages from the voltage supply lines and an internal high-ohmic DC feed-back loop give a very stable IF performance. The amplifier gain is virtually independent from temperature changes.

FM demodulator

The demodulator is fully balanced and comprises two cross-coupled differential amplifiers. Quadrature detection of the FM signal is performed by feeding one differential amplifier directly from the limiter-amplifier output, and the other via an external 90° phase-shifting network. The demodulator has good stability and its zero cross-over shift is small. The bandwidth of the demodulator output is restricted to approximately 1 MHz by an internal low-pass filter.

THD compensation

This circuit compensates non-linearities introduced by demodulation. For this to operate correctly the demodulator circuit between pins 10 and 11 must have a loaded Q-factor of 19. Consequently there is no need for the demodulator tuned circuit to be adjusted for minimum THD, instead the adjustment criterium is for a symmetrical stop pulse.

Mute attenuator and AF output

The control voltage for the mute attenuator at pin 16 is generated from the values of the level detector and the detuning detector outputs. The mute attenuator has a fast attack and a slow decay which is determined by the capacitor at pin 16. The AF signal is passed via the mute attenuator to the output at pin 4.

A weighted control voltage, available from pin 6, is obtained from the mute attenuator control voltage via a buffer-amplifier which introduces an additional voltage shift and gain.

Level detector

The level detector generates a voltage output which is proportional to the field strength of the input signal. The unweighted level detector output is available when the mode switch is operating in the FM, mute-on condition.

Tuning-stop outputs

The open collector outputs STOP-0 and STOP-1 (from pins 15 and 14 respectively) are voltages derived from the detuning level and the field strength of the input signal. If only one tuning-stop output is required, pins 14 and 15 may be tied together.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage (pin 1)	$V_P = V_{1-17}$	−0.3	+16	V
Reference voltage range (pin 5)	V_{5-17}	−0.3	+10	V
Level adjustment range (pin 2)	V_{2-17}	−0.3	+10	V
Mode switch voltage range (pin 7)	V_{7-17}	−0.3	V_P	V
Control input voltage range (pin 13)	V_{13-17}	−	+6	V
THD compensation/unweighted field strength voltage range (pin 3)	V_{3-17}	−0.3	V_P	V
Tuning-stop output voltage range				
STOP-0 (pin 15)	V_{15-17}	−0.3	V_P	V
STOP-1 (pin 14)	V_{14-17}	−0.3	V_P	V
Tuning-stop output current				
STOP-0 (pin 15)	I_{15}	−	2	mA
STOP-1 (pin 14)	I_{14}	−	2	mA
Storage temperature range	T_{stg}	−55	+150	°C
Operating ambient temperature range	T_{amb}	−40	+85	°C
Electrostatic handling*				
all pins except pins 5 and 6	V_{es}	−2000	+2000	V
pin 5	V_{es}	−2000	+900	V
pin 6	V_{es}	−2000	+1600	V

THERMAL RESISTANCE

From junction to ambient (in free air) $R_{th\ j\text{-}a\ (max.)} = 95$ K/W

* Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

CHARACTERISTICS

f = 10.7 MHz; $V_P = V_{1-17} = 8.5$ V; $V_I = V_{20(rms)} = 1$ mV; $T_{amb} = 25\ ^oC$; measured in the circuit of Fig. 3; tuned circuit at pins 10, 11 aligned for symmetrical stop pulses; all voltages are referred to ground (pin 17), unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supplies					
Supply voltage	$V_P = V_1$	7.5	8.5	12.0	V
Supply current at $I_2 = I_7 = 0$ mA	I_1	–	20	26	mA
FM demodulator					
Input impedance	R_{10-11}	25	40	55	kΩ
	C_{10-11}	–	6	–	pF
DC output voltage (no-signal condition) at $V_{10, 11(p-p)} \leqslant 100\ \mu V$; $V_{20(rms)} \leqslant 5\ \mu V$	V_4	2.75	3.10	3.45	V
Output impedance	R_{4-17}	–	400	–	Ω
Mute attenuator control voltage					
Control voltage (pin 16)					
at $V_{20(rms)} \leqslant 5\ \mu V$	V_{16}	–	2.0	–	V
at $V_{20(rms)} = 1$ mV	V_{16}	–	3.45	–	V
Output impedance (pin 16)	R_{10-17}	–	–	2.0	MΩ
Level shift input (pin 2)					
internal bias voltage at $I_2 = 0$ mA	V_2	–	1.4	–	V
input impedance	R_{2-17}	15	–	–	kΩ
Internal muting (Fig. 6)					
Internal attenuation of signals ± 22.5 kHz ⩽ detuning ⩽ ± 80 kHz $A = 20\log[\Delta V_4(\text{FM mute-off})/\Delta V_4(\text{FM})]$					
at $V_{16} \geqslant 1\ V_5$	A	–	0	–	dB
at $V_{16} = 0.77\ V_5$	A	1.5	3.0	4.5	dB
at $V_{16} = 0.55\ V_5$	A	–	20	–	dB

parameter	symbol	min.	typ.	max.	unit
Attack and decay (pin 16)					
Pin 13 connected to ground *					
charge current	$+I_{16}$	–	8	–	μA
discharge current	$-I_{16}$	–	120	–	μA
Pin 13 connected to V_{ref}					
charge current	$+I_{16}$	–	100	–	μA
discharge current	$-I_{16}$	–	120	–	μA
Level detector					
Dependence of output voltage on temperature	$\frac{\Delta V_6}{V_6 \Delta T}$	–	3.3	–	mV/VK
Output impedance	R_6	–	–	500	Ω
Dependence of output voltage (pin 6) on input voltage (pin 20) (Fig. 7):					
$V_{20(rms)} \leqslant 5$ μV; $I_2 = I_7 = 0$ mA	V_6	0.1	0.7	1.3	V
$V_{20(rms)} = 1$ mV; $I_2 = I_7 = 0$ mA	V_6	3.0	3.6	4.2	V
Slope of output voltage (pin 6) for input voltage range					
$V_{20(rms)} \geqslant 50$ μV to $V_{20(rms)} \leqslant 50$ mV	$\frac{\Delta V_6}{20 \Delta \log V_{20}}$	1.4	1.7	2.0	V/20 dB
Dependence of output voltage (pin 6) on detuning (Fig. 8) at input voltage $V_{20(rms)} = 10$ mV:					
detuning $\leqslant \pm 45$ kHz	ΔV_6	–	–	0.2	V
detuning for $V_6 = 1.8$ V	$\pm \Delta f$	90	–	160	kHz
detuning = ±200 kHz	V_6	0.5	0.7	0.9	V
Slope of output voltage with detuning = 125 ± 20 kHz at $V_{20(rms)} = 10$ mV	$\lvert \Delta V_6 / \Delta f \rvert$	–	35	–	mV/kHz
Level shift control (pin 2) (Fig. 9)					
adjustment range	$\pm \Delta V_6$	1.6	2.0	–	V
adjustment gain	$-(\Delta V_6 / \Delta V_2)$	–	1.7	–	V
output voltage at $V_2 = V_5$; $V_{20(rms)} \leqslant 5$ μV	V_6	–	–	0.3	V
Low-pass filter at pin 8					
Output voltage at $I_7 = 0$ mA; $V_{20(rms)} \leqslant 5$ μV	V_8	–	2.2	–	V
Internal resistance	$R_{8(int)}$	12	25	50	kΩ

* Connecting pin 13 to ground is only allowed for measuring the current at pin 16. It is not for use in application.

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Tuning-stop detector (Figs 10 and 11)					
Stop-0: detuning at $V_{20(rms)}$ = 10 mV					
for $V_{15} \geqslant 3.5$ V	$+\Delta f$	–	–	10	kHz
for $V_{15} \leqslant 0.3$ V	$+\Delta f$	18	–	–	kHz
Stop-1: detuning at $V_{20(rms)}$ = 10 mV					
for $V_{14} \geqslant 3.5$ V	$-\Delta f$	–	–	10	kHz
for $V_{14} \leqslant 0.3$ V	$-\Delta f$	18	–	–	kHz
Dependence of STOP-0, STOP-1 on input voltage (pin 20)					
input voltage (RMS value) for $V_{14} = V_{15} \geqslant 3.5$ V	$V_{20(rms)}$	250	–	–	μV
input voltage (RMS value) for $V_{14} = V_{15} \leqslant 0.3$ V	$V_{20(rms)}$	–	–	50	μV
Output voltage when $I_{14} = I_{15}$ = 1 mA	$V_{14, 15}$	–	–	0.3	V
Mode switch and pin 3 (Fig. 12)					
FM-off position					
Control voltage for 60 dB muting depth	V_7	–	–	1.4	V
FM, mute-on position (pin 3 = output)					
Internal bias voltage at $R_{7-17} \geqslant 10$ MΩ	V_7	–	2.8	–	V
Input current	$\|I_7\|$	–	–	2.5	μA
Output voltage with R_{3-17} = 10 kΩ; $C_{3-17} \geqslant 1$ nF*	V_3	–	2	–	V
Output impedance for $V_{20} = \leqslant 5$ μV; I_3 = 500 μA	R_{3-17}	–	–	100	Ω
FM, mute-off position (pin 3 = input)					
Control voltage	V_7	0.9 V_5	–	–	V
Input current at $V_7 = V_5$	I_7	–	–	15	μA
Input resistance	R_{3-17}	1	–	–	MΩ
Reference voltage source					
Output voltage at $I_5 = -1$ mA	V_5	3.3	3.7	4.1	V
Output impedance at $I_5 = -1$ mA	$\Delta V_5/\Delta I_5$	–	40	80	Ω
Temperature coefficient	TC	–	3.3	–	mV/K

* Without input voltage.

OPERATING CHARACTERISTICS

f = 10.7 MHz; $V_I = V_{20(rms)}$ = 1 mV; deviation (Δf) = 22.5 kHz; modulation frequency (f_m) = 400 Hz; de-emphasis (pin 4) = 50 μs; test circuit as per Fig. 3; tuned circuit (Q_L = 19) aligned for symmetrical stop pulses; T_{amb} = + 25 °C; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
AF output voltage (RMS value) at $V_{20(rms)}$ = 10 mV	$V_{4(rms)}$	180	200	220	mV
Start of limiting (FM, mute-off); (RMS value) (Fig. 13)	$V_{20(rms)}$	14	22	35	μV
Dependence of signal-to-noise ratio (in noise frequency band 250 Hz to 15 kHz, unweighted) on input voltage					
for S/N = 26 dB	$V_{18(rms)}$	–	15	–	μV
for S/N = 46 dB	$V_{18(rms)}$	–	60	–	μV
at $V_{20(rms)}$ = 10 mV; Δf = 75 kHz	S/N	–	82	–	dB
THD (FM, mute-on) at $V_{20(rms)}$ = 10 mV; Δf = 75 kHz; f_m = 1 kHz; without detuning; without de-emphasis; I_7 = 0 mA	THD	–	0.1	0.3	%
Dynamic mute attenuation (Fig. 14) $\alpha_D = 20\log \frac{V_4 \text{ (FM mute-off)}}{V_4 \text{ (FM, mute-on)}}$ with f_m = 100 kHz; Δf = 75 kHz	α_D	–	16	–	dB
Slope of attenuation curve	$\alpha_D \Delta f$	–	0.8	–	dB/kHz
THD (FM, mute-on) at $V_{20(rms)}$ = 10 mV; Δf = 75 kHz; f_m = 1 kHz; detuning ⩽ ± 25 kHz without de-emphasis; I_7 = 0 mA (Fig. 15)	THD	–	–	0.6	%
THD (FM, mute-off and compensated via pin 3) at $V_{20(rms)}$ = 10 mV; Δf = 75 kHz; f_m = 1 kHz; $V_7 = V_5$	THD	–	0.07	0.25	%
Voltage range at pin 3 for THD compensation	V_3	0	–	V_5	V
AM suppression (FM, mute-off) with amplitude modulation at 30%; input voltage range V_{20} = 300 μV to 100 mV (Fig. 16)		–	65	–	dB
Power supply ripple rejection = 20log [$\Delta V_1/\Delta V_4$]		33	36	–	dB
Mute attenuation (FM-off) = 20log [$V_{4(FM\text{-}on}/V_{4(FM\text{-}off)}$]		60	–	–	dB

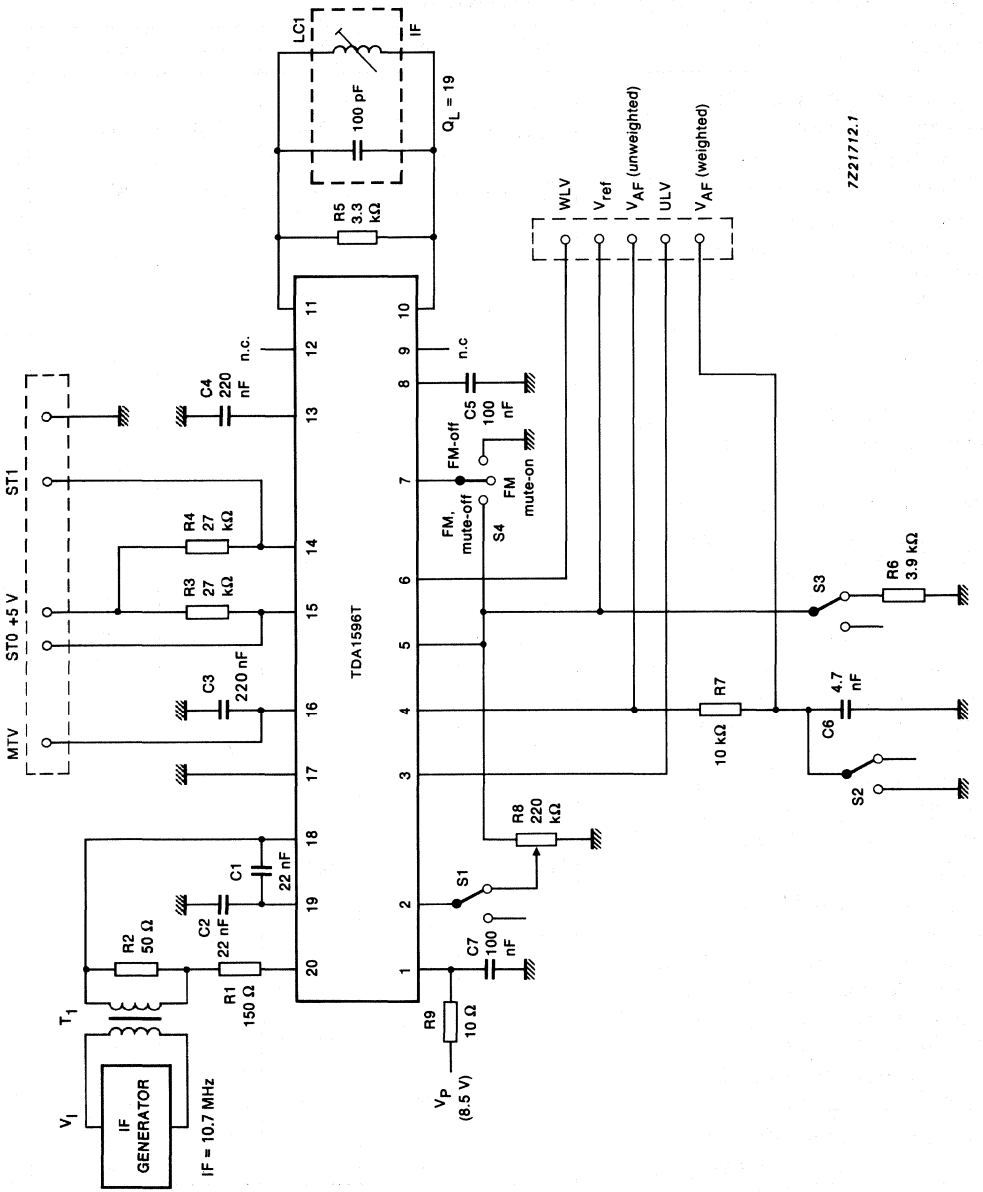


Fig. 3 Test circuit.

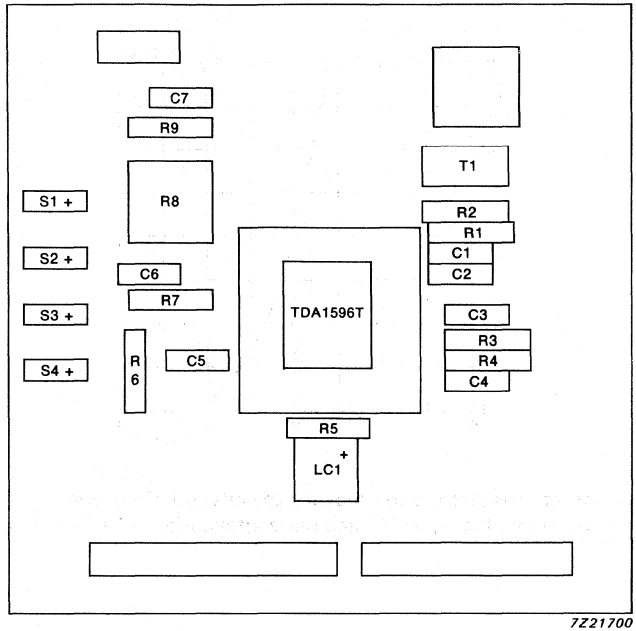


Fig. 4 Printed-circuit board component side, showing component layout. For circuit diagram see Fig. 3.

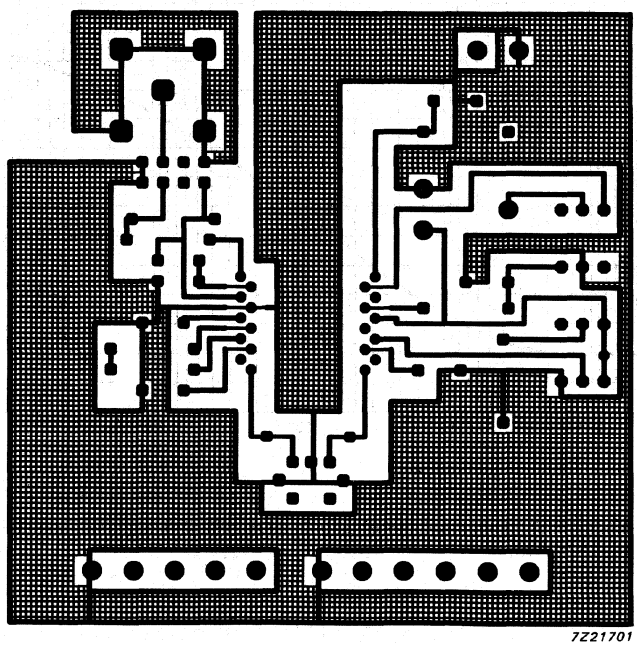


Fig. 5 Printed-circuit board showing track side.

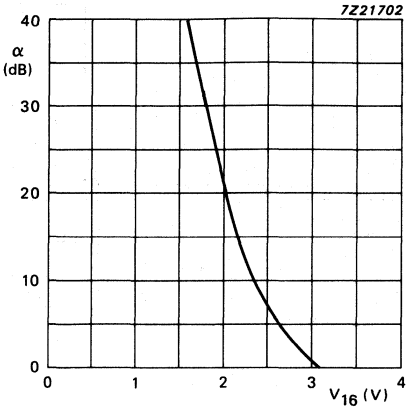


Fig. 6 Typical curve of internal attenuation showing the relationship between the mute attenuator control voltage (pin 16) and mute attenuation; $I_2 = I_7 = 0$ mA.

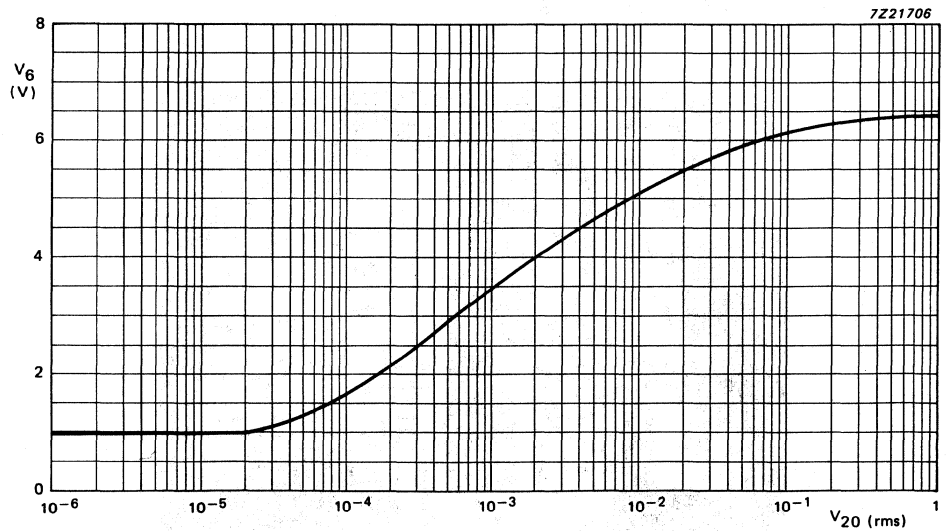


Fig. 7 Weighted field strength output voltage (pin 6) as a function of input voltage (pin 20); $R_{6\text{-}17} \geqslant 10$ kΩ; $I_2 = I_7 = 0$ mA.

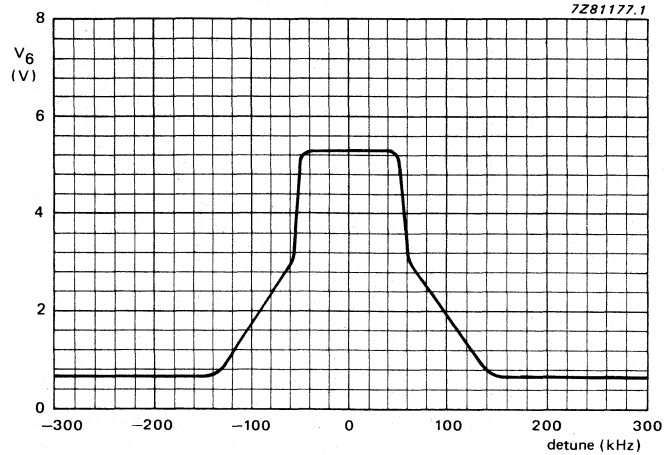


Fig. 8 Weighted field strength output voltage (pin 6) as a function of detuning; $R_{6\text{-}17} \geqslant 10\ k\Omega$; $I_2 = I_7 = 0\ mA$; $V_{20} = 10\ mV$.

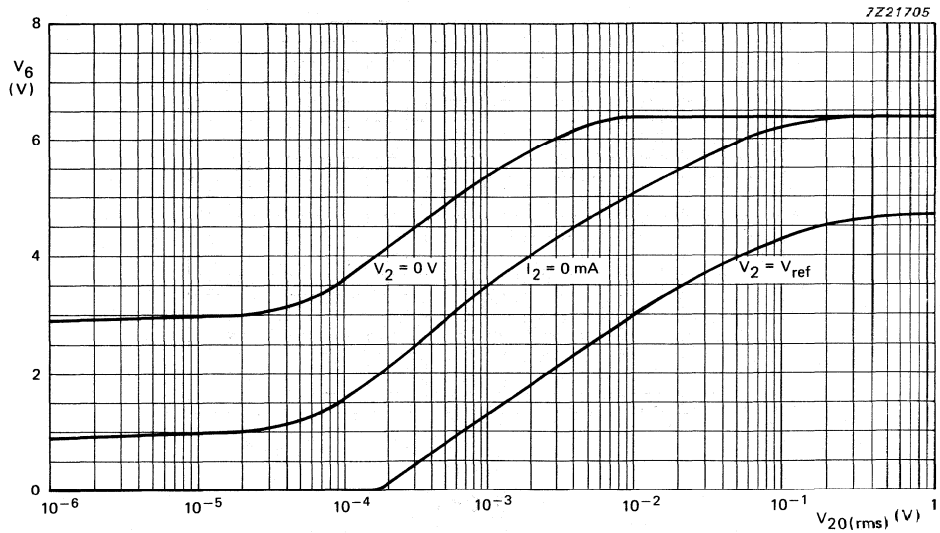
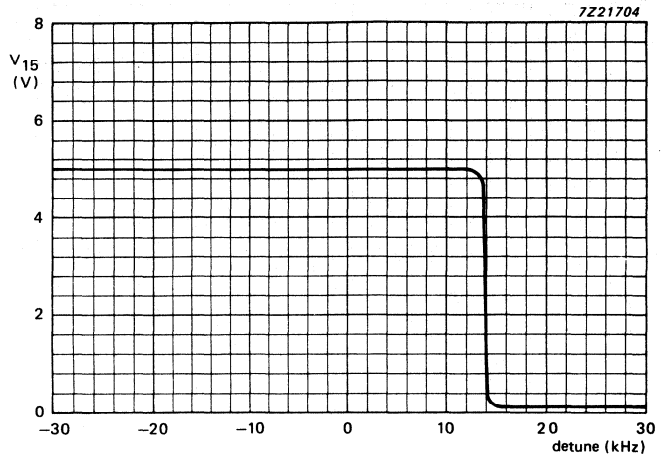
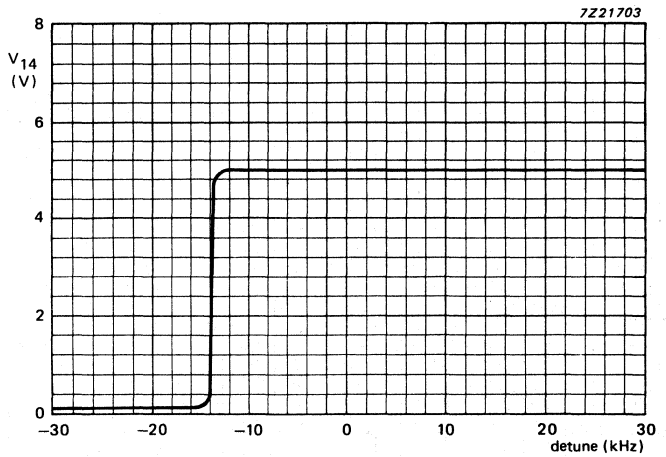


Fig. 9 Adjustment range of weighted field strength output voltage (pin 6) with level shift control (pin 2); $R_{6\text{-}17} \geqslant 10\ k\Omega$; $I_7 = 0\ mA$.



(a) STOP-0.



(b) STOP-1.

Fig. 10 STOP-0 and STOP-1 output voltages as a function of detuning, measured at V_{20} = 10 mV.

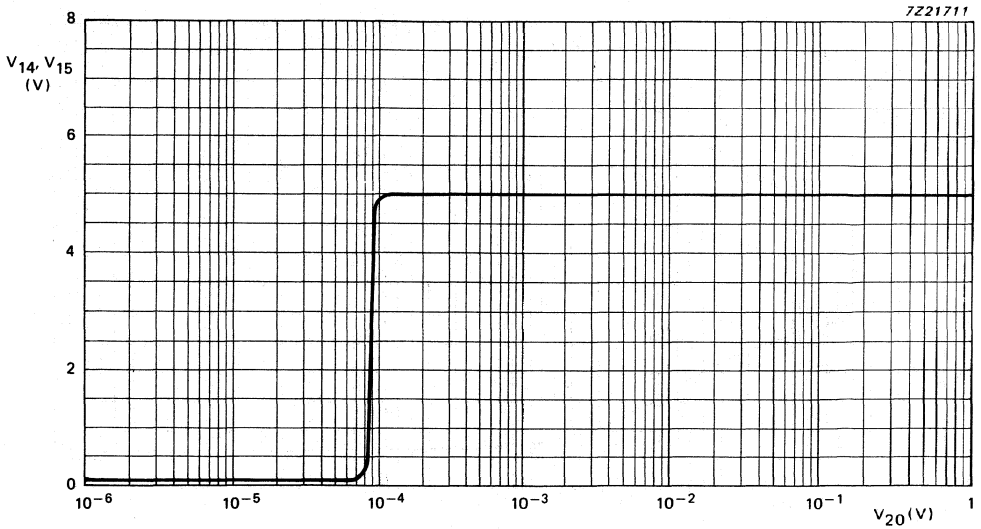


Fig. 11 STOP-0 or STOP-1 output voltages as a function of input voltage at pin 20.

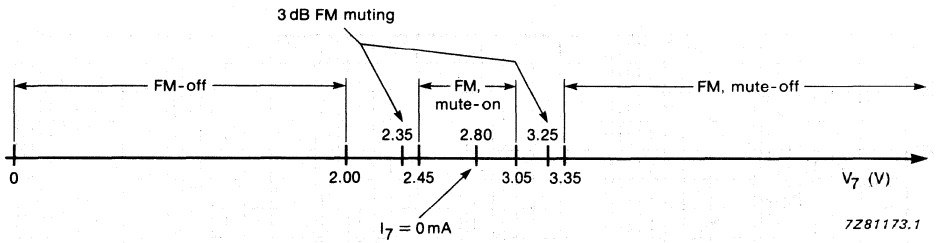
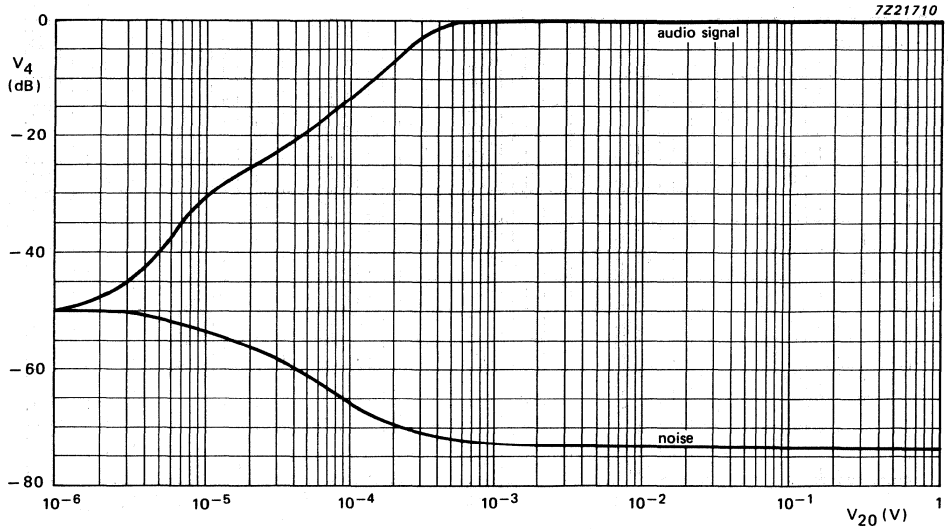
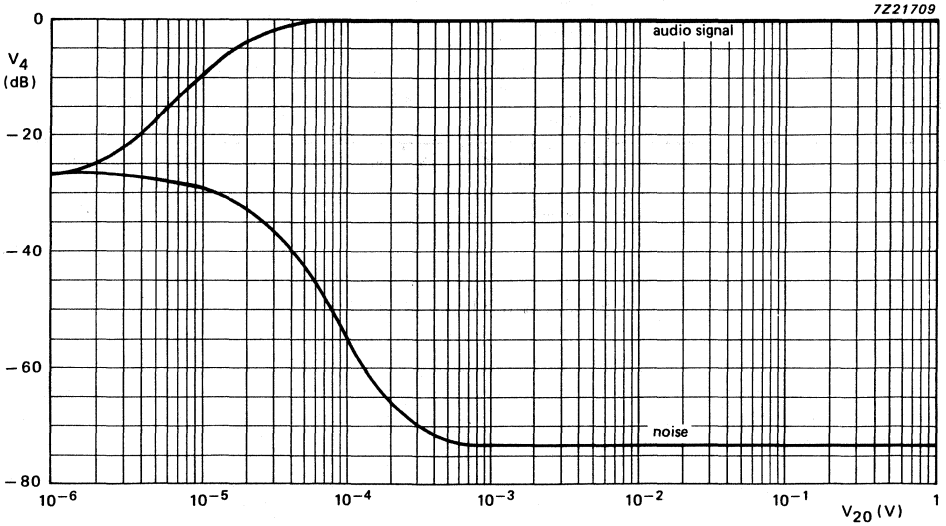


Fig. 12 Switch levels at pin 7.



(a) mode switch at FM, mute-on



(b) mode switch at FM, mute-off

Fig. 13 Audio signal (Δf = 22.5 kHz; f_m = 1 kHz) and noise as functions of input voltage at pin 20; measured with 50 μs de-emphasis.

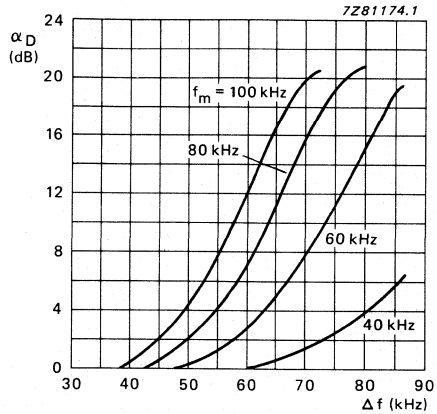


Fig. 14 Dynamic mute attenuation as a function of frequency deviation for modulation frequencies of 40, 60, 80 and 100 kHz.

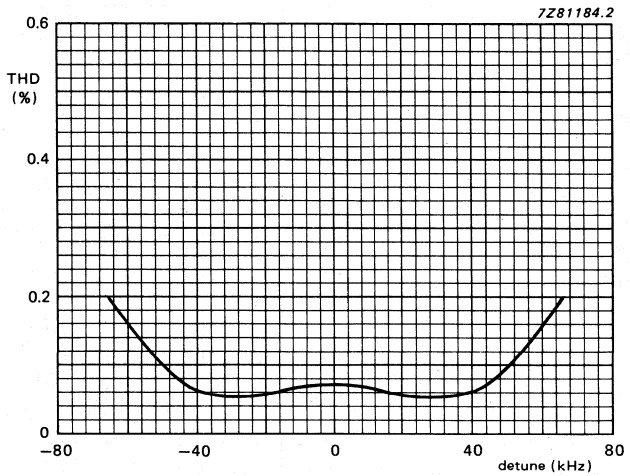
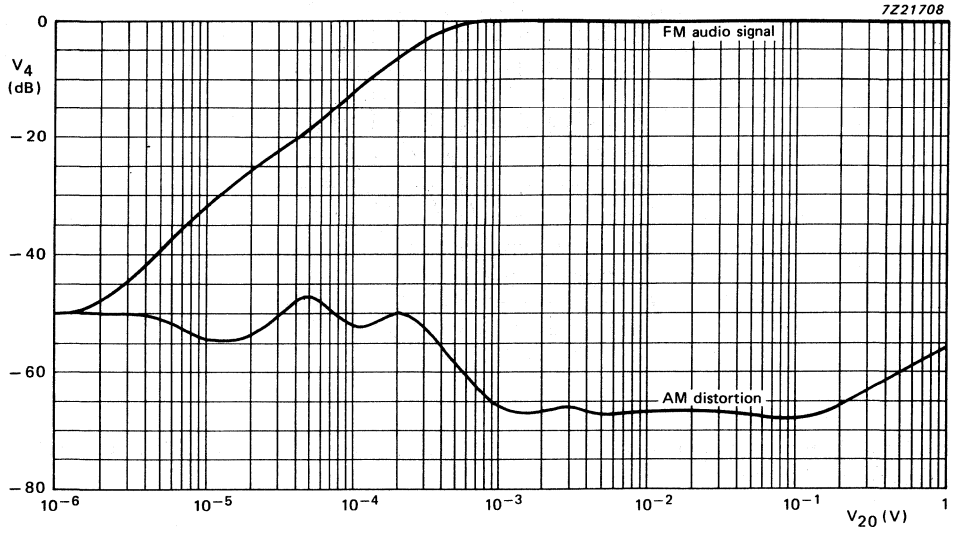
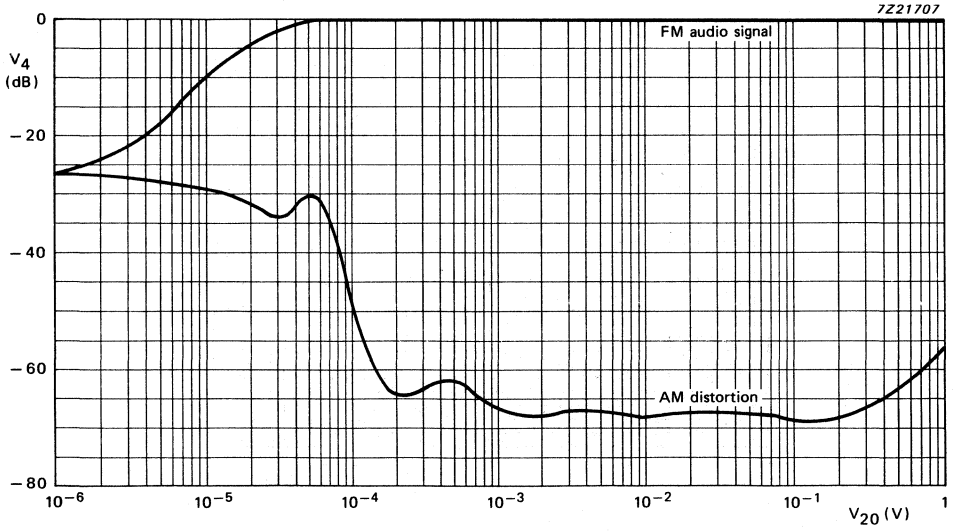


Fig. 15 THD as a function of detuning, mode switch at FM, mute-on position; Δf = 75 kHz; f_m = 1 kHz; $V_{20(rms)}$ = 10 mV.



(a) mode switch at FM, mute-on



(b) mode switch at FM, mute-off

Fig. 16 Typical curves showing AM suppression for an input signal having frequency modulation at Δf = 22.5 kHz and f_m = 1 kHz, and amplitude modulation of 30% at a frequency of 400 Hz; de-emphasis time = 50 μs and bandwidth = 250 Hz to 15 kHz.

IF amplifier/demodulator for FM radio receivers TDA1597

FEATURES

- Balanced limiting amplifier
- Balanced coincidence demodulator
- Two open-collector stop pulse outputs for microcomputer tuning control
- Simulated behaviour of a ratio detector (internal field strength and detuning dependent voltage for dynamic AF signal muting)
- Mono/stereo blend field strength indication control voltage
- AFC output
- 3-state mode switch for FM-MUTE-ON, FM-MUTE-OFF and FM-OFF
- Internal compensation of AF signal total harmonic distortion (THD)
- Built-in hum and ripple rejection circuits.

GENERAL DESCRIPTION

The TDA1597 provides IF amplification, symmetrical quadrature demodulation and level detection for quality home and car FM radio receivers and is suitable for mono and stereo reception. It may also be applied to common front ends, stereo decoders and AM receiver circuits.

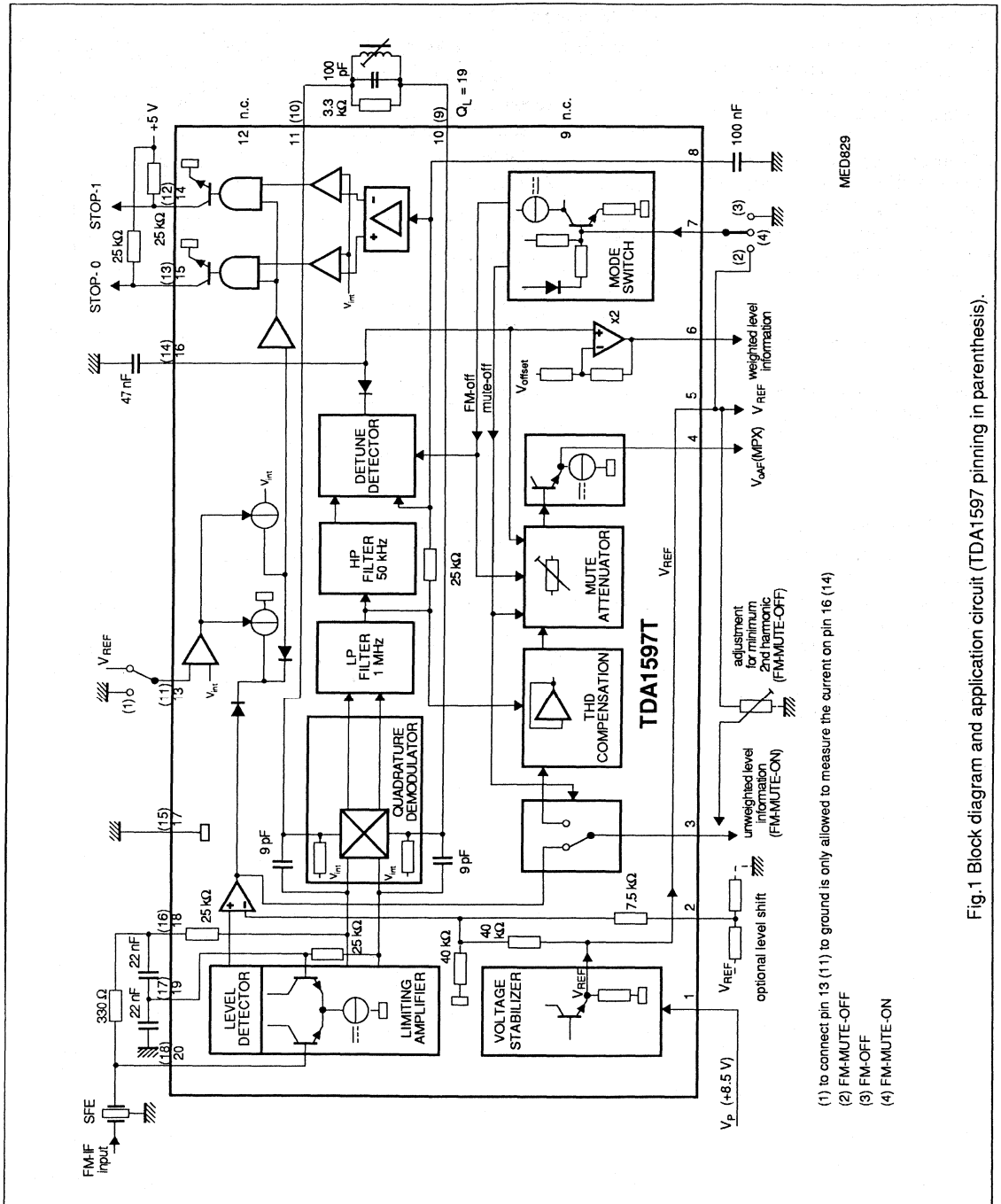
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_P	positive supply voltage (pin 1)	7.5	8.5	12	V
I_P	supply current ($I_2 = I_7 = 0$)	–	20	26	mA
V_i	IF input sensitivity for limiting on pin 20 (RMS value)	14	22	35	μV
V_o	AF output signal on pin 4 (RMS value)	180	200	220	mV
S/N	signal-to-noise ratio (f_m = 400 Hz; Δf = ±75 kHz)	–	82	–	dB
THD	total harmonic distortion (f_m = 1 kHz; Δf = ±75 kHz)	–	0.1	0.3	%
	with K2 adjustment and FM-MUTE-OFF	–	0.07	0.25	%
T_{amb}	operating ambient temperature	–40	–	+85	°C

All pin numbers mentioned in this data sheet refer to the SO-version (TDA1597T) unless otherwise specified.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA1597	18	DIL	plastic	SOT102
TDA1597T	20	mini-pack	plastic	SOT163A



(1) to connect pin 13 (11) to ground is only allowed to measure the current on pin 16 (14)
(2) FM-MUTE-OFF
(3) FM-OFF
(4) FM-MUTE-ON

Fig.1 Block diagram and application circuit (TDA1597 pinning in parenthesis).

PINNING (SO-version TDA1597T; pinning for DIL-version in parenthesis)

SYMBOL	PIN	DESCRIPTION
V_P	1 (1)	supply voltage (+8.5 V)
LVA	2 (2)	level adjustment for stop condition
ULV	3 (3)	unweighted level output / K2 adjustment
V_{oAF}	4 (4)	audio frequency output (MPX signal)
V_{REF}	5 (5)	reference voltage output
WLV	6 (6)	weighted level output
MODE	7 (7)	mode switch input
DDV	8 (8)	detune detector voltage
n.c.	9 (–)	not connected
DEMI1	10 (9)	demodulator input 1
DEMI2	11 (10)	demodulator input 2
n.c.	12 (–)	not connected
TSW	13 (11)	tau switch input
ST1	14 (12)	STOP-1, stop pulse output 1
ST0	15 (13)	STOP-0, stop pulse output 0
MUTE	16 (14)	muting voltage
GND	17 (15)	ground (0 V)
LFB1	18 (16)	IF limiter feedback 1
LFB2	19 (17)	IF limiter feedback 2
V_{iIF}	20 (18)	IF signal input

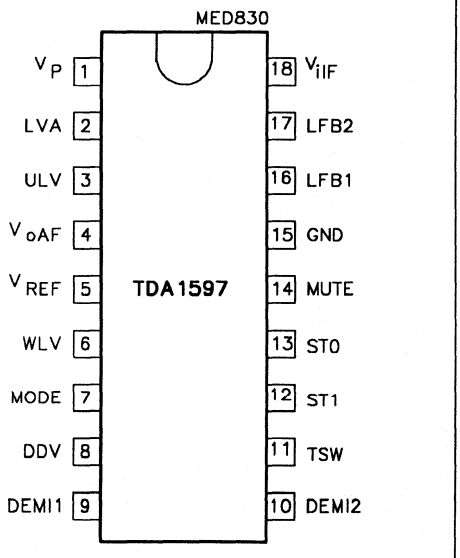


Fig.2 Pin configuration for DIL-version.

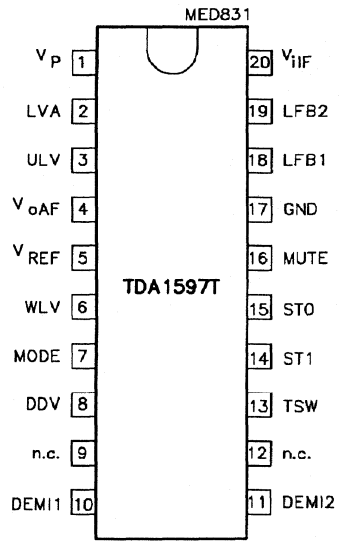


Fig.3 Pin configuration for SO-version.

FUNCTIONAL DESCRIPTION

The limiter amplifier has five stages of IF amplification using balanced differential limiter amplifiers with emitter follower coupling.
Decoupling of the stages from the supply voltage line and an internal high-ohmic DC feedback loop give a very stable IF performance. The amplifier gain is virtually independent of changes in temperature.
The FM demodulator is fully balanced and compromises two cross-coupled differential amplifiers. The quadrature detection of the FM signal is performed by direct feeding of one differential amplifier from the limiter amplifier output, and the other via an external 90 degrees phase shifting network. The demodulator has a good stability and a small zero-cross-over shift. The bandwidth on the demodulator output is restricted by an internal low-pass filter to approximately 1 MHz.

Non-linearities, which are introduced by demodulation, are compensated by the THD compensation circuit. For this reason, the demodulator resonance circuit (between pins 10 and 11) must have a loaded Q-factor of 19. Consequently, there is no need for the demodulator tuned circuit to be adjusted for minimum distortion. Adjustment criterion is a symmetrical stop pulse.
The control voltage for the mute attenuator (pin 16) is derived from the values of the level detector and the detuning detector output signals. The mute attenuator has a fast attack and a slow decay determined by the capacitor on pin 16. The AF signal is fed via the mute attenuator to the output (pin 4). A weighted control voltage (pin 6) is obtained from the mute attenuator control voltage via a buffer amplifier that introduces an additional voltage shift and gain.

The level detector generates a voltage output signal proportional to the amplitude of the input signal. The unweighted level detector output signal is available in FM-MUTE-ON condition (mode switch).
The open-collector tuning stop output voltages STOP-0 and STOP-1 (pins 15 and 14) are derived from the detuning and the input signal level. The pins 14 and 15 may be tied together, if only one tuning-stop output is required.

LIMITING VALUES (TDA1597T pinning)

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_P	supply voltage (pin 1)	–0.3	+13	V
V_{n1}	voltage at pins 2, 4, 5, 6, 10, 11 and 16	–0.3	+10	V
V_{n2}	voltage at pins 7, 3, 8, 14, 15, 18, 19 and 20	–0.3	V_P	V
V_{13}	voltage on pin 13	–	6	V
$I_{14, 15}$	current at pins 14 and 15	–	2	mA
P_{tot}	total power dissipation	–	360	mW
T_{stg}	storage temperature	–55	+150	°C
T_{amb}	operating ambient temperature	–40	+85	°C
V_{ESD}	electrostatic handling; note 1			
	all pins except 5 and 7	–	±2000	V
	pin 5	–	+800	V
			–2000	V
	pin 7	–	+1000	V
			–2000	V

Note to the limiting values

1. Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient in free air	
	SOT102	80 K/W
	SOT163A	90 K/W

CHARACTERISTICS (TDA1597T pinning)

V_P = 8.5 V; T_{amb} = +25 °C; FM-MUTE-ON (I_7 = 0); f_{IF} = 10.7 MHz; deviation ±22.5 kHz with f_m = 400 Hz; V_i = 10 mV RMS at pin 20; de-emphasis of 50 µs; tuned circuit at pins 10 and 11 aligned for symmetrical stop pulses; measurements taken in Fig.4 unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	positive supply voltage (pin 1)		7.5	8.5	12	V
I_P	supply current	$I_2 = I_7 = 0$	–	20	26	mA
Mode switch input						
I_7	input current for FM-MUTE-ON		–	0	–	mA
V_7	input voltage for FM-MUTE-ON		2.4	2.8	3.2	V
	input voltage for FM-MUTE-OFF		$0.9V_{REF}$	–	–	V
	input voltage for FM-OFF	AF attenuation > 60 dB	–	–	1.4	V
IF amplifier and demodulator						
Z_i	demodulator input impedance between pins 10 and 11		25	40	55	kΩ
C_i	demodulator input capacitance between pins 10 and 11		–	6	–	pF
AF output (pin 4)						
R_o	output resistance		–	400	–	Ω
V_4	DC output level	$V_{iIF} \leq 5$ µV RMS on pin 20	2.75	3.1	3.45	V
RR_{1000}	power supply ripple rejection on pin 4	f = 1000 Hz; V_{ripple} = 50 mV RMS	33	36	–	dB
Tuning stop detector						
Δf	detuning frequency for STOP-0	on pin 15; Fig.11				
	for $V_{15} \geq 3.5$ V		–	–	+26.0	kHz
	for $V_{15} \leq 0.3$ V		+38.0	–	–	kHz
Δf	detuning frequency for STOP-1	on pin 14; Fig.10				
	for $V_{14} \geq 3.5$ V		–	–	–26.0	kHz
	for $V_{14} \leq 0.3$ V		–38.0	–	–	kHz
V_{20}	dependence on input voltage for STOP-0 and STOP-1 (RMS value)	Fig.9;				
		$V_{14, 15} \geq 3.5$ V	250	–	–	µV
		$V_{14, 15} \leq 0.3$ V	–	–	50	µV
$V_{14, 15}$	output voltage	$I_{14, 15}$ = 1 mA	–	–	0.3	V
Reference voltage source (pin 5)						
V_{REF}	reference output voltage	I_5 = –1 mA	3.3	3.7	4.1	V
R_5	output resistance	I_5 = –1 mA	–	40	80	Ω
TC	temperature coefficient		–	3.3	–	mV/VK
External muting						
V_{16}	muting voltage at I_2 = 0	$V_{20} \leq 5$ µV RMS; Fig.12	1.45	1.75	2.05	V
		V_{20} = 1 mV RMS	3.0	3.45	3.9	V
S	steepness of control voltage (slope: 100 µV ≤ V_{20} ≤ 100 mV) 20 Δlog V_{20} = 20 dB (ΔV_{16} / Δlog V_{20})		–	0.85	–	V/dec

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Internal mute $\alpha = 20 \log (\Delta V_{4(FM\text{-}MUTE\text{-}OFF)} / \Delta V_{4(FM\text{-}MUTE\text{-}ON)})$						
α	mute voltage	$V_{16} \geq V_{REF}$	–	0	–	dB
		$V_{16} = 0.77V_{REF}$	1.5	–	4.5	dB
		$V_{16} = 0.55V_{REF}$	–	20	–	dB
I_{16}	current for capacitor (pin 16)					
	charge current	$V_{13} = 0$ V	–	–8	–	μA
	discharge current	$V_{13} = 0$ V	–	+120	–	μA
	charge current	$V_{13} = V_{REF}$	–	–100	–	μA
	discharge current	$V_{13} = V_{REF}$	–	+120	–	μA
Level detector						
R_6	output resistance		–	–	500	Ω
V_6	output voltage at $I_2 = 0$	$V_{20} \leq 5$ μV RMS; Fig.14	0.1	–	1.1	V
		$V_{20} = 1$ mV RMS	3.0	–	4.2	V
		±200 kHz detuning	1.2	1.5	1.8	V
	output voltage at $V_2 = V_5$	$V_{20} \leq 5$ μV RMS	–	–	0.3	V
ΔV_6	output voltage at detuning	±45 kHz detuning	–	–	0.2	V
TC	temperature coefficient		–	3.3	–	mV/VK
Δf	detuning frequency	$V_6 = 1.8$ V; Fig.13	90	–	160	kHz
S	steepness of control voltage (slope: 50 μV ≤ V_{20} ≤ 50 mV) 20 $\Delta \log V_{20}$ = 20 dB (ΔV_6 / $\Delta \log V_{20}$)		1.4	1.7	2.0	V/dec
$\Delta V_6/\Delta f$	slope of output voltage at detuning	$\Delta f = 125 \pm 20$ kHz	–	35	–	mV/kHz
S	level shift adjustments					
	range by pin 2	$\pm\Delta V_6/V_{REF}$	0.42	0.5	–	V/V
	gain	$-\Delta V_6/\Delta V_2$	–	1.7	–	V/V
	range by pin 2	$\pm\Delta V_{16}/V_{REF}$	0.21	0.25	–	V/V
	gain	$-\Delta V_{16}/\Delta V_2$	–	0.85	–	V/V

OPERATING CHARACTERISTICS (TDA1597T pinning)

V_P = 7.5 to 12 V; T_{amb} = +25 °C; FM-MUTE-ON (I_7 = 0); f_{IF} = 10.7 MHz; deviation ±22.5 kHz with f_m = 400 Hz; V_i = 10 mV RMS at pin 20; de-emphasis of 50 µs; tuned circuit at pins 10 and 11 aligned for symmetrical stop pulses; measurements taken in Fig.4 unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
IF amplifier and demodulator						
V_i	input signal for start of limiting (–3 dB) (RMS value; pin 20)	$V_7 = V_{REF}$; FM-MUTE-OFF	14	22	35	µV
	input signal for signal-to-noise ratio (RMS value)	f = 250 to 15000 Hz				
	S/N = 26 dB	$V_7 = V_{REF}$	–	15	–	µV
	S/N = 46 dB	$V_7 = V_{REF}$	–	60	–	µV
S/N	signal-to-noise ratio	deviation ±75 kHz	–	82	–	dB
V_o	AF output signal (RMS value; pin 4)		180	200	220	mV
THD	total harmonic distortion without de-emphasis	deviation ±75 kHz; f_m = 1 kHz; I_7 = 0				
	without detuning		–	0.1	0.3	%
	±25 kHz detuning		–	–	0.6	%
	compensated via pin 3	$V_7 = V_{REF}$	–	0.07	0.25	%
ΔV_4	K2 adjustment ($\Delta V_4 = V_4(V_3 = 0) - V_4(V_3 = V_{REF})$)		10	–	–	mV
α_{AM}	AM suppression on pin 4	$V_7 = V_{REF}$; m = 30%				
	V_i = 0.3 to 1000 mV RMS	on pin 20	46	55	–	dB
	V_i = 1 to 300 mV RMS	on pin 20	60	65	–	dB
Dynamic mute attenuation $\alpha = 20 \log (\Delta V_{4(FM\text{-}MUTE\text{-}OFF)} / \Delta V_{4(FM\text{-}MUTE\text{-}ON)})$						
α	dynamic mute attenuation	deviation ±75 kHz; f_m = 100 kHz; V_2 = 1 V	–	14	–	dB
Tuning stop detector						
Δf	detuning frequency for STOP-0	on pin 15; Fig.11				
	for $V_{15} \geq 3.5$ V		–	–	+26.0	kHz
	for $V_{15} \leq 0.3$ V		+38.0	–	–	kHz
Δf	detuning frequency for STOP-1	on pin 14; Fig.10				
	for $V_{14} \geq 3.5$ V		–	–	–26.0	kHz
	for $V_{14} \leq 0.3$ V		–38.0	–	–	kHz
V_{20}	dependence on input voltage for STOP-0 and STOP-1 (RMS value)	Fig.9; $V_{14, 15} \geq 3.5$ V	250	–	–	µV
		$V_{14, 15} \leq 0.3$ V	–	–	50	µV
R_8	internal low-pass resistance of detune detector		12	25	50	kΩ
V_8	voltage on capacitor	I_7 = 0; $V_i \leq 5$ µV RMS on input pin 20	–	2.2	–	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Level detector ($I_2 = 0$)						
V_6	output voltage	$V_{20} \leq 5$ μV RMS	0.1	–	1.1	V
		$V_{20} = 1$ mV RMS	3.0	–	4.2	V
Reference voltage source (pin 5)						
V_{REF}	reference output voltage	$I_5 = -1$ mA	3.3	3.7	4.1	V

Operation with AM-IF

Level and stop information (on pins 6, 13, 14, 15 and 16) is provided for the modes FM-MUTE-ON and FM-MUTE-OFF. This information is also available in the FM-OFF mode when an AM-IF signal is input (for example 455 kHz). This can also provide a valid detuning information when a suitable AM-IF resonance circuit is provided for demodulator (Fig.18).

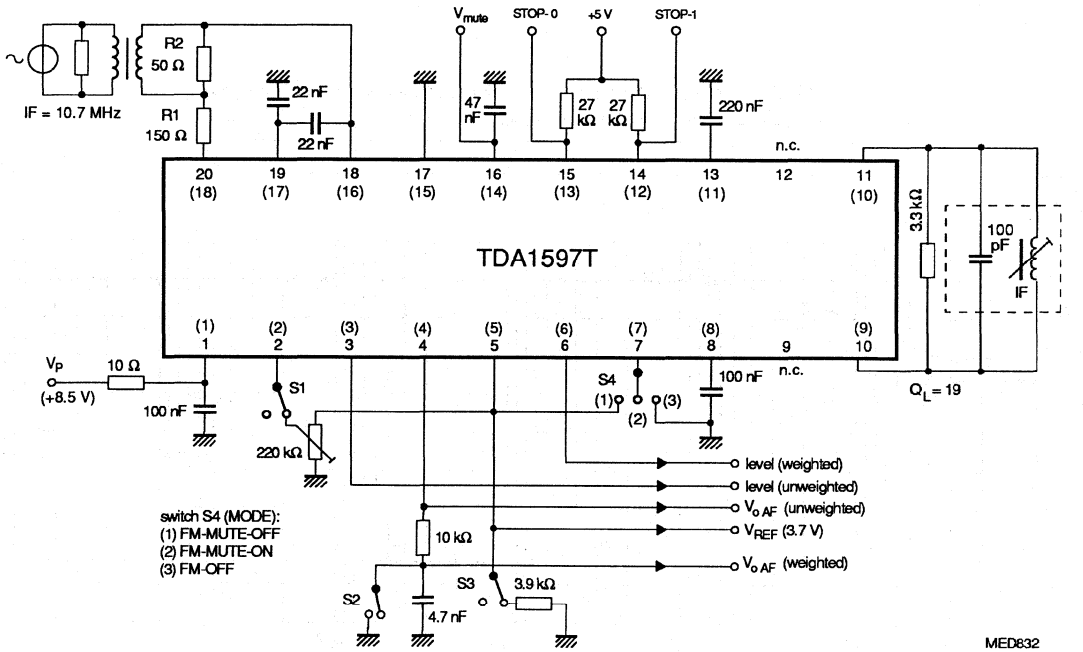
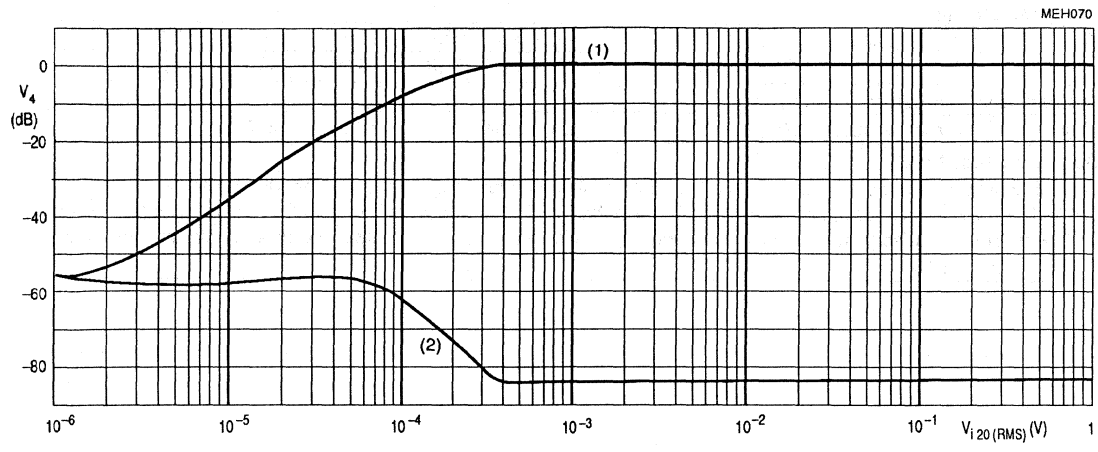
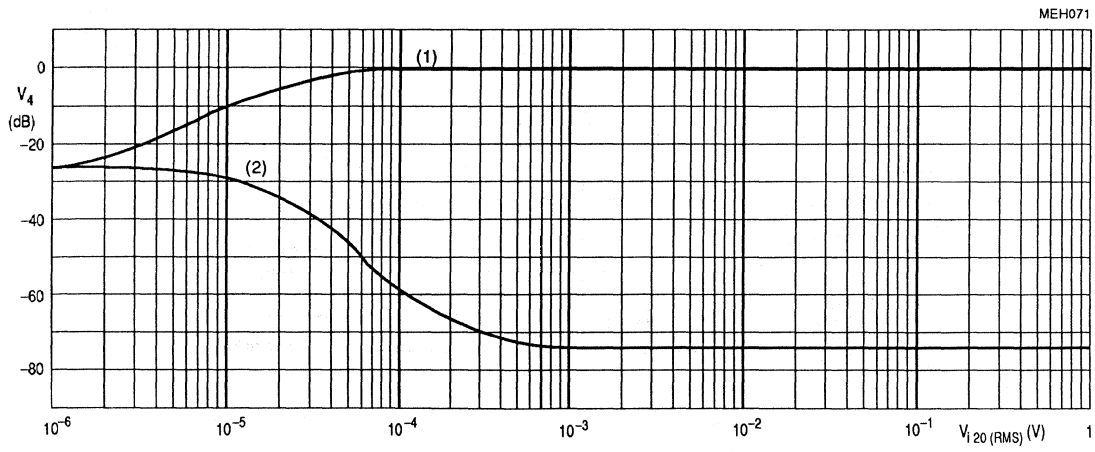


Fig.4 Test circuit (TDA1597 pinning in parenthesis).



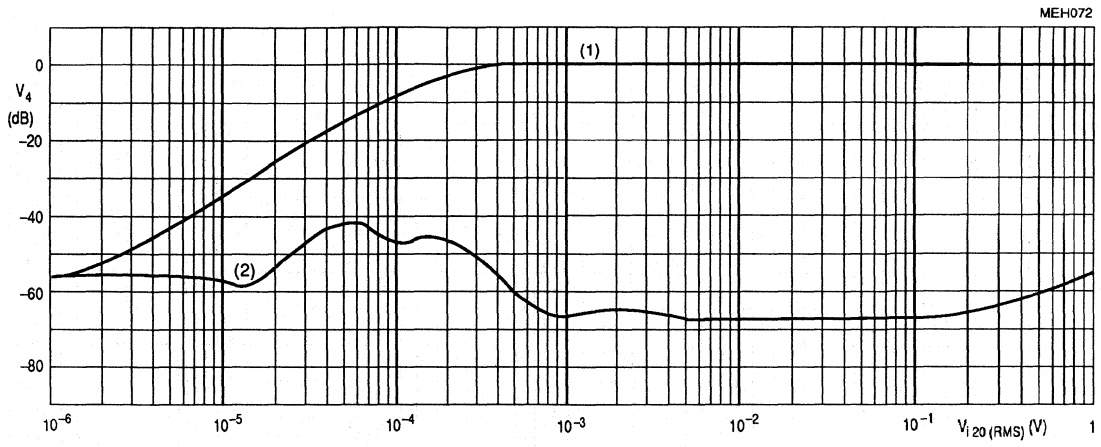
(1) audio signal
(2) noise

Fig.5 FM-MUTE-ON: Audio signal and noise as functions of the input signal V_{iIF} (pin 20) with $\Delta f = \pm 22.5$ kHz; $f_m = 1$ kHz; de-emphasis 50 µs.



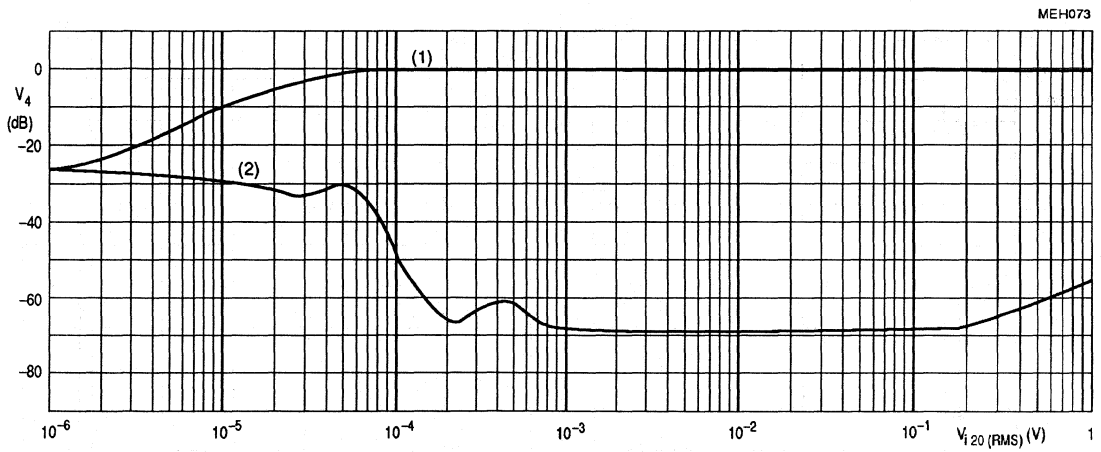
(1) audio signal
(2) noise

Fig.6 FM-MUTE-OFF: Audio signal and noise as functions of the input signal V_{iIF} (pin 20) with $\Delta f = \pm 22.5$ kHz; $f_m = 1$ kHz; de-emphasis 50 µs.



(1) audio signal
(2) spurious AM signal

Fig.7 FM-MUTE-ON: Typical AM suppression as a function of the input signal V_{iIF} (pin 20) with $\Delta f = \pm 22.5$ kHz; $f_m = 1$ kHz; AM with $f_m = 400$ Hz; m = 0.3 and 250 to 15000 Hz bandwidth.



(1) audio signal
(2) spurious AM signal

Fig.8 FM-MUTE-OFF: Typical AM suppression as a function of the input signal V_{iIF} (pin 20) with $\Delta f = \pm 22.5$ kHz; $f_m = 1$ kHz; AM with $f_m = 400$ Hz; m = 0.3 and 250 to 15000 Hz bandwidth.

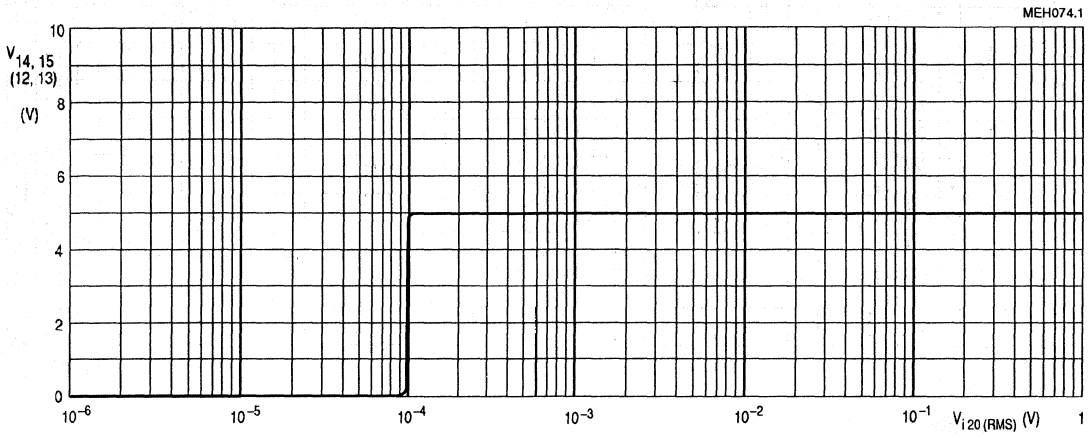


Fig.9 STOP-0 and STOP-1 output voltage dependent on input signal V_{iIF} (pin 20).

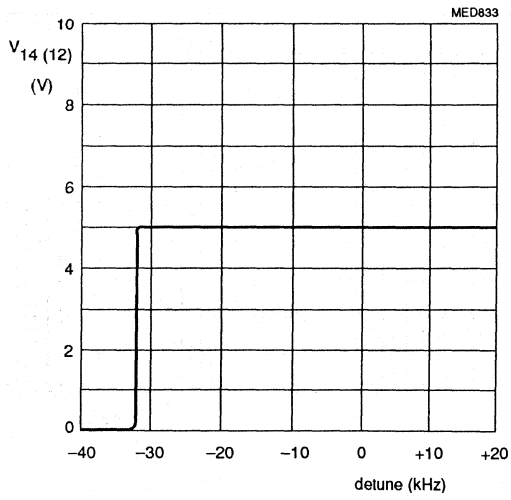


Fig.10 STOP-1 output voltage dependent on V_{iIF} = 10 mV RMS (pin 20).

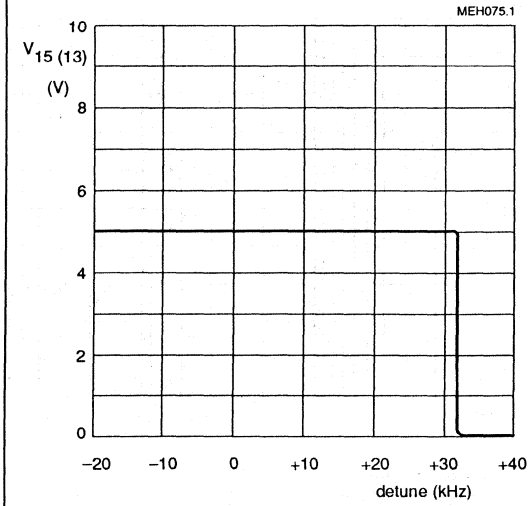


Fig.11 STOP-0 output voltage dependent on V_{iIF} = 10 mV RMS (pin 20).

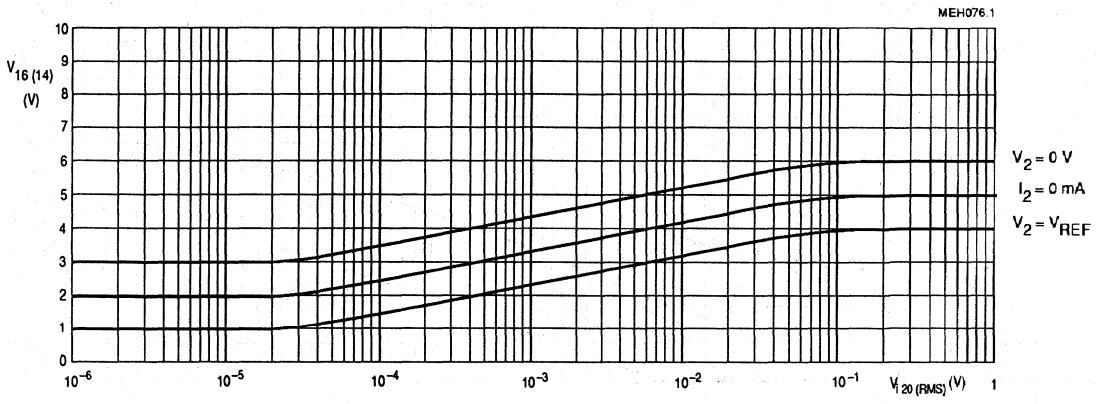


Fig.12 External mute voltage $V_{16\,(14)}$ dependent on input signal V_{iIF} (pin 20); typical adjusting range.

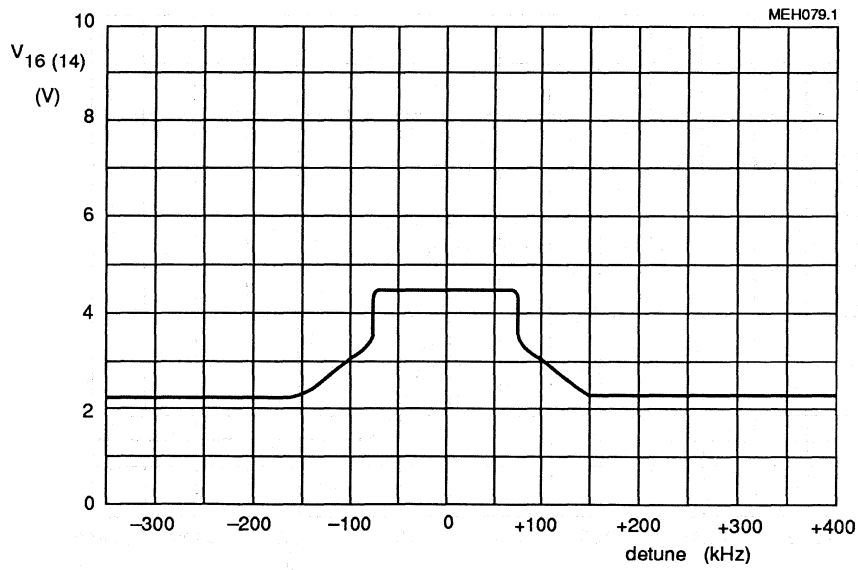


Fig.13 Mute voltage $V_{16\,(14)}$ dependent on detuning; V_{iIF} = 10 mV RMS.

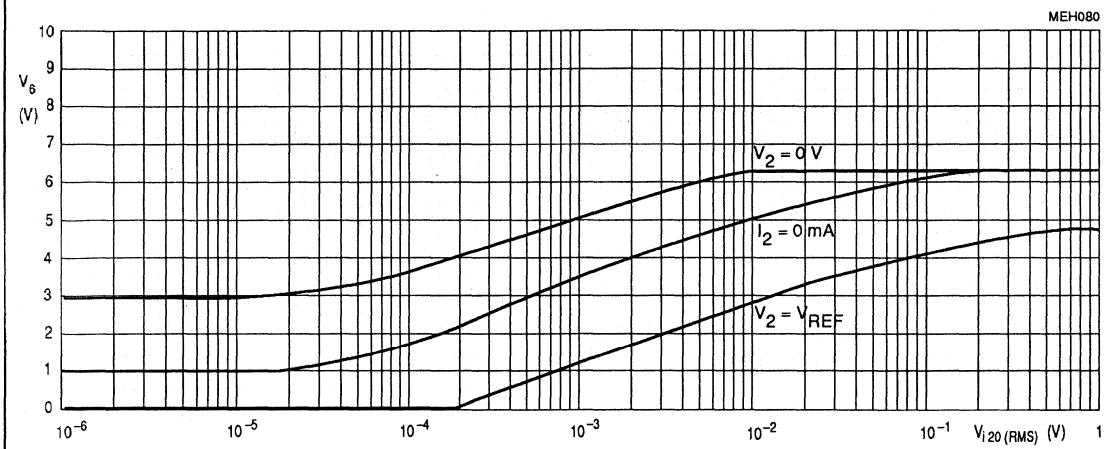


Fig.14 Control voltage V_6 dependent on input signal V_{iIF} (pin 20); typical adjusting range.

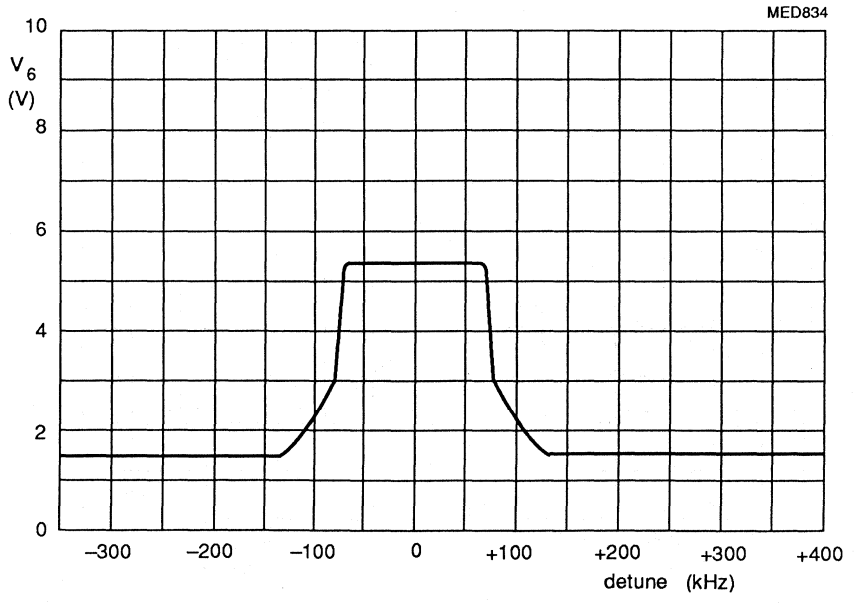


Fig.15 Control voltage V_6 dependent on detuning; V_{iIF} = 10 mV RMS.

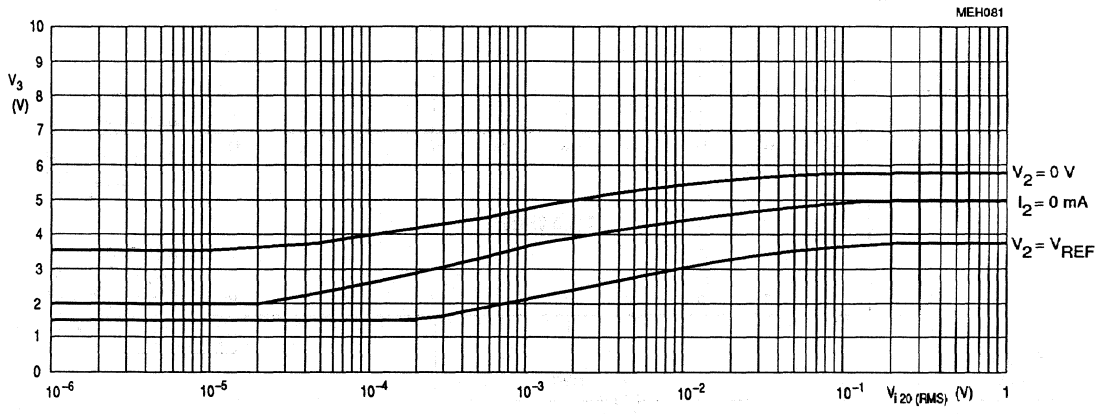


Fig.16 Level output voltage V_3 dependent on input signal V_{iIF} (pin 20); typical adjusting range.

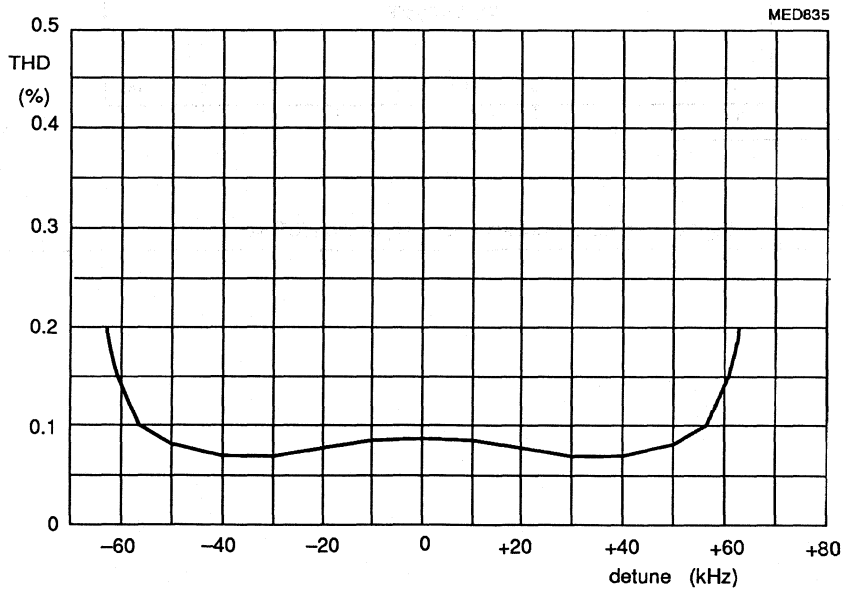


Fig.17 Total harmonic distortion dependent on detuning at FM-MUTE-ON; deviation ±75 kHz; f_m = 1 kHz; V_{iIF} = 10 mV.

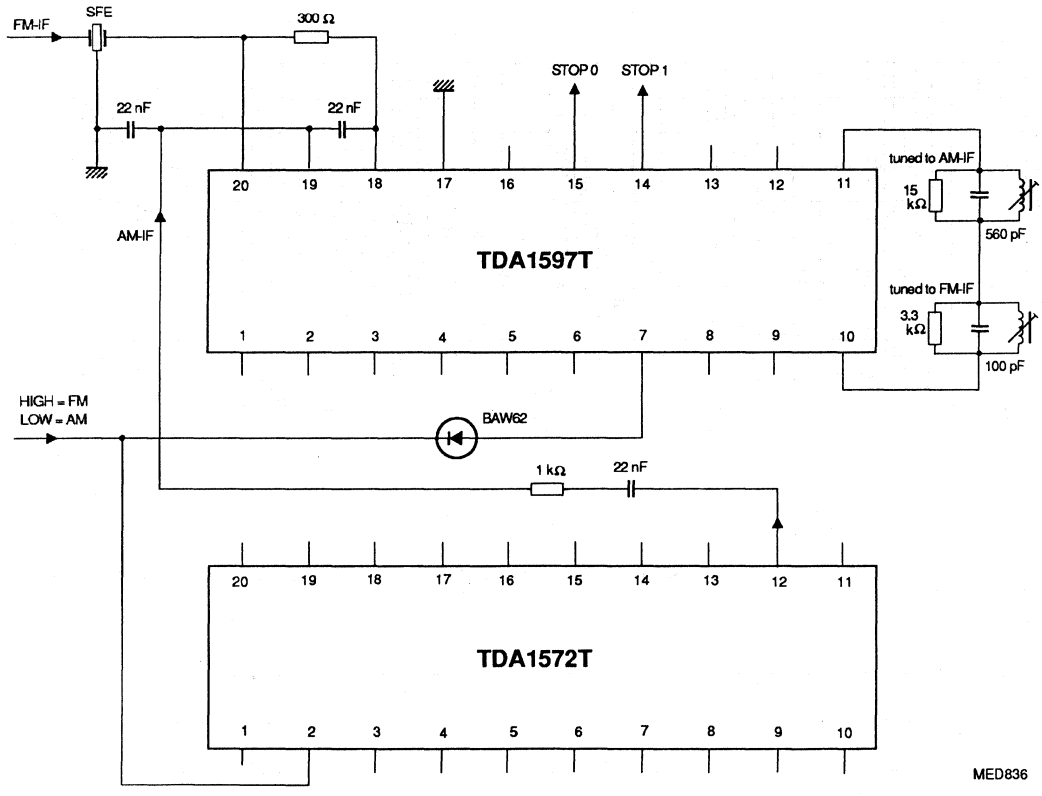


Fig.18 Interface for AM stop pulse application (SO-version).

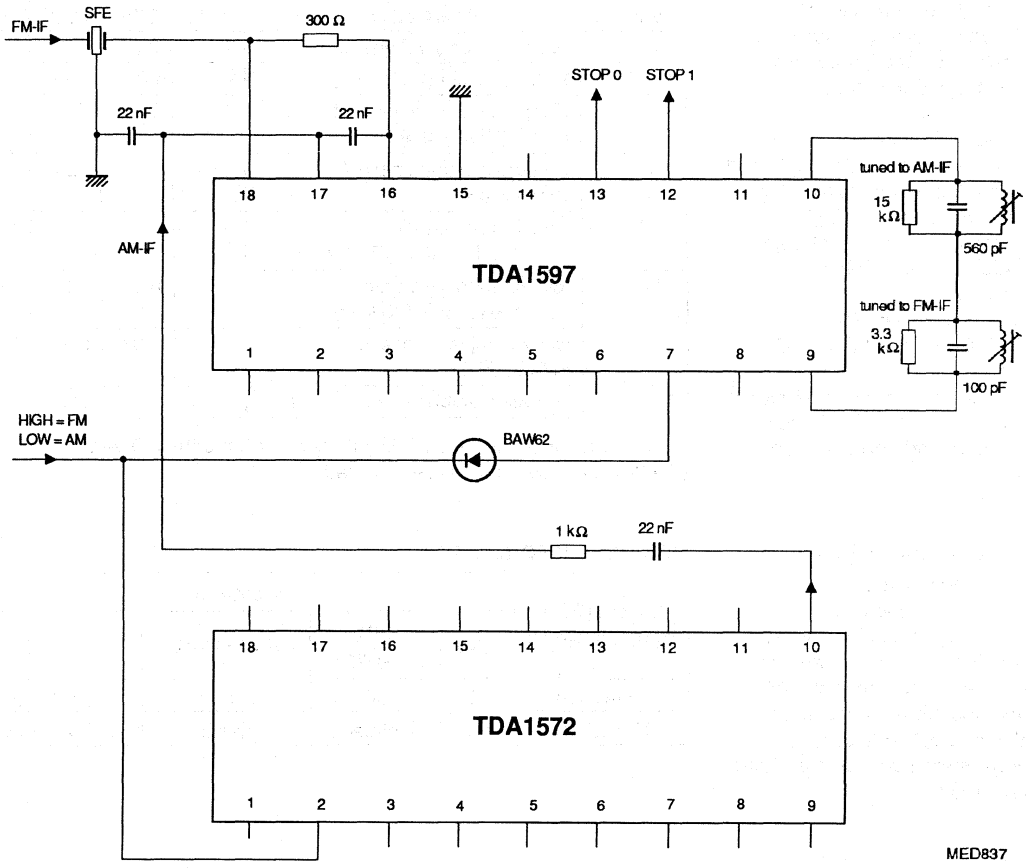


Fig.19 Interface for AM stop pulse application (DIL-version).

IF amplifier/demodulator for FM radio receivers TDA1599

FEATURES

- Balanced limiting amplifier
- Balanced coincidence demodulator
- Two open-collector stop pulse outputs for microcomputer tuning control
- Simulated behaviour of a ratio detector (internal field strength and detuning dependent voltage for dynamic AF signal muting)
- Mono/stereo blend field strength indication control voltage
- AFC output
- 3-state mode switch for FM-MUTE-ON, FM-MUTE-OFF and FM-OFF
- Internal compensation of AF signal total harmonic distortion (THD)
- Built-in hum and ripple rejection circuits.

GENERAL DESCRIPTION

The TDA1599 provides IF amplification, symmetrical quadrature demodulation and level detection for quality home and car FM radio receivers and is suitable for mono and stereo reception. It may also be applied to common front ends, stereo decoders and AM receiver circuits.

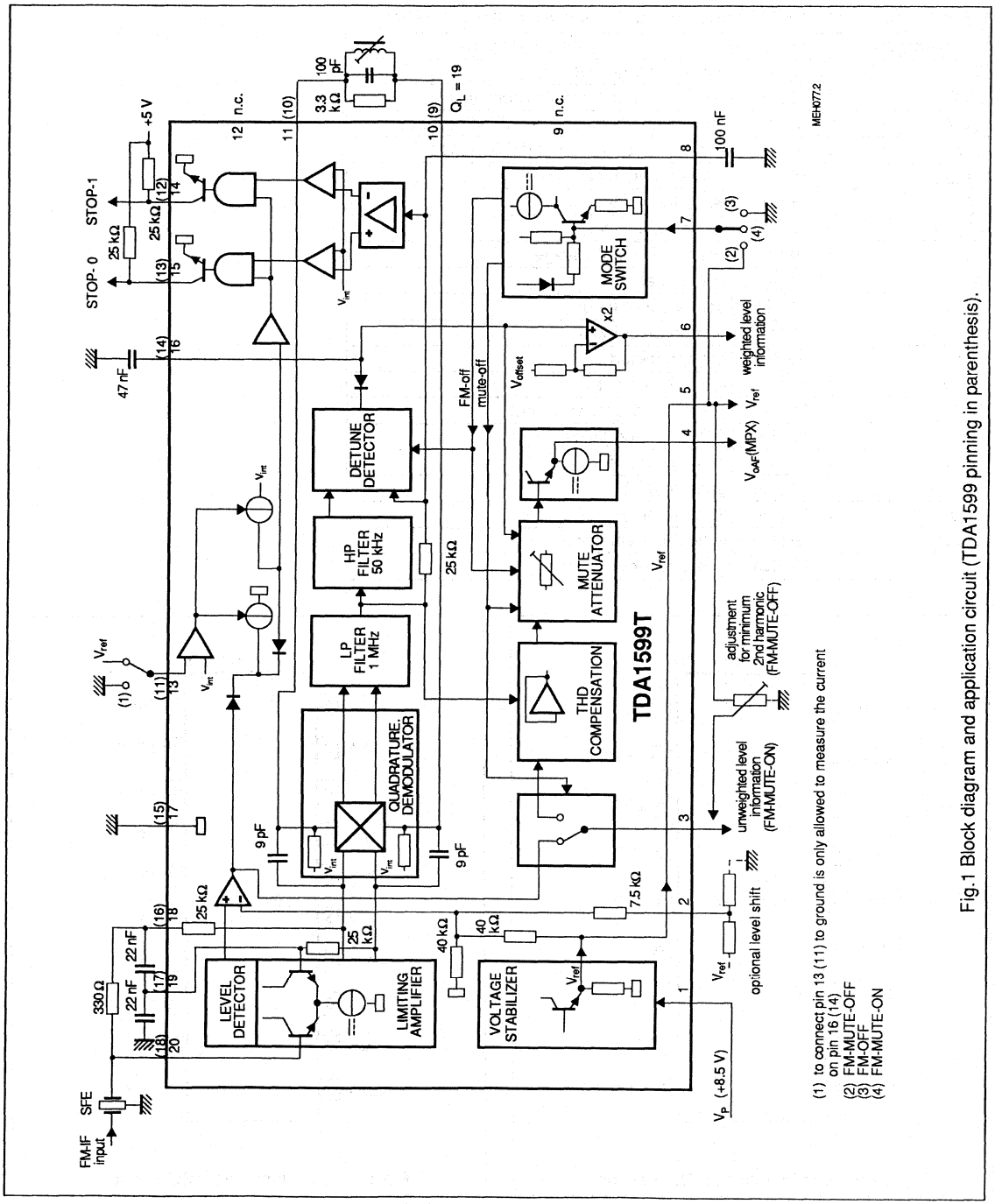
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_P	positive supply voltage (pin 1)	7.5	8.5	12	V
I_P	supply current ($I_2 = I_7 = 0$)	–	20	26	mA
V_i	IF input sensitivity for limiting on pin 20 (RMS value)	14	22	35	μV
V_o	AF output signal on pin 4 (RMS value)	180	200	220	mV
S/N	signal-to-noise ratio (f_m = 400 Hz; $\Delta f = \pm 75$ kHz)	–	82	–	dB
THD	total harmonic distortion (f_m = 1 kHz; $\Delta f = \pm 75$ kHz)	–	0.1	0.3	%
	with K2 adjustment and FM-MUTE-OFF	–	0.07	0.25	%
T_{amb}	operating ambient temperature	−40	–	+85	°C

All pin numbers mentioned in this data sheet refer to the SO-version (TDA1599T) unless otherwise specified.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA1599	18	DIL	plastic	SOT102
TDA1599T	20	mini-pack	plastic	SOT163A



(1) to connect pin 13 (11) to ground is only allowed to measure the current on pin 16 (14).
(2) FM-MUTE-OFF
(3) FM-OFF
(4) FM-MUTE-ON

Fig.1 Block diagram and application circuit (TDA1599 pinning in parenthesis).

PINNING (SO-version TDA1599T; pinning for DIL-version in parenthesis)

SYMBOL	PIN	DESCRIPTION
V_P	1 (1)	supply voltage (+8.5 V)
LVA	2 (2)	level adjustment for stop condition
ULV	3 (3)	unweighted level output / K2 adjustment
V_{oAF}	4 (4)	audio frequency output (MPX signal)
V_{REF}	5 (5)	reference voltage output
WLV	6 (6)	weighted level output
MODE	7 (7)	mode switch input
DDV	8 (8)	detune detector voltage
n.c.	9 (–)	not connected
DEMI1	10 (9)	demodulator input 1
DEMI2	11 (10)	demodulator input 2
n.c.	12 (–)	not connected
TSW	13 (11)	tau switch input
ST1	14 (12)	STOP-1, stop pulse output 1
ST0	15 (13)	STOP-0, stop pulse output 0
MUTE	16 (14)	muting voltage
GND	17 (15)	ground (0 V)
LFB1	18 (16)	IF limiter feedback 1
LFB2	19 (17)	IF limiter feedback 2
V_{iIF}	20 (18)	IF signal input

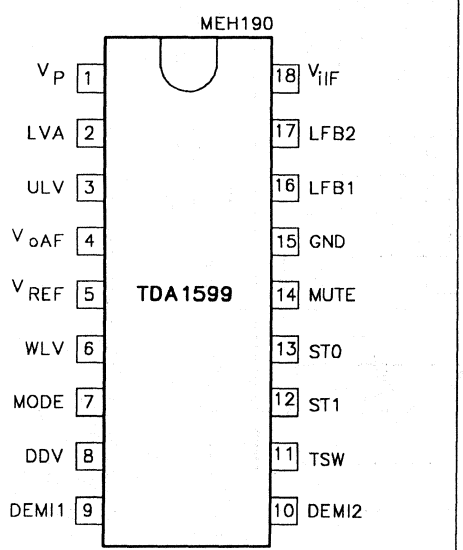


Fig.2 Pin configuration for DIL-version.

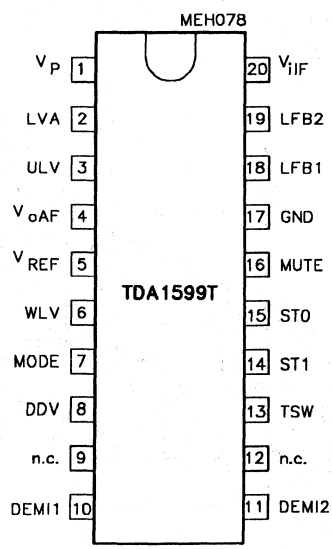


Fig.3 Pin configuration for SO-version.

FUNCTIONAL DESCRIPTION

The limiter amplifier has five stages of IF amplification using balanced differential limiter amplifiers with emitter follower coupling.
Decoupling of the stages from the supply voltage line and an internal high-ohmic DC feedback loop give a very stable IF performance. The amplifier gain is virtually independent of changes in temperature.
The FM demodulator is fully balanced and compromises two cross-coupled differential amplifiers. The quadrature detection of the FM signal is performed by direct feeding of one differential amplifier from the limiter amplifier output, and the other via an external 90 degrees phase shifting network. The demodulator has a good stability and a small zero-cross-over shift. The bandwidth on the demodulator output is restricted by an internal low-pass filter to approximately 1 MHz.

Non-linearities, which are introduced by demodulation, are compensated by the THD compensation circuit. For this reason, the demodulator resonance circuit (between pins 10 and 11) must have a loaded Q-factor of 19. Consequently, there is no need for the demodulator tuned circuit to be adjusted for minimum distortion. Adjustment criterion is a symmetrical stop pulse.
The control voltage for the mute attenuator (pin 16) is derived from the values of the level detector and the detuning detector output signals. The mute attenuator has a fast attack and a slow decay determined by the capacitor on pin 16. The AF signal is fed via the mute attenuator to the output (pin 4). A weighted control voltage (pin 6) is obtained from the mute attenuator control voltage via a buffer amplifier that introduces an additional voltage shift and gain.

The level detector generates a voltage output signal proportional to the amplitude of the input signal. The unweighted level detector output signal is available in FM-MUTE-ON condition (mode switch).
The open-collector tuning stop output voltages STOP-0 and STOP-1 (pins 15 and 14) are derived from the detuning and the input signal level. The pins 14 and 15 may be tied together, if only one tuning-stop output is required.

LIMITING VALUES (TDA1599T pinning)

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_P	supply voltage (pin 1)	−0.3	+13	V
V_{n1}	voltage at pins 2, 4, 5, 6, 10, 11 and 16	−0.3	+10	V
V_{n2}	voltage at pins 7, 3, 8, 14, 15, 18, 19 and 20	−0.3	V_P	V
V_{13}	voltage on pin 13	−	6	V
$I_{14, 15}$	current at pins 14 and 15	−	2	mA
P_{tot}	total power dissipation	−	360	mW
T_{stg}	storage temperature	−55	+150	°C
T_{amb}	operating ambient temperature	−40	+85	°C
V_{ESD}	electrostatic handling; note 1			
	all pins except 5 and 7	−	±2000	V
	pin 5	−	+800	V
			−2000	V
	pin 7	−	+1000	V
			−2000	V

Note to the limiting values

1. Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient in free air	
	SOT102	80 K/W
	SOT163A	90 K/W

CHARACTERISTICS (TDA1599T pinning)

V_P = 8.5 V; T_{amb} = +25 °C; FM-MUTE-ON (I_7 = 0); f_{IF} = 10.7 MHz; deviation ±22.5 kHz with f_m = 400 Hz; V_i = 10 mV RMS at pin 20; de-emphasis of 50 µs; tuned circuit at pins 10 and 11 aligned for symmetrical stop pulses; measurements taken in Fig.4 unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	positive supply voltage (pin 1)		7.5	8.5	12	V
I_P	supply current	$I_2 = I_7 = 0$	–	20	26	mA
Mode switch input						
I_7	input current for FM-MUTE-ON		–	0	–	mA
V_7	input voltage for FM-MUTE-ON		2.4	2.8	3.2	V
	input voltage for FM-MUTE-OFF		$0.9V_{REF}$	–	–	V
	input voltage for FM-OFF	AF attenuation > 60 dB	–	–	1.4	V
IF amplifier and demodulator						
Z_i	demodulator input impedance between pins 10 and 11		25	40	55	kΩ
C_i	demodulator input capacitance between pins 10 and 11		–	6	–	pF
AF output (pin 4)						
R_o	output resistance		–	400	–	Ω
V_4	DC output level	$V_{iIF} \leq 5$ µV RMS on pin 20	2.75	3.1	3.45	V
RR_{1000}	power supply ripple rejection on pin 4	f = 1000 Hz; V_{ripple} = 50 mV RMS	33	36	–	dB
Tuning stop detector						
Δf	detuning frequency for STOP-0	on pin 15; Fig.11				
	for $V_{15} \geq 3.5$ V		–	–	+14.0	kHz
	for $V_{15} \leq 0.3$ V		+22.0	–	–	kHz
Δf	detuning frequency for STOP-1	on pin 14; Fig.10				
	for $V_{14} \geq 3.5$ V		–	–	–14.0	kHz
	for $V_{14} \leq 0.3$ V		–22.0	–	–	kHz
V_{20}	dependence on input voltage for STOP-0 and STOP-1 (RMS value)	Fig.9;				
		$V_{14, 15} \geq 3.5$ V	250	–	–	µV
		$V_{14, 15} \leq 0.3$ V	–	–	50	µV
$V_{14, 15}$	output voltage	$I_{14, 15}$ = 1 mA	–	–	0.3	V
Reference voltage source (pin 5)						
V_{REF}	reference output voltage	$I_5 = -1$ mA	3.3	3.7	4.1	V
R_5	output resistance	$I_5 = -1$ mA	–	40	80	Ω
TC	temperature coefficient		–	3.3	–	mV/VK
External muting						
V_{16}	muting voltage at $I_2 = 0$	$V_{20} \leq 5$ µV RMS; Fig.12	1.45	1.75	2.05	V
		V_{20} = 1 mV RMS	3.0	3.45	3.9	V
S	steepness of control voltage (slope: 100 µV ≤ V_{20} ≤ 100 mV) 20 Δlog V_{20} = 20 dB (ΔV_{16} / Δlog V_{20})		–	0.85	–	V/dec

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Internal mute $\alpha = 20 \log (\Delta V_{4(FM\text{-}MUTE\text{-}OFF)} / \Delta V_{4(FM\text{-}MUTE\text{-}ON)})$						
α	mute voltage	$V_{16} \geq V_{REF}$	–	0	–	dB
		$V_{16} = 0.77V_{REF}$	1.5	–	4.5	dB
		$V_{16} = 0.55V_{REF}$	–	20	–	dB
I_{16}	current for capacitor (pin 16)					
	charge current	$V_{13} = 0$ V	–	–8	–	µA
	discharge current	$V_{13} = 0$ V	–	+120	–	µA
	charge current	$V_{13} = V_{REF}$	–	–100	–	µA
	discharge current	$V_{13} = V_{REF}$	–	+120	–	µA
Level detector						
R_6	output resistance		–	–	500	Ω
V_6	output voltage at $I_2 = 0$	$V_{20} \leq 5$ µV RMS; Fig.14	0.1	–	1.1	V
		$V_{20} = 1$ mV RMS	3.0	–	4.2	V
		±200 kHz detuning	1.2	1.5	1.8	V
	output voltage at $V_2 = V_5$	$V_{20} \leq 5$ µV RMS	–	–	0.3	V
ΔV_6	output voltage at detuning	±45 kHz detuning	–	–	0.2	V
TC	temperature coefficient		–	3.3	–	mV/VK
Δf	detuning frequency	$V_6 = 1.8$ V; Fig.13	90	–	160	kHz
S	steepness of control voltage (slope: 50 µV ≤ V_{20} ≤ 50 mV) 20 $\Delta \log V_{20}$ = 20 dB (ΔV_6 / $\Delta \log V_{20}$)		1.4	1.7	2.0	V/dec
$\Delta V_6/\Delta f$	slope of output voltage at detuning	$\Delta f = 125 \pm 20$ kHz	–	35	–	mV/kHz
S	level shift adjustments					
	range by pin 2	$\pm\Delta V_6/V_{REF}$	0.42	0.5	–	V/V
	gain	$-\Delta V_6/\Delta V_2$	–	1.7	–	V/V
	range by pin 2	$\pm\Delta V_{16}/V_{REF}$	0.21	0.25	–	V/V
	gain	$-\Delta V_{16}/\Delta V_2$	–	0.85	–	V/V

OPERATING CHARACTERISTICS (TDA1599T pinning)

V_P = 7.5 to 12 V; T_{amb} = +25 °C; FM-MUTE-ON (I_7 = 0); f_{IF} = 10.7 MHz; deviation ±22.5 kHz with f_m = 400 Hz; V_i = 10 mV RMS at pin 20; de-emphasis of 50 µs; tuned circuit at pins 10 and 11 aligned for symmetrical stop pulses; measurements taken in Fig.4 unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
IF amplifier and demodulator						
V_i	input signal for start of limiting (–3 dB) (RMS value; pin 20)	$V_7 = V_{REF}$; FM-MUTE-OFF	14	22	35	µV
	input signal for signal-to-noise ratio (RMS value)	f = 250 to 15000 Hz				
	S/N = 26 dB	$V_7 = V_{REF}$	–	15	–	µV
	S/N = 46 dB	$V_7 = V_{REF}$	–	60	–	µV
S/N	signal-to-noise ratio	deviation ±75 kHz	–	82	–	dB
V_o	AF output signal (RMS value; pin 4)		180	200	220	mV
THD	total harmonic distortion without de-emphasis	deviation ±75 kHz; f_m = 1 kHz; I_7 = 0				
	without detuning		–	0.1	0.3	%
	±25 kHz detuning		–	–	0.6	%
	compensated via pin 3	$V_7 = V_{REF}$	–	0.07	0.25	%
ΔV_4	K2 adjustment ($\Delta V_4 = V_4(V_3 = 0) - V_4(V_3 = V_{REF})$)		10	–	–	mV
α_{AM}	AM suppression on pin 4	$V_7 = V_{REF}$; m = 30%				
	V_i = 0.3 to 1000 mV RMS	on pin 20	46	55	–	dB
	V_i = 1 to 300 mV RMS	on pin 20	60	65	–	dB
Dynamic mute attenuation $\alpha = 20 \log (\Delta V_{4(FM\text{-}MUTE\text{-}OFF)} / \Delta V_{4(FM\text{-}MUTE\text{-}ON)})$						
α	dynamic mute attenuation	deviation ±75 kHz; f_m = 100 kHz; V_2 = 1 V	–	14	–	dB
Tuning stop detector						
Δf	detuning frequency for STOP-0	on pin 15; Fig.11				
	for $V_{15} \geq 3.5$ V		–	–	+14.0	kHz
	for $V_{15} \leq 0.3$ V		+22.0	–	–	kHz
Δf	detuning frequency for STOP-1	on pin 14; Fig.10				
	for $V_{14} \geq 3.5$ V		–	–	–14.0	kHz
	for $V_{14} \leq 0.3$ V		–22.0	–	–	kHz
V_{20}	dependence on input voltage for STOP-0 and STOP-1 (RMS value)	Fig.9; $V_{14, 15} \geq 3.5$ V	250	–	–	µV
		$V_{14, 15} \leq 0.3$ V	–	–	50	µV
R_8	internal low-pass resistance of detune detector		12	25	50	kΩ
V_8	voltage on capacitor	I_7 = 0; $V_i \leq 5$ µV RMS on input pin 20	–	2.2	–	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Level detector ($I_2 = 0$)						
V_6	output voltage	$V_{20} \leq 5$ μV RMS	0.1	–	1.1	V
		$V_{20} = 1$ mV RMS	3.0	–	4.2	V
Reference voltage source (pin 5)						
V_{REF}	reference output voltage	$I_5 = -1$ mA	3.3	3.7	4.1	V

Operation with AM-IF

Level and stop information (on pins 6, 13, 14, 15 and 16) is provided for the modes FM-MUTE-ON and FM-MUTE-OFF. This information is also available in the FM-OFF mode when an AM-IF signal is input (for example 455 kHz). This can also provide a valid detuning information when a suitable AM-IF resonance circuit is provided for demodulator (Fig.18).

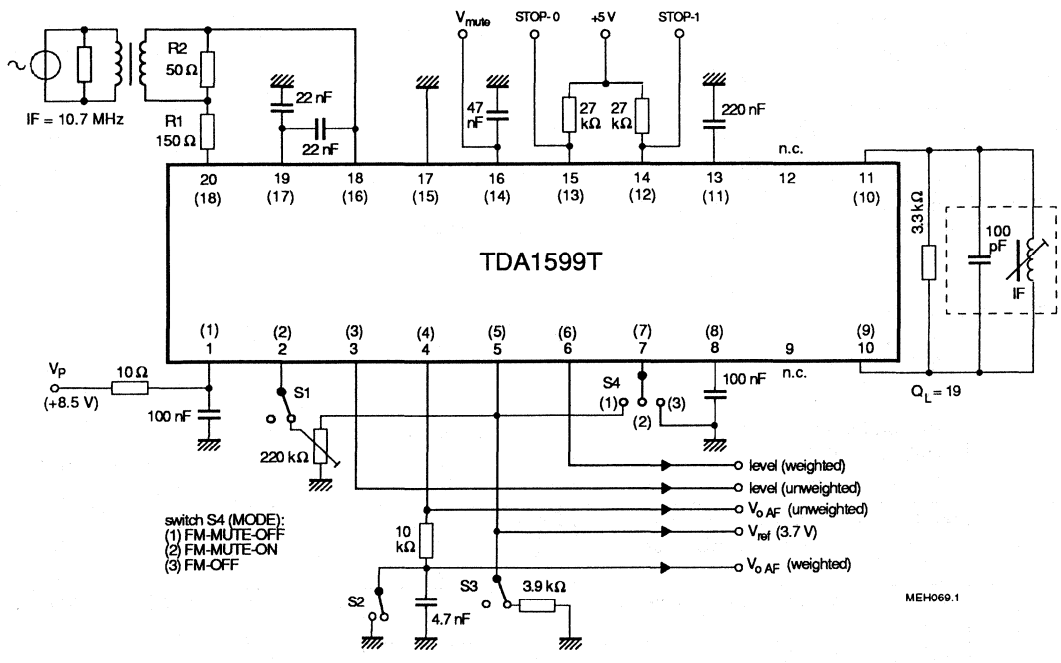
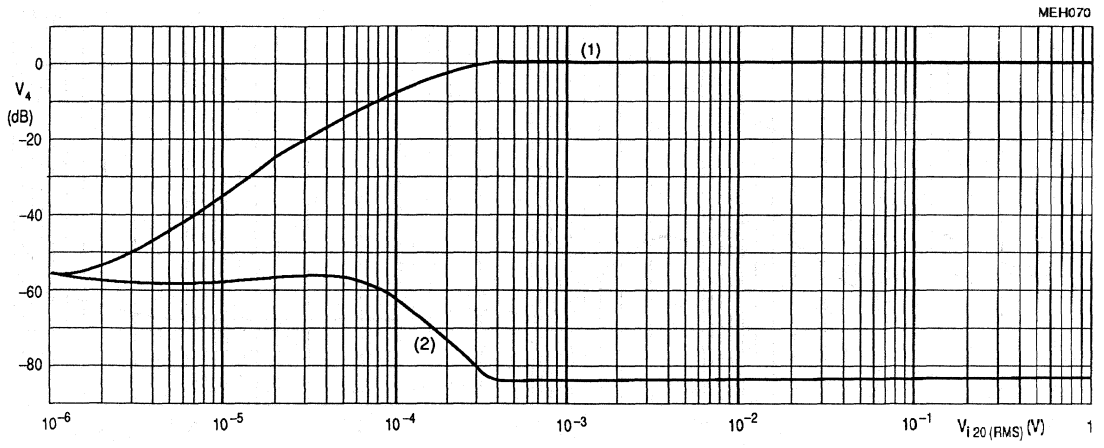
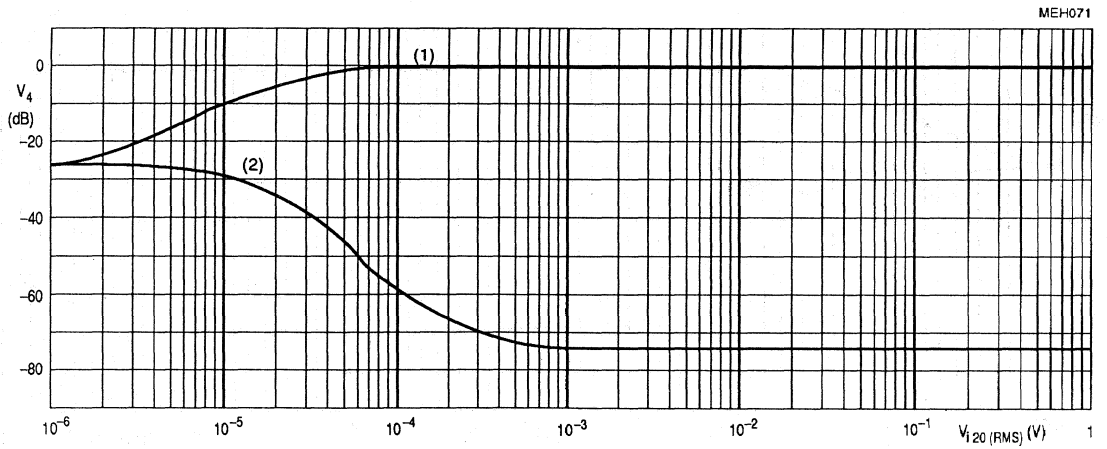


Fig.4 Test circuit (TDA1599 pinning in parenthesis).



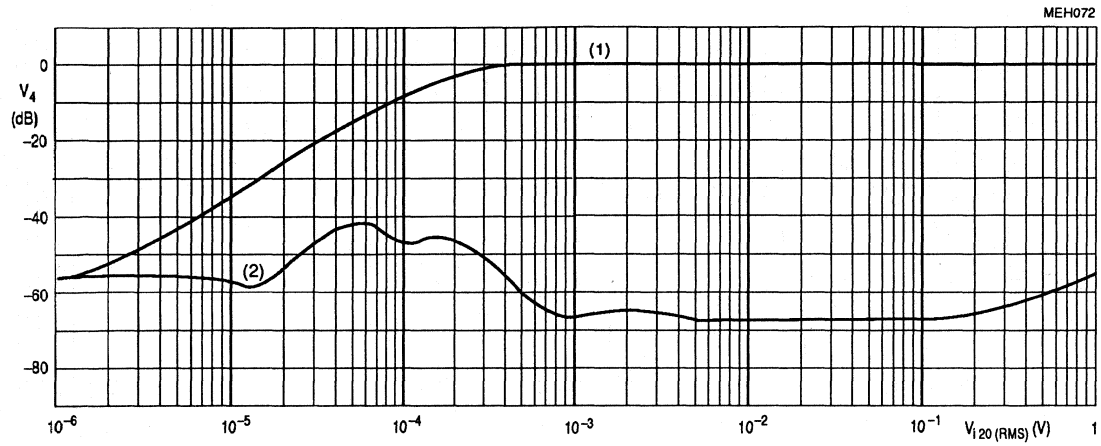
(1) audio signal
(2) noise

Fig.5 FM-MUTE-ON: Audio signal and noise as functions of the input signal V_{iIF} (pin 20) with $\Delta f = \pm 22.5$ kHz; $f_m = 1$ kHz; de-emphasis 50 µs.



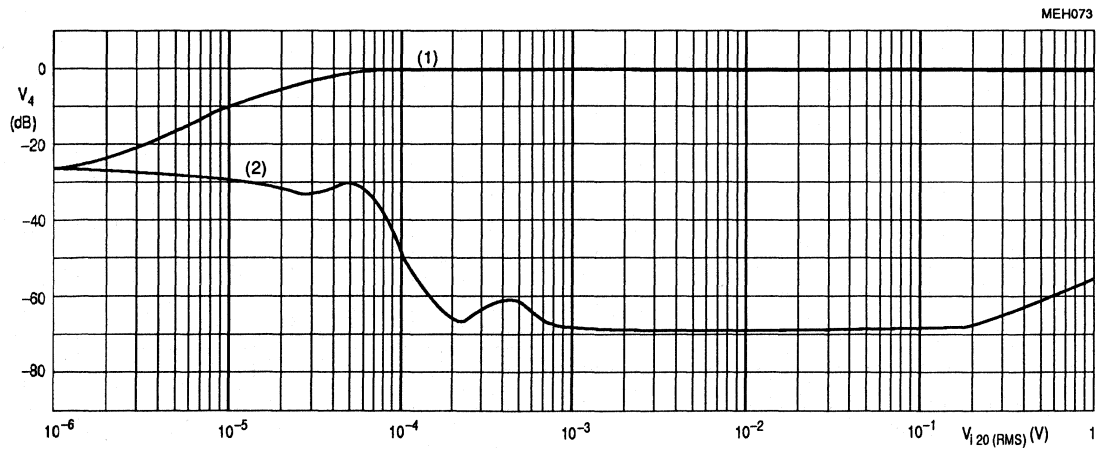
(1) audio signal
(2) noise

Fig.6 FM-MUTE-OFF: Audio signal and noise as functions of the input signal V_{iIF} (pin 20) with $\Delta f = \pm 22.5$ kHz; $f_m = 1$ kHz; de-emphasis 50 µs.



(1) audio signal
(2) spurious AM signal

Fig.7 FM-MUTE-ON: Typical AM suppression as a function of the input signal V_{iIF} (pin 20) with $\Delta f = \pm 22.5$ kHz; $f_m = 1$ kHz; AM with $f_m = 400$ Hz; m = 0.3 and 250 to 15000 Hz bandwidth.



(1) audio signal
(2) spurious AM signal

Fig.8 FM-MUTE-OFF: Typical AM suppression as a function of the input signal V_{iIF} (pin 20) with $\Delta f = \pm 22.5$ kHz; $f_m = 1$ kHz; AM with $f_m = 400$ Hz; m = 0.3 and 250 to 15000 Hz bandwidth.

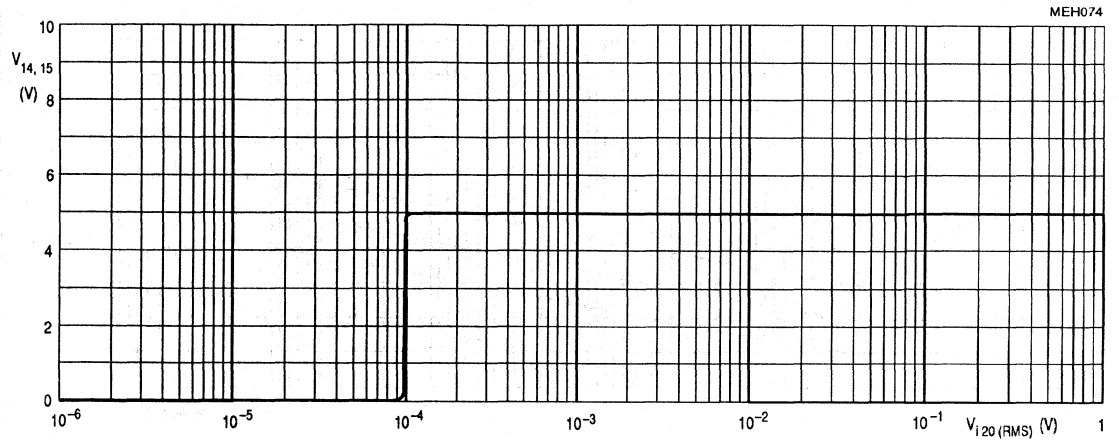


Fig.9 STOP-0 and STOP-1 output voltage dependent on input signal V_{iIF} (pin 20).

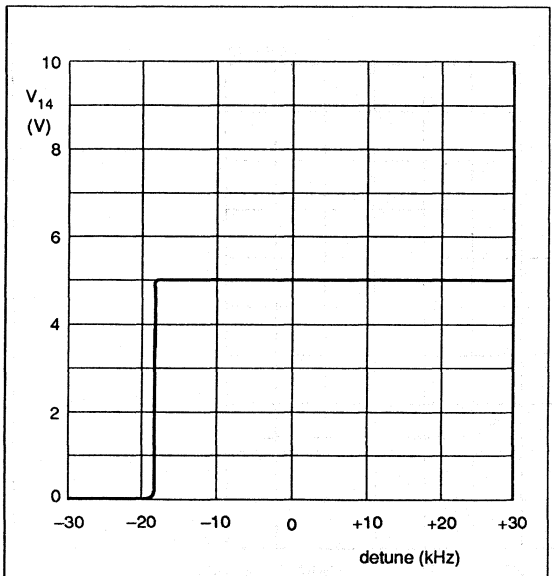


Fig.10 STOP-1 output voltage dependent on V_{iIF} = 10 mV RMS (pin 20).

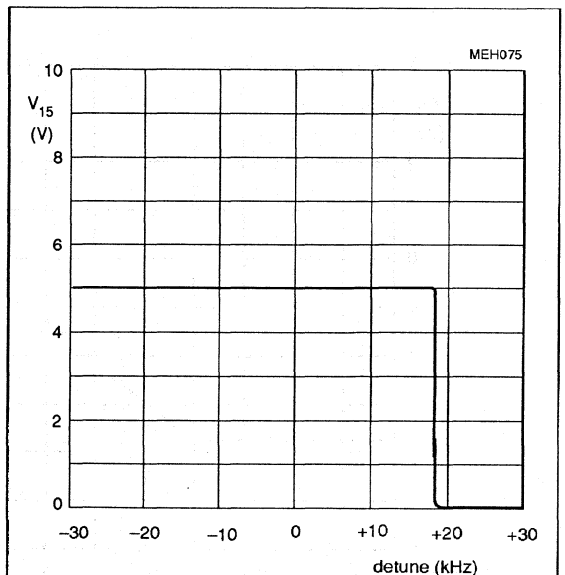


Fig.11 STOP-0 output voltage dependent on V_{iIF} = 10 mV RMS (pin 20).

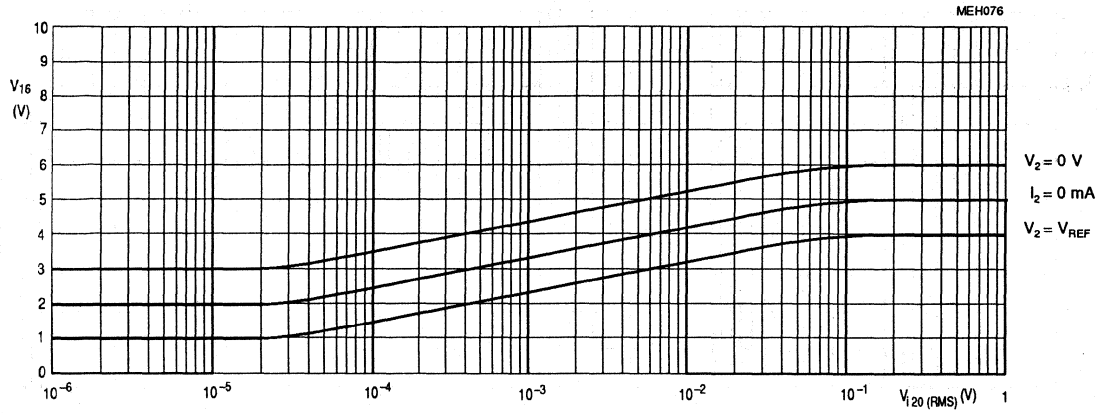


Fig.12 External mute voltage V_{16} dependent on input signal V_{iIF} (pin 20); typical adjusting range.

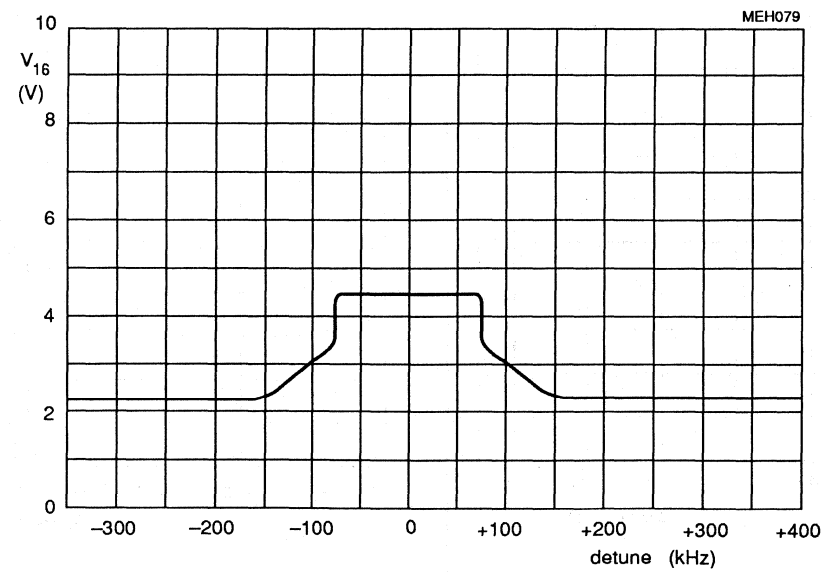


Fig.13 Mute voltage V_{16} dependent on detuning; V_{iIF} = 10 mV RMS.

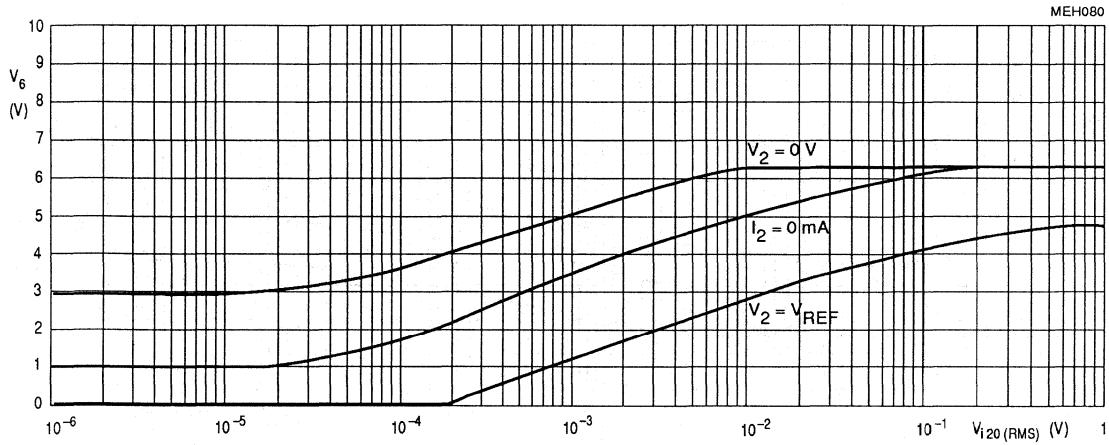


Fig.14 Control voltage V_6 dependent on input signal V_{iIF} (pin 20); typical adjusting range.

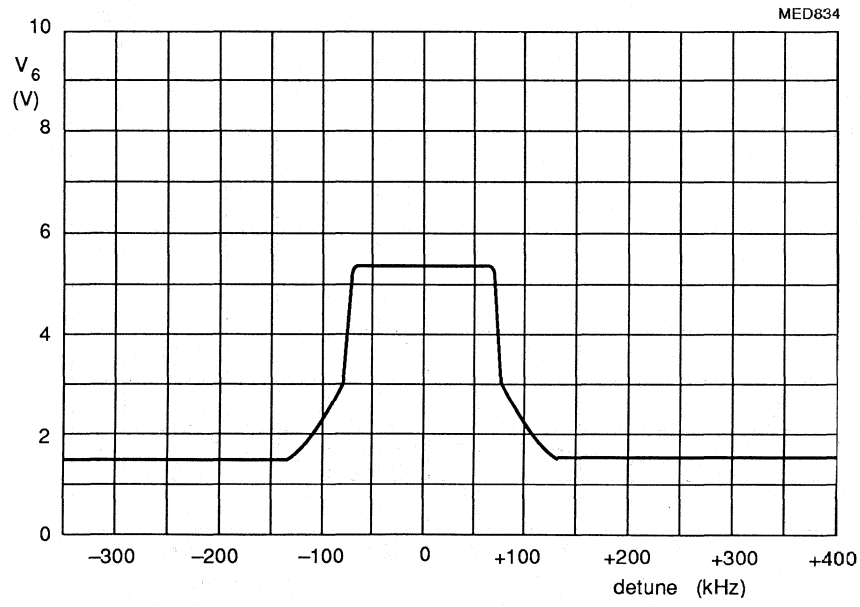


Fig.15 Control voltage V_6 dependent on detuning; V_{iIF} = 10 mV RMS.

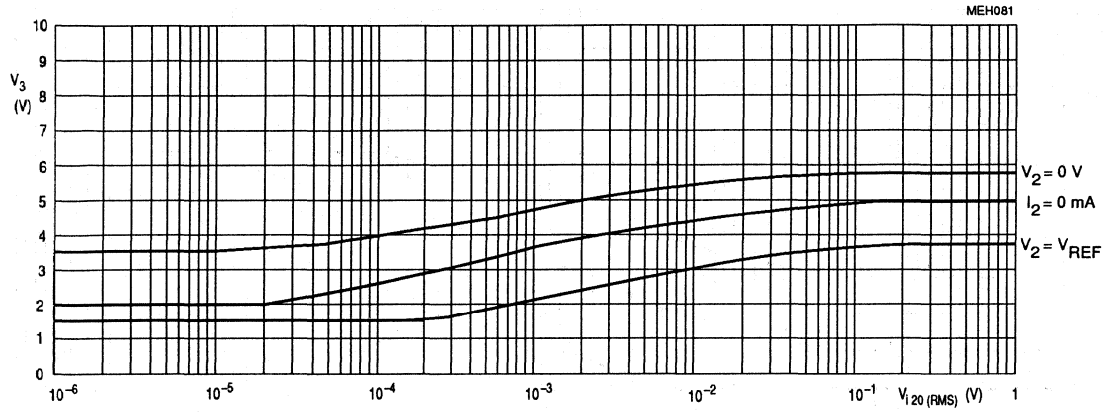


Fig.16 Level output voltage V_3 dependent on input signal V_{iIF} (pin 20); typical adjusting range.

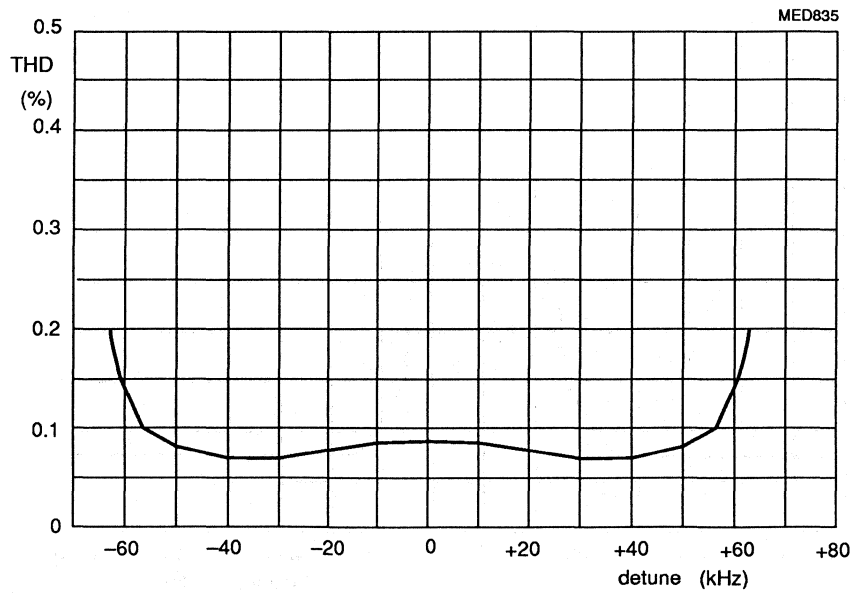


Fig.17 Total harmonic distortion dependent on detuning at FM-MUTE-ON; deviation ±75 kHz; f_m = 1 kHz; V_{iIF} = 10 mV.

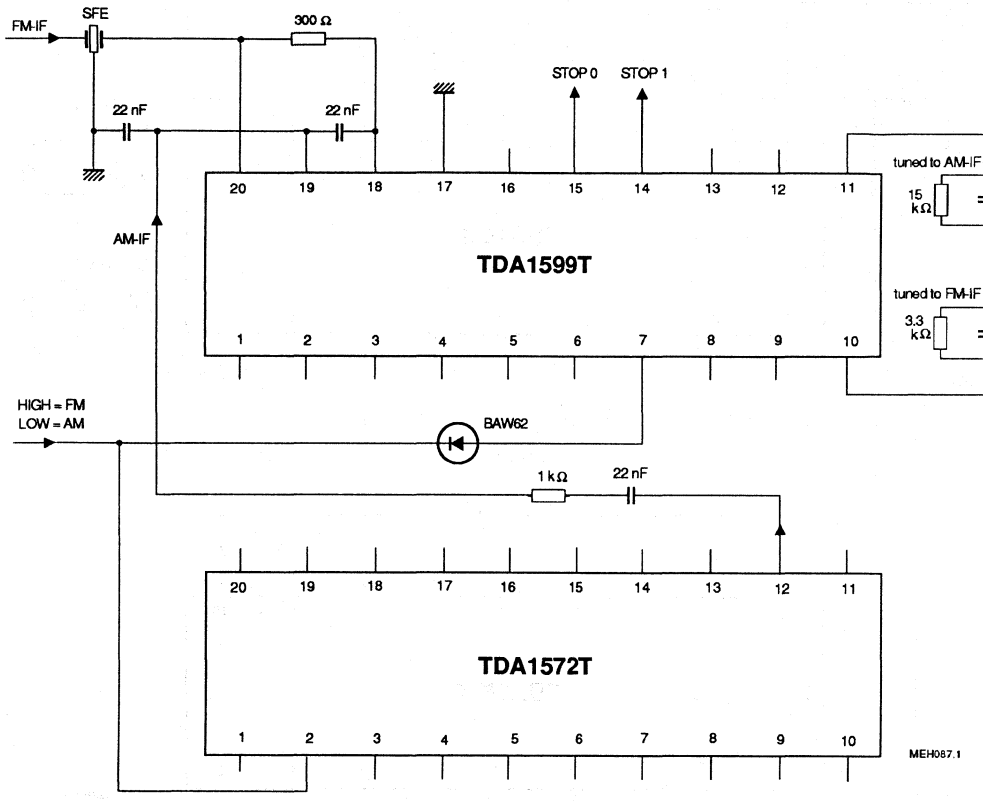


Fig.18 Interface for AM stop pulse application (SO-version).

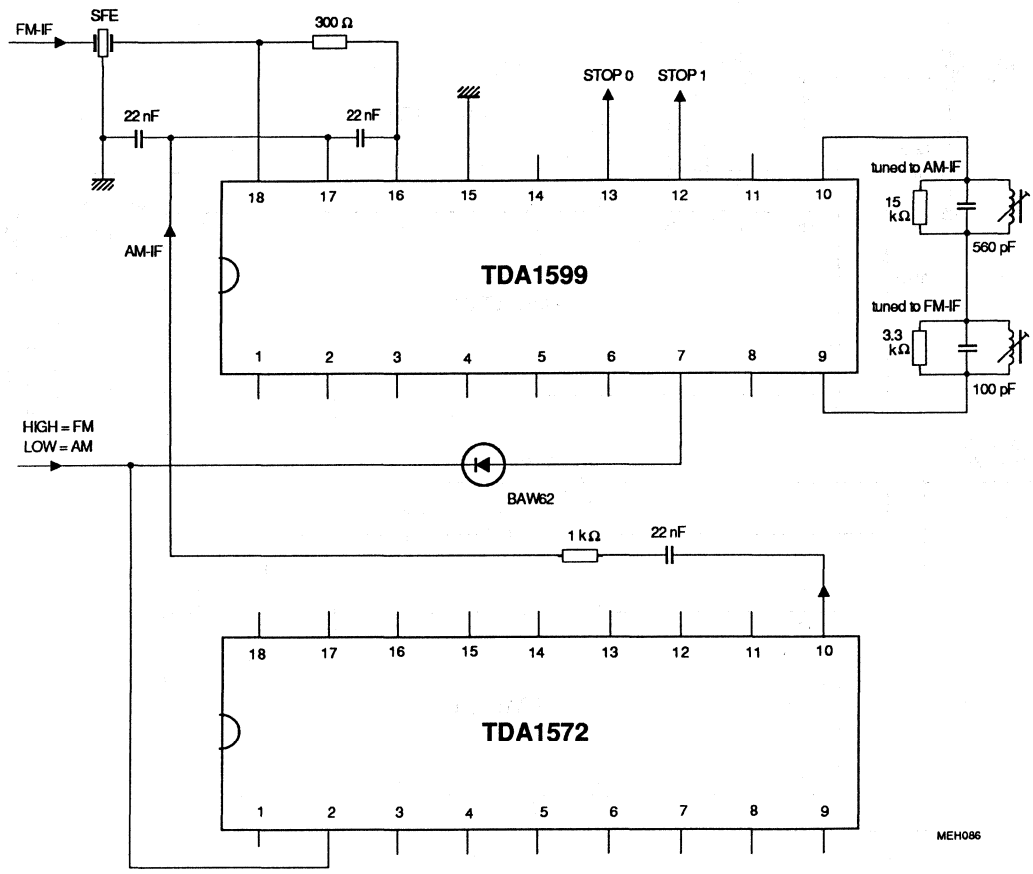


Fig.19 Interface for AM stop pulse application (DIL-version).

Double-deck playback/record IC (DDPR)

TDA1602A

FEATURES

- Two stereo playback preamplifiers
- Stereo playback amplifier
- High speed dubbing headswitch for channel A
- Record/playback headswitch for channel B
- Dubbing switch
- Stereo record amplifier
- Automatic level control
- Erase and bias oscillator
- Tape selector
- Reference voltage source (1/2 V_P)
- Logic part

GENERAL DESCRIPTION

The TDA1602A is a Dolby B compatible recorder IC, which has been designed for use in double-deck recorders for Ferro/Chrome with high speed dubbing. The device performs all the basic recorder functions and needs only a very simple peripheral circuit of a few components. The DDPR may also be used in applications with automatic reverse.

All functions of the DDPR are selected by externally applied DC voltage levels. The circuit is designed for use with a mains-fed asymmetrical power supply but can also be used with a symmetrical power supply (because of its own 1/2 V_P reference voltage source).

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA1602A	40	DIL	plastic	SOT129

Double-deck playback/record IC (DDPR) TDA1602A

QUICK REFERENCE DATA

All voltages referenced to pin 12, all currents positive into the IC

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage range		7.0	–	18.0	V
Playback amplifier						
G	gain	f = 315 Hz	–	57	–	dB
S/N	signal-to-noise ratio		–	53	–	dB
THD	total harmonic distortion	V_O = 150 mV	–	0.1	–	%
Headswitch						
$V_{ON(p-p)}$	maximum voltage (peak-to-peak value)	record mode	–	–	90	V
Record amplifier						
G	gain	f = 315 Hz	–	14	–	dB
S/N	signal-to-noise ratio		–	65	–	dB
THD	total harmonic distortion	$V_{Orecord}$ = 1.5 mV	–	0.3	–	%
Automatic level control						
ΔV_O	output voltage variation	ΔV_{line} = 20 dB	–	1	–	dB
Oscillator						
f_{OSC}	frequency range		60	–	120	kHz
$I_{O(peak)}$	output current (peak value)		140	–	–	mA
$V_{O(p-p)}$	output voltage (peak-to-peak value)		–	–	36	V
Reference voltage						
V_{ref}	output voltage		–	1/2 V_P	–	V
Logic part						
I_I	input current					
	pins 8 and 10		–	100	–	µA
	pins 7 and 9		–	–	900	µA

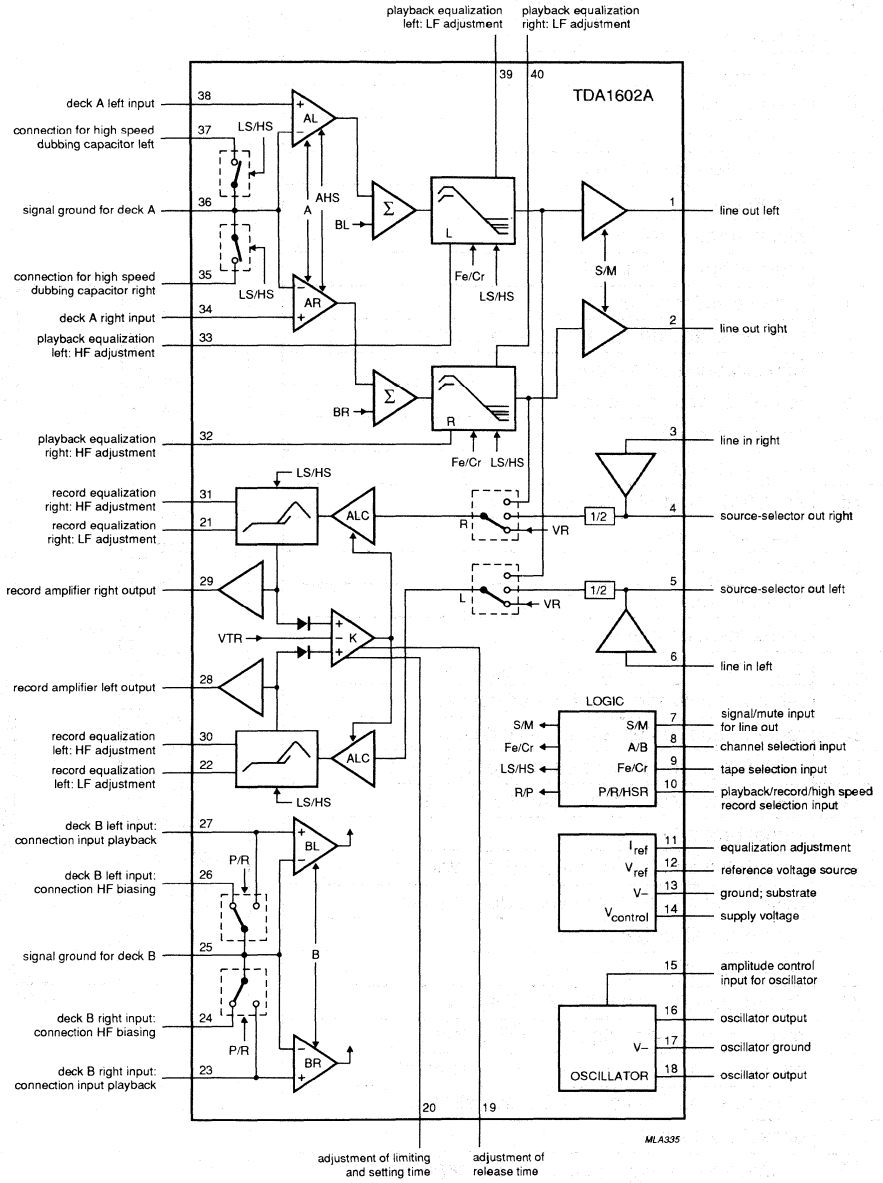


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
LOL	1	line out left
LOR	2	line out right
LIR	3	line in right
SOR	4	source-selector out right
SOL	5	source-selector out left
LIL	6	line in left
S/M	7	signal/mute input for line out
A/B	8	channel selection input
TS	9	tape selection input
P/R/HSR	10	playback/record/high-speed record selection input
EQUADJ	11	equalization adjustment
V_{ref}	12	reference voltage source
GND	13	ground; substrate
V_P	14	supply voltage
OSCCON	15	amplitude control input for oscillator
OSCO1	16	oscillator output 1
OSCGND	17	oscillator ground
OSCO2	18	oscillator output 2
ADJRT	19	adjustment of release time
ADJLST	20	adjustment of limiting and setting time
RECERLF	21	record equalization right: LF adjustment
RECELLF	22	record equalization left: LF adjustment
BRIP	23	deck B right input: connection input playback
BRIBHF	24	deck B right input: connection HF biasing
SGNDB	25	signal ground for deck B
BLIBHF	26	deck B left input: connection HF biasing
BLIP	27	deck B left input: connection input playback
RECOL	28	record amplifier left output
RECOR	29	record amplifier right output
RECELHF	30	record equalization left: HF adjustment
RECERHF	31	record equalization right: HF adjustment
PERHF	32	playback equalization right: HF adjustment
PELHF	33	playback equalization left: HF adjustment
ARI	34	deck A right input
HSDR	35	connection for high speed dubbing capacitor right
SGNDA	36	signal ground for deck A
HSDL	37	connection for high speed dubbing capacitor left
ALI	38	deck A left input

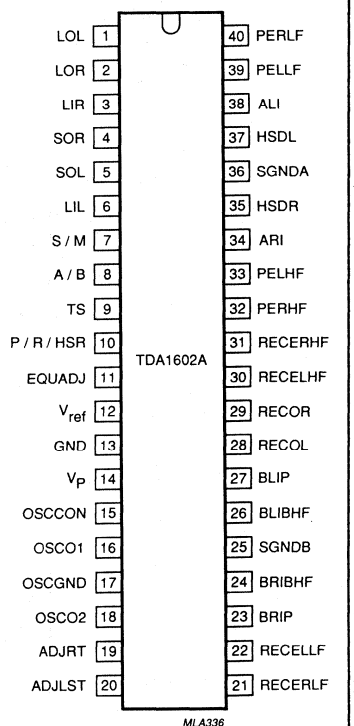


Fig.2 Pin configuration.

SYMBOL	PIN	DESCRIPTION
PELLF	39	playback equalization left: LF adjustment
PERLF	40	playback equalization right: LF adjustment

FUNCTIONAL DESCRIPTION

Playback pre-amplifier

The playback preamplifier is a linear low-noise amplifier with an internal fixed gain of 26.4 dB. The relevant preamplifier for playback of channel A or B can be selected externally.

Playback amplifier

The frequency response of the playback amplifier is determined by two external capacitors (Right: C6 and C21, Left: C5 and C20). The different equalization curves for Ferro and Chrome (with time constants of 120 µs and 70 µs respectively) are controlled by the logic part of the circuit.

High speed dubbing headswitch

This electronic switch is used to connect, or disconnect, an extra external capacitor (Right: C4, Left: C1) in parallel with the gap-loss correction capacitor.

Record/playback headswitch

This is a two position electronic switch which switches the relevant side of the head to the signal ground.

RECORD POSITION

In the record mode the input of the playback amplifier is switched to the signal ground. In this way the bias and audio signal current can be applied to the head.

PLAYBACK POSITION

In the playback mode the biasing side of the head is switched to the signal ground.

Record amplifier

The frequency response of the record amplifier is determined by means of two external capacitors (Right: C11 and C12; Left: C17 and C18).
By omitting these capacitors a flat frequency response is obtained for Dolby application.

Automatic level control

The automatic level control (ALC) has a control range of 20 dB. The variation in the output voltage is less than 2 dB (see Fig.5). The attack and recovery time of the ALC can be adjusted externally.

Erase and bias oscillator

The erase and bias oscillator provides the following:

A high frequency bias current to enable a linear magnetic recording process on the tape.
A sinusoidal voltage, the amplitude of which is determined by the applied voltage at pin 15 (see also Fig.6).
The necessary current for erasing the tape which is only activated when the circuit is switched to the record mode.

Reference voltage source

This circuit delivers an output voltage which is half the supply voltage. The output voltage can be taken as signal ground. In this way a symmetrical power supply is available for the total recorder application.

Logic part

The logic part converts the incoming information from the logic input into the necessary switching signals, used in the analog parts of the circuit. The conversion is determined by the level of the input signal (see Fig.7). The logic inputs (pins 8 and 10) are independent of signal rise and fall times. The inputs at pins 7 and 9 enable smooth switching between signal/mute and Ferro/Chrome respectively.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134). All voltages referenced to pin 12; all currents positive into the IC

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_P	positive supply voltage		–	18	V
V_{7-10}	logic input voltage (pins 7 to 10)		0	V_P	V
V_{15}	control input voltage (pin 15)		0	V_P	V
$V_{16,18}$	oscillator output voltage (pins 16 and 18)		0	36	V
$V_{28,30}$	headswitch voltage (pins 28 and 30)		–45	+45	V
T_{stg}	storage temperature range		–55	+150	°C
T_j	junction temperature		–	+150	°C
P_{tot}	total power dissipation	T_{amb} = +60 °C	–	1.8	W

DC CHARACTERISTICS

All voltages referenced to pin 12; all currents positive into the IC; All parameters are measured in the test circuit (Fig.11) at nominal supply voltage (V_P = 15 V); f = 315 Hz; tape selectors at Fe02 position; normal speed; non-Dolby application; T_{amb} = 25 °C; unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_P	supply voltage range		7.0	–	18.0	V
I_P	supply current	note 1				
		playback mode	35	39	43	mA
		record mode	39	43	47	mA
Playback amplifier (Fe02/Cr02)						
G	gain at normal speed	f = 315 Hz	55	57	59	dB
B	frequency response with respect to gain	f = 30 Hz	10	12	14	dB
		Cr02, f = 10 kHz	−18	−17	−16	dB
		Fe02, f = 10 kHz	−13.5	−12.5	−11.5	dB
	left/right balance		−1	0	+1	dB
	A/B balance		−1	0	+1	dB
G	gain at double speed	f = 630 Hz	49	51	53	dB
B	frequency response with respect to gain	f = 60 Hz	10	12	14	dB
		Cr02; f = 20 kHz	−18	−17	−16	dB
		Fe02; f = 20 kHz	−13.5	−12.5	−11.5	dB
	left/right balance		−1	0	+1	dB
V_O	nominal output voltage	note 2; V_I = 200 μV	–	150	–	mV
THD	total harmonic distortion	V_I = 200 μV	–	0.1	0.3	%
		V_I = 280 μV	–	–	1	%
S/N	signal-to-noise ratio	note 3; weighted curve; 20 Hz to 20 kHz	51	53	–	dB
		weighted curve A(IEC179)	–	60	–	dB
	left/right separation	V_O = 150 mV	40	50	–	dB
SVRR	supply voltage ripple rejection	V_{ripple} = 100 mV; f = 100 Hz	–	25	–	dB
$\|Z_i\|$	input impedance		100	–	–	kΩ
I_{bias}	input bias current		–	0.5	–	μA
V_O	DC output voltage with respect to V_{ref} (V_{1-12} and V_{2-12})		−30	0	+30	mV
	A/B separation	note 4	–	340	–	μV
		note 5	–	tbf	–	mV
	suppression of output signal (channel A and B)	$V_7 = V_P$	–	90	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Record/playback headswitch						
$\|Z_{ON}\|$	impedance ON					
	playback mode	between pins 26 and 25 and pins 24 and 25; I = 100 μA(RMS)	–	35	100	Ω
	record mode	between pins 27 and 25 and pins 23 and 25; I = 1.5 mA(RMS)	–	25	50	Ω
I_{IL}	OFF-state leakage current	voltage on pins 24 and 26 of V_{DC} = ±45 V with respect to V_{ref} (pin 12)	–	1.0	2.5	μA
$\|Z_{ON}\|$	high-speed dubbing headswitch	normal speed, between pins 35 and 36 and pins 36 and 37; I = 100 μA(RMS)	–	100	1000	Ω
Record amplifier (ALC off)						
G	gain at normal speed	f = 315 Hz				
		note 6	13	14	15	dB
		note 7	–	20	–	dB
B	frequency response with respect to gain	f = 10 kHz	8.5	10.0	11.5	dB
		Dolby; f = 10 kHz				
		note 6	13	14	15	dB
		note 7	–	20	–	dB
	left/right balance		−1	0	+1	dB
G	gain at double speed	note 7; f = 630 Hz	19	20	21	dB
B	frequency response with respect to gain	f = 20 kHz	8	10	12	dB
	left/right balance		−1	0	+1	dB
V_O	maximum output voltage	V_{Osel} = 800 mV; f = 1 kHz; THD = 3%	–	4.0	–	V
THD	total harmonic distortion	ALC switch ON; f = 1 kHz				
		V_{Osel} = 1 V	–	–	0.7	%
		V_{Osel} = 3 V	–	0.5	–	%
S/N	signal-to-noise ratio	note 8; weighted curve 20 Hz to 20 kHz	–	60	–	dB
		weighted curve A(IEC179)	–	65	–	dB
		Dolby; weighted curve 20 Hz to 20 kHz	70	73	–	dB
	left/right separation	V_{Osel} = 300 mV	40	50	–	dB
SVRR	supply voltage ripple rejection	V_{ripple} = 100 mV; f = 100 Hz	–	30	–	dB
$\|Z_I\|$	input impedance		100	–	–	kΩ

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Record amplifier (ALC off)						
V_O	DC output voltage with respect to V_{ref}	normal speed record, V_{28-12} and V_{29-12}	−30	0	30	mV
R_L	load impedance on the output		10	–	–	kΩ
$\|Z_O\|$	output impedance	note 9	–	tbf	–	Ω
	suppression of line input	dubbing mode; V_{Osel} = 300 mV	–	tbf	–	dB
		deck B in playback; V_{Osel} = 300 mV	–	tbf	–	dB
Source-selector						
I_{bias}	input bias current		–	15	–	nA
S/N	signal-to-noise ratio	note 10; weighted curve 20 Hz to 20 kHz	77	90	–	dB
		weighted curve A(IEC179)	–	96	–	dB
Automatic Level Control (ALC); see Fig.5						
V_{Iref}	input reference voltage for ALC start operation		–	300	–	mV
V_{Oref}	output reference voltage	ALC switched ON; V_{Osel} = 300 mV	1.35	1.5	1.65	V
ΔV	output voltage variation	V_{Osel} = 330 mV				
		ΔV_{Osel} = 10 dB	–	0.2	1	dB
		ΔV_{Osel} = 20 dB	–	1	–	dB
t_l	limiting time	ΔV_{Osel} = 10 dB	–	1	–	ms
t_s	setting time		–	2	–	ms
t_r	release time		–	10	–	s
Erase and bias oscillator						
f_{OSC}	oscillator frequency	note 11	–	80	–	kHz
$I_{O(p-p)}$	maximum output current pins 16 and 18 (peak-to-peak value)		140	–	–	mA
V_{OSC}	output voltage pins 16 to 17 and pins 17 to 18 (peak-to-peak value)	V_P = 18 V	–	–	36	V
V_{15}	voltage control range	note 12	2.0	–	13.0	V
V_{OSC}	peak output voltage	see Fig.6; $V_{control} = V_P$–8 V between pins 16 and 18	–	8.0	–	V
I_I	input current of control inputs		–	0.1	–	μA
THD	total harmonic distortion between pins 16 and 18	I_O = 80 mA	–	0.5	–	%

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Reference voltage source						
V_{12}	output voltage	note 13; no external load	7.25	7.5	7.75	V
ΔV_{12}	output voltage deviation	ΔI_{ref} = 1 mA	−100	–	+100	mV
Logics inputs (pins 7 to 10); see Figs 7, 8 and 9						
I_7	signal/mute input current	$V_7 = V_P$	–	–	900	µA
V_7	signal/mute input voltage					
		signal	0	–	0.3	V
		mute	6.0	–	15.0	V
I_8	input current for channel A/B selection	$V_8 = V_P$	–	100	150	µA
	input voltage for channel A/B selection					
		deck A	0	–	3.0	V
		mute	5.0	–	10.0	V
		deck B	12.0	–	15.0	V
I_9	input current for tape selection	$V_9 = V_P$	–	–	900	µA
V_9	input voltage for tape selection					
		Cr02	0	–	0.3	V
		Fe02	6.0	–	15.0	V
I_{10}	input current for mode selection	$V_{10} = V_P$	–	100	150	µA
V_{10}	input voltage for mode selection					
		playback	0	–	4.0	V
		record	6.0	–	9.0	V
		high-speed record	11.0	–	15.0	V

Notes to the characteristics

1. The supply current is measured in the test circuit without an additional load of the 1/2 V_P reference voltage source. In the record mode the tape selector is at position Cr02; the oscillator is OFF.
2. The output impedance of the output buffer is typical Z_O = 1 kΩ.
3. The signal-to-noise ratio is related to an output signal V_O = 150 mV with R_S = 1 kΩ. The circuit is switched at normal speed and the tape selector is at position Cr02.
4. Channel A is switched in the playback mode, at deck B a signal of V_I = 200 µV (f = 315 Hz) is applied. The output voltage at the playback amplifier is not measured selectively (bandwidth = 20 Hz to 20 kHz).
5. Deck B is switched in the record mode, at pins 24 and 26 a signal of I_I = 1 mA (f = 80 kHz) is applied.
6. Line input selected, measured relative to source selector output.
7. Switched in dubbing mode, measured relative to line output.
8. The signal-to-noise ratio is related to an output signal V_O = 1.5 V. The circuit is switched at normal speed.
9. Measured with f = 80 kHz and I_I = 1 mA.
10. The signal-to-noise ratio is related to an output signal V_O = 300 mV.
11. The oscillator frequency is determined by L_L and C_L and may be adjusted between 60 kHz and 120 kHz.
12. For stable oscillator operation the control voltage must be greater than 1 V.
13. The output voltage is independent of the operating mode (playback/record).

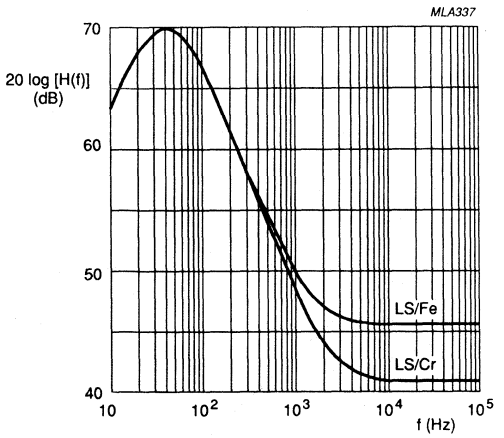


Fig.3 Typical playback frequency response.

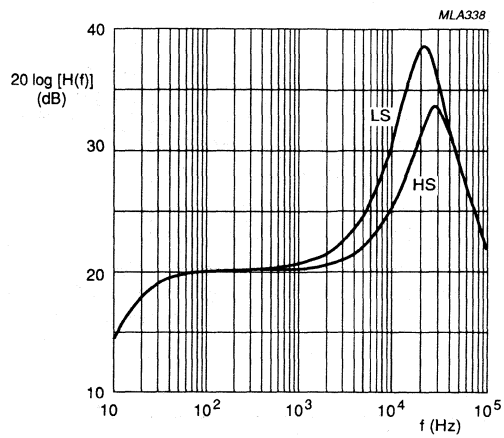


Fig.4 Typical record frequency response.

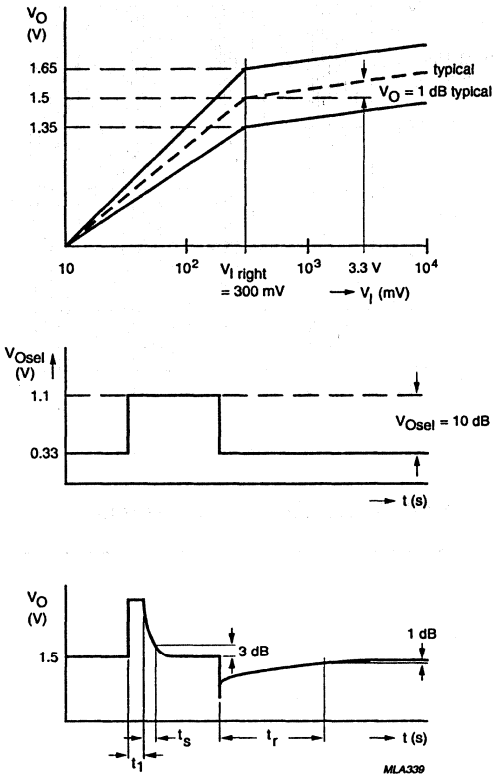


Fig.5 Typical ALC curve.

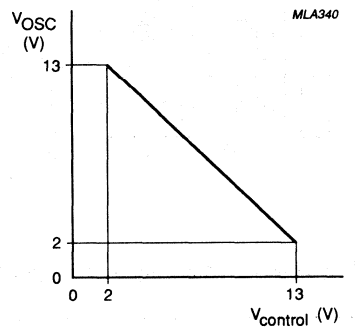


Fig.6 Control voltage/oscillator output voltage (V peak).

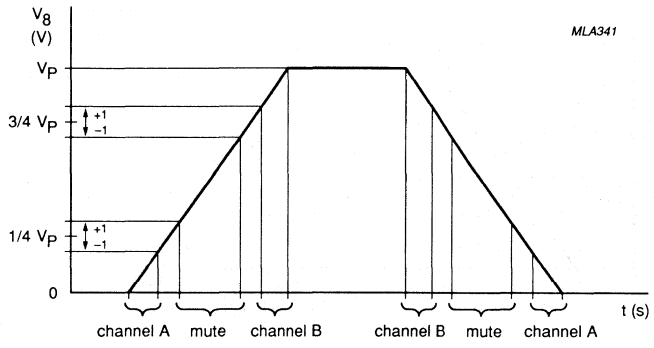
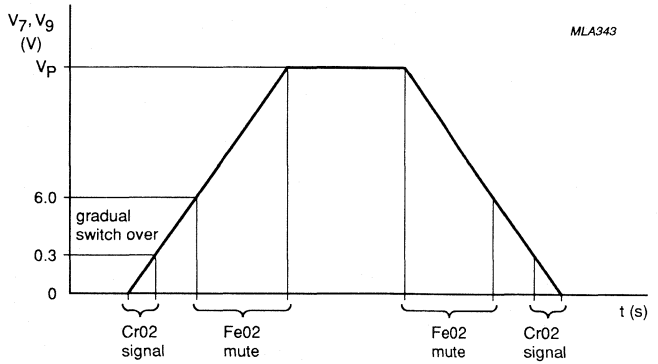


Fig.7 Channel selection input.



Cr02 and Fe02 = pin 9; signal and mute = pin 7

Fig.8 Tape selection input and signal/mute input.

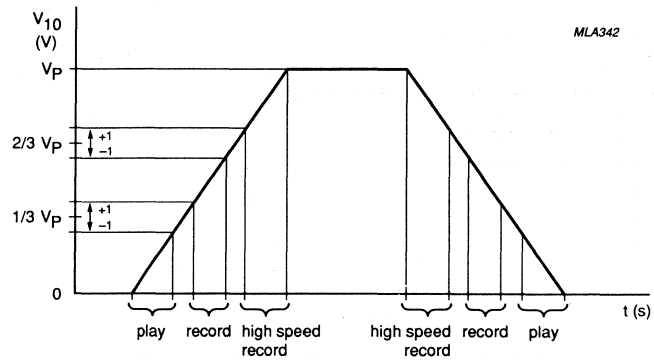


Fig.9 Playback/record/high-speed record selection input.

Table 1 Logic DDPR (S/M input not included)

LOGIC INPUTS A/B	LOGIC INPUTS Fe/CrA	CHANNEL SELECT	R/P SWITCH	HS SWITCH	Fe/Cr PB	PB AMP.	DUB. SWITCH	REC. AMP.	ALC OP.	BIAS OSC.
Playback										
A	Fe	A	P	ON	Fe	ON	mute	OFF	OFF	OFF
A	Cr	A	P	ON	Cr	ON	mute	OFF	OFF	OFF
B	Fe	B	P	ON	Fe	ON	mute	OFF	OFF	OFF
B	Cr	B	P	ON	Cr	ON	mute	OFF	OFF	OFF
Record										
A	Fe	A	R	ON	Fe	ON	dubbing	ON	OFF	ON
A	Cr	A	R	ON	Cr	ON	dubbing	ON	OFF	ON
B	Fe	A	R	ON	Fe	ON	line	ON	ON	ON
B	Cr	A	R	ON	Cr	ON	line	ON	ON	ON
High speed record										
A	Fe	AHS	R	OFF	Fe	ON	dubbing	ON	OFF	ON
A	Cr	AHS	R	OFF	Cr	ON	dubbing	ON	OFF	ON
B	Fe	A	R	ON	Fe	ON	line	ON	ON	ON
B	Cr	A	R	ON	Cr	ON	line	ON	ON	ON

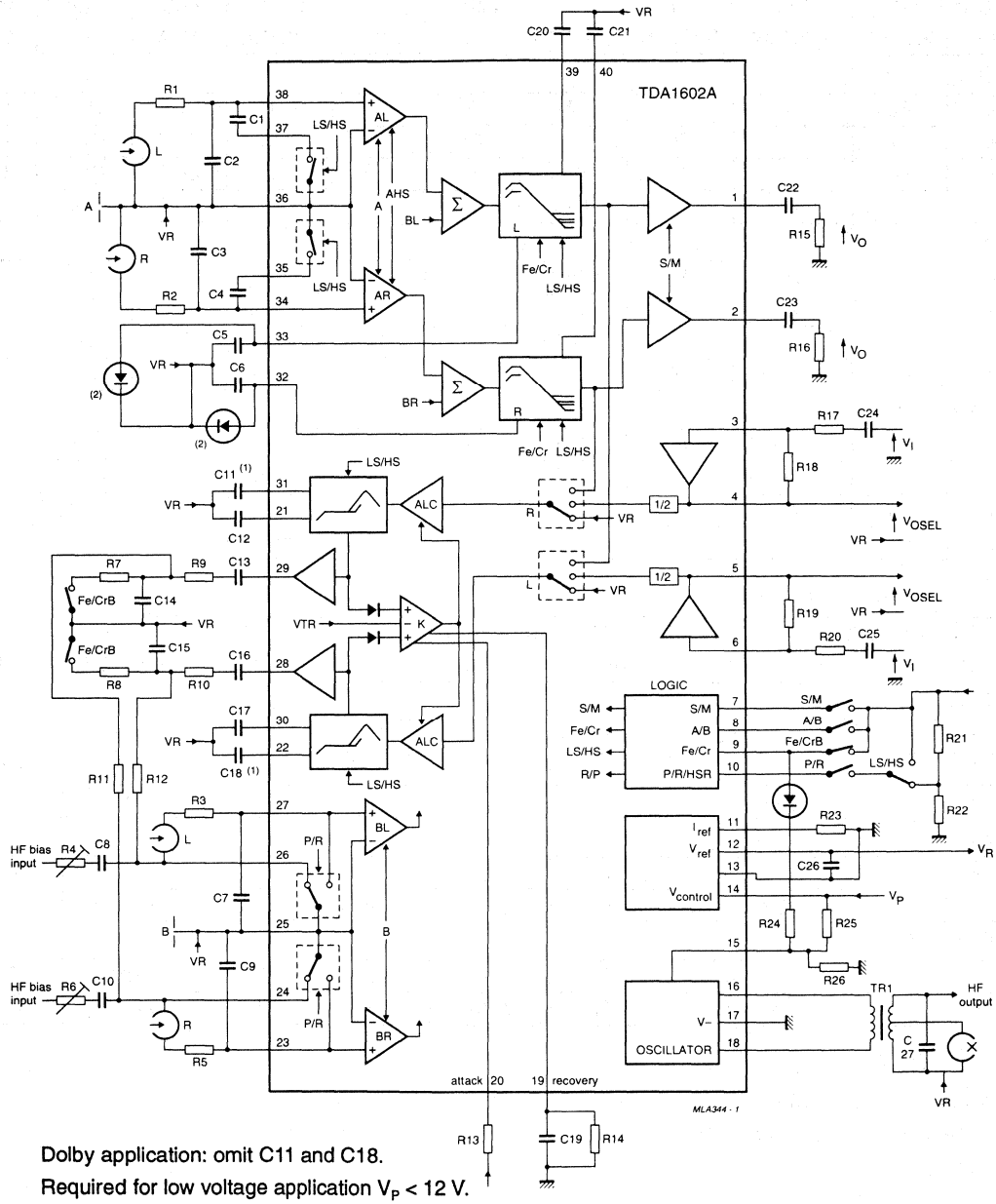
Table 2 Double deck application

DECK SELECT A(P)	DECK SELECT B(R/P)	A/B INPUT	S/M INPUT	CHANNEL SELECT	HS SWITCH	PB AMP.	DUB. SWITCH	ALC OP.
Playback								
$\overline{A}$	$\overline{B}$	don't care	M	A or B	OFF	OFF	mute	OFF
$\overline{A}$	B	B	S	B	OFF	ON	mute	OFF
A	$\overline{B}$	A	S	A	OFF	ON	mute	OFF
Record								
$\overline{A}$	B	B	M (1)	A	OFF	OFF (1)	line	ON
A	B	A	S	A	OFF	ON	dubbing	OFF
High speed record								
$\overline{A}$	B	B	M (1)	A	OFF	OFF (1)	line	ON
A	B	A	M (1)	AHS	ON	OFF (1)	dubbing	OFF

Notes to Table 2

1. Fe/Cr selection not included.
2. S is also possible; play buffer = ON.

APPLICATION INFORMATION



(1) Dolby application: omit C11 and C18.

(2) Required for low voltage application $V_P < 12$ V.

Fig.10 Application diagram.

TEST INFORMATION

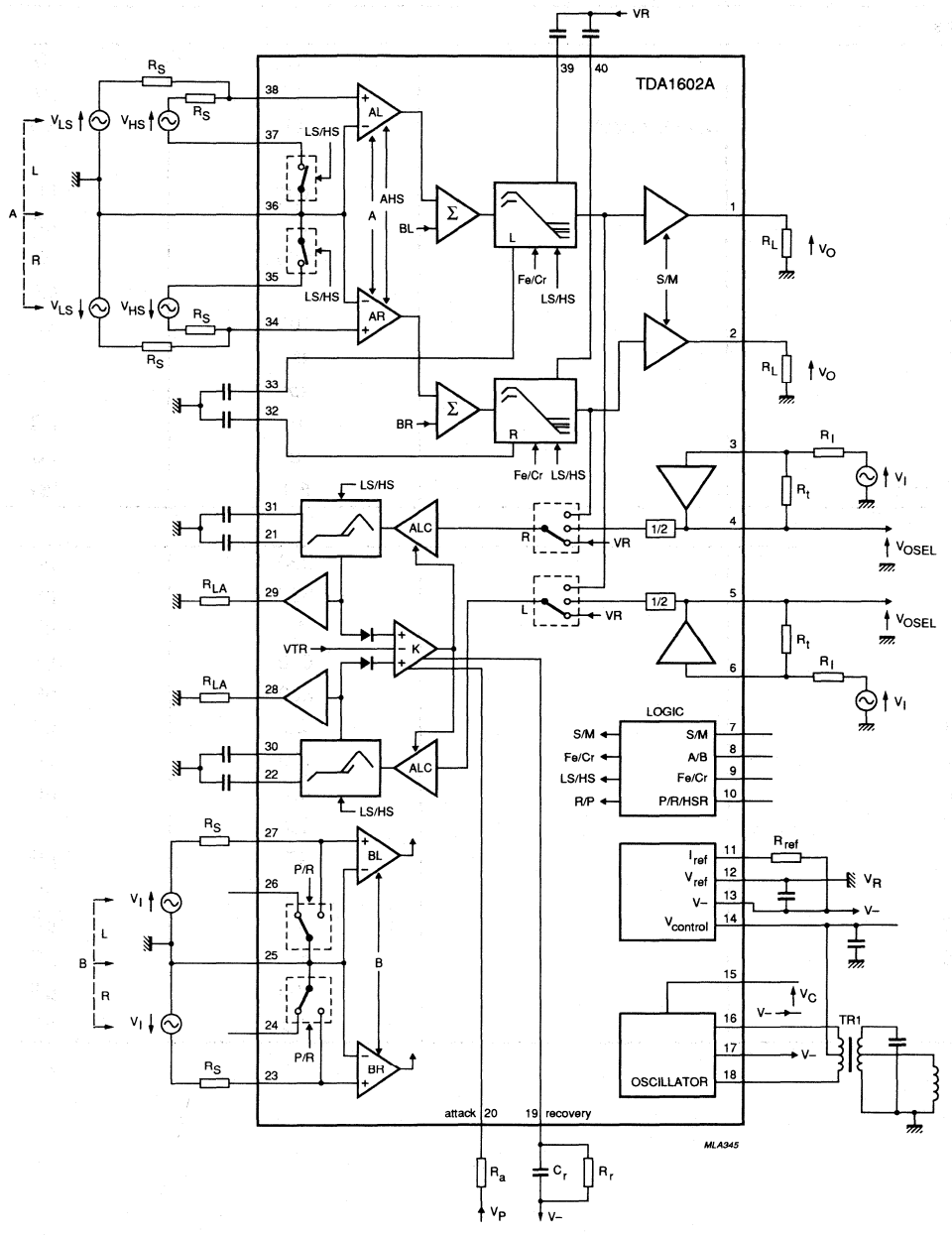


Fig.11 Test circuit diagram.

Table 3 Component values used in the application diagram

COMPONENT	CONDITION	VALUE	UNIT
Resistors			
R1, R2		47	Ω
R3, R5		47	Ω
R4, R6	potentiometer	47	kΩ
R7, R8		tbf	
R9, R10		6.8	kΩ
R11, R12		8.2	kΩ
R13		100	Ω
R14		1	MΩ
R15, R16		100	kΩ
R17, R20		tbf	
R18, R19		tbf	
R21, R22		10	kΩ
R23		2	kΩ
R24, R25, R26		5.1	kΩ
Capacitors			
C1, C4		330	pF
C2, C3		330	pF
C5, C6		47	nF
C7, C9		680	pF
C8, C10		820	pF
C11, C18		68	nF
C12, C17		100	µF
C13, C16		4.7	µF
C14, C15		tbf	
C19		47	µF
C20, C21		100	nF
C22, C23		4.7	µF
C24, C25		4.7	µF
C26		100	µF
C27		3.9	nF

Table 4 Component values used in the test circuit

COMPONENT	CONDITION	VALUE	UNIT
Resistors			
R_S		1	kΩ
R_L		100	kΩ
R_{LA}		10	kΩ
R_I		4.7	kΩ
R_t		22.6	kΩ
R_{ref}		2	kΩ
R_a		1	kΩ
R_r		3.3	MΩ
Capacitors			
C_r		1	μF

5 W AUDIO POWER AMPLIFIER

The TDA2611A is a monolithic integrated circuit in a 9-lead single in-line (SIL) plastic package with a high supply voltage audio amplifier. Special features are:

- **possibility for increasing the input impedance**
- single in-line (SIL) construction for easy mounting
- very suitable for application in mains-fed apparatus
- extremely low number of external components
- thermal protection
- well defined open loop gain circuitry with simple quiescent current setting and fixed integrated closed loop gain

QUICK REFERENCE DATA

Supply voltage range	V_P		6 to 35	V
Repetitive peak output current	I_{ORM}	<	1,5	A
Output power at d_{tot} = 10%				
V_P = 18 V; R_L = 8 Ω	P_o	typ.	4,5	W
V_P = 25 V; R_L = 15 Ω	P_o	typ.	5	W
Total harmonic distortion at P_o < 2 W; R_L = 8 Ω	d_{tot}	typ.	0,3	%
Input impedance	$\lvert Z_i \rvert$	typ.	45	kΩ
Total quiescent current at V_P = 18 V	I_{tot}	typ.	25	mA
Sensitivity for P_o = 2,5 W; R_L = 8 Ω	V_i	typ.	55	mV
Operating ambient temperature	T_{amb}		−25 to + 150	°C
Storage temperature	T_{stg}		−55 to + 150	°C

PACKAGE OUTLINE

9-lead SIL; plastic (SOT110B).

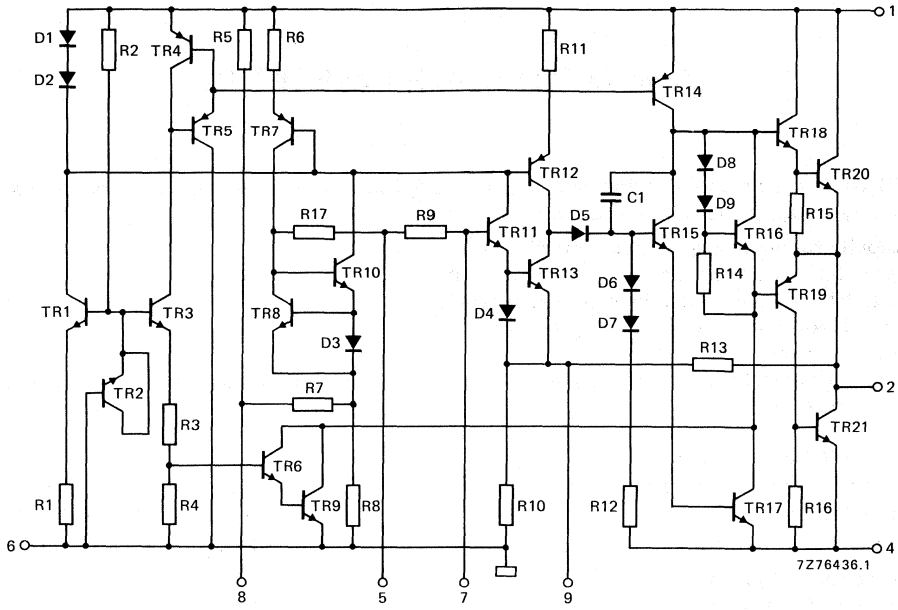


Fig. 1 Circuit diagram; pin 3 not connected.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	35 V
Non-repetitive peak output current	I_{OSM}	max.	3 A
Repetitive peak output current	I_{ORM}	max.	1,5 A
Total power dissipation	see derating curves Fig. 2		
Storage temperature	T_{stg}		−55 to + 150 °C
Operating ambient temperature	T_{amb}		−25 to + 150 °C

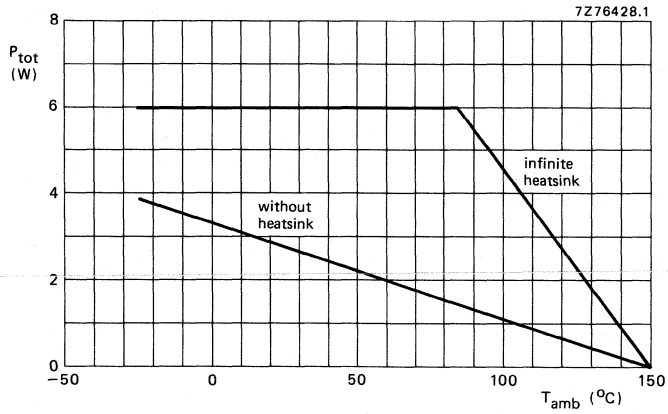


Fig. 2 Power derating curves.

HEATSINK EXAMPLE

Assume V_P = 18 V; R_L = 8 Ω; T_{amb} = 60 °C maximum; T_j = 150 °C (max. for a 4 W application into an 8 Ω load, the maximum dissipation is about 2,2 W).
The thermal resistance from junction to ambient can be expressed as:

$$R_{th\ j\text{-}a} = R_{th\ j\text{-}tab} + R_{th\ tab\text{-}h} + R_{th\ h\text{-}a} = \frac{150 - 60}{2,2} = 41\ K/W.$$

Since $R_{th\ j\text{-}tab}$ = 11 K/W and $R_{th\ tab\text{-}h}$ = 1 K/W, $R_{th\ h\text{-}a}$ = 41 − (11 + 1) = 29 K/W.

D.C. CHARACTERISTICS

Supply voltage range	V_P		6 to 35 V
Repetitive peak output current	I_{ORM}	<	1,5 A
Total quiescent current at V_P = 18 V	I_{tot}	typ.	25 mA

A.C. CHARACTERISTICS

T_{amb} = 25 °C; V_P = 18 V; R_L = 8 Ω; f = 1 kHz unless otherwise specified; see also Fig. 3

A.F. output power at d_{tot} = 10%			
V_P = 18 V; R_L = 8 Ω	P_o	>	4 W
		typ.	4,5 W
V_P = 12 V; R_L = 8 Ω	P_o	typ.	1,7 W
V_P = 8,3 V; R_L = 8 Ω	P_o	typ.	0,65 W
V_P = 20 V; R_L = 8 Ω	P_o	typ.	6 W
V_P = 25 V; R_L = 15 Ω	P_o	typ.	5 W
Total harmonic distortion at P_o = 2 W	d_{tot}	typ.	0,3 %
		<	1 %
Frequency response		>	15 kHz
Input impedance	$\|Z_i\|$	typ.	45 kΩ *
Noise output voltage at R_S = 5 kΩ; B = 60 Hz to 15 kHz	V_n	typ.	0,2 mV
		<	0,5 mV
Sensitivity for P_o = 2,5 W	V_i	typ.	55 mV
			44 to 66 mV

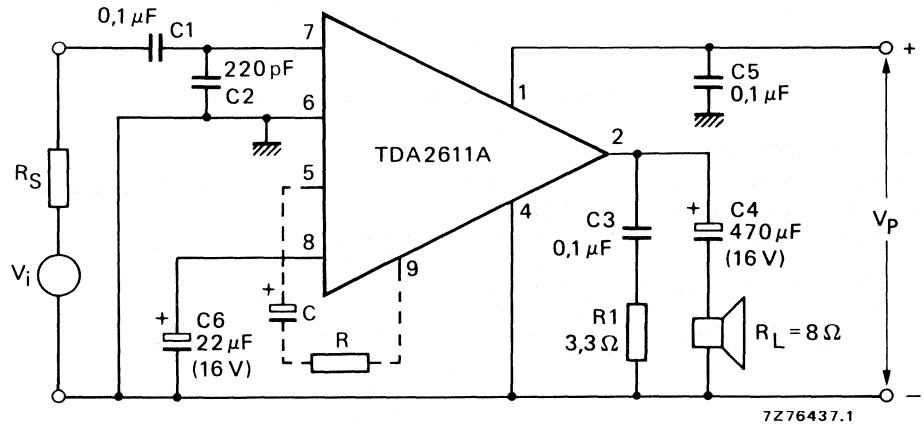


Fig. 3 Test circuit; pin 3 not connected.

* Input impedance can be increased by applying C and R between pins 5 and 9 (see also Figures 6 and 7).

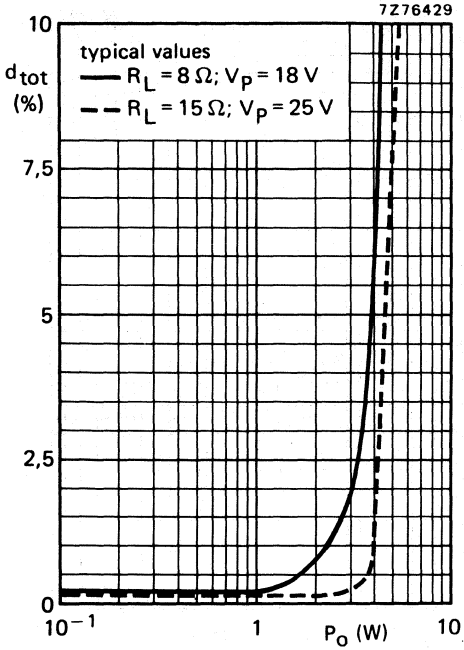


Fig. 4 Total harmonic distortion as a function of output power.

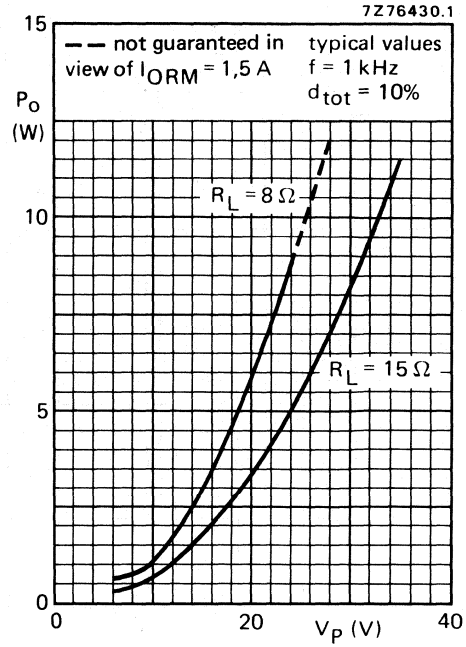


Fig. 5 Output power as a function of supply voltage.

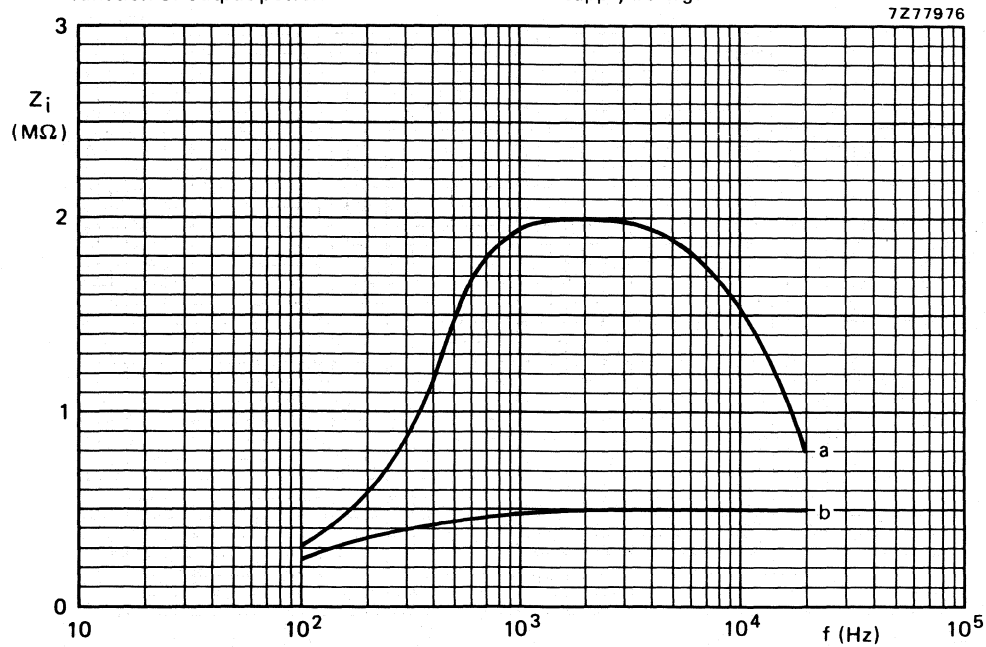


Fig. 6 Input impedance as a function of frequency; curve a for C = 1 μF, R = 0 Ω; curve b for C = 1 μF, R = 1 kΩ; circuit of Fig. 3; C2 = 10 pF; typical values.

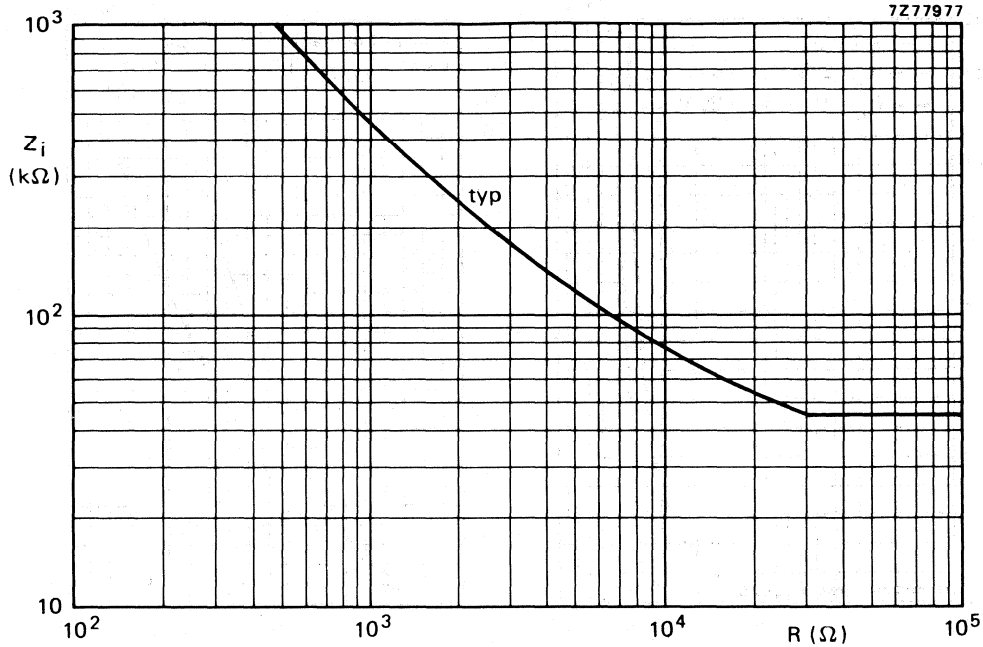


Fig. 7 Input impedance as a function of R in circuit of Fig. 3; C = 1 μF; f = 1 kHz.

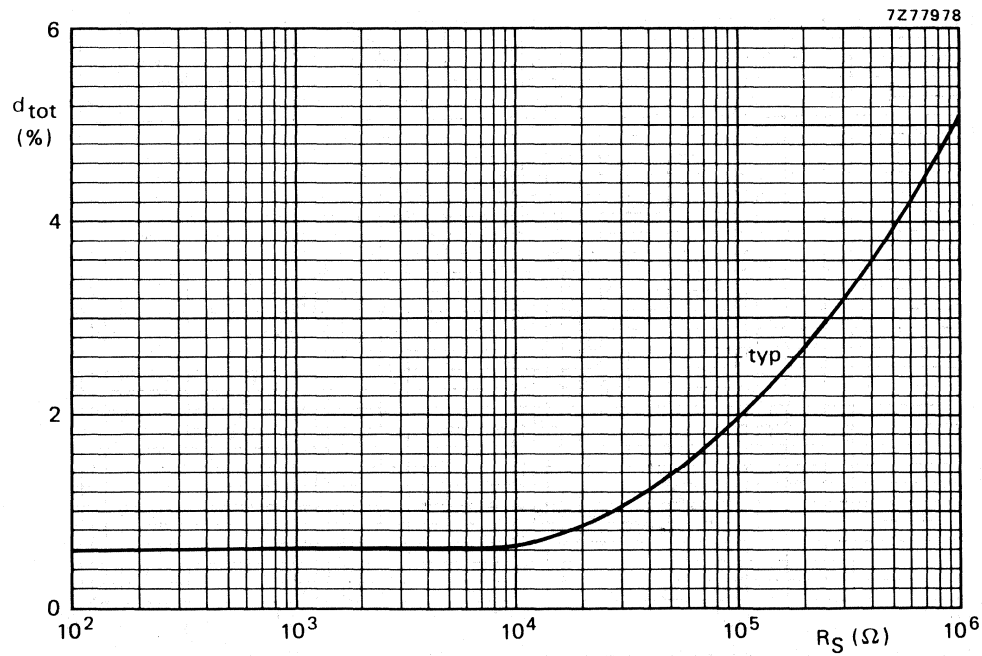


Fig. 8 Total harmonic distortion as a function of R_S in the circuit of Fig. 3; P_o = 3,5 W; f = 1 kHz.

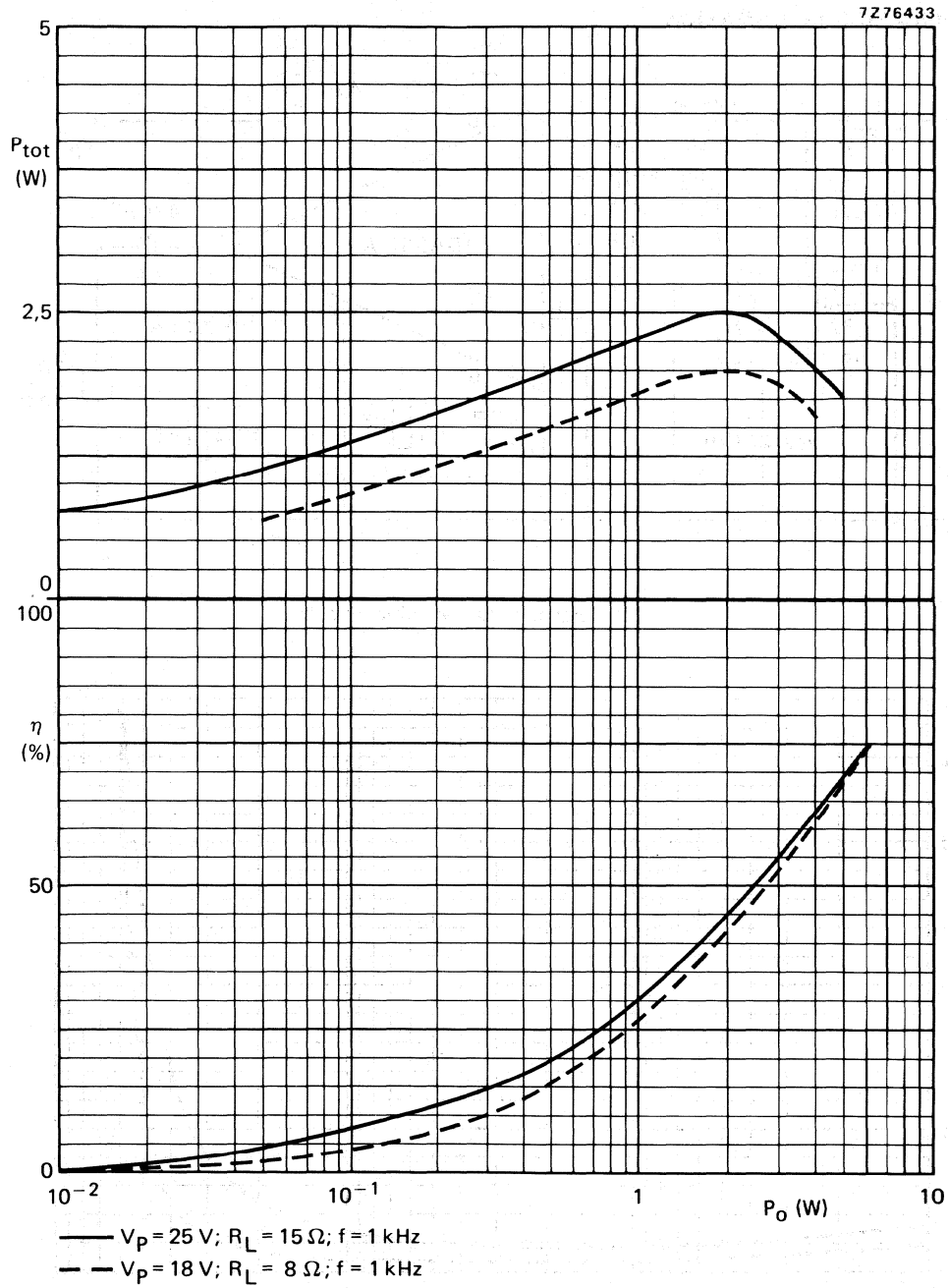


Fig. 9 Total power dissipation and efficiency as a function of output power.

APPLICATION INFORMATION

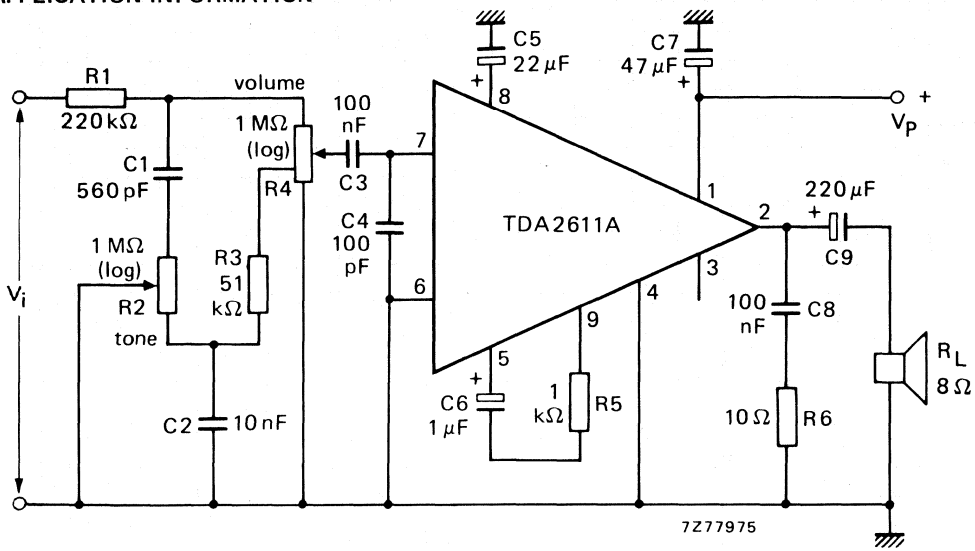


Fig. 10 Ceramic pickup amplifier circuit.

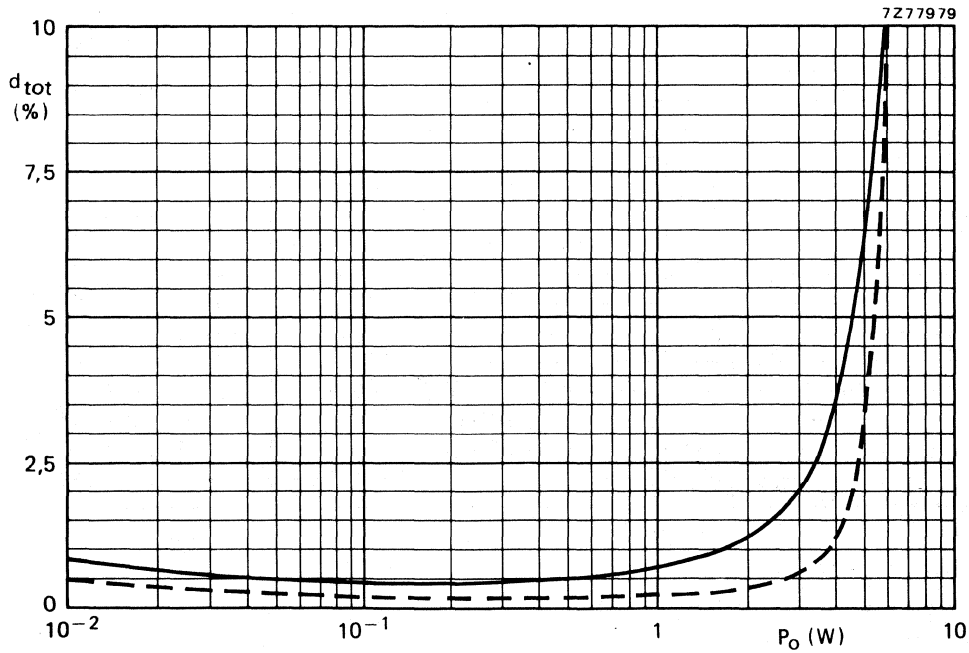


Fig. 11 Total harmonic distortion as a function of output power; —— with tone control; – – – without tone control; in circuit of Fig. 10; typical values.

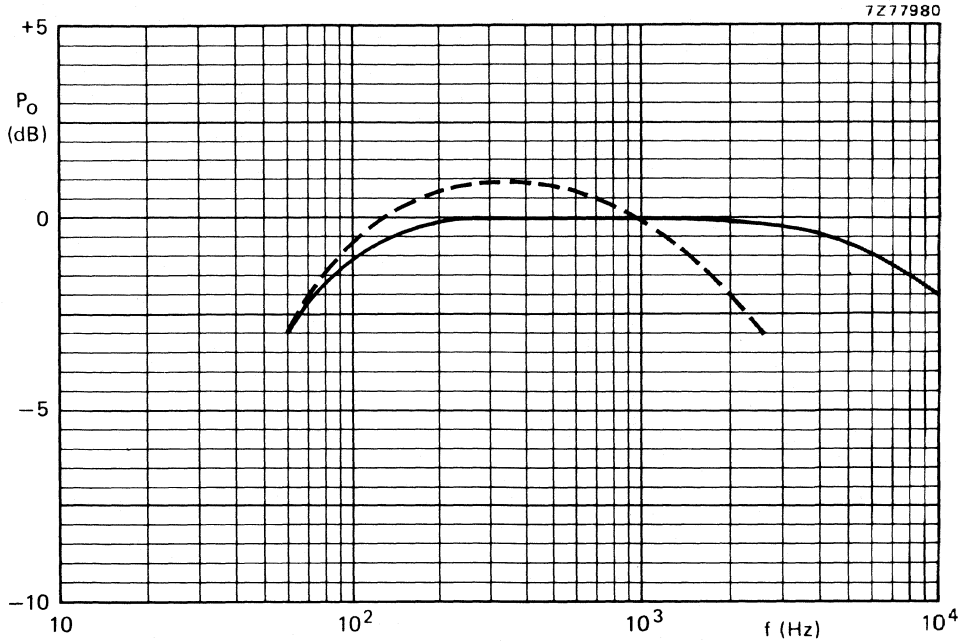


Fig. 12 Frequency characteristics of the circuit of Fig. 10; —— tone control max. high; – – – tone control min. high; P_O relative to 0 dB = 3 W; typical values.

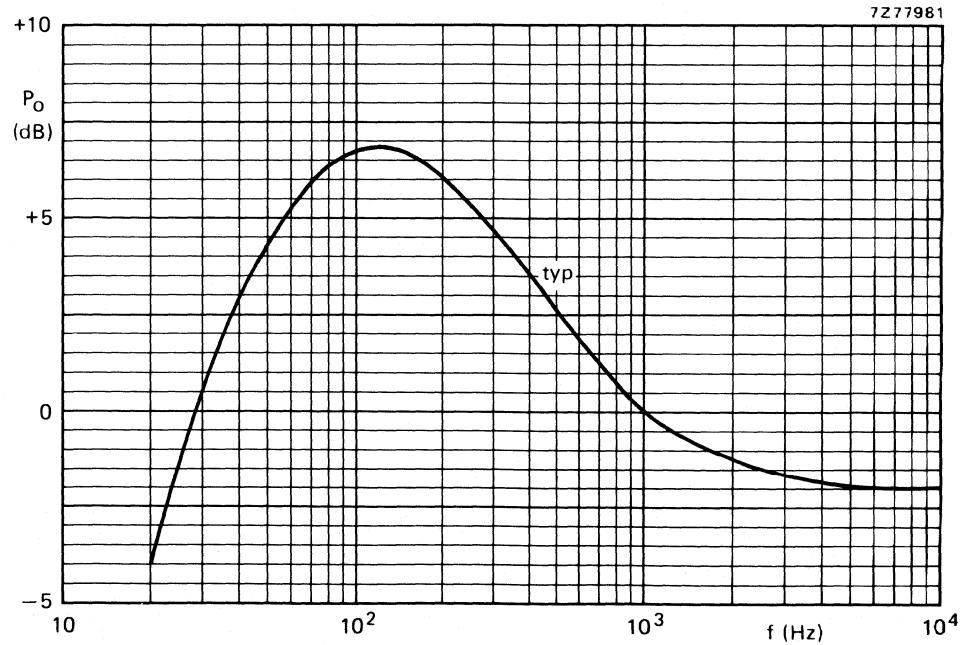


Fig. 13 Frequency characteristic of the circuit of Fig. 10; volume control at the top; tone control max. high.

6 W HI-FI AUDIO POWER AMPLIFIER

GENERAL DESCRIPTION

The TDA2613 is a hi-fi audio power amplifier encapsulated in a 9-lead SIL plastic power package. The device is especially designed for mains fed applications (e.g. tv and radio).

Features

- Requires very few external components
- Input muted during power-on and off (no switch-on or switch-off clicks)
- Low offset voltage between output and ground
- Hi-fi according to IEC 268 and DIN 45500
- Short-circuit-proof
- Thermally protected

QUICK REFERENCE DATA

Supply voltage range	V_P		15 to 42 V
Output power at THD = 0,5%, V_P = 24 V	P_O	typ.	6 W
Voltage gain	G_V	typ.	30 dB
Supply voltage ripple rejection	SVRR	typ.	60 dB
Noise output voltage	$V_{no(rms)}$	typ.	70 μV

PACKAGE OUTLINE

TDA2613: 9-lead SIL; plastic power (SOT110B).

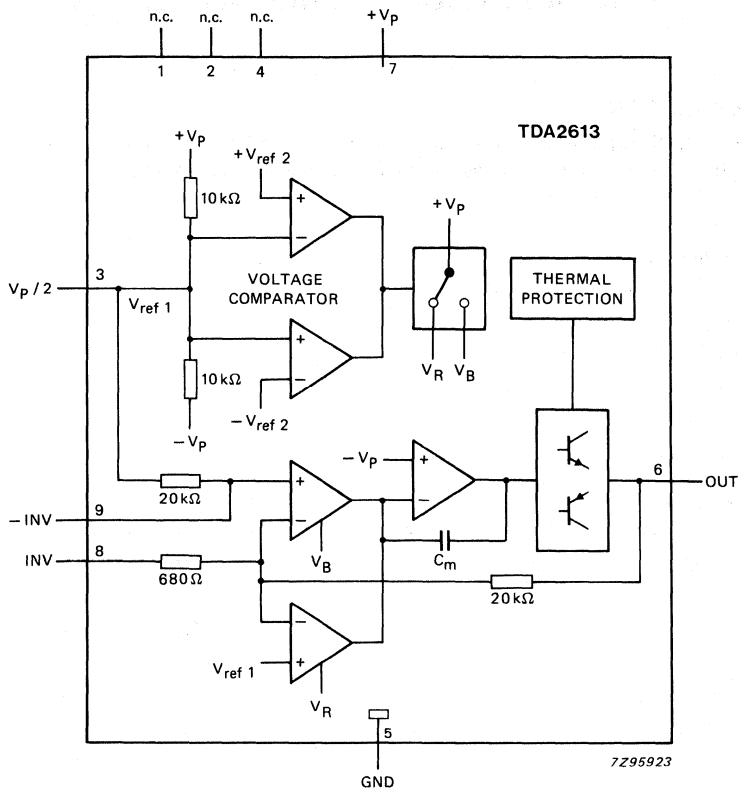


Fig. 1 Block diagram.

PINNING

1.	n.c.	not connected
2.	n.c.	not connected
3.	$V_P/2$	½ V_P (asymmetrical) or ground (symmetrical)
4.	n.c.	not connected
5.	GND	ground (asymmetrical) or negative supply (symmetrical)
6.	OUT	output
7.	+Vp	positive supply
8.	INV	inverting input
9.	−INV	non-inverting input

FUNCTIONAL DESCRIPTION

This hi-fi power amplifier is designed for mains fed applications. The device is intended for asymmetrical power supplies, but a symmetrical supply may also be used. An output power of 6 watts (THD = 0,5%) can be delivered into an 8 Ω load with an asymmetrical power supply of 24 V.

The gain is fixed internally at 30 dB. Internal gain fixing gives low gain spread.

A special feature of this device is a mute circuit which suppresses unwanted input signals during switching on and off. Referring to Fig. 4, the 100 μF capacitor creates a time delay when the voltage at pin 3 is lower than an internally fixed reference voltage. During the delay the amplifier remains in the DC operating mode but is isolated from the non-inverting input on pin 9.

Two thermal protection circuits are provided, one monitors the average junction temperature and the other the instantaneous temperature of the power transistors. Both protection circuits activate at 150 °C allowing safe operation to a maximum junction temperature of 150 °C without added distortion.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage		V_P	–	42	V
Non-repetitive peak output current		I_{OSM}	–	4	A
Total power dissipation	see Fig. 2	P_{tot}			
Storage temperature range		T_{stg}	–55	+ 150	°C
Junction temperature		T_j	–	150	°C
Short-circuit time: outputs short-circuited to ground (full signal drive)	see note	t_{sc}	–	1	hour

Note to the Ratings

For asymmetrical power supplies (at short-circuiting of the load) the maximum supply voltage is limited to V_P = 28 V. If the total internal resistance of the supply (R_S) ⩾ 4 Ω, the maximum unloaded supply voltage is increased to 32 V. For symmetrical power supplies the circuit is short-circuit proof to V_P = ± 21 V.

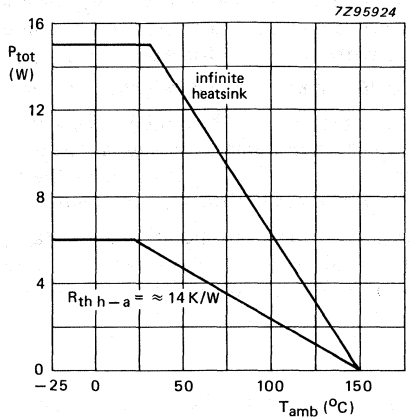


Fig. 2 Power derating curve.

THERMAL RESISTANCE

From junction to case $R_{th\ j\text{-}c} = 8$ K/W

HEATSINK DESIGN EXAMPLE

With derating of 8 K/W, the value of heatsink thermal resistance is calculated as follows:

given $R_L = 8\ \Omega$ and $V_P = 24$ V, the measured maximum dissipation is 4,1 W; then, for a maximum ambient temperature of 60 °C, the required thermal resistance of the heatsink is:

$$R_{th\ h\text{-}a} = \frac{150 - 60}{4{,}1} - 8 \approx 14\ \text{K/W}$$

Note: The metal tab (heatsink) has the same potential as pin 5 (GND).

CHARACTERISTICS

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage range						
operating mode		V_P	15	24	42	V
input mute mode		V_P	4	–	10	V
Repetitive peak output current		I_{ORM}	2.2	–	–	A
Operating mode: asymmetrical power supply; test circuit as per Fig. 4; V_P = 24 V; R_L = 8 Ω; T_{amb} = 25 °C; f = 1 kHz						
Total quiescent current		I_{tot}	10	20	35	mA
Output power	THD = 0,5%	P_o	5	6	–	W
	THD = 10%	P_o	6,5	8,0	–	W
Total harmonic distortion	P_o = 4 W	THD	–	0,15	0,2	%
Power bandwidth	THD = 0,5%; note 1	B	–	20 to 16 k	–	Hz
Voltage gain		G_v	29	30	31	dB
Noise output voltage (r.m.s. value); unweighted (20 Hz to 20 kHz)	R_S = 2 kΩ	$V_{no(rms)}$	–	70	140	μV
Input impedance		$\|Z_i\|$	14	20	26	kΩ
Supply voltage ripple rejection	note 2	SVRR	35	44	–	dB
Input bias current		I_{ib}	–	0,3	–	μA
DC output offset voltage	with respect to $V_P/2$	V_{os}	–	30	200	mV
Input mute mode: asymmetrical power supply; test circuit as per Fig. 4; V_P = 8 V; R_L = 8 Ω; T_{amb} = 25 °C; f = 1 kHz						
Total quiescent current		I_{tot}	5	15	20	mA
Output voltage	V_i = 600 mV	V_{out}	–	2,0	2,8	mV
Noise output voltage (r.m.s. value); unweighted (20 Hz to 20 kHz)	R_S = 2 kΩ	$V_{no(rms)}$	–	70	140	μV
Supply voltage ripple rejection	note 2	SVRR	35	55	–	dB
DC output offset voltage	with respect to $V_P/2$	V_{os}	–	40	200	mV

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Operating mode: symmetrical power supply; test circuit as per Fig. 3; $V_P = \pm 12$ V; $R_L = 8\ \Omega$; $T_{amb} = 25\ ^oC$; f = 1 kHz						
Total quiescent current		I_{tot}	10	20	35	mA
Output power	THD = 0,5%	P_o	5	6	–	W
	THD = 10%	P_o	6,5	8,5	–	W
Total harmonic distortion	$P_o = 4$ W	THD	–	0,13	0,2	%
Power bandwidth	THD = 0,5% note 1	B	–	40 to 16 k	–	Hz
Voltage gain		G_v	29	30	31	dB
Noise output voltage (r.m.s. value); unweighted (20 Hz to 20 kHz)	$R_S = 2\ k\Omega$	$V_{no(rms)}$	–	70	140	μV
Input impedance		$\|Z_i\|$	14	20	26	$k\Omega$
Supply voltage ripple rejection		SVRR	40	60	–	dB
DC output offset voltage	with respect to ground	V_{os}	–	30	200	mV

Notes to the characteristics

1. Power bandwidth at $P_{o\ max}$ –3 dB.
2. Ripple rejection at $R_S = 0\ \Omega$, f = 100 Hz to 20 kHz; ripple voltage = 200 mV (r.m.s. value) applied to positive or negative supply rail.

APPLICATION INFORMATION

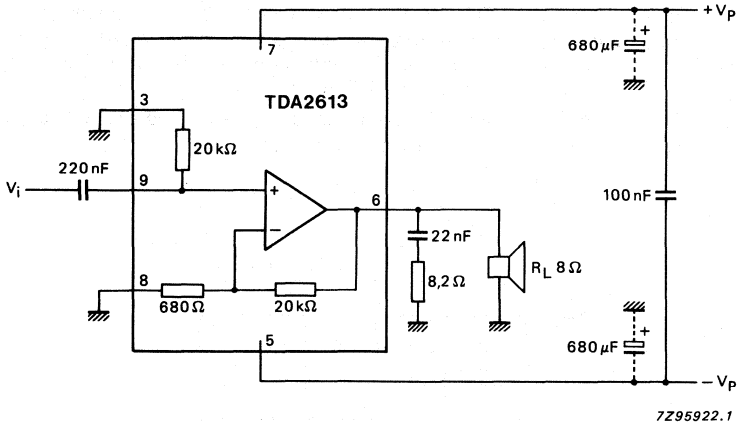


Fig. 3 Test and application circuit; symmetrical power supply.

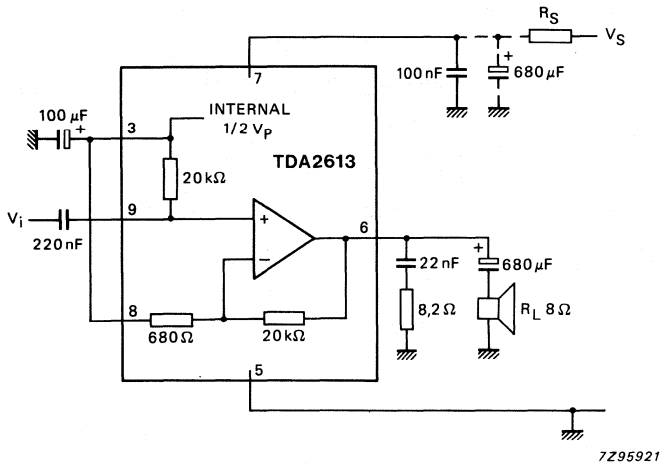


Fig. 4 Test and application circuit; asymmetrical power supply.

APPLICATION INFORMATION (continued)

Input mute circuit

The input mute circuit operates only during switching on and off of the supply voltage. The circuit compares the ½ supply voltage (at pin 3) with an internally fixed reference voltage (V_{ref}), derived directly from the supply voltage. When the voltage at pin 3 is lower than V_{ref} the non-inverting input (pin 9) is disconnected from the amplifier. The voltage at pin 3 is determined by an internal voltage divider and the external 100 μF capacitor.
During switching on, a time delay is created between the reference voltage and the voltage at pin 3, during which the input terminal is disconnected, (as illustrated in Fig. 5).

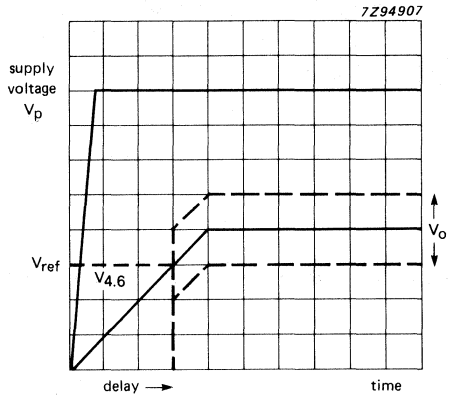


Fig. 5 Input mute circuit; time delay.

6 W hi-fi audio power amplifier TDA2614

FEATURES

- Requires very few external components
- No switch-on/switch-off clicks
- Input mute during switch-on and switch-off
- Low offset voltage between output and ground
- Hi-fi in accordance with IEC 268 and DIN 45500
- Short-circuit proof and thermal protected
- Mute possibility.

GENERAL DESCRIPTION

The TDA2614 is a power amplifier in a 9-lead single-in-line (SIL9) plastic medium power package. It has been especially designed for mains fed applications, such as TV and radio.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	positive supply voltage range		15	–	42	V
P_O	output power	V_S = 24 V; THD = 0.5%	–	6.5	–	W
G_v	internal voltage gain		–	30	–	dB
SVRR	supply voltage ripple rejection		–	45	–	dB
V_{no}	noise output voltage		–	70	–	μV

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA2614	9	SIL	plastic	SOT110

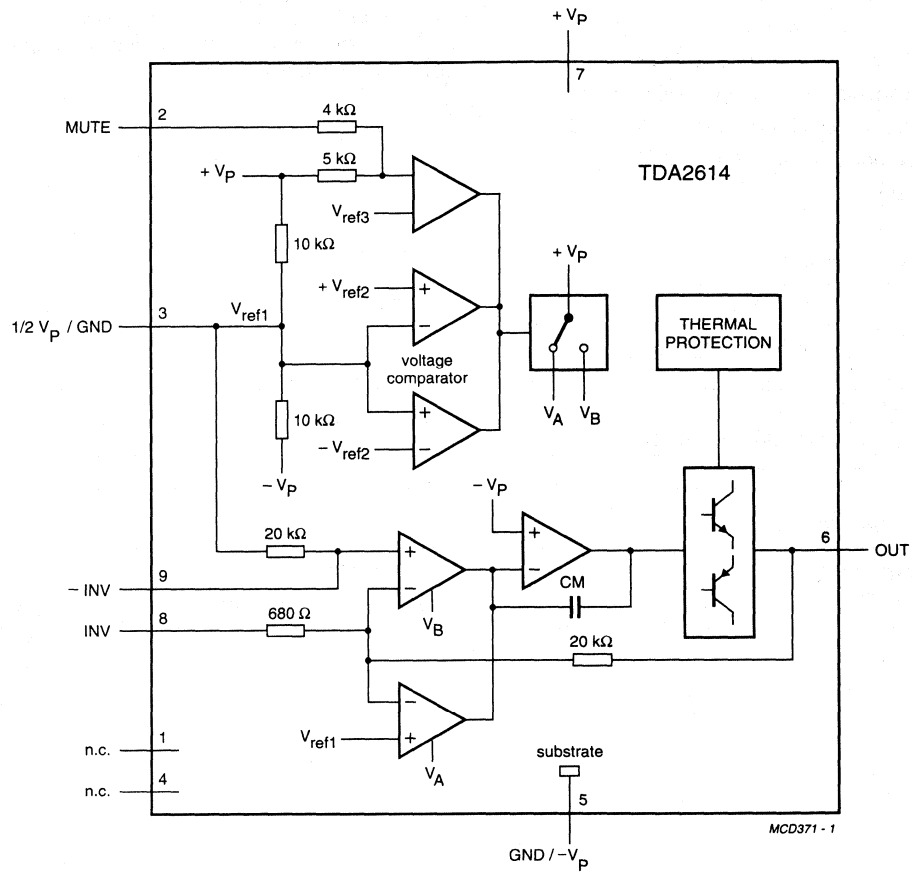


Fig.1 Block diagram.

6 W hi-fi audio power amplifier TDA2614

PINNING

SYMBOL	PIN	DESCRIPTION
n.c.	1	not connected
MUTE	2	mute input
$1/2V_P$/GND	3	1/2 supply (or ground at symmetrical power supplies)
n.c.	4	not connected
GND/$-V_P$	5	ground (or negative supply rail at symmetrical power supplies)
OUT	6	output
V_P	7	supply voltage
INV	8	inverting input
–INV	9	non-inverting input

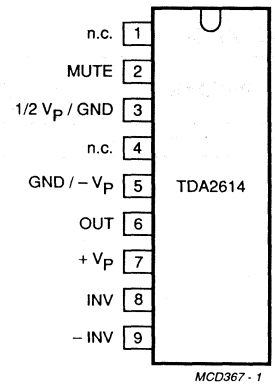


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The TDA2614 is a hi-fi power amplifier designed for mains fed applications, such as radio and TV. The circuit is optimally designed for asymmetrical power supplies, but is also well-suited to symmetrical power supply systems.

An output power of 6 W (THD = 0.5%) can be delivered into an 8 Ω load with a supply of 24 V. The gain is internally fixed at 30 dB, thus offering a low gain spread.

A special feature is the input mute circuit. This circuit disconnects the non-inverting input when the supply voltage drops below 10 V, while the amplifier still retains its DC operating adjustment. The circuit features suppression of unwanted signals at the input, during switch-on and switch-off.

The mute circuit can also be activated via pin 2. When a current of 300 μA is present at pin 2, the circuit is in the mute condition.

The device is provided with two thermal protection circuits. One circuit measures the average temperature of the crystal and the other measures the momentary temperature of the power transistors. These control circuits attack at temperatures in excess of 150 °C, so a crystal operating temperature of max. 150 °C can be used without extra distortion.

With the derating value of 8 K/W, the heatsink can be calculated as follows:

at $R_L = 8\ \Omega$ and $V_S = 24$ V, dissipation is 4.1 W.

With a maximum ambient temperature of 60 °C, the thermal resistance of the heatsink is:

$$R_{th} = \frac{150 - 60}{4.1} - 8 = 14 \text{ K/W}.$$

LIMITING VALUES

In accordance with the Absolute maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_P	positive supply voltage		–	42	V
I_{OSM}	non-repetitive peak output current		–	4	A
P_{tot}	total power dissipation	see Fig.3	–	15	W
T_{stg}	storage temperature range		−55	+150	°C
T_{XTAL}	crystal temperature		–	+150	°C
T_{amb}	ambient operating temperature range		−25	+150	°C
t_{sc}	short circuit time	short circuit to ground; note 1	–	1	h

Note to the limiting values

1. For asymmetrical power supplies (with the load short-circuited), the maximum unloaded supply voltage is limited to V_P = 28 V, and with an internal supply resistance of $R_S \geq 4\ \Omega$, the maximum unloaded supply voltage is limited to 32 V (with the load short-circuited). For symmetrical power supplies, the circuit is short-circuit-proof up to V_P = ±21 V.

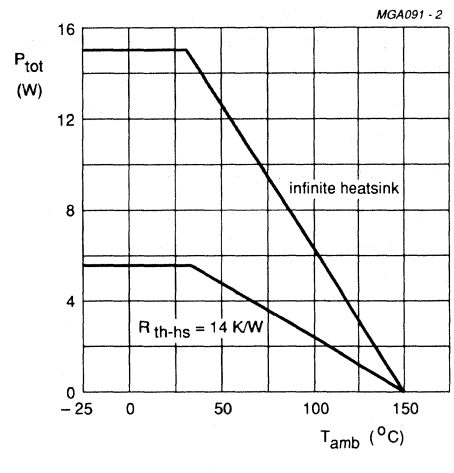


Fig.3 Power derating curve.

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}c}$	from junction to case	8 K/W

CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_P	supply voltage range		–	24	42	V
I_{ORM}	repetitive peak output current		–	2.2	–	A
Operating position; note 1						
V_P	supply voltage range		15	24	42	V
I_P	total quiescent current		10	20	35	mA
P_O	output power					
		THD = 0.5%	5	6.5	–	W
		THD = 10%	6.5	8.5	–	W
		THD = 0.5%; R_L = 4 Ω	–	10	–	W
		THD = 10%; R_L = 4 Ω	–	14	–	W
THD	total harmonic distortion	P_O = 4 W	–	0.15	0.2	%
B	power bandwidth	THD = 0.5%; note 2	–	30 to 20 000	–	Hz
G_v	voltage gain		29	30	31	dB
$\lvert\Delta V_{3\text{-}6}\rvert$	DC output offset voltage		–	30	200	mV
V_{no}	noise output voltage	note 3	–	70	140	μV
$\lvert Z_i\rvert$	input impedance		14	20	26	kΩ
SVRR	supply voltage ripple rejection	note 4	35	45	–	dB
I_{bias}	input bias current		–	0.3	–	μA
MUTE POSITION (AT $I_{MUTE} \geq 300$ μA)						
V_O	output voltage	V_I = 600 mV	–	0.1	1.0	mV
$Z_{2\text{-}7}$	mute input impedance		–	9	–	kΩ
I_P	total quiescent current		10	20	35	mA
V_{no}	noise output voltage	note 3	–	70	140	μV
SVRR	supply voltage ripple rejection	note 4	35	44	–	dB
$\lvert\Delta V_{3\text{-}6}\rvert$	DC output offset voltage		–	40	200	mV
$\lvert\Delta V_{off}\rvert$	offset voltage with respect to operating position		–	4	150	mV
I_2	current if pin 2 is connected to pin 5		–	–	6	mA
Mute position; note 5						
V_P	positive supply voltage range		4	–	10	V
I_P	total quiescent current	$R_L = \delta$	5	15	20	mA
V_O	output voltage	V_I = 600 mV	–	0.1	1.0	mV
V_{no}	noise output voltage	note 3	–	70	140	μV
SVRR	supply voltage ripple rejection	note 4	35	44	–	dB
$\lvert\Delta V_{3\text{-}6}\rvert$	DC output offset voltage		–	40	200	mV

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Operating position; note 6						
$\pm V_P$	supply voltage range		7.5	12	21	V
I_P	total quiescent current		10	20	35	mA
P_O	output power					
		THD = 0.5%	5	6.5	–	W
		THD = 10%	6.5	8	–	W
THD	total harmonic distortion	P_o = 4 W	–	0.13	0.2	%
B	power bandwidth	THD = 0.5%; note 2	–	40 to 20 000	–	Hz
G_v	voltage gain		29	30	31	dB
V_{no}	noise output voltage	note 3	–	70	140	μV
$\|Z_i\|$	input impedance		14	20	26	kΩ
SVRR	supply voltage ripple rejection		40	55	–	dB
I_{bias}	input bias current		–	0.3	–	μA
$\|V_{GND}\|$	DC output offset voltage		–	30	200	mV
MUTE POSITION (AT $I_{MUTE} \geq 300$ μA)						
V_O	output voltage	V_I = 600 mV	–	0.1	1.0	mV
Z_{2-7}	mute input impedance	note 7	6.7	9	11.3	kΩ
I_P	total quiescent current	$R_L = \infty$	10	20	35	mA
V_{no}	noise output voltage	note 3	–	70	140	μV
SVRR	supply voltage ripple rejection	note 4	40	55	–	dB
$\|\Delta V_{GND}\|$	DC output offset voltage		–	40	200	mV
$\|\Delta V_{off}\|$	offset voltage with respect to operating position		–	4	150	mV
I_2	current if pin 2 is connected to pin 5		–	–	6	mA

Notes to the characteristics

1. V_P = 24 V; R_L = 8 Ω; T_{amb} = 25 °C; f = 1 kHz; asymmetrical power supply I_{MUTE} < 30 μA. See Fig.5
2. The power bandwidth is measured at an output power of $P_{O\ max}$ – 3 dB.
3. The noise output voltage (RMS value) is measured at R_S = 2 kΩ, unweighted (20 Hz to 20 kHz).
4. The ripple rejection is measured at R_S = 0 and f = 100 Hz to 20 kHz, at a ripple voltage of 200 mV. With symmetrical power supplies, the ripple (200 mV) is applied in phase to the positive and the negative supply rails. With asymmetrical power supplies, the ripple rejection is measured at f = 1 kHz.
5. V_P = 8 V; R_L = 8 Ω; T_{amb} = 25 °C; f = 1 kHz; asymmetrical power supply. See Fig.5
6. $\pm V_P$ = 12 V; R_L = 8 Ω; T_{amb} = 25 °C; f = 1 kHz; symmetrical power supply I_{MUTE} < 30 μA. See Fig.4
7. The internal network at pin 2 is a resistor devider of typical 4 kΩ and 5 kΩ to the positive supply rail. At the connection of the 4 kΩ and 5 kΩ resistor a zener diode of typical 6.6 V is also connected to the positive supply rail. The spread of the zener voltage is 6.1 to 7.1 V.

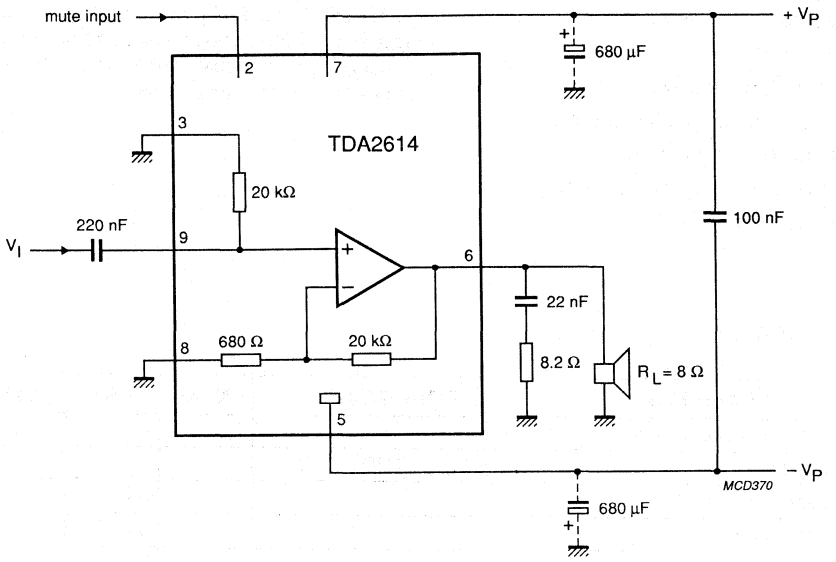


Fig.4 Test and application circuit with symmetrical power supply.

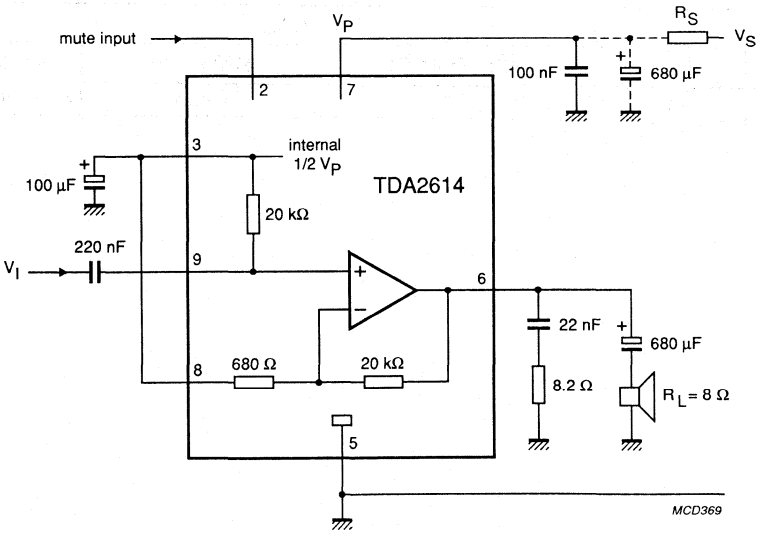


Fig.5 Test and application circuit with asymmetrical power supply.

2 x 6 W hi-fi audio power amplifier TDA2615

FEATURES

- Requires very few external components
- No switch-on/switch-off clicks
- Input mute during switch-on and switch-off
- Low offset voltage between output and ground
- Excellent gain balance of both amplifiers
- Hi-fi in accordance with IEC 268 and DIN 45500
- Short-circuit proof and thermal protected
- Mute possibility.

GENERAL DESCRIPTION

The TDA2615 is a dual power amplifier in a 9-lead single-in-line (SIL9) plastic medium power package. It has been especially designed for mains fed applications, such as stereo radio and stereo TV.

QUICK REFERENCE DATA

Stereo application

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$\pm V_P$	positive supply voltage range		7.5	–	21	V
P_O	output power	$V_S = \pm 12$ V; THD = 0.5%	–	6	–	W
G_v	internal voltage gain		–	30	–	dB
$\lvert G_v \rvert$	channel unbalance		–	0.2	–	dB
α	channel separation		–	70	–	dB
SVRR	supply voltage ripple rejection		–	60	–	dB
V_{no}	noise output voltage		–	70	–	μV

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA2615	9	SIL	plastic	SOT110

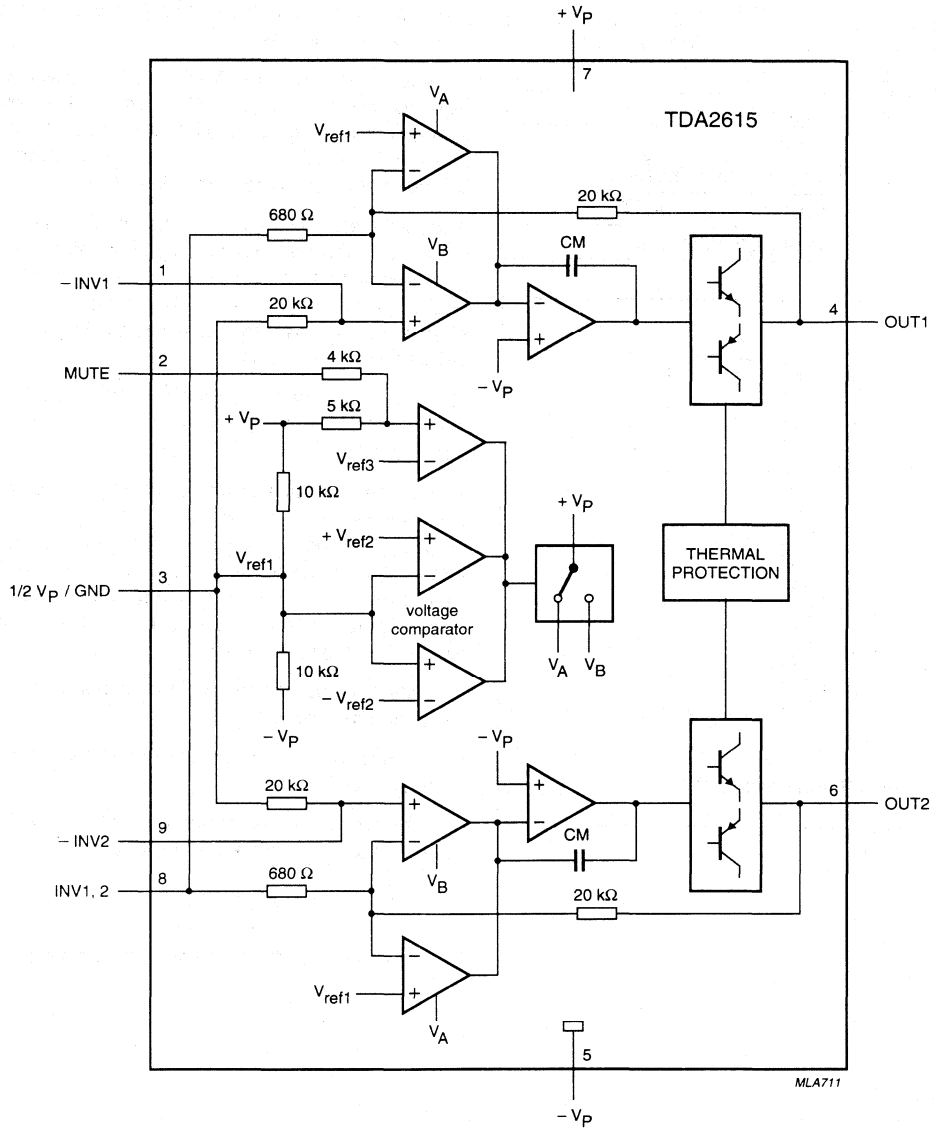


Fig.1 Block diagram.

2 x 6 W hi-fi audio power amplifier TDA2615

PINNING

SYMBOL	PIN	DESCRIPTION
–INV1	1	non-inverting input 1
MUTE	2	mute input
1/2V_P/GND	3	1/2 supply voltage or ground
OUT1	4	output 1
$-V_P$	5	supply voltage (negative)
OUT2	6	output 2
V_P	7	supply voltage (positive)
INV1, 2	8	inverting input 1 and 2
–INV2	9	non-inverting input 2

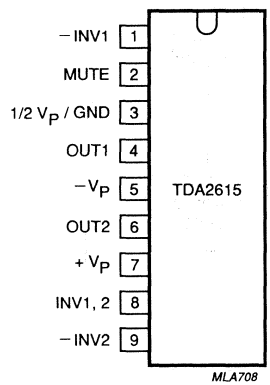


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The TDA2615 is a hi-fi stereo amplifier designed for mains fed applications, such as stereo radio and stereo TV. The circuit is optimally designed for symmetrical power supplies, but is also well-suited to asymmetrical power supply systems.

An output power of 2 x 6 W (THD = 0.5%) can be delivered into an 8 Ω load with a symmetrical power supply of ±12 V. The gain is internally fixed at 30 dB, thus offering a low gain spread and a very good gain balance between the two amplifiers (0.2 dB).

A special feature is the input mute circuit. This circuit disconnects the non-inverting inputs when the supply voltage drops below ±6 V, while the amplifier still retains its DC operating adjustment. The circuit features suppression of unwanted signals at the inputs, during switch-on and switch-off.

The mute circuit can also be activated via pin 2. When a current of 300 μA is present at pin 2, the circuit is in the mute condition.

The device is provided with two thermal protection circuits. One circuit measures the average temperature of the crystal and the other measures the momentary temperature of the power transistors. These control circuits attack at temperatures in excess of +150 °C, so a crystal operating temperature of max. +150 °C can be used without extra distortion.

With the derating value of 6 K/W, the heatsink can be calculated as follows:

at R_L = 8 Ω and V_S = ±12 V, the measured maximum dissipation is 7.8 W.

With a maximum ambient temperature of +60 °C, the thermal resistance of the heatsink is:

$$R_{th} = \frac{150 - 60}{7.8} - 6 = 5.5 \text{ K/W}.$$

The metal tab has the same potential as pin 5.

LIMITING VALUES

In accordance with the Absolute maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$\pm V_P$	supply voltage		–	21	V
I_{OSM}	non-repetitive peak output current		–	4	A
P_{tot}	total power dissipation	see Fig.3	–	15	W
T_{stg}	storage temperature range		–55	+150	°C
T_{XTAL}	crystal temperature		–	+150	°C
T_{amb}	ambient operating temperature range		–25	+150	°C
t_{sc}	short-circuit time	short-circuit to ground; note 1	–	1	h

Note to the limiting values

1. For asymmetrical power supplies (with the load short-circuited), the maximum unloaded supply voltage is limited to V_P = 28 V and with an internal supply resistance of $R_S \geq 4\ \Omega$, the maximum unloaded supply voltage is limited to 32 V (with the load short-circuited). For symetrical power supplies the circuit is short-circuit-proof up to V_P = 21 V

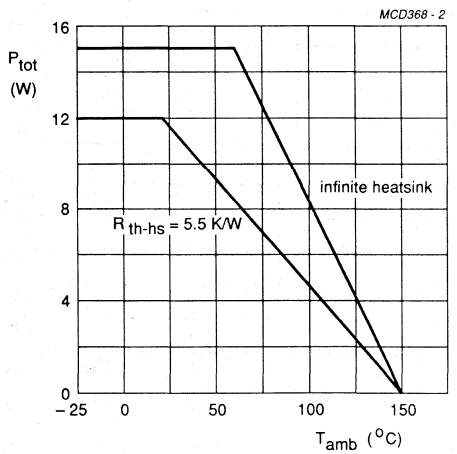


Fig.3 Power derating curve.

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}c}$	from junction to case	6 K/W

CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
$\pm V_P$	supply voltage range		–	12	21	V
I_{ORM}	repetitive peak output current		–	2.2	–	A
Operating position; note 1						
$\pm V_P$	supply voltage range		7.5	12	21	V
I_P	total quiescent current	$R_L = \infty$	18	40	70	mA
P_O	output power					
		THD = 0.5%	5	6	–	W
		THD = 10%	6.5	8	–	W
THD	total harmonic distortion	P_O = 4 W	–	0.15	0.2	%
B	power bandwidth	THD = 0.5%; note 2	–	20 to 20 000	–	Hz
G_v	voltage gain		29	30	31	dB
$\lvert G_v \rvert$	gain unbalance		–	0.2	1	dB
V_{no}	noise output voltage	note 3	–	70	140	μV
$\lvert Z_i \rvert$	input impedance		14	20	26	kΩ
SVRR	supply voltage ripple rejection	note 4	40	60	–	dB
α	channel separation	$R_S = 0$	46	70	–	dB
I_{bias}	input bias current		–	0.3	–	μA
$\lvert \Delta V_{GND} \rvert$	DC output offset voltage		–	30	200	mV
$\lvert \Delta V_{4-6} \rvert$	DC output offset voltage	between two channels	–	4	150	mV
MUTE POSITION (AT $I_{MUTE} \geq 300$ μA)						
V_O	output voltage	V_I = 600 mV	–	0.3	1.0	mV
Z_{2-7}	mute input impedance		–	9	–	kΩ
I_P	total quiescent current	$R_L = \infty$	18	40	70	mA
V_{no}	noise output voltage	note 3	–	70	140	μV
SVRR	supply voltage ripple rejection	note 4	40	55	–	dB
$\lvert \Delta V_{GND} \rvert$	DC output offset voltage		–	40	200	mV
$\lvert \Delta V_{off} \rvert$	offset voltage with respect to operating position		–	4	150	mV
I_2	current if pin 2 is connected to pin 5		–	–	6	mA
Mute position; note 5						
$\pm V_P$	supply voltage range		2	–	5.8	V
I_P	total quiescent current	$R_L = \infty$	9	30	40	mA
V_O	output voltage	V_I = 600 mV	–	0.3	1.0	mV
V_{no}	noise output voltage	note 3	–	70	140	μV
SVRR	supply voltage ripple rejection	note 4	40	55	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$\lvert\Delta V_{GND}\rvert$	DC output offset voltage		–	40	200	mV
Operating position; note 6						
I_P	total quiescent current		18	40	70	mA
P_O	output power					
		THD = 0.5%	5	6	–	W
		THD = 10%	6.5	8	–	W
THD	total harmonic distortion	P_O = 4 W	–	0.13	0.2	%
B	power bandwidth	THD = 0.5%; note 1	–	40 to 20 000	–	Hz
G_v	voltage gain		29	30	31	dB
$\lvert G_v\rvert$	gain unbalance		–	0.2	1	dB
V_{no}	noise output voltage	note 3	–	70	140	μV
$\lvert Z_i\rvert$	input impedance		14	20	26	kΩ
SVRR	supply voltage ripple rejection		35	44	–	dB
α	channel separation		–	45	–	dB
MUTE POSITION ($I_{MUTE} \geq 300$ μA)						
V_O	output voltage	V_I = 600 mV	–	0.3	1.0	mV
Z_{2-7}	mute input impedance		–	9	–	kΩ
I_P	total quiescent current		18	40	70	mA
V_{no}	noise output voltage	note 3	–	70	140	μV
SVRR	supply voltage ripple rejection	note 4	35	44	–	dB
$\lvert\Delta V_{off}\rvert$	offset voltage with respect to operating position		–	4	150	mV
I_2	current if pin 2 is connected to pin 5		–	–	6	mA

Notes to the characteristics

1. V_P = ±12 V; R_L = 8 Ω; T_{amb} = 25 °C; f = 1 kHz; symmetrical power supply I_{MUTE} = < 30 μA. See Fig.4
2. The power bandwidth is measured at an output power of $P_{O\ max}$ –3 dB.
3. The noise output voltage (RMS value) is measured at R_S = 2 kΩ, unweighted (20 Hz to 20 kHz).
4. The ripple rejection is measured at R_S = 0 and f = 100 Hz to 20 kHz. The ripple voltage (200 mV) is applied in phase to the positive and the negative supply rails. With asymmetrical power supplies, the ripple rejection is measured at f = 1 kHz.
5. ±V_P = 4 V; R_L = 8 Ω; T_{amb} = 25 °C; f = 1 kHz; symmetrical power supply. See Fig.4
6. V_P = 24 V; R_L = 8 Ω; T_{amb} = 25 °C; f = 1 kHz; asymmetrical power supply I_{MUTE} < 30 μA. See Fig.5

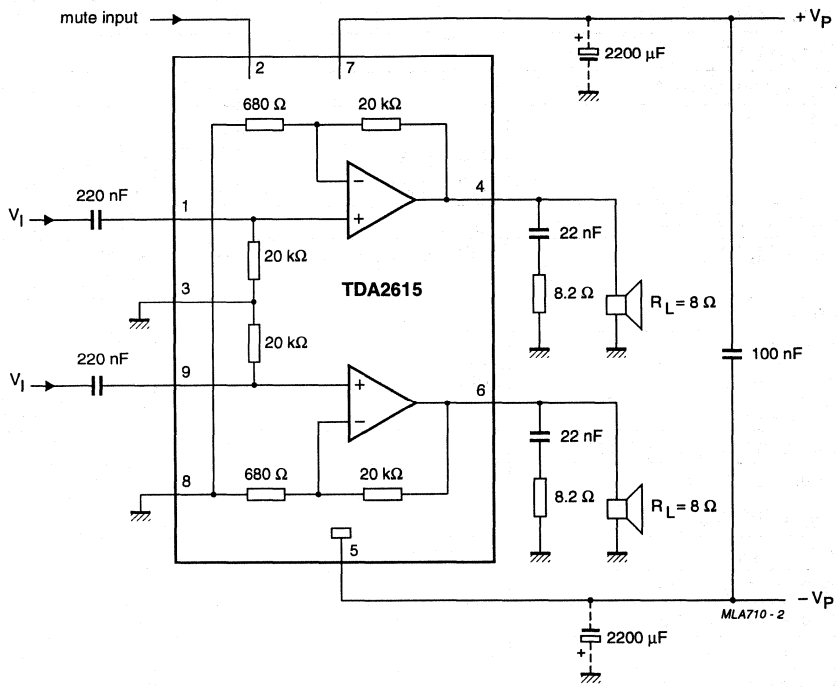


Fig.4 Test and application circuit with symmetrical power supply.

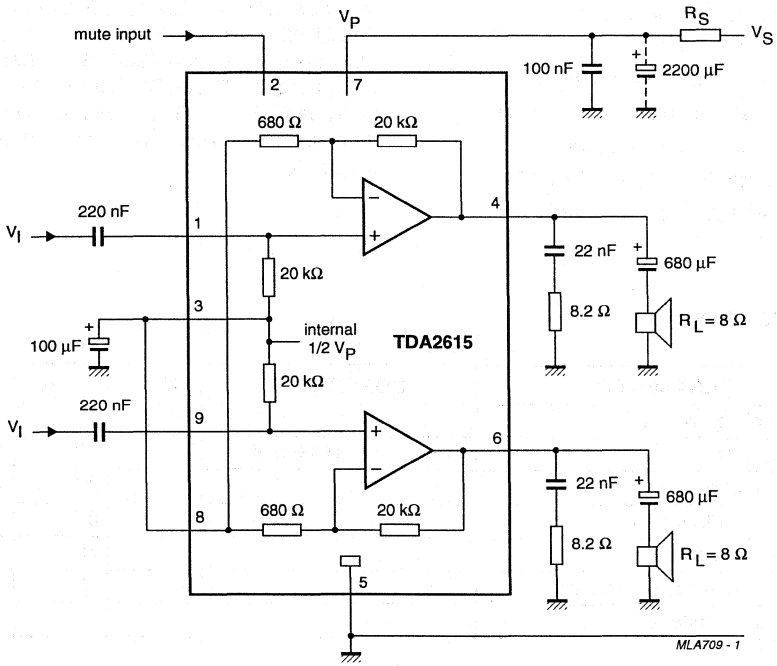


Fig.5 Test and application circuit with asymmetrical power supply.

2 x 12 W hi-fi audio power amplifiers with mute

TDA2616/TDA2616Q

FEATURES

- Requires very few external components
- No switch-on/switch-off clicks
- Input mute during switch-on and switch-off
- Low offset voltage between output and ground
- Excellent gain balance of both amplifiers
- Hi-fi in accordance with IEC 268 and DIN 45500
- Short-circuit proof and thermal protected
- Mute possibility.

GENERAL DESCRIPTION

The TDA2616 and TDA2616Q are dual power amplifiers. The TDA2616 is supplied in a 9-lead single-in-line (SIL9) plastic power package (SOT131), while the TDA2616Q is supplied in a 9-lead SIL-bent-to-DIL plastic power package (SOT157). They have been especially designed for mains fed applications, such as stereo radio and stereo TV.

QUICK REFERENCE DATA

Stereo application

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$\pm V_P$	supply voltage range		7.5	–	21	V
P_O	output power	$V_P = \pm 16$ V; THD = 0.5%	–	12	–	W
G_v	internal voltage gain		–	30	–	dB
$\lvert G_v \rvert$	channel unbalance		–	0.2	–	dB
α	channel separation		–	70	–	dB
SVRR	supply voltage ripple rejection		–	60	–	dB
V_{no}	noise output voltage		–	70	–	μV

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA2616	9	SIL	plastic	SOT131
TDA2616Q	9	SIL-bent-to-DIL	plastic	SOT157

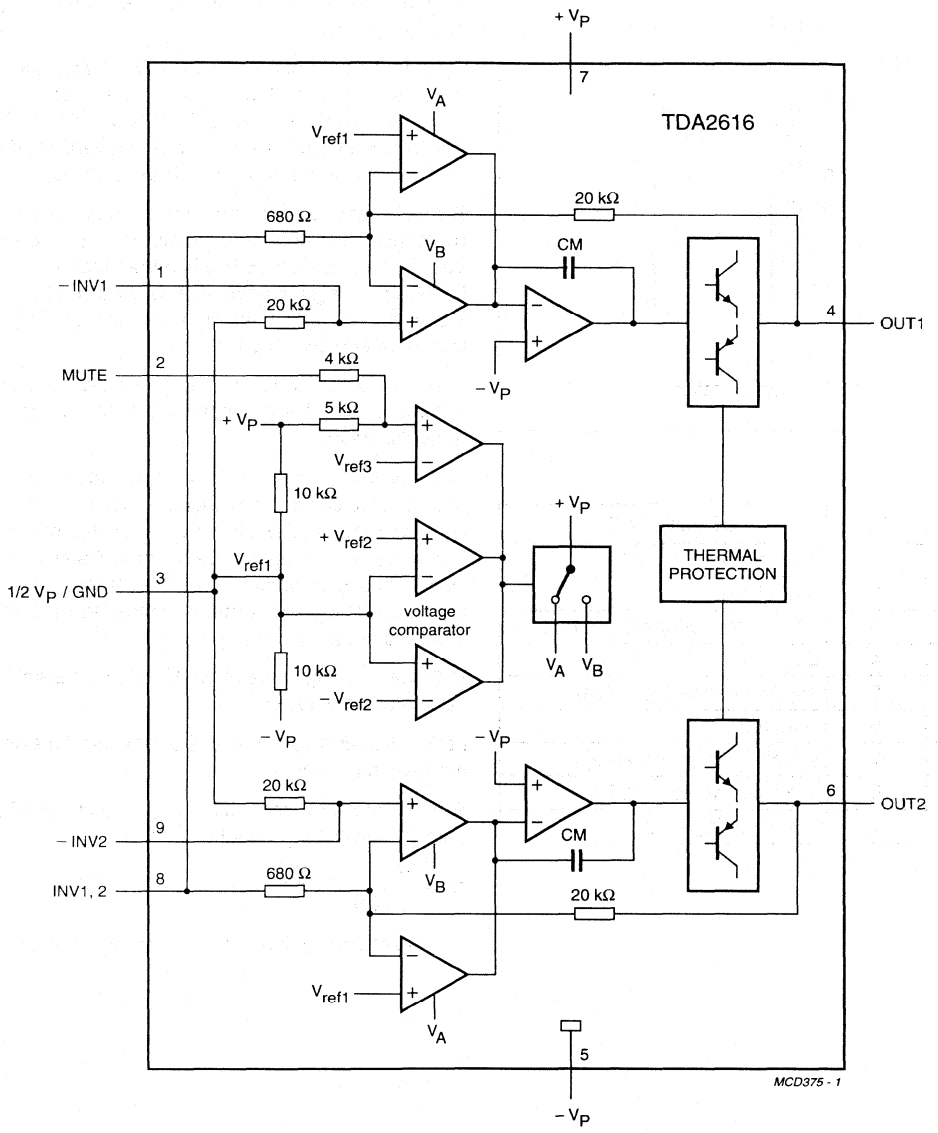


Fig.1 Block diagram.

2 x 12 W hi-fi audio power amplifiers with mute

TDA2616/TDA2616Q

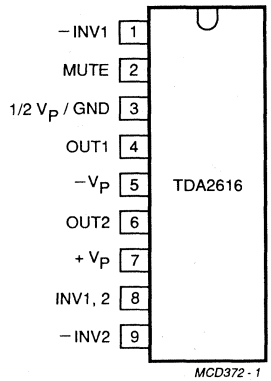


Fig.2 Pin configuration.

PINNING

SYMBOL	PIN	DESCRIPTION
−INV1	1	non-inverting input 1
MUTE	2	mute input
1/2V_P/GND	3	1/2 supply voltage or ground
OUT1	4	output 1
$-V_P$	5	supply voltage (negative)
OUT2	6	output 2
$+V_P$	7	supply voltage (positive)
INV1, 2	8	inverting inputs 1 and 2
−INV2	9	non-inverting input 2

FUNCTIONAL DESCRIPTION

The TDA2616 is a hi-fi stereo amplifier designed for mains fed applications, such as stereo radio and TV. The circuit is optimally designed for symmetrical power supplies, but is also well-suited to asymmetrical power supply systems.

An output power of 2 x 12 W (THD = 0.5%) can be delivered into an 8 Ω load with a symmetrical power supply of ±16 V. The gain is internally fixed at 30 dB, thus offering a low gain spread and a very good gain balance between the two amplifiers (0.2 dB).

A special feature is the input mute circuit. This circuit disconnects the non-inverting inputs when the supply voltage drops below ±6 V, while the amplifier still retains its DC operating adjustment. The circuit features suppression of unwanted signals at the inputs, during switch-on and switch-off.

The mute circuit can also be activated via pin 2. When a current of 300 μA is present at pin 2, the circuit is in the mute condition.

The device is provided with two thermal protection circuits. One circuit measures the average temperature of the crystal and the other measures the momentary temperature of the power transistors. These control circuits attack at temperatures in excess of +150 °C, so a crystal operating temperature of max. +150 °C can be used without extra distortion.

With the derating value of 2.5 K/W, the heatsink can be calculated as follows:

at R_L = 8 Ω and V_P = ±16 V, the measured maximum dissipation is 14.6 W.

With a maximum ambient temperature of +65 °C, the thermal resistance of the heatsink is:

$$R_{th} = \frac{150 - 65}{14.6} - 2.5 = 3.3 \text{ K/W}.$$

The internal metal block has the same potential as pin 5.

LIMITING VALUES

In accordance with the Absolute maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$\pm V_P$	supply voltage		–	21	V
I_{OSM}	non-repetitive peak output current		–	4	A
P_{tot}	total power dissipation	see Fig.3	–	25	W
T_{stg}	storage temperature range		−55	+150	°C
T_{XTAL}	crystal temperature		–	+150	°C
T_{amb}	ambient operating temperature range		−25	150	°C
t_{sc}	short circuit time	short-circuit to ground; note 1	–	1	h

Note to the limiting values

1. For asymmetrical power supplies (with the load short-circuited), the maximum unloaded supply voltage is limited to V_P = 28 V and with an internal supply resistance of $R_S \geq 4\ \Omega$, the maximum unloaded supply voltage is limited to 32 V (with the load short-circuited). For symmetrical power supplies the circuit is short-circuit-proof up to V_P = ±21 V.

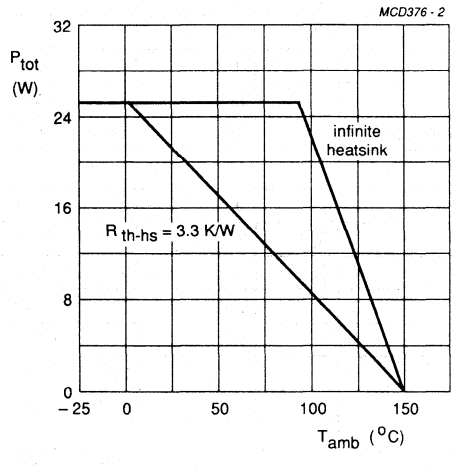


Fig.3 Power derating curve.

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient in free air	2.5 K/W

CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
$\pm V_P$	supply voltage range		–	16	21	V
I_{ORM}	repetitive peak output current		–	2.2	–	A
Operating position; note 1						
$\pm V_P$	supply voltage range		7.5	16	21	V
I_P	total quiescent current	$R_L = \infty$	18	40	70	mA
P_O	output power					
		THD = 0.5%	10	12	–	W
		THD = 10%	12	15	–	W
THD	total harmonic distortion	P_O = 6 W	–	0.15	0.2	%
B	power bandwidth	THD = 0.5%; note 2	–	20 to 20 000	–	Hz
G_v	voltage gain		29	30	31	dB
$\lvert G_v \rvert$	gain unbalance		–	0.2	1	dB
V_{no}	noise output voltage	note 3	–	70	140	μV
$\lvert Z_i \rvert$	input impedance		14	20	26	kΩ
SVRR	supply voltage ripple rejection	note 4	40	60	–	dB
α	channel separation	$R_S = 0$	46	70	–	dB
I_{bias}	input bias current		–	0.3	–	μA
$\lvert \Delta V_{GND} \rvert$	DC output offset voltage		–	30	200	mV
$\lvert \Delta V_{4-6} \rvert$	DC output offset voltage	between two channels	–	4	150	mV
MUTE POSITION (AT $I_{MUTE} \geq 300$ μA)						
V_O	output voltage	V_I = 600 mV	–	0.3	1.0	mV
Z_{2-7}	mute input impedance	note 7	6.7	9	11.3	kΩ
I_P	total quiescent current	$R_L = \infty$	18	40	70	mA
V_{no}	noise output voltage	note 3	–	70	140	μV
SVRR	supply voltage ripple rejection	note 4	40	55	–	dB
$\lvert \Delta V_{GND} \rvert$	DC output offset voltage		–	40	200	mV
$\lvert \Delta V_{off} \rvert$	offset voltage with respect to operating position		–	4	150	mV
I_2	current if pin 2 is connected to pin 5		–	–	8.2	mA
Mute position; note 5						
$\pm V_P$	supply voltage range		2	–	5.8	V
I_P	total quiescent current	$R_L = \infty$	9	30	40	mA
V_O	output voltage	V_I = 600 mV	–	0.3	1.0	mV
V_{no}	noise output voltage	note 3	–	70	140	μV
SVRR	supply voltage ripple rejection	note 4	40	55	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$\lvert\Delta V_{GND}\rvert$	DC output offset voltage		–	40	200	mV
Operating position; note 6						
I_P	total quiescent current		18	40	70	mA
P_O	output power					
		THD = 0.5%	5	6	–	W
		THD = 10%	6.5	8	–	W
		THD = 0.5%; R_L = 4 Ω	–	10	–	W
		THD = 10%; R_L = 4 Ω	–	14	–	W
THD	total harmonic distortion	P_O = 4 W	–	0.13	0.2	%
B	power bandwidth	THD = 0.5%; note 2	–	40 to 20 000	–	Hz
G_v	voltage gain		29	30	31	dB
$\lvert G_v\rvert$	gain unbalance		–	0.2	1	dB
V_{no}	noise output voltage	note 3	–	70	140	μV
$\lvert Z_i\rvert$	input impedance		14	20	26	kΩ
SVRR	supply voltage ripple rejection		35	44	–	dB
α	channel separation		–	45	–	dB
MUTE POSITION ($I_{MUTE} \geq 300$ μA)						
V_O	output voltage	V_I = 600 mV	–	0.3	1.0	mV
Z_{2-7}	mute input impedance	note 7	6.7	9	11.3	kΩ
I_P	total quiescent current		18	40	70	mA
V_{no}	noise output voltage	note 3	–	70	140	μV
SVRR	supply voltage ripple rejection	note 4	35	44	–	dB
$\lvert\Delta V_{off}\rvert$	offset voltage with respect to operating position		–	4	150	mV
I_2	current if pin 2 is connected to pin 5		–	–	8.2	mA

Notes to the characteristics

1. V_P = ±16 V; R_L = 8 Ω; T_{amb} = 25 °C; f = 1 kHz; symmetrical power supply I_{MUTE} < 30 μA. See Fig.4
2. The power bandwidth is measured at an output power of $P_{O\ max}$ – 3 dB
3. The noise output voltage (RMS value) is measured at R_S = 2 kΩ, unweighted (20 Hz to 20 kHz)
4. The ripple rejection is measured at R_S = 0 and f = 100 Hz to 20 kHz. The ripple voltage (200 mV) is applied in phase to the positive and the negative supply rails. With asymmetrical power supplies, the ripple rejection is measured at f = 1 kHz
5. ±V_P = 4 V; R_L = 8 Ω; T_{amb} = 25 °C; f = 1 kHz; symmetrical power supply. See Fig.4
6. V_P = 24 V; R_L = 8 Ω; T_{amb} = 25 °C; f = 1 kHz; asymmetrical power supply I_{MUTE} < 30 μA. See Fig.5
7. The internal network at pin 2 is a resistor devider of typical 4 kΩ and 5 kΩ to the positive supply rail. At the connection of the 4 kΩ and 5 kΩ resistor a zener diode of typical 6.6 V is also connected to the positive supply rail. The spread of the zener voltage is 6.1 to 7.1 V.

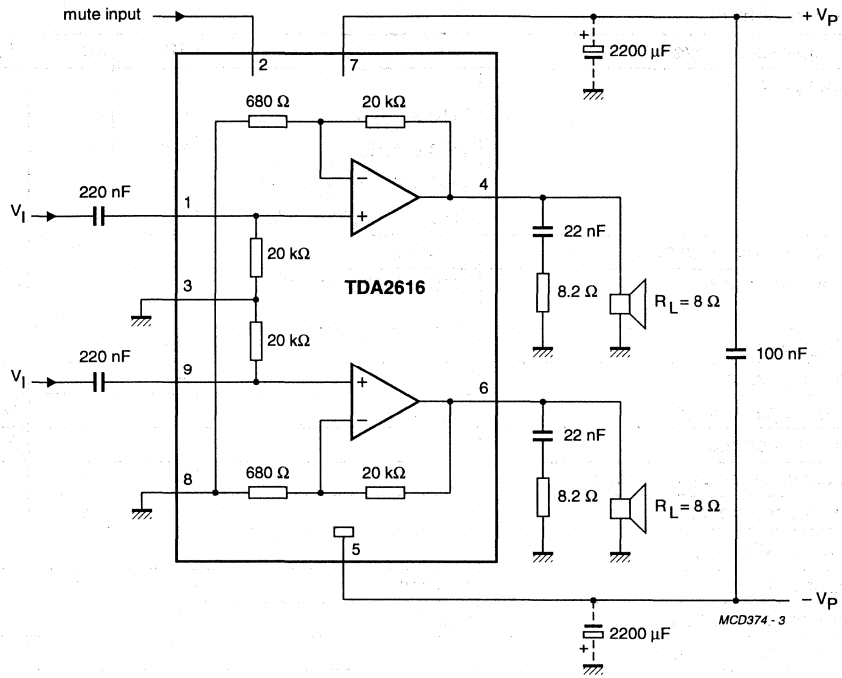


Fig.4 Test and application circuit with symmetrical power supply.

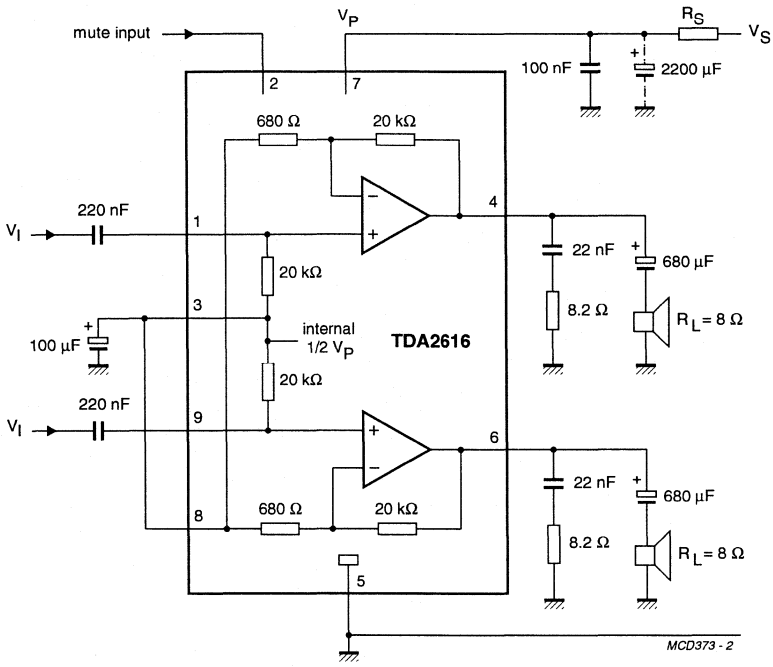


Fig.5 Test and application circuit with asymmetrical power supply.

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC02 OR DATASHEET

INFRARED RECEIVER

The TDA3047 is for infrared reception with low power consumption.
The difference between the TDA3047 and TDA3048 is the polarity of the output signal.

Features

- H.F. amplifier with a control range of 66 dB
- Synchronous demodulator and reference amplifier
- A.G.C. detector
- Pulse shaper
- Q-factor killing of the input selectivity, which is controlled by the a.g.c. circuit
- Input voltage limiter

QUICK REFERENCE DATA

Supply voltage (pin 8)	$V_P = V_{8-16}$	typ.	5 V
Supply current (pin 8)	$I_P = I_8$	typ.	2,1 mA
Input signal (peak-to-peak value) (100% AM; f = 36 kHz)	$V_{2-15(p-p)}$		0,03 to 200 mV
Output signal (peak-to-peak value)	$V_{9-16(p-p)}$	typ.	4,5 V

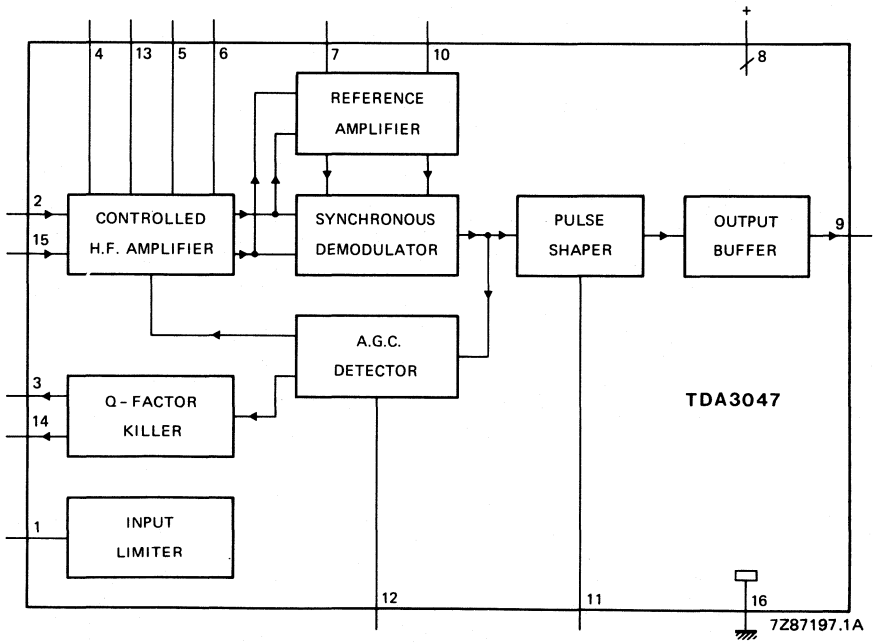


Fig. 1 Block diagram of TDA3047.

PACKAGE OUTLINES

TDA3047P: 16-lead DIL; plastic (SOT38).
TDA3047T: 16-lead mini-pack; plastic (SO16L; SOT162A).

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC02 OR DATASHEET

INFRARED RECEIVER

The TDA3048 is for infrared reception with low power consumption.
The difference between the TDA3048 and TDA3047 is the polarity of the output signal.

Features

- H.F. amplifier with a control range of 66 dB
- Synchronous demodulator and reference amplifier
- A.G.C. detector
- Pulse shaper
- Q-factor killing of the input selectivity, which is controlled by the a.g.c. circuit
- Input voltage limiter

QUICK REFERENCE DATA

Supply voltage (pin 8)	$V_P = V_{8\text{-}16}$	typ.	5 V
Supply current (pin 8)	$I_P = I_8$	typ.	2,1 mA
Input signal (peak-to-peak value) (100% AM; f = 36 kHz)	$V_{2\text{-}15(p\text{-}p)}$		0,03 to 200 mV
Output signal (peak-to-peak value)	$V_{9\text{-}16(p\text{-}p)}$	typ.	4,5 V

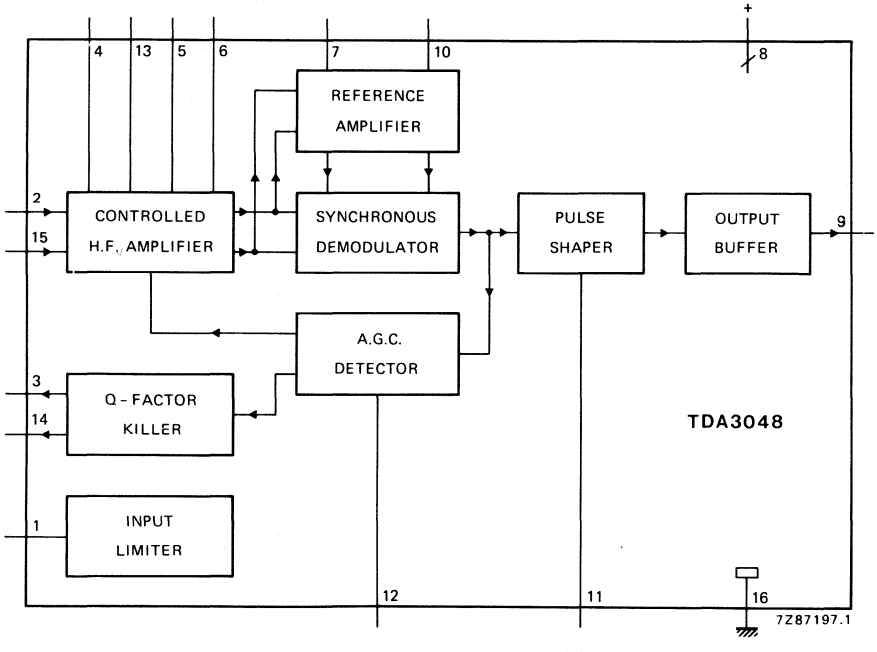


Fig. 1 Block diagram of TDA3048.

PACKAGE OUTLINES

TDA3048P: 16-lead DIL; plastic (SOT38).
TDA3048T: 16-lead mini-pack; plastic (SO16L; SOT162A).

Multiple output voltage regulators

TDA3601Q
TDA3601AQ

FEATURES

- Six fixed voltage regulators
- Three microprocessor-controlled regulators
- Two V_P-state controlled regulators
- One fixed voltage regulator (can operate during load dump or thermal shutdown)
- V_{P1} supply pin (low current pin)
- V_{P2} supply pin (high current pin)
- RESET output (TDA3601Q) or $\overline{\text{RESET}}$ output (TDA3601AQ)
- Internally fixed timer of 100 µs
- Externally fixed delay timer
- High ripple rejection
- Flexible leads.

PROTECTION

- Current limit protection for regulator 1
- Foldback current limit protection (regulators 2 to 6)
- Load dump protection
- Thermal protection
- Regulator outputs DC short-circuit-safe to ground, V_P and other regulator outputs
- Capable of handling high energy on any of the output pins
- Reverse polarity safe.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Entire device						
V_{P1}	supply voltage range	operating	11	13.2	18	V
		load dump; notes 1 and 2	–	–	50	V
V_{P2}	supply voltage range	operating	11	13.2	18	V
		non-operating	–	–	30	V
		load dump; note 1	–	–	50	V
$I1_{tot}$	total quiescent current, V_{P1}	V_{P2} = 0; note 3	–	1	1.4	mA
T_c	crystal temperature		–	–	150	°C
Voltage regulators						
V_{R1}	output voltage regulator 1	0.5 mA ≤ I_{R1} ≤ 20 mA	4.75	5	5.25	V
V_{R2}	output voltage regulator 2	5 mA ≤ I_{R2} ≤ 200 mA	1.9	2.1	2.3	V
V_{R3}	output voltage regulator 3	5 mA ≤ I_{R3} ≤ 150 mA	4.75	5	5.25	V
V_{R4}	output voltage regulator 4	5 mA ≤ I_{R4} ≤ 150 mA	9	9.5	10	V
V_{R5}	output voltage regulator 5	5 mA ≤ I_{R5} ≤ 200 mA	9	9.5	10	V
V_{R6}	output voltage regulator 6	5 mA ≤ I_{R6} ≤ 200 mA	9.3	9.75	10.2	V

Notes

1. Load dump, during 50 ms, t_r > 2.5 ms.
2. Regulator 1 operating, 0.5 mA ≤ I_{R1} ≤ 20 mA.
3. V_{P1} = 13.2 V; V_{P2} = R4-sel = R5-sel = 0; I_{R1} = 0.

BLOCK DIAGRAM

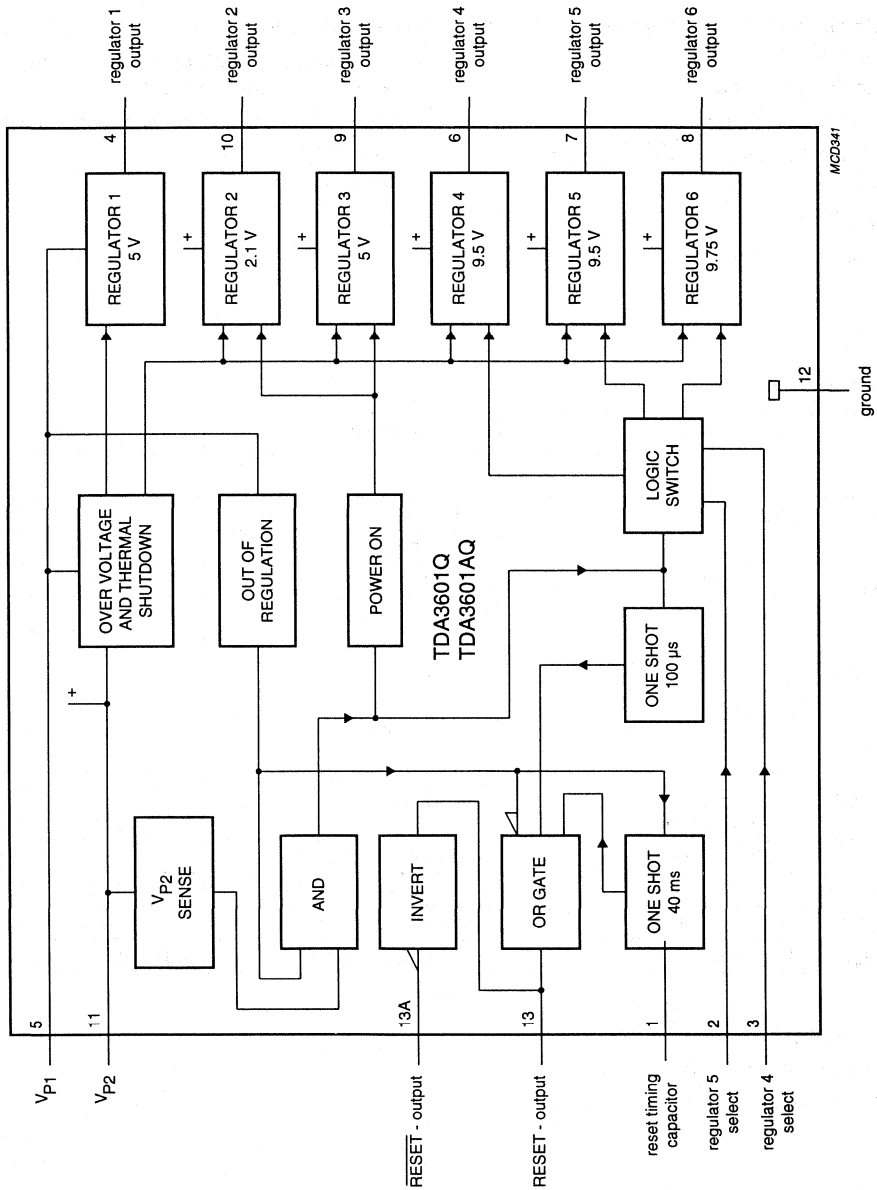


Fig.1 Block diagram.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA3601Q/AQ	13	DIL	plastic	SOT141-6

GENERAL DESCRIPTION

The circuit contains five fixed voltage regulators with foldback current protection and one fixed voltage regulator (REGULATOR 1) that also operates during a load dump. In addition, a RESET function (TDA3601Q) or $\overline{\text{RESET}}$ function (TDA3601AQ), timer functions and a logic multiplexer are implemented.

PINNING

SYMBOL	PIN	DESCRIPTION
C_{RESET}	1	reset timing capacitor
R5-sel	2	regulator 5 select
R4-sel	3	regulator 4 select
REG1	4	regulator 1 output (5 V)
V_{P1}	5	supply voltage
REG4	6	regulator 4 output (9.5 V)
REG5	7	regulator 5 output (9.5 V)
REG6	8	regulator 6 output (9.75 V)
REG3	9	regulator 3 output (5 V)
REG2	10	regulator 2 output (2.4 V)
V_{P2}	11	supply voltage
GND	12	ground
RES	13	RESET output (TDA3601Q)
$\overline{\text{RES}}$	13A	$\overline{\text{RESET}}$ output (TDA3601AQ)

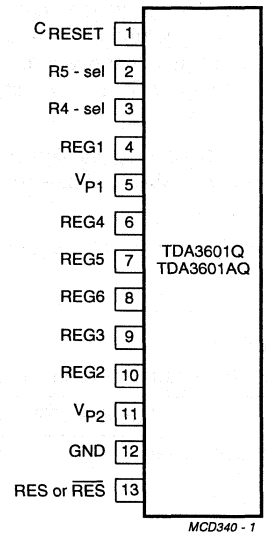


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The TDA3601Q is a multiple output voltage regulator with six fixed voltage regulators. Three, logical switch controlled, voltage regulators (numbers 4 to 6) are available, and one non-switchable voltage regulator (number 1). In addition, there are two further regulators (numbers 2 and 3), which are controlled by supply voltages V_{P1} and V_{P2} (Schmitt trigger).

Regulator 1 is not affected by load dump or thermal shutdown. Regulators 2 to 6 are supplied by V_{P2}; they can therefore be switched of by an ignition switch, for example. An internal bandgap voltage reference, which provides a reference voltage for each independent regulator, is supplied by V_{P1}. This supply voltage V_{P1} also supplies regulator 1.

A V_{P2} sense circuit outputs a logical high when the V_{P2} voltage rises through V_{thr}, which remains high until the V_{P2} voltage falls through V_{thf}.

The supply voltage V_{P1} is sensed by an out-of-regulation Schmitt trigger.

When this voltage drops below 5.95 V typical, the reset output is disabled, to prevent a microprocessor being disturbed by a too-low supply voltage. An out-of-regulation condition is indicated by a logical low and an in-regulation condition indicated by a logical high.

The 'Power On' switch low will disable regulator 2 and 3 outputs. In addition, the logic switch will be disabled, so that regulators 4 to 6 are switched off. When both V_{P2}-sense and out-of-regulation are high, the 'Power On' will be high, so that the logic multiplexer and regulators 2 and 3 are enabled. Regulators 4 to 6 can now be selected by the multiplexer.

Re-triggerable one-shot circuits produce a RESET (open collector output) when V_{P1} is available (40 ms delay signal), or when both V_{P1} and V_{P2} are available (100 µs pulse). RESET will be held in a constant high state when the supply voltage V_{P1} is less than 5.5 V (5.95 V typical).

The TDA3601 has a RESET output, but the TDA3601A has an inverted RESET output ($\overline{\text{RESET}}$).

LIMITING VALUES

In accordance with the Absolute maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{P1}, V_{P2}	supply voltage	operating	–	18	V
		non-operating	–	30	V
		load dump protected; during 50 ms; $t_r > 2.5$ ms; note 1	–	50	V
P_{tot}	total power dissipation	$T_{case} < 30$ °C	–	15	W
T_{stg}	storage temperature range	non-operating	–55	150	°C
T_{vj}	virtual junction temperature	operating	–40	150	°C
V_{pr}	reverse polarity	non-operating	–	6	V

Note

1. Regulator 1 operating, $0.5 \text{ mA} \leq I_{R1} \leq 20 \text{ mA}$.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}c}$	thermal resistance from junction to case	8	K/W
$R_{th\ j\text{-}amb}$	thermal resistance from junction to ambient in free air	40	K/W

QUALITY SPECIFICATION

Quality according to UZW-BO/FQ-0601.

CHARACTERISTICS

$V_{P1} = V_{P2} = 13.2$ V, $T_{amb} = 25$ °C, $C_{out} = 10$ µF; unless otherwise specified (see Fig.5).

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{P1}	supply voltage range	operating	11	13.2	18	V
V_{P1}	supply voltage range	load dump; notes 1and 2	–	–	50	V
V_{P2}	supply voltage range	operating	11	13.2	18	V
V_{P2}	supply voltage range	load dump; note 1	–	–	50	V
I_{P1}	quiescent current	$V_{P2} = 0$; note 3	–	1.1	1.4	mA
Schmitt triggers						
V_{P2}-SENSE THRESHOLD						
V_{thr}	rising threshold voltage		7.6	8	8.4	V
V_{thf}	falling threshold voltage		6.2	6.5	6.8	V
V_{hy}	hysteresis		1.35	1.5	1.65	V
OUT-OF-REGULATION THRESHOLD						
V_{thr}	rising threshold voltage		6.8	7.35	7.9	V
V_{thf}	falling threshold voltage		5.5	5.95	6.4	V
V_{hy}	hysteresis		1.2	1.4	1.6	V
Reset circuits (for timing, see Fig.3)						
t_{rst1}	reset delay time	$C_{rst} = 100$ nF	20	40	100	ms
t_{rst}	reset hold time		50	100	150	µs
V_{rl}	reset low	$I_{sync} = 1$ mA	–	0.15	0.8	V
I_{cr}	delay current (pin 1 to C_{rst})		–	–5	–	µA
t_r	reset rise time	note 4	–	–	1	µs
t_f	reset fall time	note 4	–	–	1	µs
V_{CAP}	voltage pin 1	$C_{rst} = 0$	5.5	6.0	–	V
R_{sp}	spike-on reset	on-state; note 5	–	0	100	mV
Regulators						
SELECTOR CONTROL INPUTS R4-SEL AND R5-SEL						
V_{sl}	input low voltage		–0.5	–	0.8	V
V_{sh}	input high voltage		2	–	–	V
I_{hs}	input high current	$V_{RXsel} > 2$ V	–	–	1	µA
I_{ls}	input low current	$V_{RXsel} < 0.8$ V	–1	–	–	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
REGULATOR 1 (I_{R1} = 1 mA UNLESS OTHERWISE SPECIFIED)						
V_{R1}	output voltage	0.5 mA ≤ I_{R1} ≤ 20 mA	4.75	5	5.25	V
		6.25 V ≤ V_{P1} ≤ 18 V	4.75	5	5.25	V
V_{R1L}	output voltage	18 V ≤ V_P ≤ 50 V	4.75	5	5.25	V
ΔV_{R1}	line regulation	6.25 V ≤ V_P ≤ 18 V	–	–	50	mV
ΔV_{RL1}	load regulation	0.5 mA ≤ I_{R1} ≤ 20 mA	–	–	60	mV
RR1	ripple rejection	f_o = 120 Hz; V_{P1} = V_{P2}; note 6	60	–	–	dB
V_{Rd1}	drop-out voltage	I_{R1} = 20 mA	–	–	1	V
I_{Rm1}	current limit		30	–	–	mA
$\Delta V/\Delta T$	thermal drift	–40 ≤ T ≤ 80 °C	–	tbn	–	mV/°C
REGULATOR 2 (I_{R2} = 5 mA UNLESS OTHERWISE SPECIFIED)						
V_{R2}	output voltage	5 mA ≤ I_{R2} ≤ 200 mA	1.9	2.1	2.3	V
		7 V ≤ V_P ≤ 18 V	1.9	2.1	2.3	V
ΔV_{R2}	line regulation	7 V ≤ V_P ≤ 18 V	–	–	50	mV
ΔV_{RL2}	load regulation	5 mA ≤ I_{R2} ≤ 200 mA	–	–	70	mV
RR2	ripple rejection	f_o = 120 Hz; V_{P1} = V_{P2}; note 6	60	–	–	dB
I_{Rm2}	current limit	V_{R2} > 1.75 V; note 7	250	–	–	mA
I_{Rsc2}	short-circuit current	R_L ≤ 0.5 Ω; note 7	–	tbn	–	mA
$\Delta V/\Delta T$	thermal drift	–40 ≤ T ≤ 80 °C	–	tbn	–	mV/°C
REGULATOR 3 (I_{R3} = 5 mA UNLESS OTHERWISE SPECIFIED)						
V_{R3}	output voltage	5 mA ≤ I_{R3} ≤ 150 mA	4.75	5	5.25	V
		7 V ≤ V_P ≤ 18 V	4.75	5	5.25	V
ΔV_{R3}	line regulation	7 V ≤ V_P ≤ 18 V	–	–	50	mV
ΔV_{RL3}	load regulation	5 mA ≤ I_{R3} ≤ 150 mA	–	–	70	mV
RR3	ripple rejection	f_o = 120 Hz; V_{P1} = V_{P2}; note 6	60	–	–	dB
I_{Rm3}	current limit	V_{R3} > 4.5 V; note 7	200	–	–	mA
I_{Rsc3}	short-circuit current	R_L ≤ 0.5 Ω; note 7	–	tbn	–	mA
$\Delta V/\Delta T$	thermal drift	–40 ≤ T ≤ 80 °C	–	tbn	–	mV/°C
REGULATOR 4 (I_{R4} = 5 mA UNLESS OTHERWISE SPECIFIED)						
V_{R4}	output voltage	5 mA ≤ I_{R4} ≤ 150 mA	9	9.5	10	V
		11 V ≤ V_P ≤ 18 V	9	9.5	10	V
ΔV_{R4}	line regulation	11 V ≤ V_P ≤ 18 V	–	–	50	mV
ΔV_{RL4}	load regulation	5 mA ≤ I_{R4} ≤ 150 mA	–	–	70	mV
RR4	ripple rejection	f_o = 120 Hz; V_{P1} = V_{P2}; note 6	60	–	–	dB
V_{Rd4}	drop-out voltage	I_{R4} = 150 mA	–	–	1	V
I_{Rm4}	current limit	V_{R4} > 8.5 V; note 7	200	–	–	mA
I_{Rsc4}	short-circuit current	R_L ≤ 0.5 Ω; note 7	–	tbn	–	mA
$\Delta V/\Delta T$	thermal drift	–40 ≤ T ≤ 80 °C	–	tbn	–	mV/°C

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
REGULATOR 5 (I_{R5} = 5 mA UNLESS OTHERWISE SPECIFIED)						
V_{R5}	output voltage	5 mA ≤ I_{R5} ≤ 200 mA	9	9.5	10	V
		11 V ≤ V_P ≤ 18 V	9	9.5	10	V
ΔV_{R5}	line regulation	11 V ≤ V_P ≤ 18 V	–	–	50	mV
ΔV_{RL5}	load regulation	5 mA ≤ I_{R5} ≤ 200 mA	–	–	70	mV
RR5	ripple rejection	f_o = 120 Hz; V_{P1} = V_{P2}; note 6	60	–	–	dB
V_{Rd5}	drop-out voltage	I_{R5} = 200 mA	–	–	1	V
I_{Rm5}	current limit	V_{R5} > 8.5 V; note 7	250	–	–	mA
I_{Rsc5}	short-circuit current	R_L ≤ 0.5 Ω; note 7	–	tbn	–	mA
$\Delta V/\Delta T$	thermal drift	–40 ≤ T ≤ 80 °C	–	tbn	–	mV/°C
REGULATOR 6 (I_{R6} = 5 mA UNLESS OTHERWISE SPECIFIED)						
V_{R6}	output voltage	5 mA ≤ I_{R6} ≤ 200 mA	9.3	9.75	10.25	V
		11 V ≤ V_P ≤ 18 V	9.3	9.75	10.25	V
ΔV_{R6}	line regulation	11 V ≤ V_P ≤ 18 V	–	–	50	mV
ΔV_{RL6}	load regulation	5 mA ≤ I_{R6} ≤ 200 mA	–	–	70	mV
RR6	ripple rejection	f_o = 120 Hz; V_{P1} = V_{P2}; note 6	60	–	–	dB
V_{Rd6}	drop-out voltage	I_{R6} = 200 mA	–	–	0.5	V
I_{Rm6}	current limit	V_{R6} > 8.5 V; note 7	300	–	–	mA
I_{Rsc6}	short-circuit current	R_{bel} ≤ 0.5 Ω; note 7	–	tbn	–	mA
$\Delta V/\Delta T$	thermal drift	–40 ≤ T ≤ 80 °C	–	tbn	–	mV/°C

Notes

1. During 50 ms, t_r > 2.5 ms.
2. Regulator 1 operating, 0.5 mA ≤ I_{R1} ≤ 20 mA.
3. V_{P1} = 13.2 V, V_{P2} = R4-sel = R5-sel = 0, I_{R1} = 0.
4. External pull-up resistor of 10 kΩ to 5 V required, and C_{load} ≤ 10 pF.
5. Spike-on reset measured within a time frame of 75 msec.
6. V_{P1} = V_{P2} = 13.2 V, ripple on V_{P1} = V_{P2} of: 1 $V_{(p-p)}$, f_o = 120 Hz.
7. Foldback current protection behaviour: see Fig.4.

Reset circuits

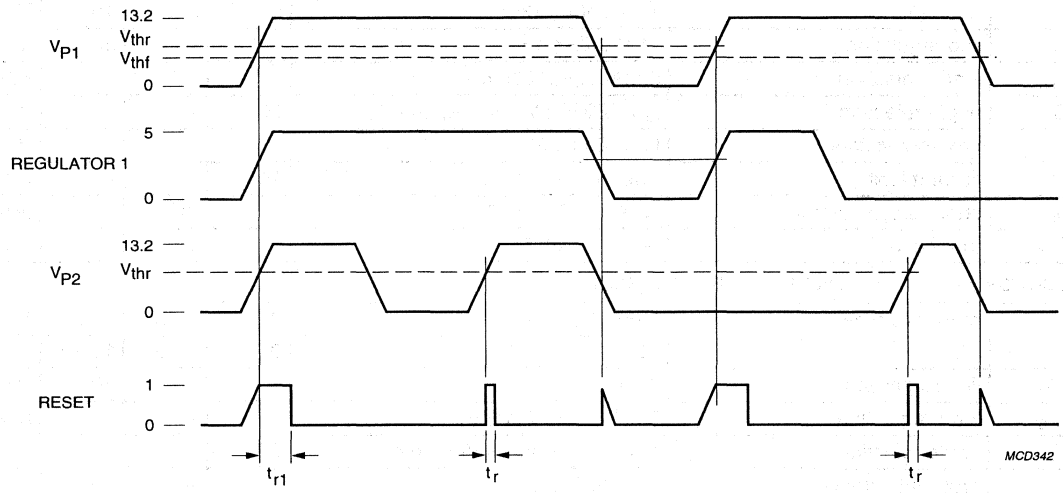


Fig.3 Timing reset.

Regulators truth table (see note 1).

INPUTS				OUTPUTS				
V_{P1}	V_{P2}	R4-SEL	R5-SEL	REG.1	REGS 2 & 3	REG.4	REG.5	REG.6
0	X	X	X	0	0	0	0	0
1	0	X	X	1	0	0	0	0
1	1	0	0	1	1	0	0	0
1	1	1	0	1	1	1	0	1
1	1	0	1	1	1	0	1	1
1	1	1	1	1	1	0	0	1

Note

1. 0 = LOW/OFF;
   1 = HIGH/ON;
   X = don't care.

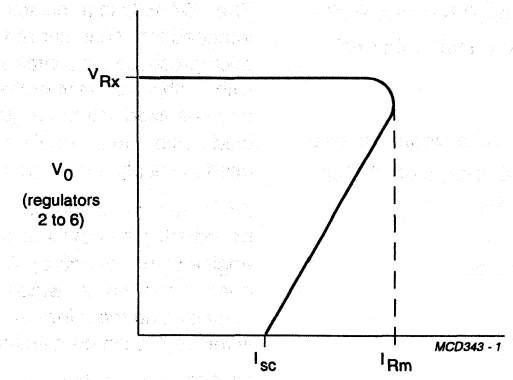
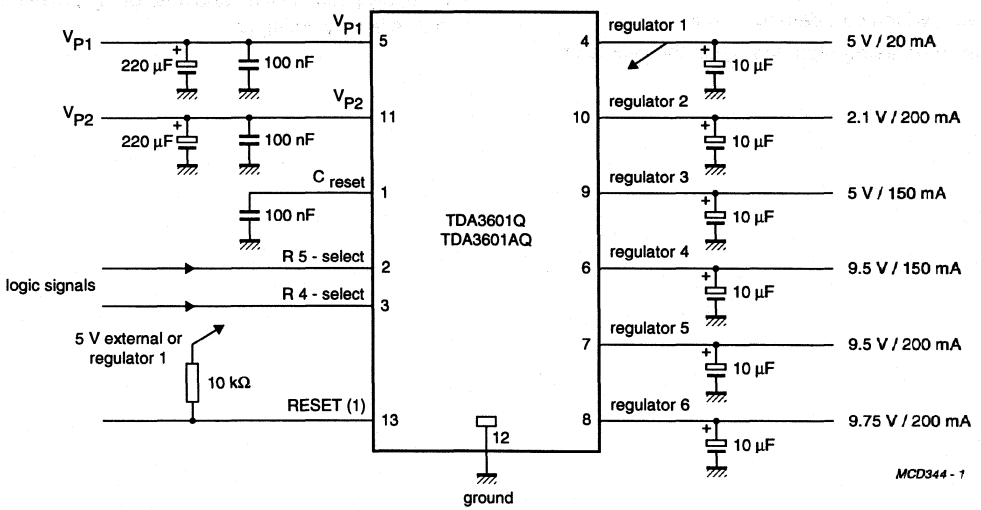


Fig.4 Foldback current protection behaviour.

TEST AND APPLICATION INFORMATION



(1) RESET output for TDA3601Q; $\overline{\text{RESET}}$ output for TDA3601AQ.

Fig.5 Application circuit.

Multiple output voltage regulator TDA3602

FEATURES

- Two V_P state controlled regulators (REG1 and REG2)
- Regulator 3 operates during load dump or thermal shutdown
- Multi-function control pin
- A back-up circuit for Regulator 3 via a single capacitor
- Supply voltage of –6 V to 50 V (a voltage of –3 V on V_P does not discharge capacitor C_{bu})
- Low reverse current Regulator 3
- Low quiescent current in coma mode
- HOLD output
- RESET output (LOW at load dump)
- High ripple rejection.

PROTECTIONS

- Foldback current limit protection (Regulators 1 and 2)
- Load dump protection
- Thermal protection
- DC short-circuit safe to ground and V_P of all regulator outputs
- Reverse polarity safe of pin 1 (V_P). No high currents are flowing which can damage the IC
- Capable of handling high energy on the regulator outputs.

GENERAL DESCRIPTION

The TDA3602 is a multiple output voltage regulator, intended for use in car radios with or without a microprocessor. It contains two fixed voltage regulators with foldback current protection (Regulators 1 and 2), and one fixed voltage regulator that also operates during load dump and thermal shutdown. This regulator can be used to supply a microprocessor.

A back-up circuit supplies Regulator 3 during a short period after the power is cut off (negative field decay or engine start procedure). A state control pin (pin 4) controls the device, which can be switched through four stages using the information at this pin. The switching levels at this pin contain hysteresis.

RESET and HOLD outputs can be used to interface with a microprocessor. The RESET signal can be used to call up or initialize a microprocessor (power-on reset). The HOLD signal can be used to control the power stages (mute signal in a low end application), or to generate a HOLD interrupt (microprocessor application).

An internal Zener diode on the back-up pin allows this pin to withstand a load dump when supplied by the pin using a 100 Ω series resistor.

The supply pin can withstand load dump pulses and negative supply voltages.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_P	positive supply voltage					
	operating		9.2	14.4	18	V
	Regulator 3 on		6.0	14.4	18	V
	jump start		–	–	30	V
	load dump; Regulator 3 on		–	–	50	V
	operating	note 1	6.5	–	30	V
	load dump; Regulator 3 on	note 1	–	–	50	V
I_P	total quiescent current	coma mode	–	290	–	µA
T_{vj}	virtual junction temperature		–	–	150	°C
Voltage regulators						
V_{R1}	output voltage Regulator 1	$0.5\ mA \leq I_{R1} \leq 250\ mA$	8.2	8.5	8.8	V
V_{R2}	output voltage Regulator 2	$0.5\ mA \leq I_{R2} \leq 140\ mA$	4.8	5.0	5.2	V
V_{R3}	output voltage Regulator 3	$0.5\ mA \leq I_{R3} \leq 50\ mA$	4.8	5	5.2	V

Note

1. V_{bu} (pin 8) supplied by V_{P2} with a 100 Ω series resistor and $I_{REG3} < 10\ mA$.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA3602	9	SIL	plastic	SOT110

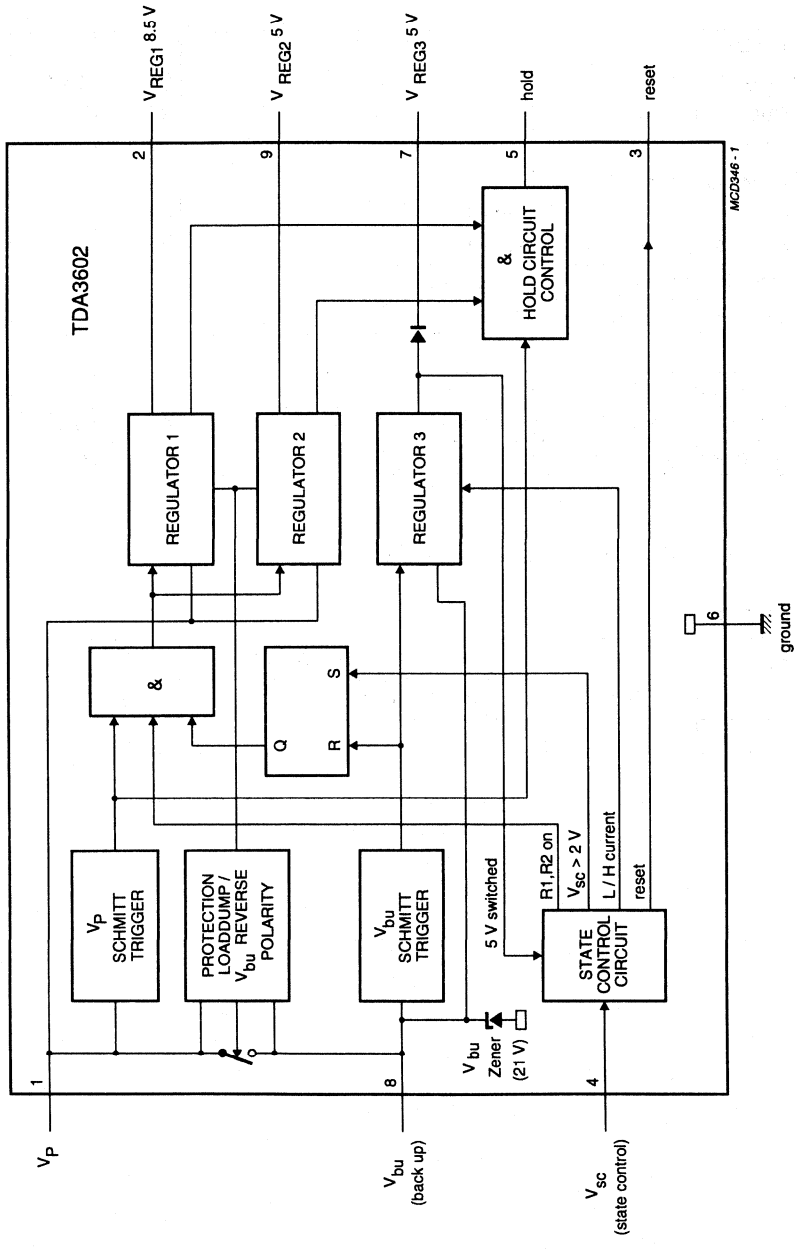


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
V_P	1	positive supply voltage
REG1	2	Regulator 1 output
RESET	3	reset output
V_{sc}	4	state control input
HOLD	5	hold output
GND	6	ground
REG3	7	Regulator 3 output
V_{bu}	8	back-up
REG2	9	Regulator 2 output

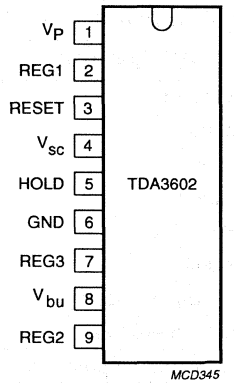


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

This multiple output voltage regulator contains three fixed voltage regulators, numbered 1, 2 and 3. Two of these can be switched between the on and off states using the state control pin (pin 4). The third (Regulator 3), which is continuously in, can be switched by the state control pin between a low and a high current mode.

In addition to Regulators 1 and 2, the device is supplied by an internal switch that is open when the supply voltage falls below the back-up voltage (negative field decay or engine start procedure), or during a load dump. (During this load dump, Regulators 1 and 2 are switched off and RESET is switched LOW). This switched supply voltage (the so-called back-up voltage (V_{bu}), is available at pin 8. An electrolytic capacitor can be connected to this pin, and the charge on this capacitor can be used to supply the device for a short period after the supply voltage is removed.

Three pins are provided for interfacing with a microprocessor:

- state control pin
- hold output pin
- reset output pin.

When the supply voltage (V_P) is connected to the device, V_{bu} will rise. When V_{bu} reaches 7.9 V, the device is in the power-on mode. The RESET output goes HIGH and Regulator 3 is switched on. In a microprocessor application, the RESET output can be used to call up the CPU and to initialize the program. What follows depends on the voltage at the state control pin (V_{sc}). In most applications, when the supply voltage is connected, V_{sc} will rise slowly (e.g. by charging a capacitor).

The device will leave the power-on mode and enter the reset mode when V_{sc} rises above 2.2 V. In both the power-on and reset modes, Regulator 3 will be in the high current mode, Regulators 1 and 2 will be switched off and the RESET output will be HIGH.

The device will enter the wake mode when V_{sc} reaches 2.8 V. The RESET pin will go LOW and the CPU must be switched to the sleep mode. Regulator 3 is still in the high current mode.

As V_{sc} continues rising and the voltage reaches 3.6 V, the stabilizer will be switched into the sleep mode. It will be in a coma mode when V_{sc} is greater than 3.8 V. In this mode, only the relevant circuits remain operating; this is to keep the power consumption as low as possible i.e. typically 290 µA.

If the device is switched on with V_{sc} already higher than 3.8 V, the device will be switched directly from the power-on mode into the coma mode.

When V_{sc} is lowered gradually from 3.6 V (or higher) to 2 V, the device will go from sleep to reset again.

V_{sc} must be lower than 1.1 V to bring the device into the on mode; note that this is not the same as the power-on mode. In this condition, Regulator 3 is in the high current mode, both Regulators 1 and 2 are switched on and the HOLD output will be HIGH (depending on the state of V_P and the in-regulation condition of Regulators 1 and 2). When the device is in the on mode, it will switch back to the reset mode when V_{sc} rises to 2 V, or when the supply voltage drops below 7.3 V.

When V_{REG3} drops below 3 V, the device will return to the power off mode, regardless of the condition the device was in.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_P	supply voltage				
	operating		–	18	V
	jump start	$t \leq 10$ min	–	30	V
	load dump	$t \leq 50$ ms; $t_r \geq 2.5$ ms	–	50	V
	Regulator 3 on	$V_P > -3$ V; note 1	–	30	V
	load dump	$t \leq 50$ ms; $t_r \geq 2.5$ ms; note 1	–	50	V
	reverse battery voltage		−6	–	V
T_{stg}	storage temperature	non-operating	−55	+150	°C
T_{vj}	virtual junction temperature	operating	−40	+150	°C
V_{pr}	reverse polarity	non-operating	–	6	V
P_{tot}	total power dissipation		–	15	W

Note

1. V_{bu} (pin 8) supplied by V_{P2} with a 100 Ω series resistor and $I_{REG3} < 10$ mA.

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient in free air	50 K/W
$R_{th\ j\text{-}c}$	from junction to case (see Fig.6)	12 K/W

CHARACTERISTICS

$V_P = 14.4$ V; $T_{amb} = 25$ °C; measured in Fig.6; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_P	supply voltage					
	operating		9.2	14.4	18	V
	Regulator 3 on	note 1	6.0	14.4	18	V
	jump start	$t \leq 10$ min	–	–	30	V
	load dump	$t \leq 50$ ms; $t_r \geq 2.5$ ms	–	–	50	V
I_P	quiescent current	$V_{sc} > 4$ V; note 2				
	$V_P = 12.4$ V		–	280	360	µA
	$V_P = 14.4$ V		–	290	–	µA
Schmitt triggers						
V_{P2} SCHMITT TRIGGER (FOR HOLD AND REGULATORS 1 AND 2)						
V_{thr}	rising voltage threshold		7.3	7.6	8.0	V
V_{thf}	falling voltage threshold		6.8	7.1	7.5	V
V_{hy}	hysteresis		–	0.5	–	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
REGULATOR 1 SCHMITT TRIGGER (FOR HOLD)						
V_{thr}	rising voltage threshold		–	$V_{R1} - 0.2$	–	V
V_{thf}	falling voltage threshold		–	$V_{R1} - 0.3$	–	V
V_{hy}	hysteresis		–	0.1	–	V
REGULATOR 2 SCHMITT TRIGGER (FOR HOLD)						
V_{thr}	rising voltage threshold		–	$V_{R2} - 0.2$	–	V
V_{thf}	falling voltage threshold		–	$V_{R2} - 0.3$	–	V
V_{hy}	hysteresis		–	0.1	–	V
VBU SCHMITT TRIGGER (REGULATOR 3)						
V_{thr}	rising voltage threshold V_{bu}		7.3	7.9	8.4	V
V_{thf}	falling voltage threshold V_{REG3}		2.5	3	3.5	V
V_{hy}	hysteresis		–	4.9	–	V
State control pin						
V_{th}	voltage threshold between sleep and coma	note 2	–	$V_{thr1} + 0.2$	–	V
V_{thr1}	voltage threshold wake to sleep		3.35	3.6	3.85	V
V_{thf1}	voltage threshold sleep to wake		2.5	2.7	2.9	V
V_{hy1}	hysteresis wake/sleep		0.85	0.92	1.0	V
V_{thr2}	voltage threshold reset to wake		2.6	2.8	3.0	V
V_{thf2}]	voltage threshold wake to reset		1.75	1.9	2.05	V
V_{hy2}	hysteresis reset/wake		0.85	0.92	1.0	V
V_{thr3}	voltage threshold on to reset		1.85	2.0	2.15	V
V_{thf3}	voltage threshold reset to on		1.0	1.1	1.2	V
V_{hy3}	hysteresis on/reset		0.85	0.92	1.0	V
I_{scl}	input current	$V_{sc} \leq 0.8$ V $V_{sc} \geq 4$ V	– –	– –	–1 1	µA µA
Reset output						
V_{OL}	LOW level output voltage	$I_{OL} = 0$	0	0.2	0.8	V
V_{OH}	HIGH level output voltage		2.0	5.0	5.25	V
I_{OL}	LOW level output current	$V_{OL} \leq 0.8$ V	0.3	0.8	–	mA
I_{OH}	HIGH level output current	$V_{OH} > 3$ V	–0.3	–2.0	–	mA
Hold output						
V_{OL}	LOW level output voltage	$I_{OL} = 0$	0	0.2	0.8	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{OH}	HIGH level output voltage		2.0	5.0	5.25	V
I_{OL}	LOW level output current	$V_{OL} \leq 0.8$ V; note 3	0.3	1.0	–	mA
I_{OH}	HIGH level output current	$V_{OH} > 3$ V	−1.5	−9.0	–	mA
Regulator 1 (I_{REG1} = 5 mA unless otherwise specified)						
V_{REG1}	output voltage off	$V_{sc} > 2.1$ V	–	1	400	mV
V_{REG1}	output voltage					
		$0.5 \text{ V} \leq I_{REG1} \leq 250$ mA	8.2	8.5	8.8	V
		$10 \text{ V} \leq V_P \leq 18$ V	8.2	8.5	8.8	V
ΔV_{REG1}	line regulation	$10 \text{ V} \leq V_P \leq 18$ V	–	–	50	mV
ΔV_{REGL1}	load regulation	$0.5 \text{ mA} \leq I_{REG1} \leq 250$ mA	–	–	50	mV
SVRR1	supply voltage ripple rejection	f = 200 Hz; 2 V (p-p)	60	–	–	dB
V_{REGd1}	drop-out voltage	I_{REG1} = 250 mA	–	–	0.4	V
I_{REGm1}	current limit	$V_{REG1} > 7$ V; note 4	0.4	–	1.2	A
I_{REGsc1}	short-circuit current	$R_L \leq 0.5\ \Omega$; note 4	–	250	–	mA
Regulator 2 (I_{REG2} = 10 mA unless otherwise specified)						
V_{REG2}	output voltage off	$V_{sc} > 2.1$ V	–	1	400	mV
V_{REG2}	output voltage					
		$0.5 \text{ V} \leq I_{REG2} \leq 140$ mA	4.8	5.0	5.2	V
		$8 \text{ V} \leq V_P \leq 18$ V	4.8	5.0	5.2	V
ΔV_{REG2}	line regulation	$8 \text{ V} \leq V_P \leq 18$ V	–	–	50	mV
ΔV_{REGL2}	load regulation	$0.5 \text{ mA} \leq I_{REG2} \leq 140$ mA	–	–	50	mV
SVRR2	supply voltage ripple rejection	f = 200 Hz; 2 V (p-p)	60	–	–	dB
V_{REGd2}	drop-out voltage	I_{REG2} = 140 mA	–	1.2	–	V
I_{REGm2}	current limit	$V_{REG2} > 4.5$ V; note 4	200	–	600	mA
I_{REGsc2}	short-circuit current	$R_L \leq 0.5\ \Omega$; note 4	–	130	–	mA
Regulator 3 (I_{REG3} = 5 mA unless otherwise specified)						
V_{REG3}	output voltage					
		$0.5 \text{ mA} \leq I_{REG3} \leq 50$ mA	4.8	5.0	5.2	V
		$7 \text{ V} \leq V_P \leq 18$ V	4.8	5.0	5.2	V
		$18 \leq V_P \leq 50$ V	4.8	5.0	5.2	V

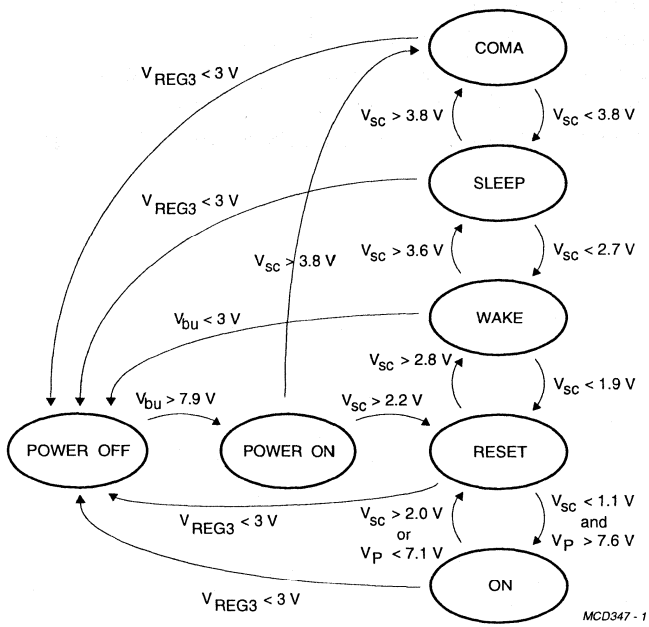
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
ΔV_{REGL3}	output voltage	sleep mode; $I_{REG3} \leq 10$ mA; note 2	4.5	5.0	5.5	V
I_{LO1}	leakage output current	$V_P = 0$; $V_{bu} = 6$ V; $V_{REG3} = 6$ V	–	–	−1	μA
ΔV_{REG3}	line regulation	$7 \text{ V} \leq V_P \leq 18$ V	–	–	50	mV
ΔV_{REGL3}	load regulation	$0.5 \text{ mA} \leq I_{REG3} \leq 50$ mA	–	–	50	mV
SVRR3	supply voltage ripple rejection	f = 200 Hz; 2 V (p-p)	60	–	–	dB
V_{REGd3}	drop-out voltage	$I_{REG3} = 50$ mA; note 5	–	–	0.4	V
I_{REGm3}	current limit	$V_{REG3} > 4.5$ V; note 6	140	–	500	mA
Switch						
V_{swd}	drop-out voltage	$I_{sw} = 50$ mA	–	–	0.45	V
I_{swm}	maximum current		140	–	–	mA

Notes

1. Minimum operating voltage only if V_P has exceeded 8 V.
2. In the sleep mode, Regulators 1 and 2 are off. In the coma mode, the state control circuit is also switched off, to make the quiescent current as low as possible.
3. Hold circuit can sink this current in the RESET state and the ON state.
4. The foldback current protection limits the dissipated power at short-circuit (see Fig.5).
5. The drop-out voltage of Regulator 3 is measured between V_{bu} and V_{REG3} (pins 8 and 7).
6. At current limit, I_{REGm} is held constant (behaviour in accordance with the broken line in Fig.5)

Table 1 State control pin.

V_{P1} SCHMITT TRIGGER IS TRUE				
STATE	**REG3 (5 V)**	**REG1 + REG2**	**RESET**	**REMARKS**
Coma	LOW current	off	0	stabilizer consumes low quiescent current; state control circuit is switched off to lower the quiescent current
Sleep	LOW current	off	0	state control circuit on
Wake	HIGH current	off	0	CPU in sleep mode
Reset	HIGH current	off	1	CPU called up
On	HIGH current	on	1	normal operation
Power on	HIGH current	off	1	V_{P1} rises from 0 to 8.5 V or higher (first start-up)
Power off	off	off	0	V_{P2} falls from V_P to less than 3 V (V_{REG3} = 2.5 V)



V_{bu} = back-up voltage.
V_{sc} = state control voltage.
V_{REG3} = Regulator 3 output voltage.

Fig.3 State diagram.

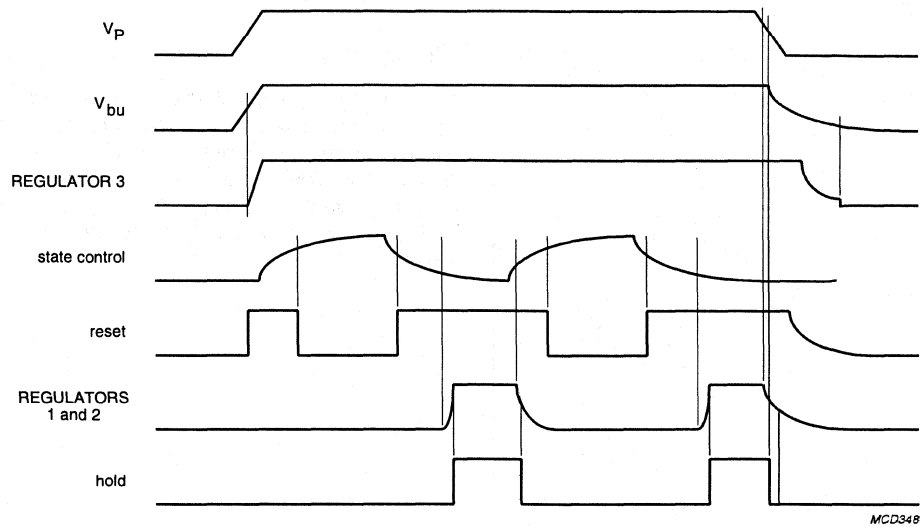


Fig.4 Timing diagram.

Table 2 Logic table HOLD function.

INPUTS FOR HOLD (note 1)					OUTPUT
V_{bu}	V_P SCHMITT TRIGGER	ON STATE	REG1	REG2	HOLD
1	0	X	0	0	0
0	1	X	0	0	0
1	1	0	0	0	0
1	1	1	0	X	0
1	1	1	X	0	0
1	1	1	1	1	1

Note

1. 0 = off; 1 = on; X = don't care.

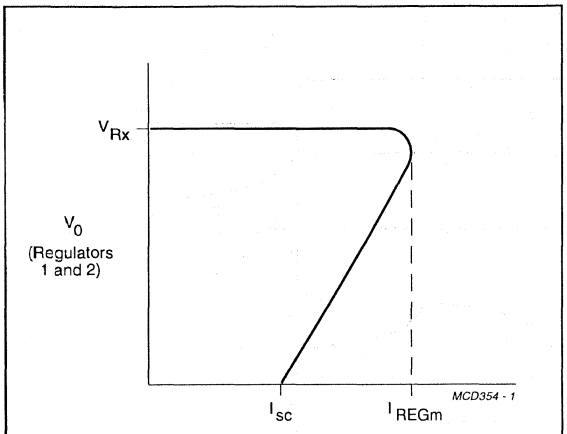


Fig.5 Foldback current protection.

QUALITY SPECIFICATION

Quality in accordance with UZW-BO/FQ-0601.

TEST INFORMATION

The outputs of the regulators are measured by means of a selector switch (one by one). In addition, switch SW2 is only closed when V_{bu} is greater than V_P; then the internal switch of the TDA3602 is opened. V_{bu} (pin 8) can only withstand a 50 V load dump pulse when switch SW2 is kept open or when switch SW2 is replaced by a 100 Ω resistor.

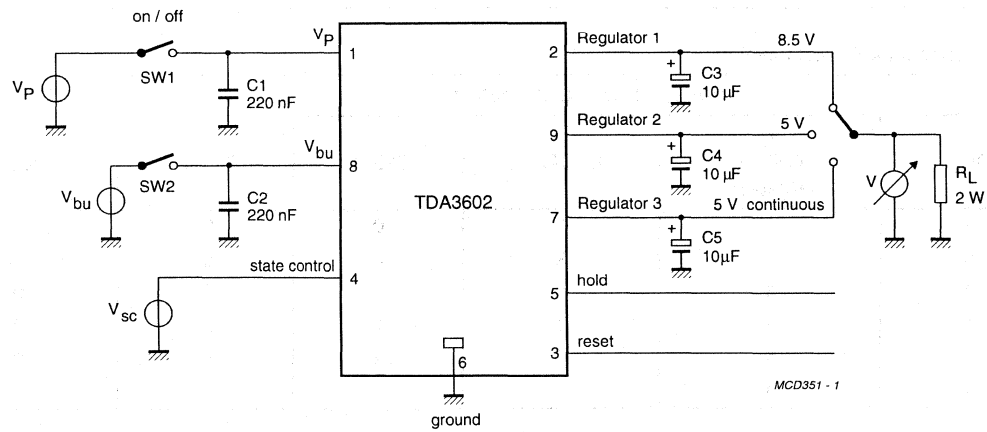


Fig.6 Test circuit.

APPLICATION INFORMATION

Noise

Table 3 Noise at regulator outputs dependent on capacitive load (C_L).

REGULATOR (note 1)		C_L		
REG	I_L	10 µF	47 µF	220 µF
1	150 mA	800 µV	220 µV	160 µV
2	100 mA	500 µV	115 µV	
3	50 mA	350 µV	190 µV	

Note

1. Regulators loaded with 100 mA; noise in µV RMS (B = 10 Hz to 1 MHz).

The available noise at the output of the regulators depends on the bandwidth of the regulators, which can be adjusted by means of the load capacitors. The noise figures are given in Table 3.

Although stability is guarenteed when C_L is higher than 10 µF (over temperature range) with tan (ϕ) = 1 in the frequency range 1 kHz to 20 kHz, it is recommended to use a 47 µF load capacitor for Regulators 1 and 2. When a microprocessor is supplied by Regulator 3 much noise can be produced by this microprocessor. This noise is not influenced by increasing the load capacitor of Regulator 3.

The noise on the supply line depends on the supply capacitor. When a high frequency capacitor of 220 nF with an electrolytic capacitor of 100 µF in parallel is placed directly over pin 1 (V_P) and pin 6 (ground) the noise is minimized.

The stabilizer is in 'power on' after the supply is reconnected ($V_{bu} > 7.9$ V) and $0.1 < V_{sc} < 2.2$ V.

Application circuits

STABILIZER WITHOUT MICROPROCESSOR 1

The low end application is illustrated in Fig.7. When switch SW1 is closed, a pulse is generated at the state control input by C5 and R1, and the regulator is switched from power off to the on mode (all three regulators are on). The HOLD signal can be used to control the mute signal for the power amplifiers. This signal is HIGH when all the regulators are in regulation and V_{P1} Schmitt trigger is true.

STABILIZER WITHOUT MICROPROCESSOR 2

Fig.8 illustrates the application circuit for a low end radio set with push switches when no microprocessor is used. The stabilizer can be switched to the on mode by pressing switch SW1. In this mode, Regulators 1 and 2 are switched on, so transistor T1 takes over from switch SW1. The stabilizer can only be switched off by connecting the base of T1 to ground (SW1 not pressed). This can be achieved by pressing switch SW2.

The hold signal is only HIGH when the device is in the on mode and both V_P and the regulators are available, so that this signal can be used to control the power stages (mute). During a fault condition, this signal turns LOW immediately.

When the stabilizer is connected to the supply for the first time, the initial state will be the power-on stage, so Regulators 1 and 2 are not switched on.

STABILIZER USED WITH MICROPROCESSOR

For a good understanding of the high end application, shown in Fig.10, consult the flow chart of Fig.9.

When the set is off, a reset can be generated by connecting the set to the supply for the first time (stabilizer in power-on), or by pressing any key on the key matrix (stabilizer in reset mode). When the reset is generated, the stabilizer is held in the reset mode for a short period by T1. The microprocessor has to take over control by making reset mode equal to 0. The microprocessor can then proceed with the initializing process. After this action, the microprocessor has to check if the correct key has been pressed. If so, the radio can be switched on by making on equal to 0; if not, the microprocessor must switch the device to the coma mode again, by making reset mode and on both equal to 1; (wake mode is entered after a short time constant, determined by R1 x C7 x constant), and switch itself to sleep mode.

When the reset is generated for the first time (power-on mode), the mode of the device can be detected by the hold signal. If on = 0 and hold remains LOW, then the microprocessor is in the power-on mode. In this event, the microprocessor must go to the switch-off routine (making on and reset mode both equal to 1).

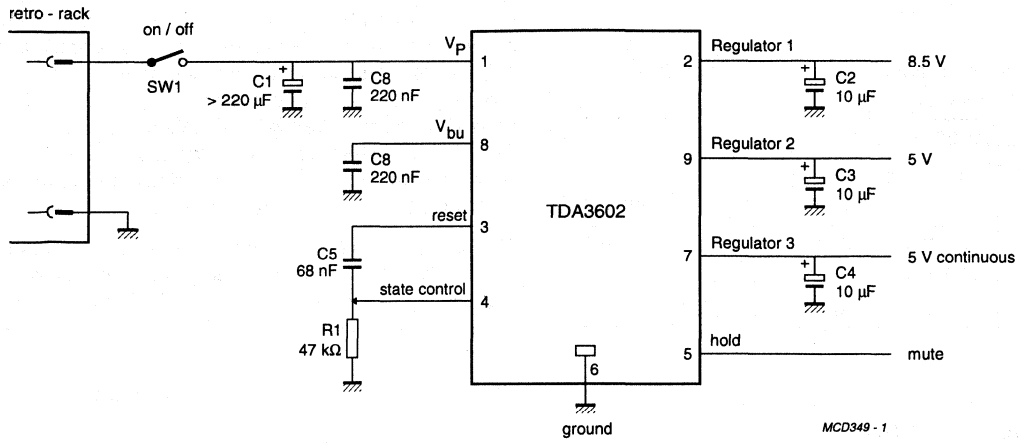


Fig.7 Low end application circuit.

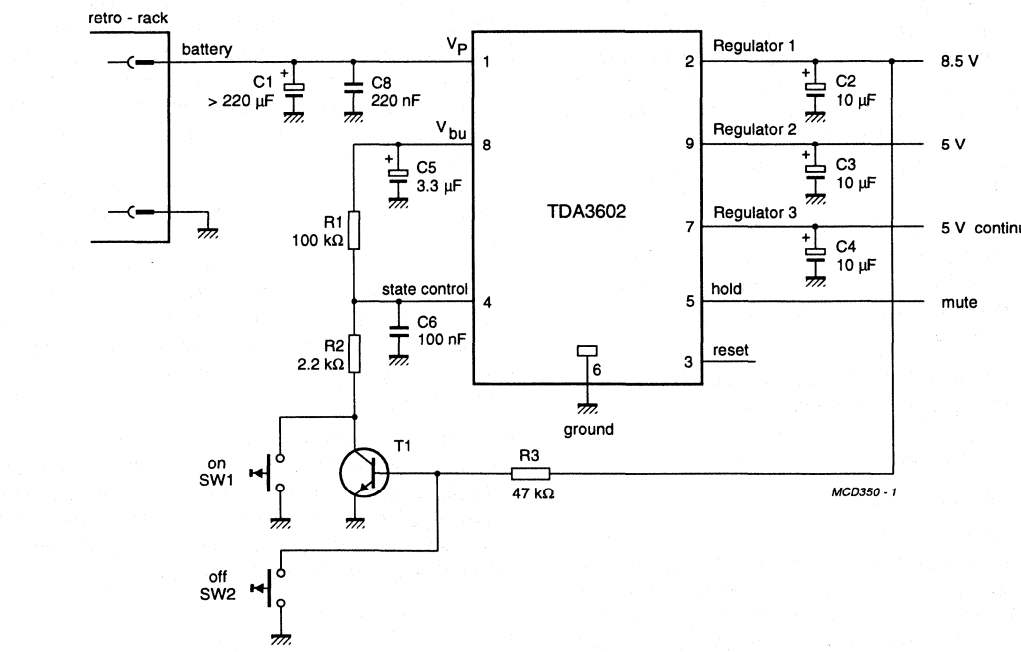


Fig.8 Application circuit 2.

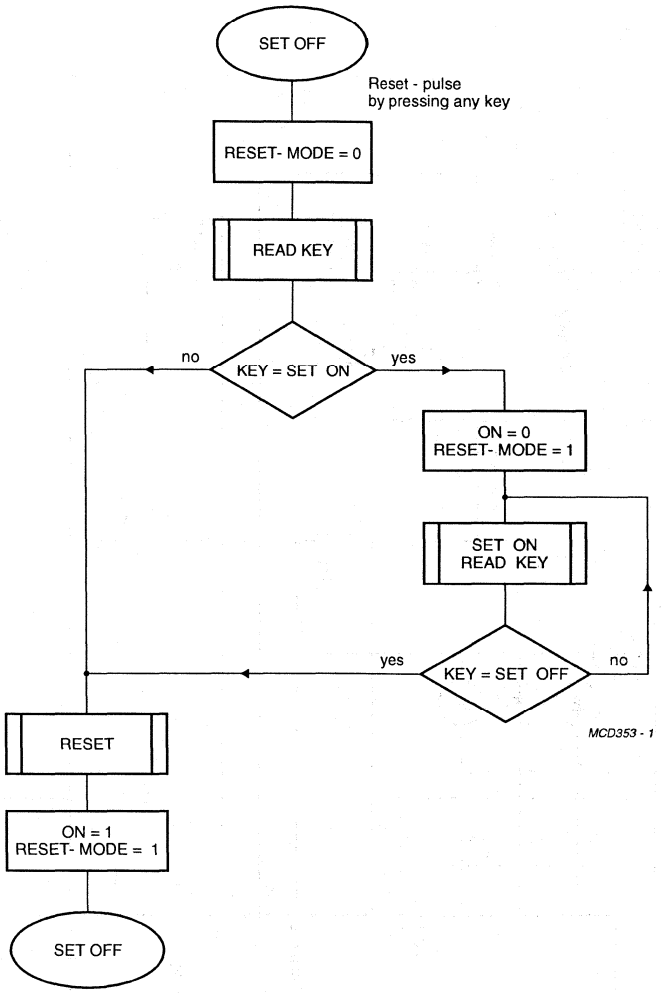


Fig.9 Flow chart for high end application.

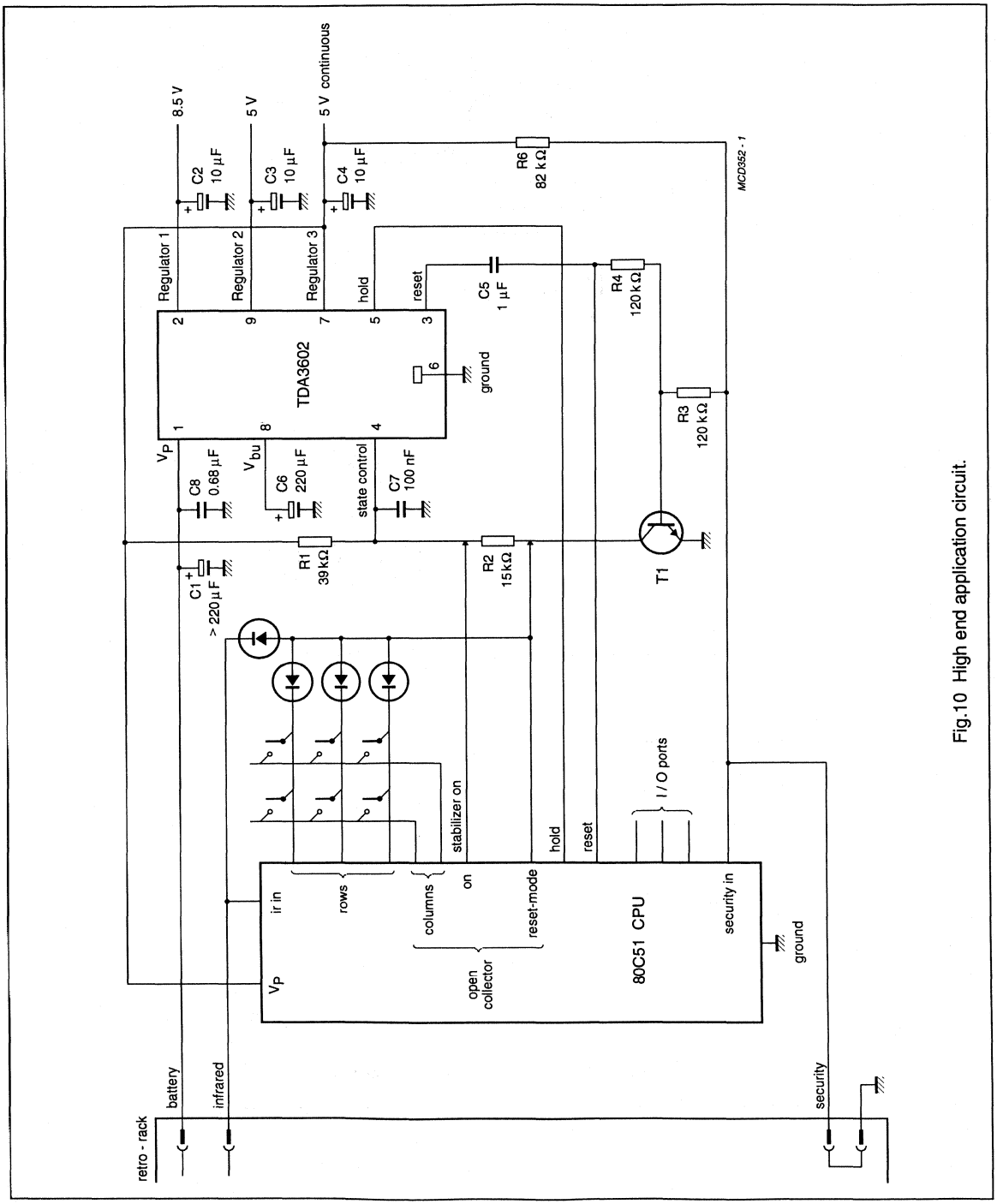


Fig.10 High end application circuit.

Example of a modern car radio design with the TDA3602

DESIGN CONSIDERATIONS

A modern car radio set meets the following design considerations:

1. Semi on/off logic. The radio set has to switch on/off by pressing the on/off key or by switching the ignition
2. Security code check
3. Low quiescent current in standby (this means that the microprocessor is off when the set is off)
4. The set must recover the state it had before an engine start or load dump
5. Apart from HOLD, RESET and V_P only two more I/O lines are used for full on/off logic
6. Supply by 1 or 2 supply lines
7. Radio Data System (RDS) should be implemented in the set, but this is not a regulator problem
8. Lights must switch off during load dump

Although the TDA3602 is designed only to be supplied by a continuous supply (battery), it is also possible to use both a continuous and a switchable supply (ignition). The ignition can be used to supply also the TDA3602, although in this event additional circuitry is needed.

APPLICATION CIRCUIT WITH (SEMI-)FULL ON/OFF LOGIC

The application circuit of Fig.11 will meet all the above mentioned design considerations. Three circuit parts can be distinguished:

Reset circuitry

A reset is required to call-up the microprocessor when it is switched to the sleep mode or the power-on reset (first initialization of the microprocessor). To achieve this, three different types of resets should be generated:

1. When the set has been disconnected from the supply, the microprocessor must be initialized at connection to the supply for the first time. The output ports of the microprocessor are in a random state. To ensure correct initialization, a reset has to be generated. This is accomplished by the power-on state of the TDA3602. In this state the reset output is HIGH and Regulators 1 and 2 are disabled (despite the voltage on the state control pin V_{sc} being below 1.1 V). Only after the voltage on the state control pin has risen above 2.2 V can Regulators 1 and 2 be switched on again by pulling the state control pin below 1.1 V.
2. In the sleep mode the microprocessor should be called up by pressing the on/off key (normal off condition). Now the reset is also generated by the RESET output of the TDA3602. This reset output will go HIGH when V_{sc} decreases from the value V_{REG3} to below 1.9 V.
3. At fault conditions (V_P below 7.1 V, $V_{REG1} < V_{REG1}$ nominal −0.3 V or $V_P > 1$ 8 V), HOLD drops to logic 0 and the microprocessor switches off the set. In accordance with the design considerations is that the mode of operation must switch to the state it was in before an engine start or load dump occurred. To achieve this the HOLD output of the TDA3602 can be used to generate a reset pulse (only when V_{sc} remains below 1.1 V).

The RESET and HOLD outputs of the TDA3602 are combined to generate the reset pulses. The pulses are created by differentiating the outputs, using capacitors C8 and C9. The reset pulses are added by means of the diodes D2 and D3. The time constants are:

- $tres_{res(rise)} = 3 \times R7 \times C8 = 3 \times 10\,k\Omega \times 1uF = 30$ ms

  on/off button S1 should be pressed for at least 30 ms, before the microprocessor will see this
- $tres_{hold(rise)} = 3 \times R7 \times C9 = 5.4$ ms
- $tres_{(dis)} = 3 \times R8 \times C8 = 140$ ms
- $tres_{hold(disl)} = 3 \times R9 \times C9 = 25$ ms

  the microprocessor has to wait and check if HOLD remains LOW for at least 25 ms before it switches off; now it is certain that a correct reset will occur to wake up the microprocessor again.

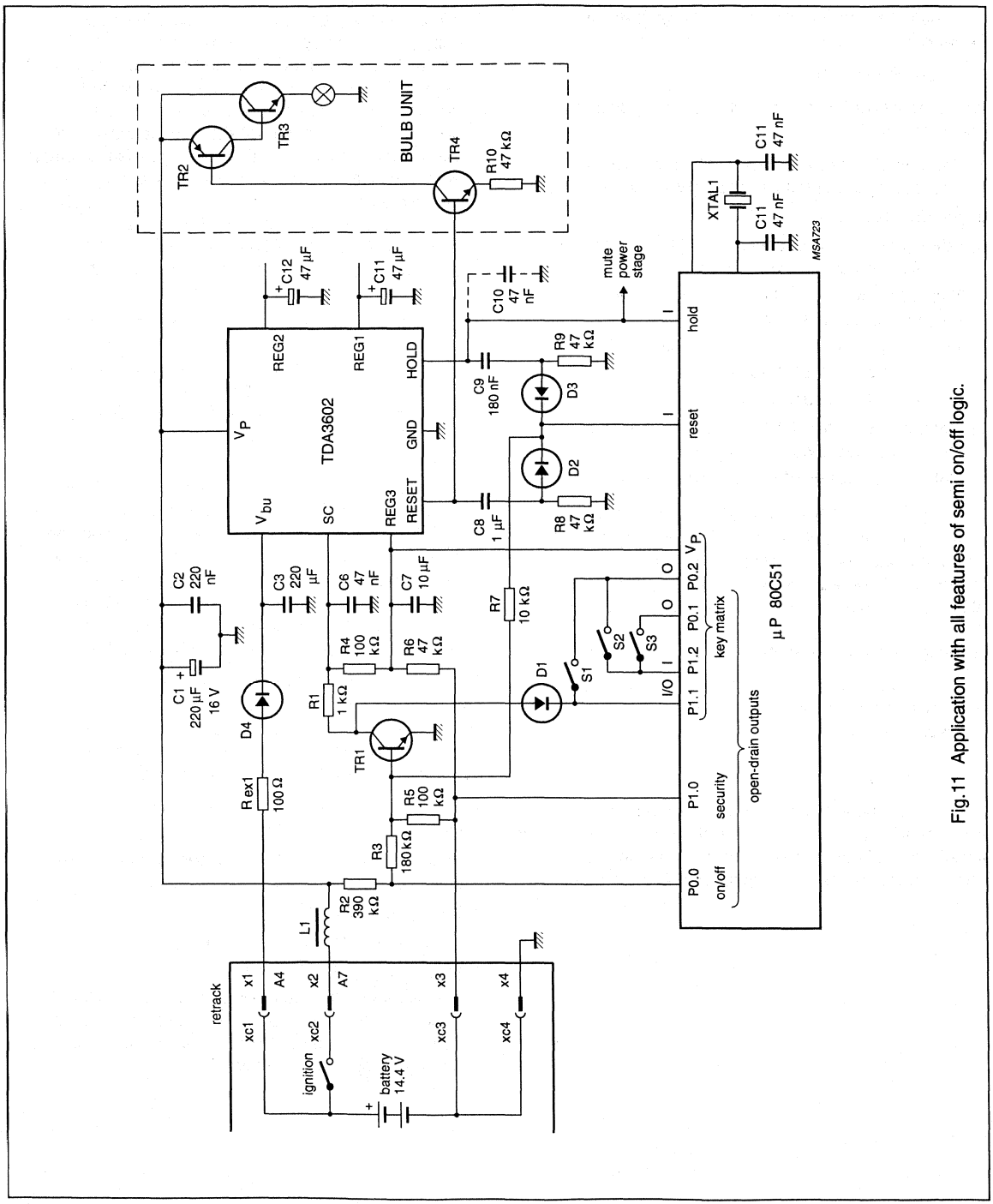


Fig.11 Application with all features of semi on/off logic.

A reset by the hold function can only be created when the state control pin remains LOW. This is accomplished by means of transistor T1 when Port P0,0 is high ohmic. Because of resistors R2, R3 and R5 the transistor will switch off when $V_{ignition}$ falls below a level of 5.0 V. During an engine start, when $V_{ignition}$ reaches voltages as low as 5 V, the transistor will switch off. Regulators 1 and 2 are already switched of by means of the V_P Schmitt-trigger, causing the HOLD output to go LOW. When $V_{ignition}$ again increases the transistor will be switched on again (Port P0,0 has to be open = logic 1), thereby switching the state control pin to 0 V. As $V_{ignition}$ continues to increase above 7.6 V (V_{rise} of the V_{P1} Schmitt-trigger) Regulators 1 and 2 will again switch on causing the HOLD output to go HIGH, creating a new reset pulse.
The set can also be switched off by opening the ignition key, causing transistor T1 to switch off. When the ignition key is closed again, the set will restart to the original situation that existed before the ignition key was opened. The charge time of C6 equals 3 x R4 x C6 = 14 ms. This is less than the reset time $tres_{res(rise)}$. To avoid the TDA3602 switching to coma mode before the microprocessor is awakened, a double function has been given to T1. During a reset pulse T1 is on (because of resistor R7), thus V_{sc} will remain 0 V provided a reset occurs. After the reset pulse has disappeared, the microprocessor is able to fully control V_{sc} by mean of Port P0,0 or Port P1,1.

Security code circuitry

When the set is off and it is pulled out of RETRACK, x3 and x4 are disconnected thereby switching the base of transistor T1 to the output voltage of Regulator 3 (using resistors R5 and R6). Transistor T1 is starting to conduct and a RESET pulse is generated. The microprocessor is activated and checks if Port P1,0 = logic 1. If this is so, the microprocessor knows that the set is pulled out of RETRACK and that time is limited to finish the program correctly (because the microprocessor is operating on the charge of capacitor C3). The security flag has to be set in an EEPROM and the microprocessor can switch to power-down before Regulator 3 switches to power-off.

Another possibility is that the set was running and pulled out of RETRACK. Now a hold is generated, and the hold interrupt routine has to check the security in Port P1,0.

R6 is an internal resistor in the microprocessor. An external resistor limits however the spread.

Bulb circuitry

The lights are switched on provided the RESET output of the TDA3602 is HIGH. This normally occurs when the set is switched on. Only at first connection (power-off) will the RESET output be HIGH when the set is off. In this event the lights are also switched on. This is not a problem because the required time for initializing the microprocessor will be very short.

When a load dump occurs, the RESET output will go LOW, disabling the lights. With the aid of this feature it is possible to prevent the light bulbs being damaged at load dump.

Noise.

Regulators 1 and 2 are loaded with a 47 µF/16 V load capacitor because of output noise. With this value the output noise will be lower than 220 µV for Regulator 1 and lower than 120 µV for Regulator 2 (see Table 3 and associated text).

To minimize the noise on the supply line, capacitors C1 and C2 should be placed as close as possible across the supply and ground pins of the TDA3602.

Timing diagram

In the timing diagram all of the situations which can occur are shown (see Fig.12). A HIGH of switch S1 indicates that S1 is pressed. A HIGH on Port P0,0 indicates that Port P0,0 is high ohmic (Port P0 is an open-collector output). If no open-collector output is available another port can be used, but an extra diode has to be added in series with this port to prevent T1 being switched on by this port. A HIGH for the microprocessor indicates that the microprocessor is operating, a LOW indicates that the microprocessor is in standby mode.

The following situations are covered in the timing diagram:

1. Initialization of the microprocessor (TDA3602 in power-off mode)
2. Switching the ignition with the set off (Port P0,0 = logic 0)
3. Switching the set on/off/on by pressing S1 sequentially (ignition available)
4. Switching behaviour at engine start and load dump (set on)
5. Switching the set off and on again by switching the ignition.

The timing diagram can only be understood after a thorough investigation of the flow charts (see section Flow chart semi on/off logic with security code). Furthermore short and long RESET pulses can be seen (see Fig.12).

Flowchart semi on/off logic with security code

This section describes the software for controlling the TDA3602 (semi on/off logic). A "o" in the flowchart flow diagram Fig.13, indicates that the port mentioned is switched as an output. A "1" indicates that the port mentioned is switched as an input (temporarily).

The flowchart of figure 13 can be used for semi on/off logic.

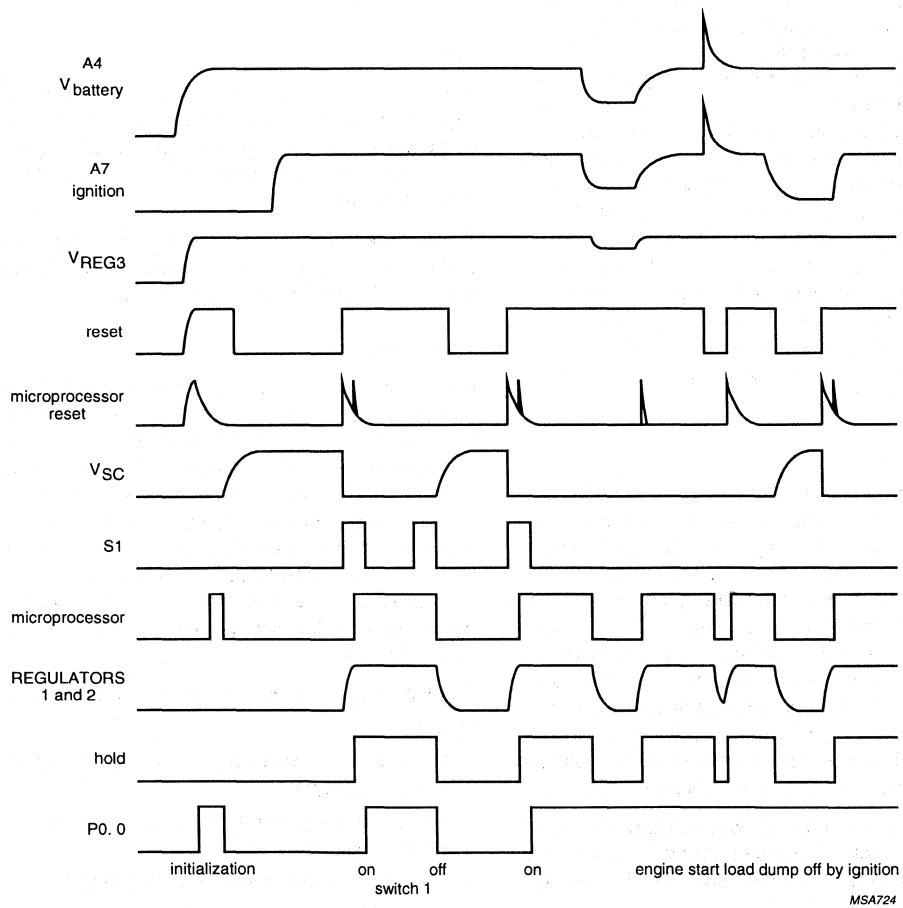


Fig.12 Timing of the applications.

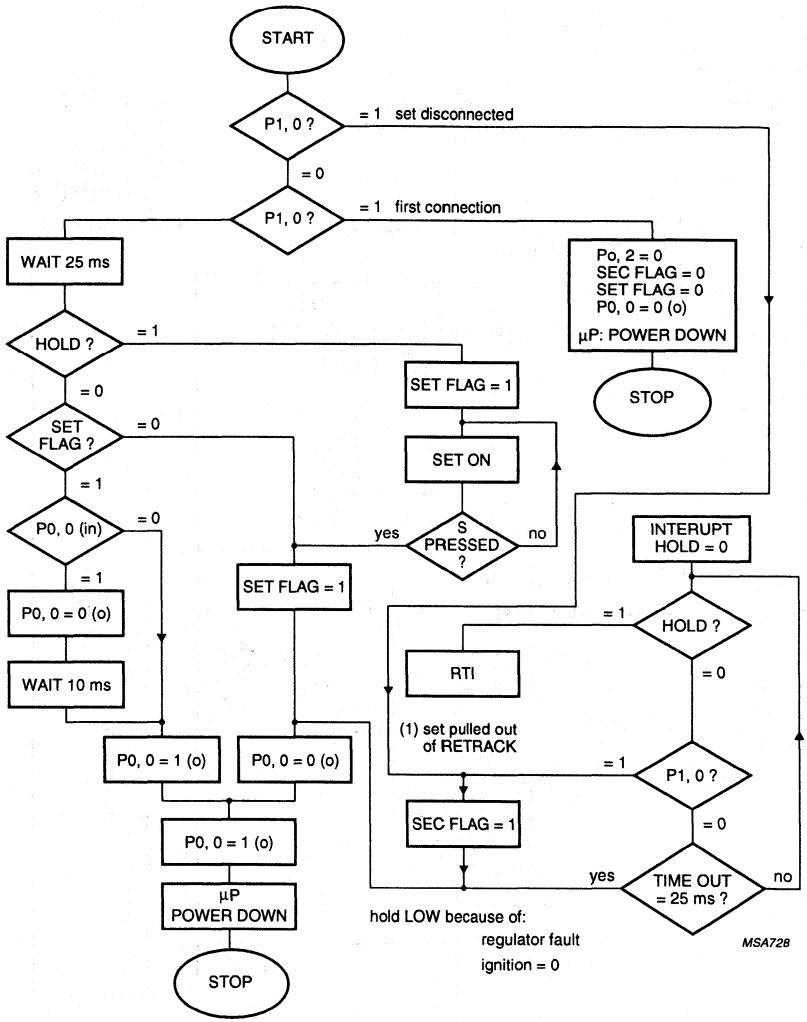


Fig.13 Interfacing flow chart TDA3602.

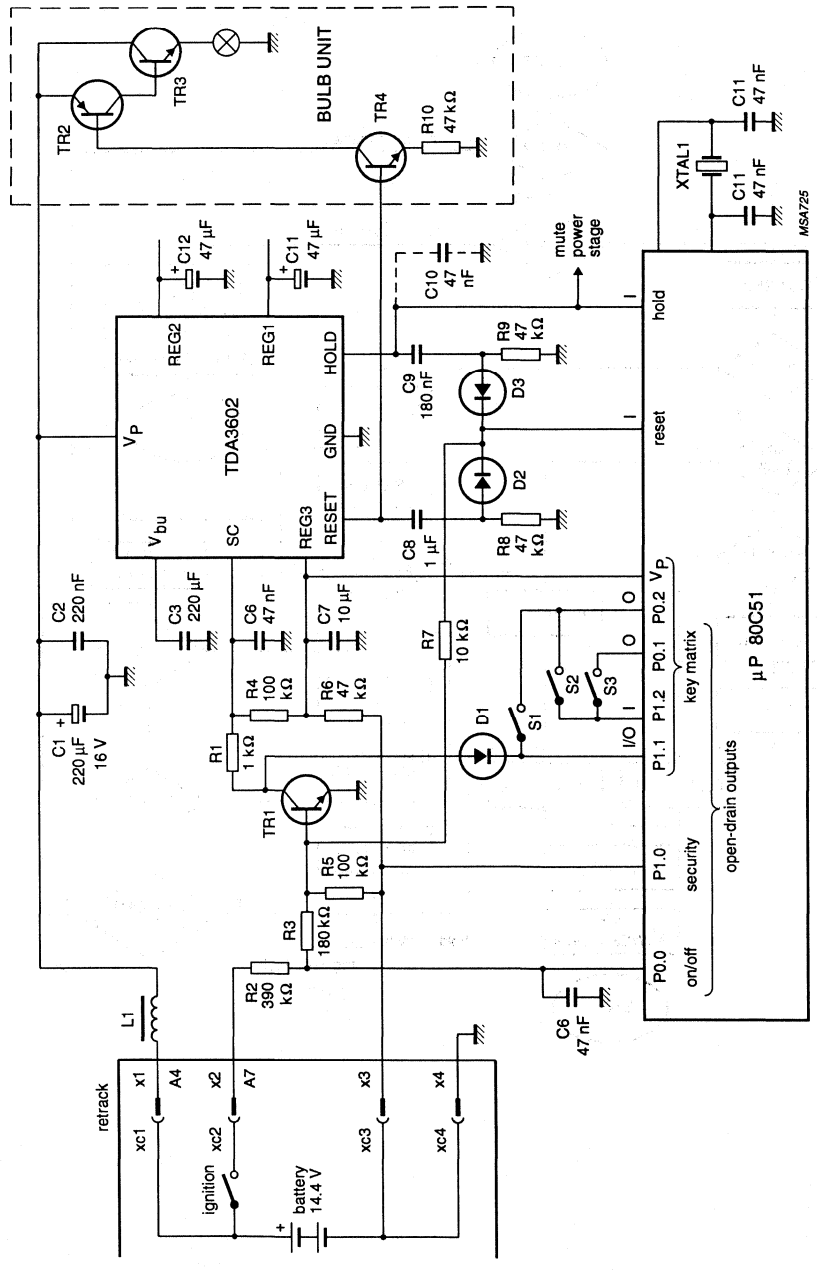


Fig.14 Application with all features of full on/off logic.

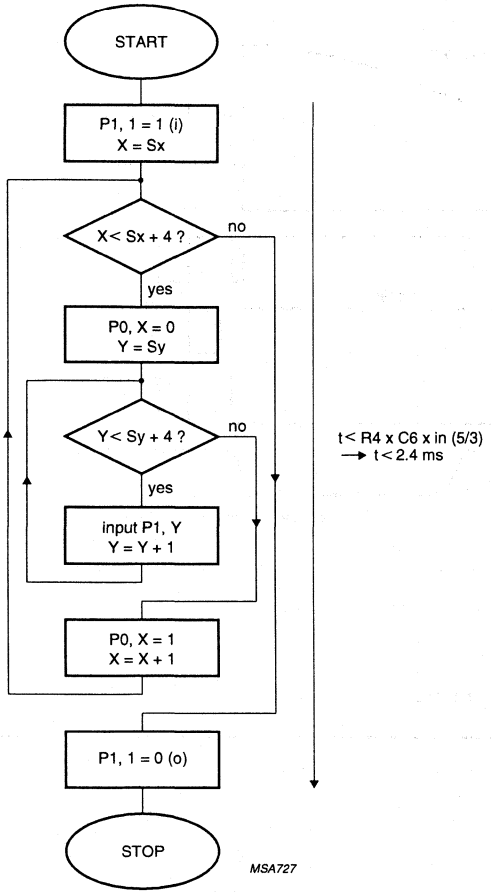


Fig.15 Software key matrix with loops.

FULL ON/OFF LOGIC

Using application circuit Fig.14, full on/off logic can be achieved. Also extra software loops are required to enable the set when ignition is off. The set can be controlled by Port P1,1 if the ignition is off (thus no extra I/O ports of the microprocessor are required for full on/off logic).

Because Port P1,1 is a part of the key matrix the complete key-scan loop must be finished within less than 0.5 x R4 x C6 = 2.4 ms, otherwise the TDA3602 will enter the reset state and Regulators 1 and 2 are switched off during this key-scan loop. When the time of the complete loop is within 2.4 ms the V_{sc} will remain below 2 V (thus Regulators 1 and 2 remain on).

It is also possible to switch Port P1,1 during the key-scan loop sequentially from output (logic 0) to input. If this is achieved within a time period of 1 ms, V_{sc} cannot become HIGH long enough to switch Regulators 1 and 2 off.

When ignition is available, transistor T1 overrules Port P1,1. In this event no variation on V_{sc} is seen during the key-scan loop.
The flow chart presented in Fig.15 is only required for the full on/off logic application of Fig.14.
The complete key-scan routine must be finished within 2.4 ms (when ignition is off) and that the key-scan routine has to end with a statement P1,1 = logic 0. In the flow chart of the key-scan routine, Sx is the start value of the rows and Sy the start value of the columns. With Sx = 1 and Sy = 1, one '0' is shifted on the output ports P0,1 to P0,5 and the input ports P1,1 to P1,5 are being read sequentially per shift action.

Connections between microprocessor and Regulator 2 supplied

When digital ICs, supplied by Regulator 2, are connected to I/O ports (especially Ports 1 and 2), special attention in the software has to be taken to avoid currents flowing from Regulator 3 to Regulator 2. Because of ESD diodes in digital ICs a current can flow from an output port (which is in a high state) through the ESD diode into Regulator 2. This will cause an increase in the quiescent current of the set. The recommended action to avoid this problem is to switch the specific I/O ports to logic 0.

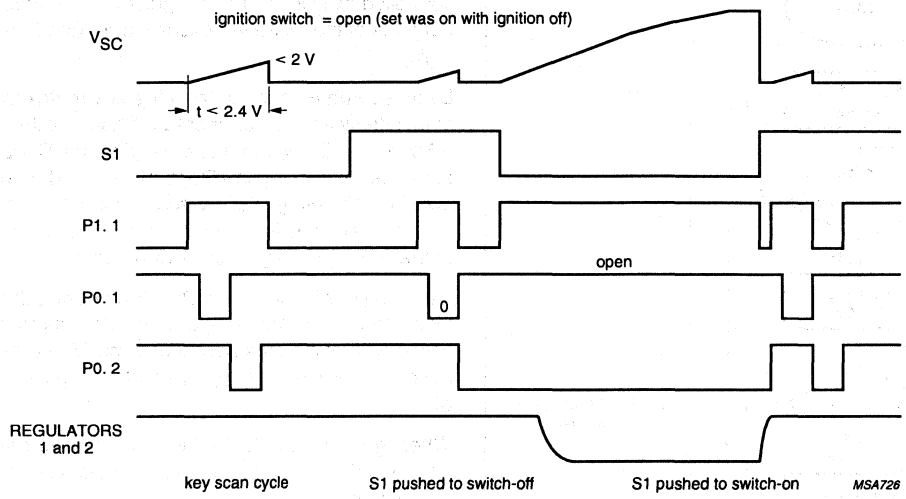


Fig.16 Timing key matrix.

FM RADIO CIRCUIT

GENERAL DESCRIPTION

The TDA7000 is a monolithic integrated circuit for mono FM portable radios, where a minimum on peripheral components is important (small dimensions and low costs).

The IC has an FLL (Frequency-Locked-Loop) system with an intermediate frequency of 70 kHz. The i.f. selectivity is obtained by active RC filters. The only function which needs alignment is the resonant circuit for the oscillator, thus selecting the reception frequency. Spurious reception is avoided by means of a mute circuit, which also eliminates too noisy input signals. Special precautions are taken to meet the radiation requirements.

The TDA7000 includes the following functions:

- R.F. input stage
- Mixer
- Local oscillator
- I.F. amplifier/limiter
- Phase demodulator
- Mute detector
- Mute switch

QUICK REFERENCE DATA

Supply voltage range (pin 5)	V_P	2,7 to 10	V
Supply current at V_P = 4,5 V	I_P	typ. 8	mA
R.F. input frequency range	f_{rf}	1,5 to 110	MHz
Sensitivity for −3 dB limiting (e.m.f. voltage) (source impedance: 75 Ω; mute disabled)	EMF	typ. 1,5	μV
Signal handling (e.m.f. voltage) (source impedance: 75 Ω)	EMF	typ. 200	mV
A.F. output voltage at R_L = 22 kΩ	V_o	typ. 75	mV

PACKAGE OUTLINE

18-lead DIL; plastic (SOT102HE).

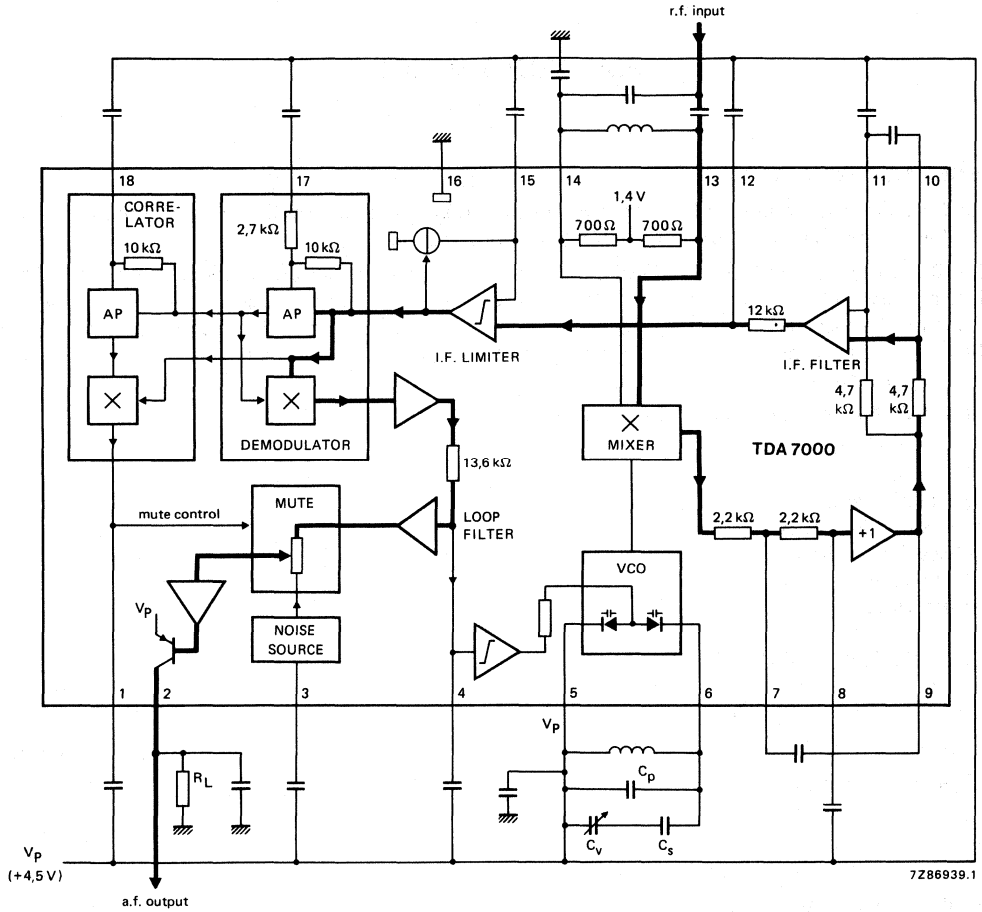


Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 5)	V_P	max.	12 V
Oscillator voltage (pin 6)	V_{6-5}	V_P–0,5 to V_P +0,5	V
Total power dissipation	see derating curve Fig. 2		
Storage temperature range	T_{stg}	−55 to + 150	°C
Operating ambient temperature range	T_{amb}	0 to + 60	°C

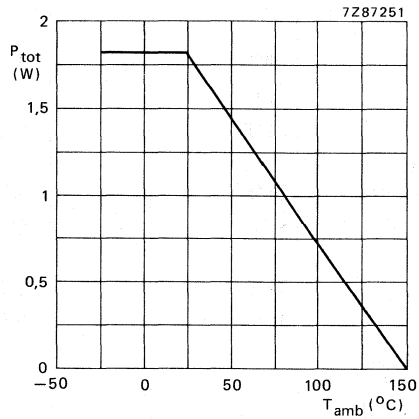


Fig. 2 Power derating curve.

D.C. CHARACTERISTICS

V_P = 4,5 V; T_{amb} = 25 °C; measured in Fig. 4; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply voltage (pin 5)	V_P	2,7	4,5	10	V
Supply current at V_P = 4,5 V	I_P	–	8	–	mA
Oscillator current (pin 6)	I_6	–	280	–	μA
Voltage at pin 14	V_{14-16}	–	1,35	–	V
Output current at pin 2	I_2	–	60	–	μA
Voltage at pin 2; R_L = 22 kΩ	V_{2-16}	–	1,3	–	V

A.C. CHARACTERISTICS

V_P = 4,5 V; T_{amb} = 25 °C; measured in Fig. 4 (mute switch open, enabled); f_{rf} = 96 MHz (tuned to max. signal at 5 μV e.m.f.) modulated with Δf = ± 22,5 kHz; f_m = 1 kHz; EMF = 0,2 mV (e.m.f. voltage at a source impedance of 75 Ω); r.m.s. noise voltage measured unweighted (f = 300 Hz to 20 kHz); unless otherwise specified.

parameter	symbol	min.	typ.	max.	unit
Sensitivity (see Fig. 3) (e.m.f. voltage)					
for −3 dB limiting; muting disabled	EMF	–	1,5	–	μV
for −3 dB muting	EMF	–	6	–	μV
for S/N = 26 dB	EMF	–	5,5	–	μV
Signal handling (e.m.f. voltage) for THD < 10%; Δf = ± 75 kHz	EMF	–	200	–	mV
Signal-to-noise ratio	S/N	–	60	–	dB
Total harmonic distortion					
at Δf = ± 22,5 kHz	THD	–	0,7	–	%
at Δf = ± 75 kHz	THD	–	2,3	–	%
AM suppression of output voltage (ratio of the AM output signal referred to the FM output signal) FM signal: f_m = 1 kHz; Δf = ± 75 kHz AM signal: f_m = 1 kHz; m = 80%	AMS	–	50	–	dB
Ripple rejection (ΔV_P = 100 mV; f = 1 kHz)	RR	–	10	–	dB
Oscillator voltage (r.m.s. value) at pin 6	$V_{6\text{-}5(rms)}$	–	250	–	mV
Variation of oscillator frequency with supply voltage (ΔV_P = 1 V)	Δf_{osc}	–	60	–	kHz/V
Selectivity	S_{+300}	–	45	–	dB
	S_{-300}	–	35	–	dB
A.F.C. range	Δf_{rf}	–	± 300	–	kHz
Audio bandwidth at ΔV_o = 3 dB measured with pre-emphasis (t = 50 μs)	B	–	10	–	kHz
A.F. output voltage (r.m.s. value) at R_L = 22 kΩ	$V_{o(rms)}$	–	75	–	mV
Load resistance					
at V_P = 4,5 V	R_L	–	–	22	kΩ
at V_P = 9,0 V	R_L	–	–	47	kΩ

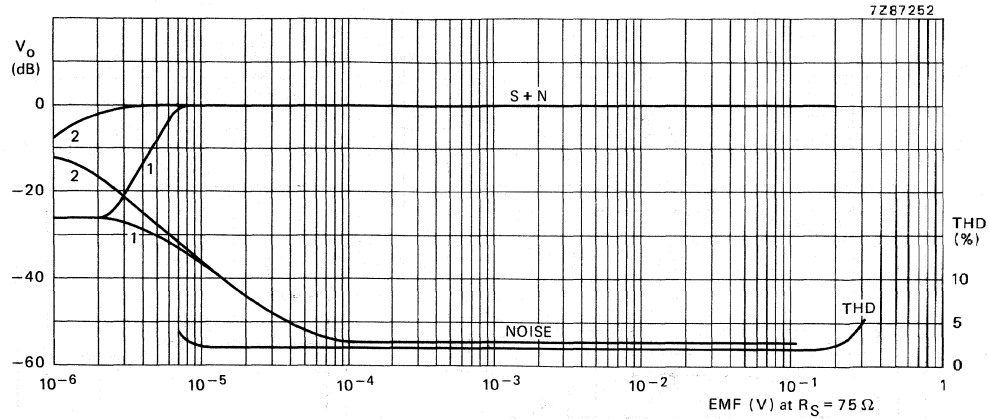


Fig. 3 A.F. output voltage (V_o) and total harmonic distortion (THD) as a function of the e.m.f. input voltage (EMF) with a source impedance (R_S) of 75 Ω: (1) muting system enabled; (2) muting system disabled.

Conditions: 0 dB = 75 mV; f_{rf} = 96 MHz.
for S + N curve: $\Delta f = \pm$ 22,5 kHz; f_m = 1 kHz.
for THD curve: $\Delta f = \pm$ 75 kHz; f_m = 1 kHz.

Notes

1. The muting system can be disabled by feeding a current of about 20 μA into pin 1.
2. The interstation noise level can be decreased by choosing a low-value capacitor at pin 3. Silent tuning can be achieved by omitting this capacitor.

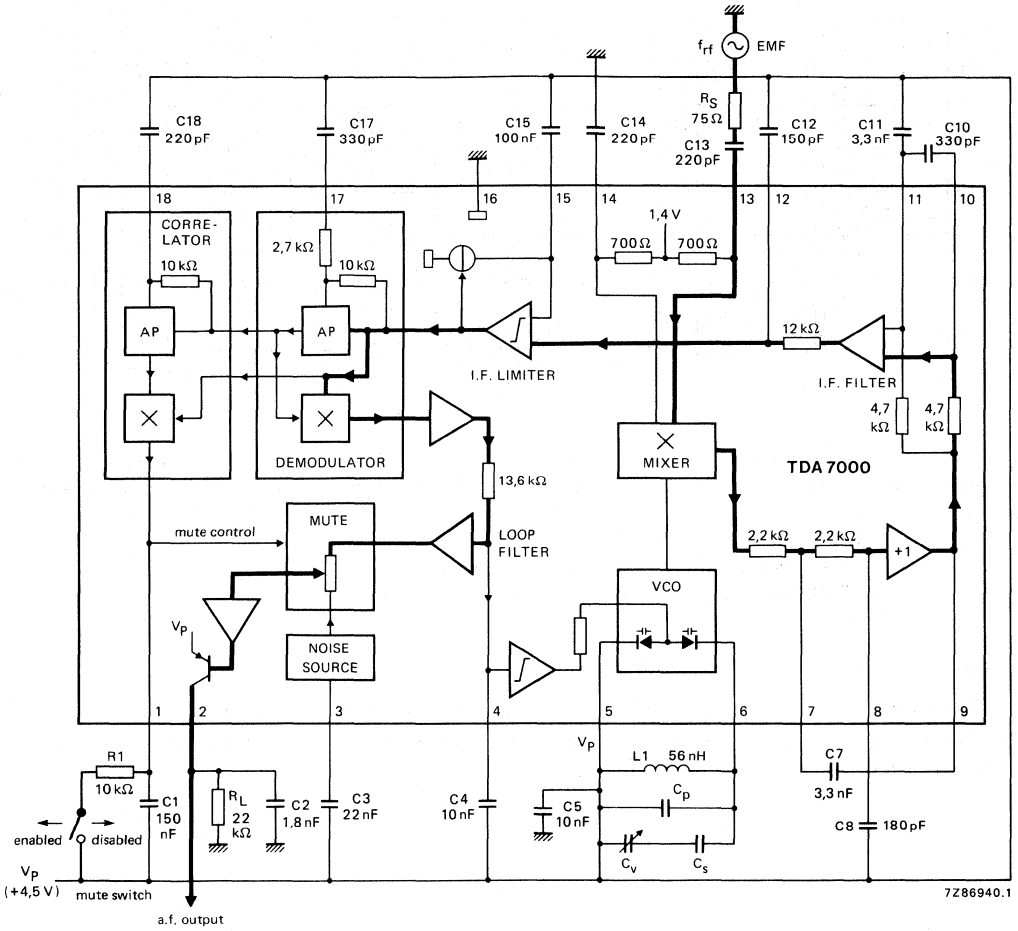


Fig. 4 Test circuit; for printed-circuit boards see Figs 5 and 6.

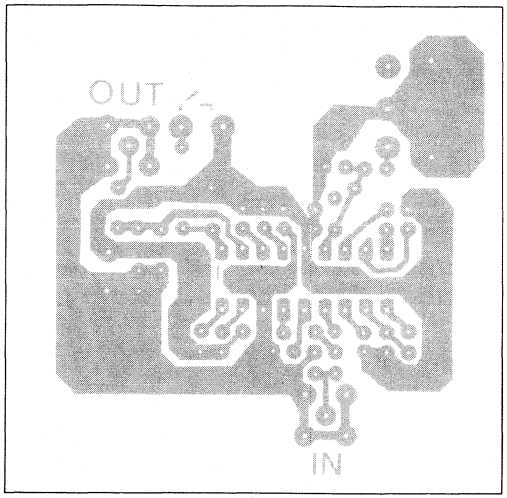


Fig. 5 Track side of printed-circuit board used for the circuit of Fig. 4.

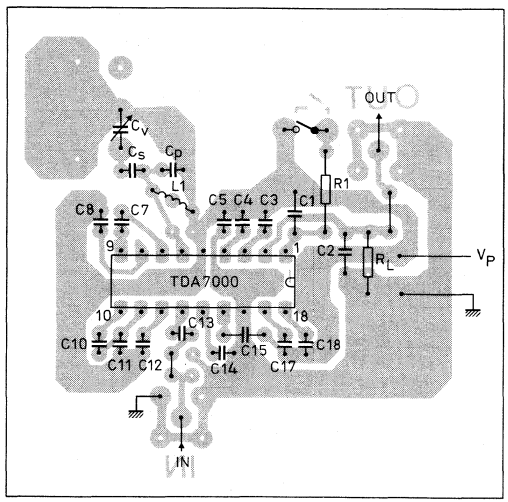


Fig. 6 Component side of printed-circuit board showing component layout used for the circuit of Fig. 4.

FM RADIO CIRCUIT

GENERAL DESCRIPTION

The TDA7010T is a monolithic integrated circuit for mono FM portable radios, where a minimum on peripheral components is important (small dimensions and low costs).

The IC has an FLL (Frequency-Locked-Loop) system with an intermediate frequency of 70 kHz. The i.f. selectivity is obtained by active RC filters. The only function which needs alignment is the resonant circuit for the oscillator, thus selecting the reception frequency. Spurious reception is avoided by means of a mute circuit, which also eliminates too noisy input signals. Special precautions are taken to meet the radiation requirements.

The TDA7010T includes the following functions:

- R.F. input stage
- Mixer
- Local oscillator
- I.F. amplifier/limiter
- Phase demodulator
- Mute detector
- Mute switch

QUICK REFERENCE DATA

Supply voltage range (pin 4)	V_P	2,7 to 10	V
Supply current at V_P = 4,5 V	I_P	typ. 8	mA
R.F. input frequency range	f_{rf}	1,5 to 110	MHz
Sensitivity for −3 dB limiting (e.m.f. voltage) (source impedance: 75 Ω; mute disabled)	EMF	typ. 1,5	μV
Signal handling (e.m.f. voltage) (source impedance: 75 Ω)	EMF	typ. 200	mV
A.F. output voltage at R_L = 22 kΩ	V_o	typ. 75	mV

PACKAGE OUTLINE

16-lead mini-pack; plastic (SO16; SOT109A).

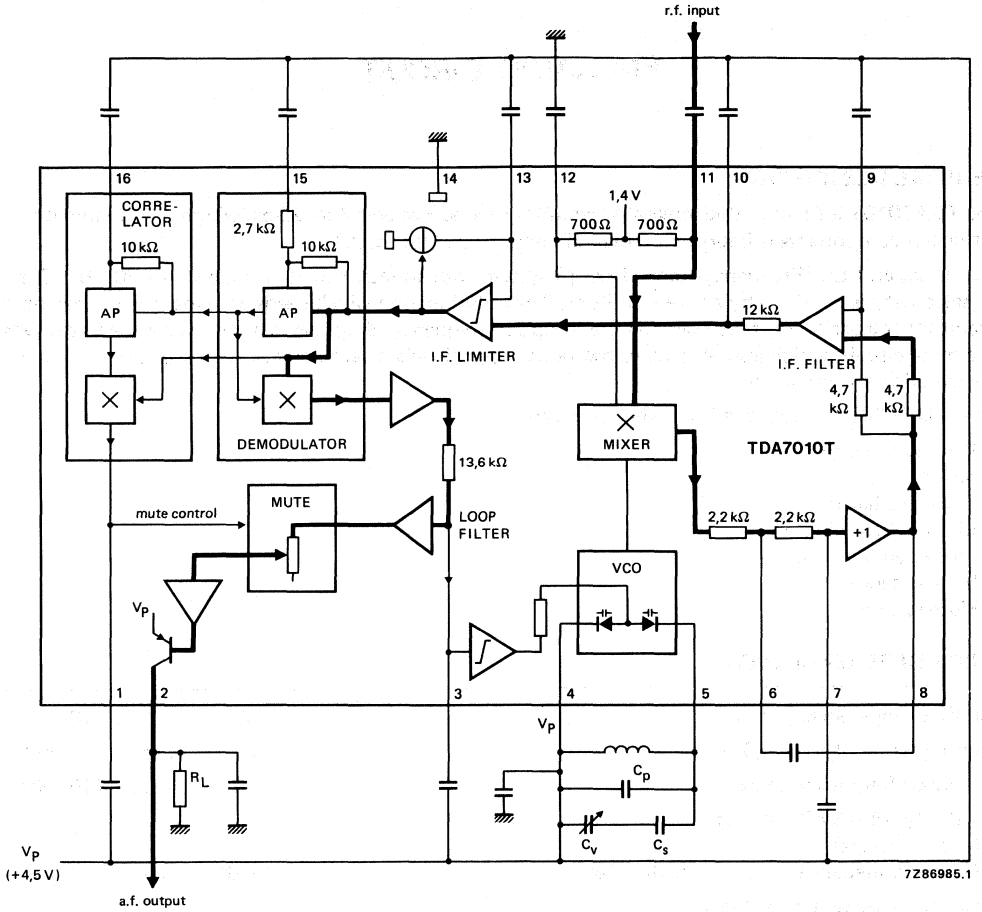


Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 4)	V_P max.	12 V
Oscillator voltage (pin 5)	V_{6-5}	$V_P - 0{,}5$ to $V_P + 0{,}5$ V
Total power dissipation	see derating curve Fig. 2	
Storage temperature range	T_{stg}	−55 to + 150 °C
Operating ambient temperature range	T_{amb}	0 to + 60 °C

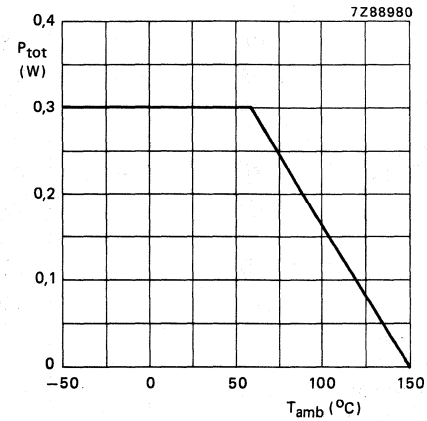


Fig. 2 Power derating curve.

D.C. CHARACTERISTICS

V_P = 4,5 V; T_{amb} = 25 °C; measured in Fig. 4; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply voltage (pin 4)	V_P	2,7	4,5	10	V
Supply current at V_P = 4,5 V	I_P	–	8	–	mA
Oscillator current (pin 5)	I_5	–	280	–	μA
Voltage at pin 12	V_{12-14}	–	1,35	–	V
Output current at pin 2	I_2	–	60	–	μA
Voltage at pin 2; R_L = 22 kΩ	V_{2-14}	–	1,3	–	V

A.C. CHARACTERISTICS

V_P = 4,5 V; T_{amb} = 25 °C; measured in Fig. 4 (mute switch open, enabled); f_{rf} = 96 MHz (tuned to max. signal at 5 μV e.m.f.) modulated with Δf = ± 22,5 kHz; f_m = 1 kHz; EMF = 0,2 mV (e.m.f. voltage at a source impedance of 75 Ω); r.m.s. noise voltage measured unweighted (f = 300 Hz to 20 kHz); unless otherwise specified.

parameter	symbol	min.	typ.	max.	unit
Sensitivity (see Fig. 3) (e.m.f. voltage)					
for −3 dB limiting; muting disabled	EMF	–	1,5	–	μV
for −3 dB muting	EMF	–	6	–	μV
for S/N = 26 dB	EMF	–	5,5	–	μV
Signal handling (e.m.f. voltage) for THD < 10%; Δf = ± 75 kHz	EMF	–	200	–	mV
Signal-to-noise ratio	S/N	–	60	–	dB
Total harmonic distortion					
at Δf = ± 22,5 kHz	THD	–	0,7	–	%
at Δf = ± 75 kHz	THD	–	2,3	–	%
AM suppression of output voltage (ratio of the AM output signal referred to the FM output signal) FM signal: f_m = 1 kHz; Δf = ± 75 kHz AM signal: f_m = 1 kHz; m = 80%	AMS	–	50	–	dB
Ripple rejection (ΔV_P = 100 mV; f = 1 kHz)	RR	–	10	–	dB
Oscillator voltage (r.m.s. value) at pin 5	$V_{5\text{-}4(rms)}$	–	250	–	mV
Variation of oscillator frequency with supply voltage (ΔV_P = 1 V)	Δf_{osc}	–	60	–	kHz/V
Selectivity	S_{+300}	–	43	–	dB
	S_{-300}	–	28	–	dB
A.F.C. range	Δf_{rf}	–	± 300	–	kHz
Audio bandwidth at ΔV_o = 3 dB measured with pre-emphasis (t = 50 μs)	B	–	10	–	kHz
A.F. output voltage (r.m.s. value) at R_L = 22 kΩ	$V_{o(rms)}$	–	75	–	mV
Load resistance					
at V_P = 4,5 V	R_L	–	–	22	kΩ
at V_P = 9,0 V	R_L	–	–	47	kΩ

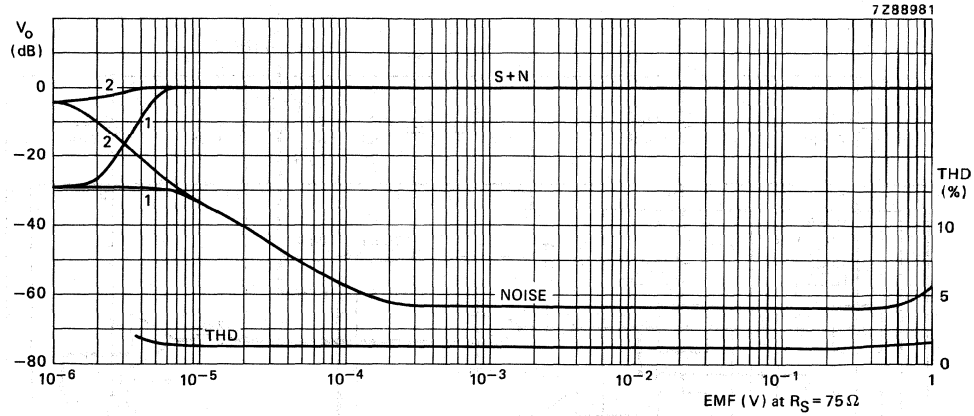


Fig. 3 A.F. output voltage (V_o) and total harmonic distortion (THD) as a function of the e.m.f. input voltage (EMF) with a source impedance (R_S) of 75 Ω: (1) muting system enabled; (2) muting system disabled.

Conditions: 0 dB = 75 mV; f_{rf} = 96 MHz.
for S + N curve: $\Delta f = \pm$ 22,5 kHz; f_m = 1 kHz.
for THD curve: $\Delta f = \pm$ 75 kHz; f_m = 1 kHz.

Notes

1. The muting system can be disabled by feeding a current of about 20 μA into pin 1.

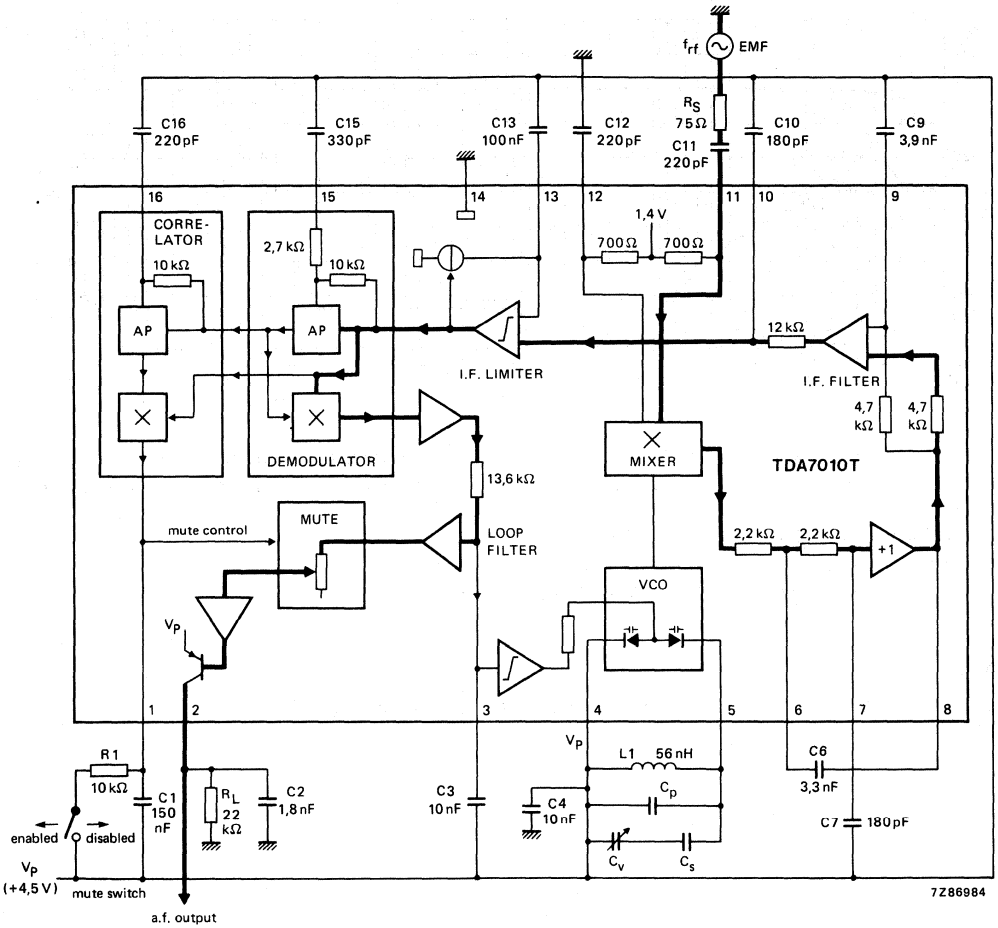


Fig. 4 Test circuit; for printed-circuit boards see Figs 5 and 6.

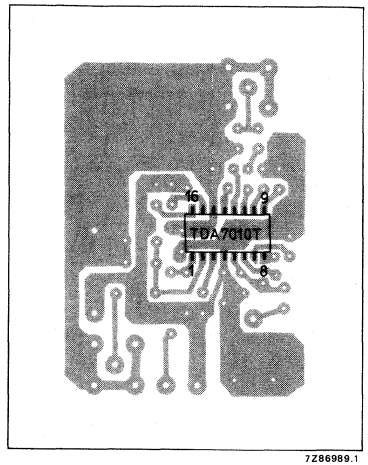


Fig. 5 Track side of printed-circuit board used for the circuit of Fig. 4.

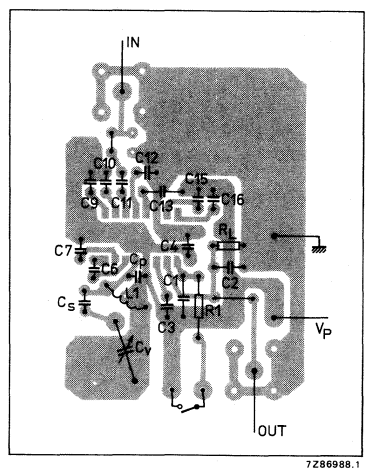


Fig. 6 Component side of printed-circuit board showing component layout used for the circuit of Fig. 4.

FM RADIO CIRCUIT FOR MTS

GENERAL DESCRIPTION

The TDA7021T integrated radio receiver circuit is for portable radios, stereo as well as mono, where a minimum of periphery is important in terms of small dimensions and low cost. It is fully compatible for applications using the low-voltage micro tuning system (MTS). The IC has a frequency locked loop (FLL) system with an intermediate frequency of 76 kHz. The selectivity is obtained by active RC filters. The only function to be tuned is the resonant frequency of the oscillator. Interstation noise as well as noise from receiving weak signals is reduced by a correlation mute system.

Special precautions have been taken to meet local oscillator radiation requirements. Because of the low intermediate frequency, low pass filtering of the MUX signal is required to avoid noise when receiving stereo. 50 kHz roll-off compensation, needed because of the low pass characteristic of the FLL, is performed by the integrated LF amplifier. For mono application this amplifier can be used to directly drive an earphone. The field-strength detector enables field-strength dependent channel separation control.

Features

- RF input stage
- Mixer
- Local oscillator
- IF amplifier/limiter
- Frequency detector
- Mute circuit
- MTS compatible
- Loop amplifier
- Internal reference circuit
- LF amplifier for
  — mono earphone amplifier or
  — MUX filter
- Field-strength dependent channel separation control facility

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage (pin 4)		$V_P = V_{4-3}$	1,8	–	6,0	V
Supply current	V_P = 3 V	I_4	–	6,3	–	mA
RF input frequency		f_{rf}	1,5	–	110	MHz
Sensitivity (e.m.f.) for –3 dB limiting	source impedance = 75 Ω; mute disabled	EMF	–	4	–	μV
Signal handling (e.m.f.)	source impedance = 75 Ω	EMF	–	200	–	mV
AF output voltage		V_o	–	90	–	mV

PACKAGE OUTLINE

16-lead mini-pack; plastic (SO16; SOT109A).

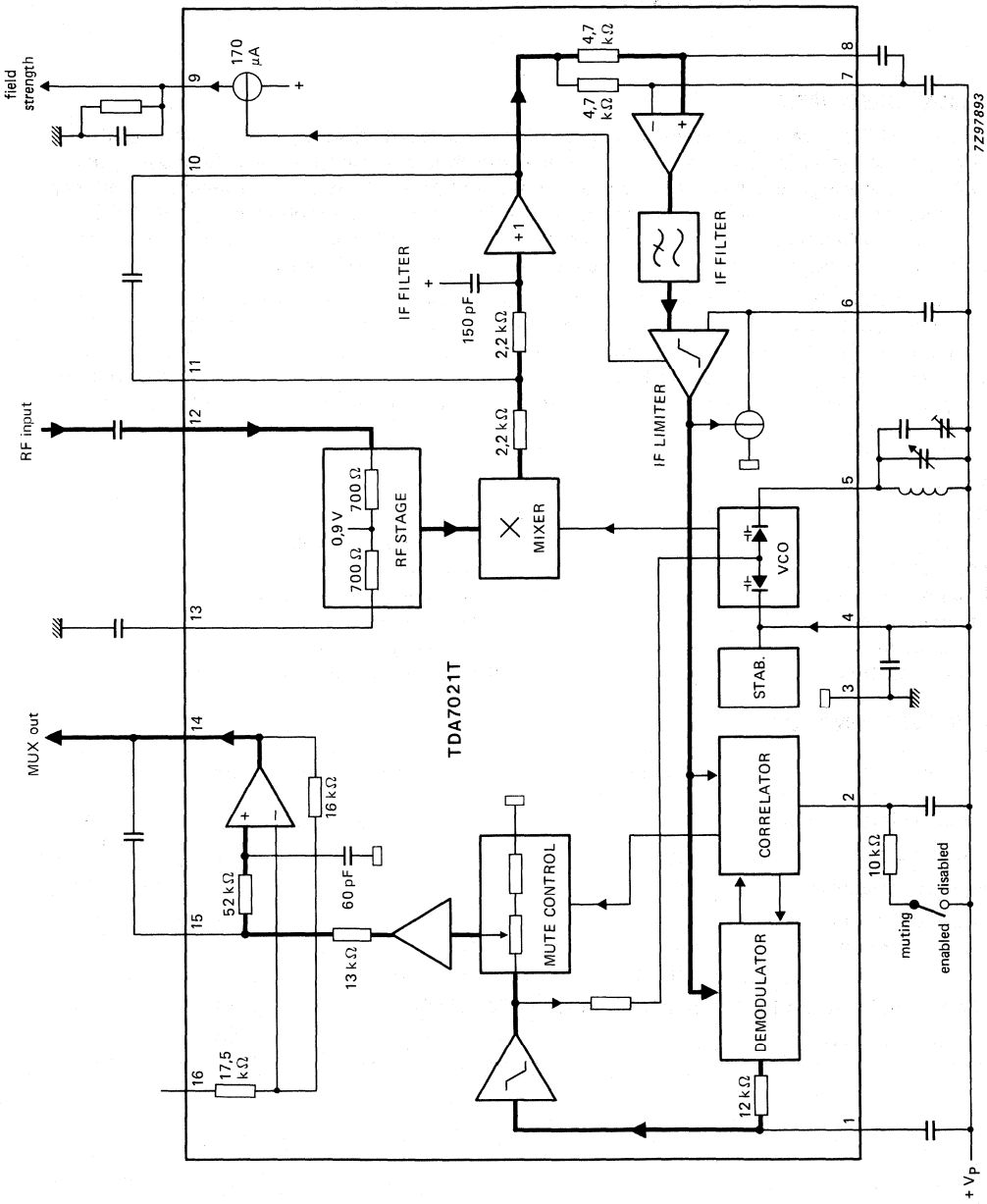


Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage (pin 4)		$V_P = V_{4-3}$	–	7,0	V
Oscillator voltage		V_{5-4}	V_P–0,5	V_P + 0,5	V
Storage temperature range		T_{stg}	–55	+150	°C
Operating ambient temperature range		T_{amb}	–10	+70	°C

THERMAL RESISTANCE

From junction to ambient $R_{th\ j\text{-}a}$ 300 K/W

DC CHARACTERISTICS

V_P = 3 V, T_{amb} = 25 °C, measured in circuit of Fig. 4, unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage (pin 4)		$V_P = V_{4-3}$	1,8	3,0	6,0	V
Supply current	V_P = 3 V	I_4	–	6,3	–	mA
Oscillator current		I_5	–	250	–	μA
Voltage at pin 13		V_{13-3}	–	0,9	–	V
Output voltage (pin 14)		V_{14-3}	–	1,3	–	V

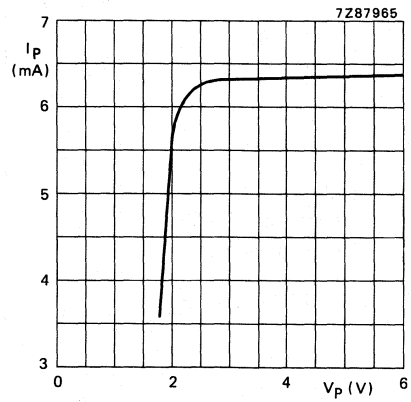


Fig. 2 Supply current as a function of the supply voltage.

AC CHARACTERISTICS (MONO OPERATION)

V_P = 3 V; T_{amb} = 25 °C; measured in Fig. 5; f_{rf} = 96 MHz modulated with Δf = ± 22,5 kHz; f_m = 1 kHz; EMF = 0,3 mV (e.m.f. at a source impedance of 75 Ω); r.m.s. noise voltage measured unweighted (f = 300 Hz to 20 kHz); unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Sensitivity (e.m.f.)	see Fig. 3					
for –3 dB limiting	muting disabled	EMF	–	4,0	–	μV
for –3 dB muting		EMF	–	5,0	–	μV
for (S+N)/N = 26 dB		EMF	–	7,0	–	μV
Signal handling (e.m.f.)	THD < 10%;					
	Δf = ± 75 kHz	EMF	–	200	–	mV
Signal-to-noise ratio		(S+N)/N	–	60	–	dB
Total harmonic distortion	Δf = ± 22,5 kHz	THD	–	0,7	–	%
	Δf = ± 75 kHz	THD	–	2,3	–	%
AM suppression of output voltage	ratio of AM signal (f_m = 1 kHz; m = 80%) to FM signal (f_m = 1 kHz; Δf = 75 kHz)	AMS	–	50	–	dB
Ripple rejection	ΔV_P = 100 mV; f = 1 kHz	RR	–	30	–	dB
Oscillator voltage (r.m.s. value)		$V_{5-4(rms)}$	–	250	–	mV
Variation of oscillator frequency with temperature	V_P = 1 V	$\frac{\Delta f_{osc}}{\Delta T_{amb}}$	–	5	–	kHz/°C
Selectivity	see Fig. 9;					
	no modulation	S_{+300}	–	46	–	dB
		S_{-300}	=	30	–	dB
AFC range		$\pm\Delta f_{rf}$	–	160	–	kHz
Mute range		$\pm\Delta f_{rf}$	–	120	–	kHz
Audio bandwidth	ΔV_o = 3 dB; measured with 50 μs pre-emphasis	B	–	10	–	kHz
AF output voltage (r.m.s. value)	R_L (pin 14) = 100 Ω	$V_{o(rms)}$	–	90	–	mV
AF output current						
max. d.c. load		$I_{o(dc)}$	–100	–	+100	μA
max. a.c. load (peak value)	THD = 10%	$I_{o(ac)}$	–	3	–	mA

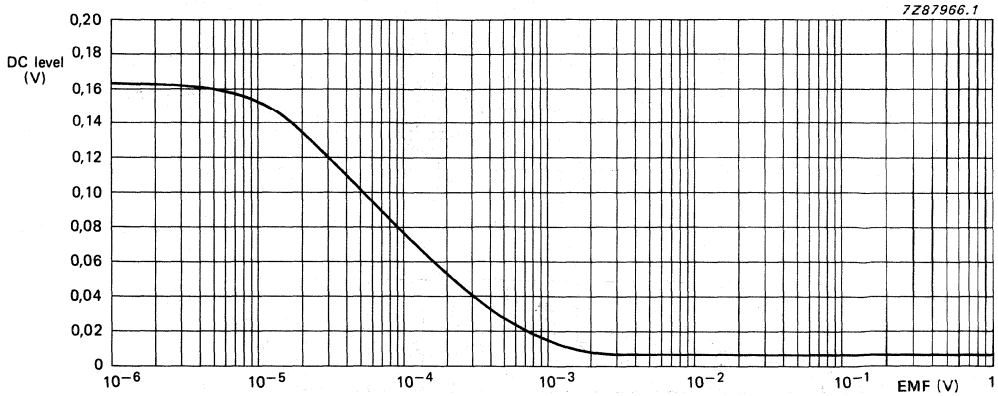


Fig. 3 Field strength voltage (V_{9-3}) at R_{source} = 1 kΩ; f = 96,75 MHz; V_P = 3 V.

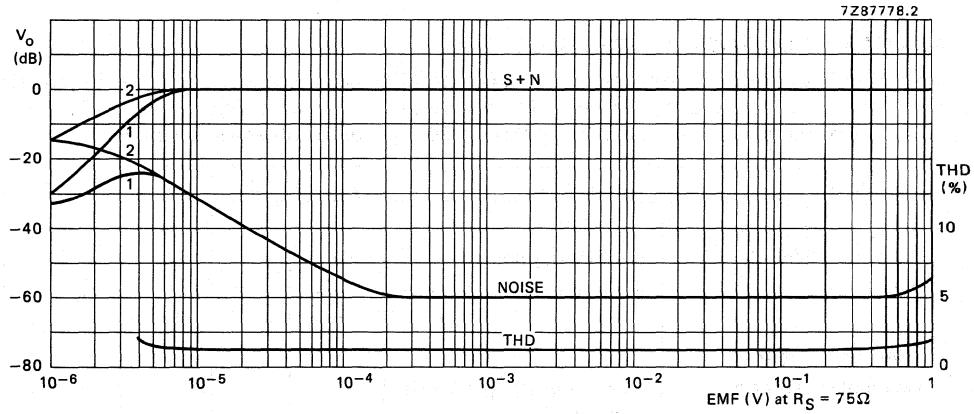
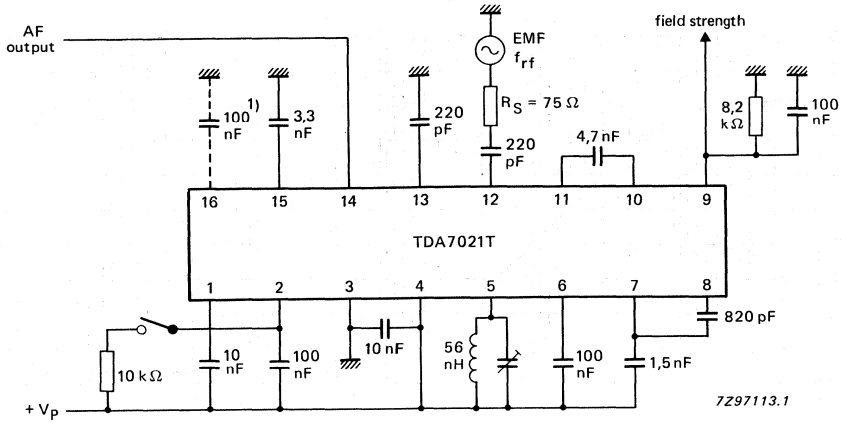


Fig. 4 Mono operation: AF output voltage (V_o) and total harmonic distortion (THD) as functions of input e.m.f. (EMF); R_{source} = 75 Ω; f_{rf} = 96 MHz; 0 dB = 90 mV. For S+N and noise curves (1) is with muting enabled and (2) is with muting disabled; signal Δf = ± 22,5 kHz and f_m = 1 kHz. For THD curve, Δf = ± 75 kHz and f_m = 1 kHz.



1) The AF output can be decreased by disconnecting the 100 nF capacitor from pin 16.

Fig. 5 Test circuit for mono operation.

AC CHARACTERISTICS (STEREO OPERATION)

V_P = 3 V; T_{amb} = 25 °C; measured in Fig. 8; f_{rf} = 96 MHz modulated with pilot Δf = ± 6,75 kHz and AF signal Δf = ± 22,5 kHz; f_m = 1 kHz; EMF = 1 mV (e.m.f. at a source impedance of 75 Ω); r.m.s. noise voltage measured unweighted (f = 300 Hz to 20 kHz); unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Sensitivity (e.m.f.) for (S+N)/N = 26 dB	see Fig. 8; pilot off	EMF	–	11	–	μV
Selectivity	see Fig. 9; no modulation	S_{+300}	–	40	–	dB
		S_{-300}	–	22	–	dB
Signal-to-noise ratio		(S+N)/N	–	50	–	dB
Channel separation	V_i = L-signal; f_m = 1 kHz; pilot on:					
	at f_{rf} = 97 MHz	α	–	26	–	dB
	at f_{rf} = 87,5 MHz and 108 MHz	α	–	14	–	dB

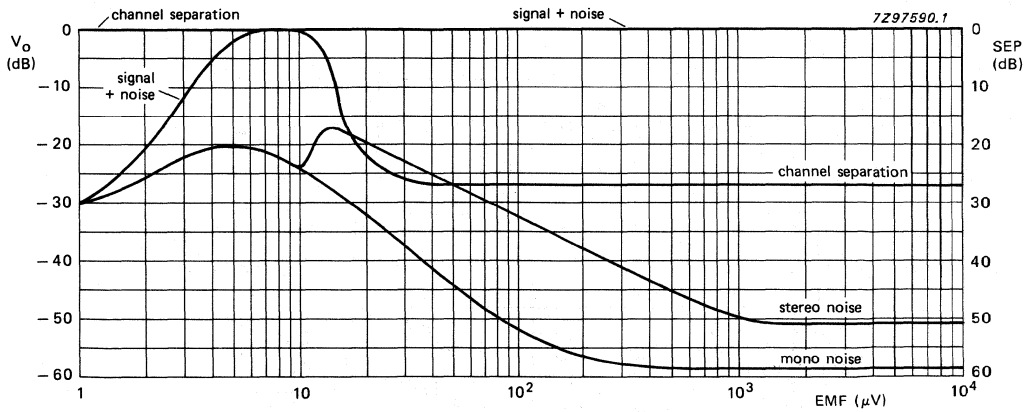


Fig. 6 Stereo operation: signal/noise and channel separation of TDA7021T when used in the circuit of Fig. 8.

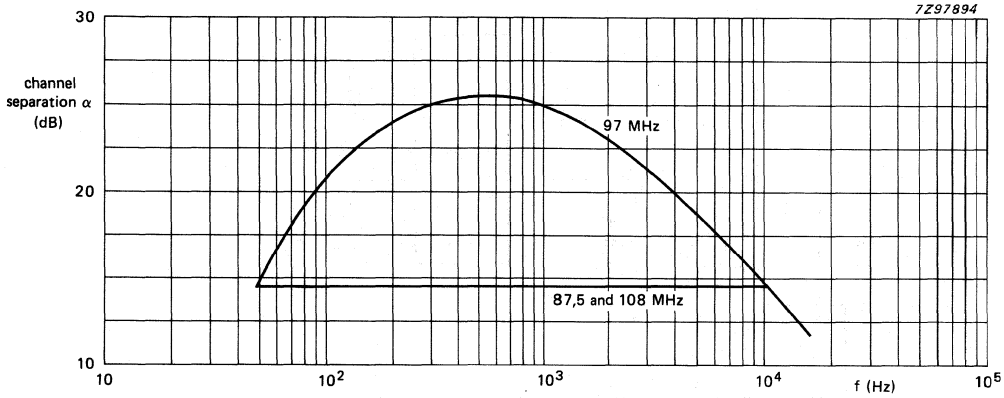


Fig. 7 Stereo operation: channel separation as a function of audio frequency in the circuit of Fig. 8.

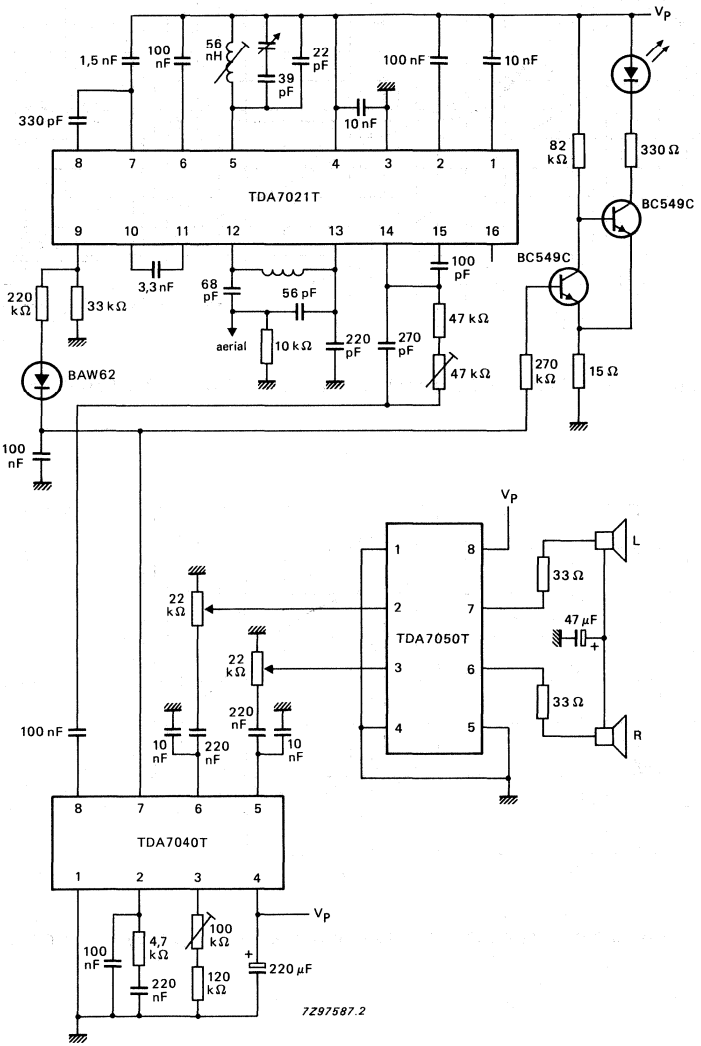


Fig. 8 Stereo application in combination with a low voltage PLL stereo decoder (TDA7040T) and a low voltage mono/stereo power amplifier (TDA7050T).

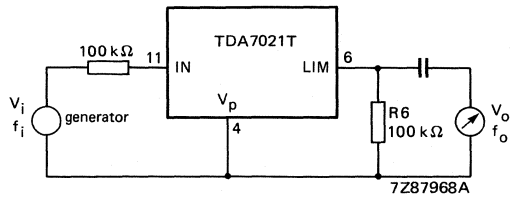


Fig. 9 Test set-up; V_i = 30 mV; f_i = 76 kHz; selective voltmeter at output has $R_i \geqslant 1$ MΩ and $C_i \leqslant 8$ pF; $f_o = f_i$.

Note to Fig. 9

This test set-up is to incorporate the circuit of Fig. 5 for mono operation or the circuit of Fig. 8 for stereo operation. For either circuit, replace the 100 nF capacitor at pin 6 with R6 (100 kΩ) as shown above.

Selectivity

$$S_{+300} = 20 \log \frac{V_o \mid (300\ \text{kHz} - f_i)}{V_o \mid f_i}$$

$$S_{-300} = 20 \log \frac{V_o \mid (300\ \text{kHz} + f_i)}{V_o \mid f_i}$$

LOW VOLTAGE PLL STEREO DECODER

GENERAL DESCRIPTION

The TDA7040T is a monolithic integrated circuit for low cost FM stereo radios with an absolute minimum of peripheral components and a simple lay-out.

Features

- Built-in four pole low pass filter with a 70 kHz corner frequency suppressing unwanted out-of-band input signals
- Fully integrated 228 kHz oscillator
- Pilot presence detector and soft mono/stereo blend
- Built-in interference suppression
- External stereo lamp driver applicable
- Adjustable gain

QUICK REFERENCE DATA

parameter	symbol	min.	typ.	max.	unit
Supply voltage (pin 4)	V_P	1,8	–	6	V
Supply current V_P = 3 V	I_P	–	3	–	mA
Total harmonic distortion	THD	–	0,3	–	%
Signal to noise ratio	S/(S + N)	–	70	–	dB
Channel separation	α	–	40	–	dB

PACKAGE OUTLINE

8-lead mini-pack; plastic (SO8; SOT96A).

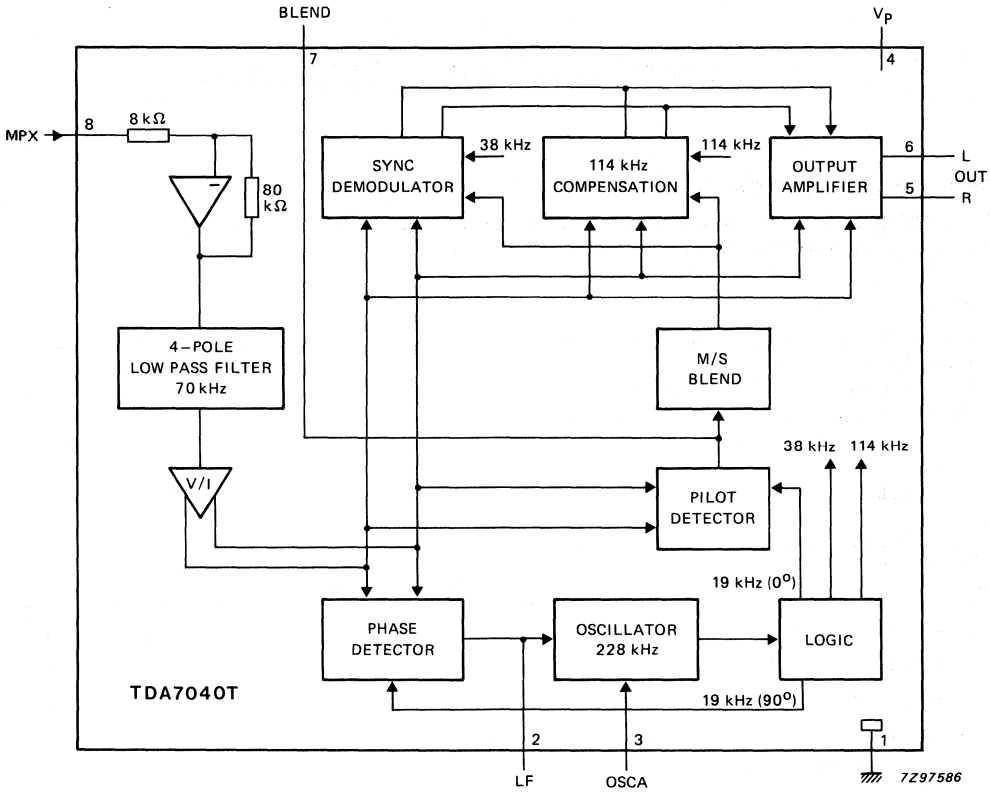


Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	typ.	max.	unit
Supply voltage range	V_P	–	–	7	V
Operating ambient temperature	T_{amb}	−10	–	+ 70	°C
Storage temperature range	T_{stg}	−55	–	+ 150	°C

CHARACTERISTICS

V_P = 3 V; T_{amb} = 25 °C; test circuit Fig. 2; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply voltage (pin 4)	V_P	1,8	3,0	6,0	V
Supply current	I_P	–	3	4	mA
Output voltage (r.m.s. value) $V_{i(rms)}$ L and R 120 mV; f = 1 kHz	$V_{5,\,6\text{-}1}$	–	240	–	mV
Channel balance $V_{i(rms)}$ L and R 40 mV; f = 1 kHz	ΔG_v	–	0	1	dB
Output resistance	R_O	–	5	–	kΩ
Total harmonic distortion $V_{i(rms)}$ L and R 40 mV; f = 1 kHz	THD	–	0,1	–	%
Total harmonic distortion $V_{i(rms)}$ L and R 40 mV; f = 1 kHz; $V_{p(rms)}$ = 12 mV	THD	–	0,3	–	%
Signal-to-noise ratio $V_{i(rms)}$ = 120 mV; f = 1 kHz	S/(S + N)	–	70	–	dB
Signal-to-noise ratio $V_{i(rms)}$ = 120 mV; f = 1 kHz $V_{p(rms)}$ = 12 mV	S/(S + N)	–	70	–	dB
Channel separation $V_{i(rms)}$ L and R 40 mV; f = 1 kHz; $V_{p(rms)}$ = 12 mV	α	–	40	–	dB
Capture range $V_{p(rms)}$ = 12 mV; deviation from centre frequency	Δf	–	± 3	–	%
Carrier leak $V_{i(rms)}$ L and R 120 mV; $V_{p(rms)}$ = 12 mV; f = 1 kHz; f = 19 kHz		–	30	–	dB
f = 38 kHz		–	50	–	dB
SCA (Subsidiary Communications Authorization) rejection $V_{i(rms)}$ L and R 120 mV; $V_{p(rms)}$ = 12 mV; f = 1 kHz; $V_{SCA(RMS)}$ = 12 mV; f = 67 kHz	α_{67}	–	70	–	dB

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
ACI (Adjacent channel interference) $V_{i(rms)}$ L and R 120 mV; $V_{p(rms)}$ = 12 mV; f = 1 kHz; $V_{ACI(RMS)}$ = 1,3 mV; f = 114 kHz $V_{ACI(RMS)}$ = 1,3 mV; f = 190 kHz	α_{114} α_{119}	– –	90 85	– –	dB dB
Traffic radio (V.W.F.) suppression $\alpha_{57(VWF)} = \frac{V_{o(signal)} \text{ (at 1 kHz)}}{V_{o(spurious)} \text{ (at 1 kHz} \pm \text{23 Hz)}}$ measured with: 91% stereo signal; f_m = 1 kHz; 9% pilot signal; 5% traffic subcarrier (f = 57 kHz, f_m = 23 Hz AM, m = 60%)	$\alpha_{57(VWF)}$	–	75	–	dB

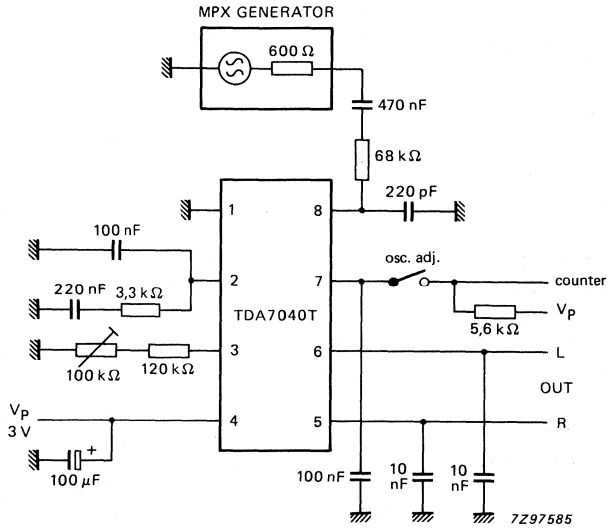


Fig. 2 Test circuit.

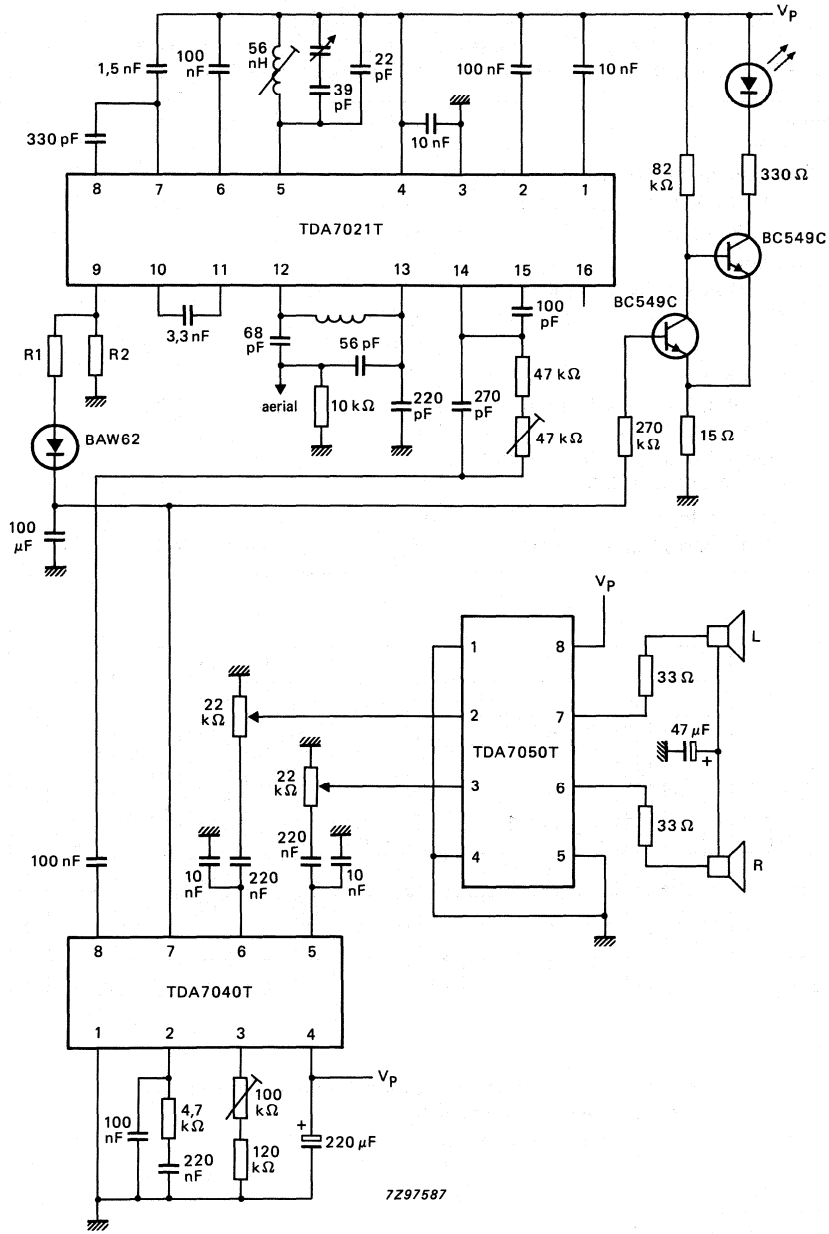


Fig. 3 Application diagram in combination with TDA7021T and TDA7050T.

CHARACTERISTICS

Of the combination TDA7021T, TDA7040T and TDA7050T (Fig. 3).
Conditions unless otherwise specified: $V_{vhf(rms)}$ = 1 mV; f_{hf} = 97 MHz; f_{dev} = 22,5 kHz; $f_{dev\ pilot}$ = 6,75 kHz; noise measured unweighted in a range from 400 Hz to 15 kHz.

parameter	symbol	min.	typ.	max.	unit
Total harmonic distortion (pilot on)					
V_i = (L + R) signal; f_{mod} = 1 kHz	THD	–	0,5	–	%
V_i = L signal; f_{mod} = 1 kHz	THD	–	1,0	–	%
Signal to noise ratio					
V_i = (L + R) signal; f_{mod} = 1 kHz					
pilot off	S/(S + N)	–	56	–	dB
pilot on	S/(S + N)	–	50	–	dB
Channel separation					
V_i = L-signal, f_{mod} = 1 kHz; pilot on; f_{RF} = 97 MHz	α	–	26	–	dB
V_i = L-signal, f_{mod} = 1 kHz; pilot on; f_{RF} = 87,5 MHz and 108 MHz	α	–	14	–	dB
Output voltage (pilot off)					
V_i = (L + R) signal, f_{mod} = 1 kHz	$V_{o(rms)}$	–	80	–	mV

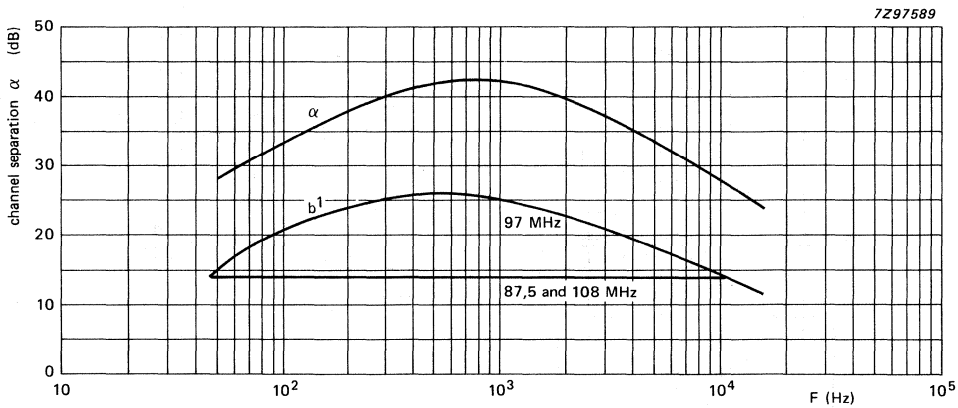


Fig. 4 Channel separation as a function of audio frequency.
a = measured in test circuit (Fig. 2)
b = measured in application diagram (Fig. 3)

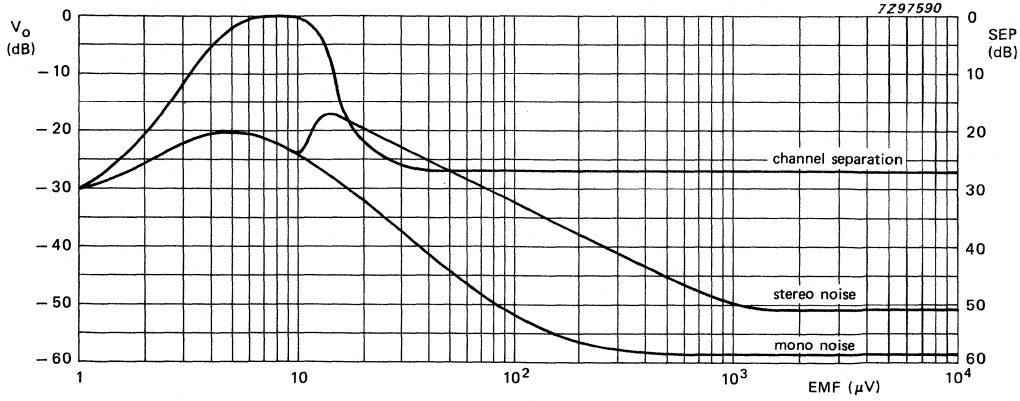


Fig. 5 Signal/noise and channel separation behaviour in Fig. 3. at R1 = 270 kΩ and R2 = 13 kΩ; without diode BAW62.

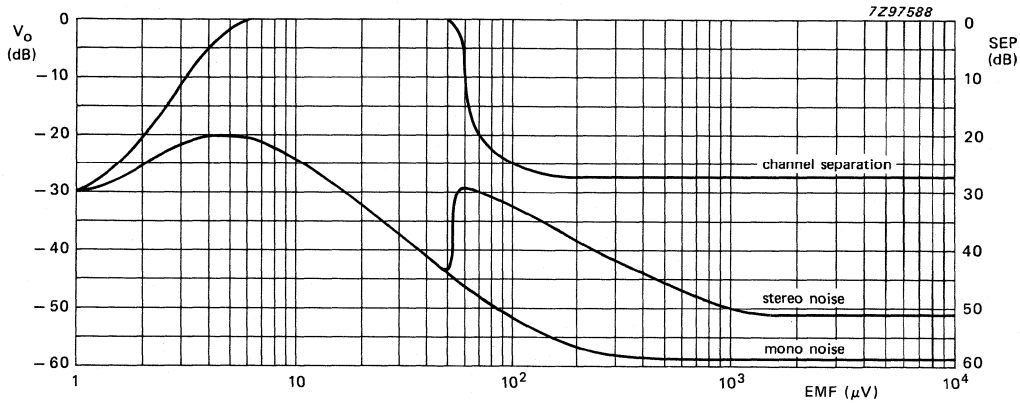


Fig. 6 Signal/noise and channel separation behaviour in Fig. 3. at R1 = 200 kΩ, R2 = 30 kΩ; with diode BAW62.

LOW VOLTAGE MONO/STEREO POWER AMPLIFIER

GENERAL DESCRIPTION

The TDA7050 is a low voltage audio amplifier for small radios with headphones (such as watch, pen and pocket radios) in mono (bridge-tied load) or stereo applications.

Features

- Limited to battery supply application only (typ. 3 and 4 V)
- Operates with supply voltage down to 1,6 V
- No external components required
- Very low quiescent current
- Fixed integrated gain of 26 dB, floating differential input
- Flexibility in use — mono BTL as well as stereo
- Small dimension of encapsulation (see package design example)

QUICK REFERENCE DATA

Supply voltage range	V_P	1,6 to 6,0	V
Total quiescent current (at V_P = 3 V)	I_{tot}	typ. 3,2	mA
Bridge tied load application (BTL)			
Output power at R_L = 32 Ω V_P = 3 V; d_{tot} = 10%	P_o	typ. 140	mW
D.C. output offset voltage between the outputs	$\|\Delta V\|$	max. 70	mV
Noise output voltage (r.m.s. value) at f = 1 kHz; R_S = 5 kΩ	$V_{no(rms)}$	typ. 140	μV
Stereo application			
Output power at R_L = 32 Ω d_{tot} = 10%; V_P = 3 V	P_o	typ. 35	mW
d_{tot} = 10%; V_P = 4,5 V	P_o	typ. 75	mW
Channel separation at R_S = 0 Ω; f = 1 kHz	α	typ. 40	dB
Noise output voltage (r.m.s. value) at f = 1 kHz; R_S = 5 kΩ	$V_{no(rms)}$	typ. 100	μV

PACKAGE OUTLINE

8-lead DIL; plastic (SOT97).

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	6 V
Peak output current	I_{OM}	max.	150 mA
Total power dissipation	see derating curve Fig. 1		
Storage temperature range	T_{stg}	−55 to + 150	°C
Crystal temperature	T_c	max.	100 °C
A.C. and d.c. short-circuit duration at V_P = 3,0 V (during mishandling)	t_{sc}	max.	5 s

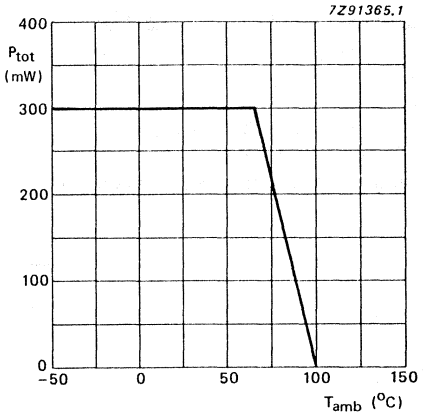


Fig. 1 Power derating curve.

THERMAL RESISTANCE

From junction to ambient R_{thj-a} = 110 K/W

CHARACTERISTICS

V_P = 3 V; f = 1 kHz; R_L = 32 Ω; T_{amb} = 25 °C; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply					
Supply voltage	V_P	1,6	–	6,0	V
Total quiescent current	I_{tot}	–	3,2	4	mA
Bridge-tied load application (BTL); see Fig. 4					
Output power*					
V_P = 3,0 V; d_{tot} = 10%	P_o	–	140	–	mW
V_P = 4,5 V; d_{tot} = 10% (R_L = 64 Ω)	P_o	–	150	–	mW
Voltage gain	G_v	–	32	–	dB
Noise output voltage (r.m.s. value)					
R_S = 5 kΩ; f = 1 kHz	$V_{no(rms)}$	–	140	–	μV
R_S = 0 Ω; f = 500 kHz; B = 5 kHz	$V_{no(rms)}$	–	tbf	–	μV
D.C. output offset voltage (at R_S = 5 kΩ)	$\lvert\Delta V\rvert$	–	–	70	mV
Input impedance (at R_S = ∞)	$\lvert Z_i\rvert$	1	–	–	MΩ
Input bias current	I_i	–	40	–	nA
Stereo application; see Fig. 5					
Output power*					
V_P = 3,0 V; d_{tot} = 10%	P_o	–	35	–	mW
V_P = 4,5 V; d_{tot} = 10%	P_o	–	75	–	mW
Voltage gain	G_v	24.5	26	27.5	dB
Noise output voltage (r.m.s. value)					
R_S = 5 kΩ; f = 1 kHz	$V_{no(rms)}$	–	100	–	μV
R_S = 0 Ω; f = 500 kHz; B = 5 kHz	$V_{no(rms)}$	–	tbf	–	μV
Channel separation					
R_S = 0 Ω; f = 1 kHz	α	30	40	–	dB
Input impedance (at R_S = ∞)	$\lvert Z_i\rvert$	2	–	–	MΩ
Input bias current	I_i	–	20	–	nA

* Output power is measured directly at the output pins of the IC. It is shown as a function of the supply voltage in Fig. 2 (BTL application) and Fig. 3 (stereo application).

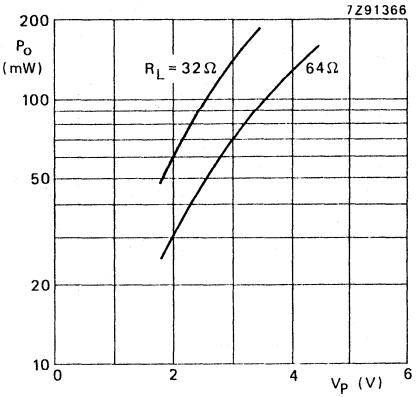


Fig. 2 Output power across the load impedance (R_L) as a function of supply voltage (V_P) in BTL application. Measurements were made at f = 1 kHz; d_{tot} = 10%; T_{amb} = 25 °C.

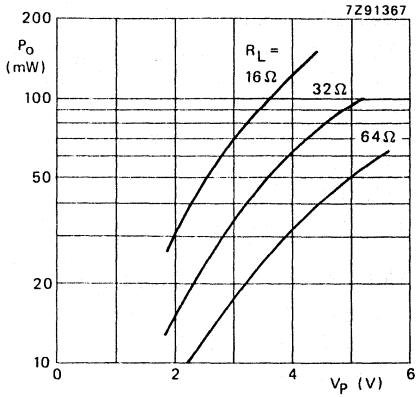


Fig. 3 Output power across the load impedance (R_L) as a function of supply voltage (V_P) in stereo application. Measurements were made at f = 1 kHz; d_{tot} = 10%; T_{amb} = 25 °C.

APPLICATION INFORMATION

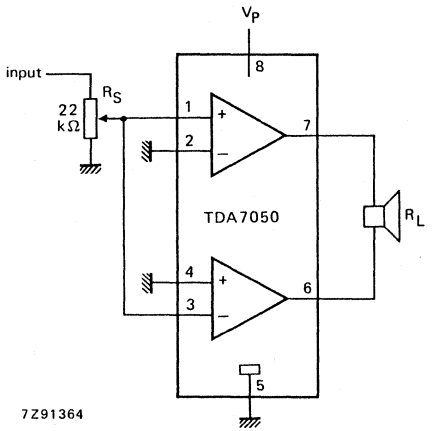


Fig. 4 Application diagram (BTL); also used as test circuit.

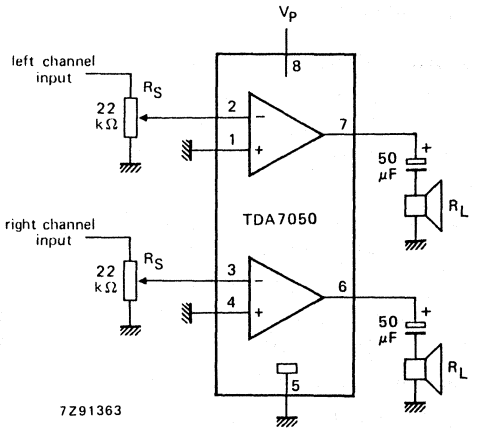


Fig. 5 Application diagram (stereo); also used as test circuit.

LOW VOLTAGE MONO/STEREO POWER AMPLIFIER

GENERAL DESCRIPTION

The TDA7050T is a low voltage audio amplifier for small radios with headphones (such as watch, pen and pocket radios) in mono (bridge-tied load) or stereo applications.

Features

- Limited to battery supply application only (typ. 3 and 4 V)
- Operates with supply voltage down to 1,6 V
- No external components required
- Very low quiescent current
- Fixed integrated gain of 26 dB, floating differential input
- Flexibility in use – mono BTL as well as stereo
- Small dimension of encapsulation (see package design example)

QUICK REFERENCE DATA

Supply voltage range	V_P	1,6 to 6,0	V
Total quiescent current (at V_P = 3 V)	I_{tot}	typ. 3,2	mA
Bridge tied load application (BTL)			
Output power at R_L = 32 Ω V_P = 3 V; d_{tot} = 10%	P_o	typ. 140	mW
D.C. output offset voltage between the outputs	$\|\Delta V\|$	max. 70	mV
Noise output voltage (r.m.s. value) at f = 1 kHz; R_S = 5 kΩ	$V_{no(rms)}$	typ. 140	μV
Stereo application			
Output power at R_L = 32 Ω d_{tot} = 10%; V_P = 3 V	P_o	typ. 35	mW
d_{tot} = 10%; V_P = 4,5 V	P_o	typ. 75	mW
Channel separation at R_S = 0 Ω; f = 1 kHz	α	typ. 40	dB
Noise output voltage (r.m.s. value) at f = 1 kHz; R_S = 5 kΩ	$V_{no(rms)}$	typ. 100	μV

PACKAGE OUTLINE

8-lead mini-pack; plastic (SO8; SOT96A).

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	6 V
Peak output current	I_{OM}	max.	150 mA
Total power dissipation	see derating curve Fig. 1		
Storage temperature range	T_{stg}	−55 to + 150	°C
Crystal temperature	T_c	max.	100 °C
A.C. and d.c. short-circuit duration at V_P = 3,0 V (during mishandling)	t_{sc}	max.	5 s

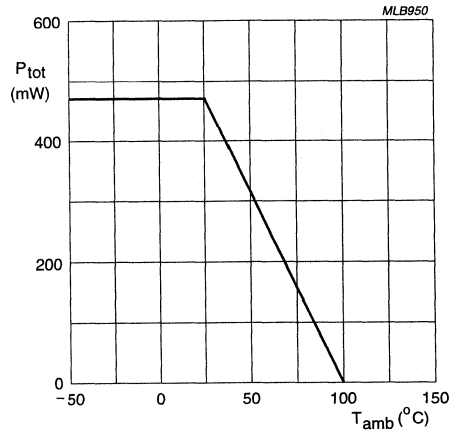


Fig. 1 Power derating curve.

SO PACKAGE DESIGN EXAMPLE

To achieve the small dimension of the encapsulation the SO package is preferred with only 8 pins. Because a heatsink is not applicable, the dissipation is limited by the thermal resistance of the 8-pin SO encapsulation until:

$$\frac{T_{j\,max} - T_{amb}}{R_{th\,j\text{-}a}} = \frac{100-60}{160} = 0.25\ W$$

CHARACTERISTICS

V_P = 3 V; f = 1 kHz; R_L = 32 Ω; T_{amb} = 25 °C; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply					
Supply voltage	V_P	1,6	–	6,0	V
Total quiescent current	I_{tot}	–	3,2	4	mA
Bridge-tied load application (BTL); see Fig. 4					
Output power*					
V_P = 3,0 V; d_{tot} = 10%	P_o	–	140	–	mW
V_P = 4,5 V; d_{tot} = 10% (R_L = 64 Ω)	P_o	–	150	–	mW
Voltage gain	G_v	–	32	–	dB
Noise output voltage (r.m.s. value)					
R_S = 5 kΩ; f = 1 kHz	$V_{no(rms)}$	–	140	–	μV
R_S = 0 Ω; f = 500 kHz; B = 5 kHz	$V_{no(rms)}$	–	tbf	–	μV
D.C. output offset voltage (at R_S = 5 kΩ)	$\|\Delta V\|$	–	–	70	mV
Input impedance (at R_S = ∞)	$\|Z_i\|$	1	–	–	MΩ
Input bias current	I_i	–	40	–	nA
Stereo application; see Fig. 5					
Output power*					
V_P = 3,0 V; d_{tot} = 10%	P_o	–	35	–	mW
V_P = 4,5 V; d_{tot} = 10%	P_o	–	75	–	mW
Voltage gain	G_v	24.5	26	27.5	dB
Noise output voltage (r.m.s. value)					
R_S = 5 kΩ; f = 1 kHz	$V_{no(rms)}$	–	100	–	μV
R_S = 0 Ω; f = 500 kHz; B = 5 kHz	$V_{no(rms)}$	–	tbf	–	μV
Channel separation					
R_S = 0 Ω; f = 1 kHz	α	30	40	–	dB
Input impedance (at R_S = ∞)	$\|Z_i\|$	2	–	–	MΩ
Input bias current	I_i	–	20	–	nA

* Output power is measured directly at the output pins of the IC. It is shown as a function of the supply voltage in Fig. 2 (BTL application) and Fig. 3 (stereo application).

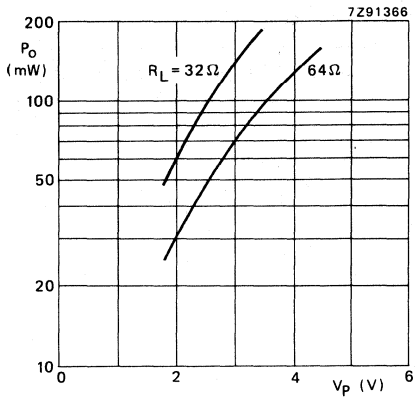


Fig. 2 Output power across the load impedance (R_L) as a function of supply voltage (V_P) in BTL application. Measurements were made at f = 1 kHz; d_{tot} = 10%; T_{amb} = 25 °C.

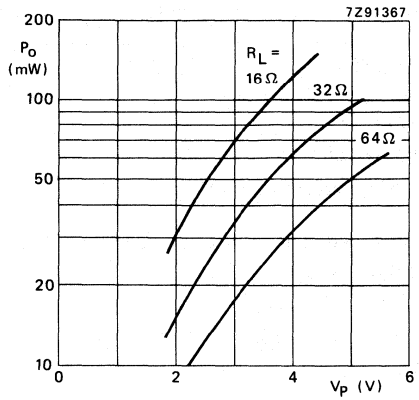


Fig. 3 Output power across the load impedance (R_L) as a function of supply voltage (V_P) in stereo application. Measurements were made at f = 1 kHz; d_{tot} = 10%; T_{amb} = 25 °C.

APPLICATION INFORMATION

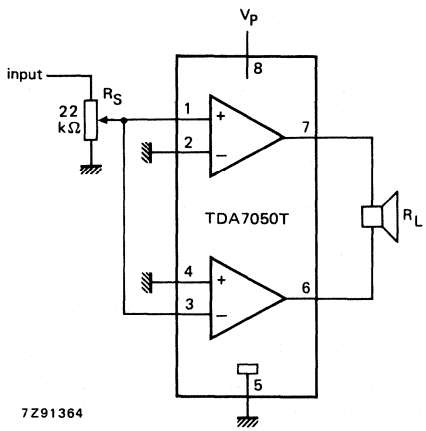


Fig. 4 Application diagram (BTL); also used as test circuit.

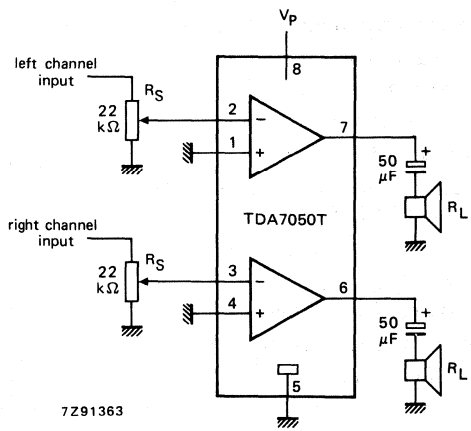


Fig. 5 Application diagram (stereo); also used as test circuit.

1 W BTL MONO AUDIO AMPLIFIER

GENERAL DESCRIPTION

The TDA7052 is a mono output amplifier in a 8-lead dual-in-line (DIL) plastic package. The device is designed for battery-fed portable audio applications.

Features:

- No external components
- No switch-on or switch-off clicks
- Good overall stability
- Low power consumption
- No external heatsink required
- Short-circuit proof

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage range		V_P	3	6	18	V
Total quiescent current	$R_L = \infty$	I_{tot}	–	4	8	mA
Voltage gain		G_v	38	39	40	dB
Output power	THD = 10%; 8 Ω	P_o	–	1,2	–	W
Total harmonic distortion	P_o = 0,1 W	THD	–	0,2	1,0	%

PACKAGE OUTLINE

8-lead DIL; plastic (SOT97).

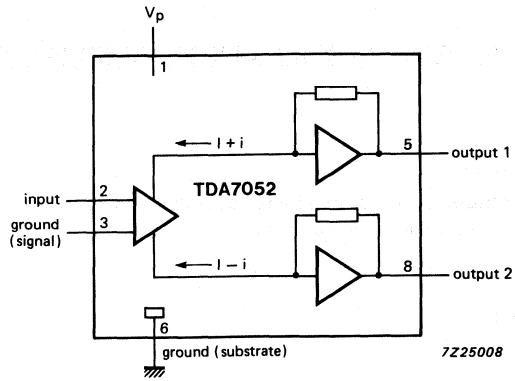


Fig. 1 Block diagram.

PINNING

1	V_P	supply voltage	5	OUT1	output 1
2	IN	input	6	GND2	ground (substrate)
3	GND1	ground (signal)	7	n.c.	not connected
4	n.c.	not connected	8	OUT2	output 2

FUNCTIONAL DESCRIPTION

The TDA7052 is a mono output amplifier designed for battery-fed portable audio applications, such as tape recorders and radios.
The gain is fixed internally at 40 dB. A large number of tape recorders and radios are still designed for mono sound, plus a space-saving trend by reduction of the number of battery cells. This means a decrease in supply voltage which results in an reduction of output power. To compensate for this reduction, the TDA7052 uses the Bridge-Tied-Load principle (BTL) which can deliver an output power of 1,2 W (THD = 10%) into an 8 Ω load with a power supply of 6 V. The load can be short-circuited at each signal excursion.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage	V_P	–	18	V
Non-repetitive peak output current	I_{OSM}	–	1,5	A
Total power dissipation	P_{tot}	see Fig. 2		
Crystal temperature	T_c	–	150	°C
Storage temperature range	T_{stg}	−55	+ 150	°C

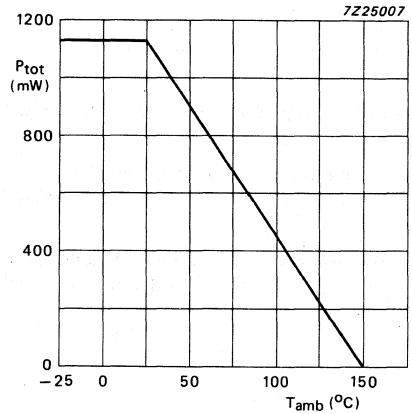


Fig. 2 Power derating curve.

POWER DISSIPATION

Assume V_P = 6 V; R_L = 8 Ω; T_{amb} = 50 °C maximum.

The maximum sinewave dissipation is 0,9 W.

$$R_{th\,j\text{-}a} = \frac{150 - 50}{0{,}9} \approx 110 \text{ K/W}.$$

Where $R_{th\,j\text{-}a}$ of the package is 110 K/W, so no external heatsink is required.

CHARACTERISTICS

V_P = 6 V; R_L = 8 Ω; f = 1 kHz; T_{amb} = 25 °C; unless otherwise specified.

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage range		V_P	3	6	18	V
Total quiescent current	$R_L = \infty$	I_{tot}	–	4	8	mA
Voltage gain		G_v	38	39	40	dB
Output power	THD = 10%	P_o	–	1,2	–	W
Noise output voltage (RMS value)						
	note 1	$V_{no(rms)}$	–	150	300	μV
	note 2	$V_{no(rms)}$	–	60	–	μV
Frequency response		f_r	–	20 Hz to 20 kHz	–	Hz
Supply voltage ripple rejection	note 3	SVRR	40	50	–	dB
DC output offset voltage pin 5 to 8	R_S = 5 kΩ	ΔV_{5-8}	–	–	100	mV
Total harmonic distortion	P_o = 0,1 W	THD	–	0,2	1,0	%
Input impedance		$\|Z_I\|$	–	100	–	kΩ
Input bias current		I_{bias}	–	100	300	nA

Notes to the characteristics

1. The unweighted RMS noise output voltage is measured at a bandwidth of 60 Hz to 15 kHz with a source impedance (R_S) of 5 kΩ.
2. The RMS noise output voltage is measured at a bandwidth of 5 kHz with a source impedance of 0 Ω and a frequency of 500 kHz. With a practical load (R = 8 Ω; L = 200 μH) the noise output current is only 100 nA.
3. Ripple rejection is measured at the output with a source impedance of 0 Ω and a frequency between 100 Hz and 10 kHz. The ripple voltage = 200 mV (RMS value) is applied to the positive supply rail.

APPLICATION INFORMATION

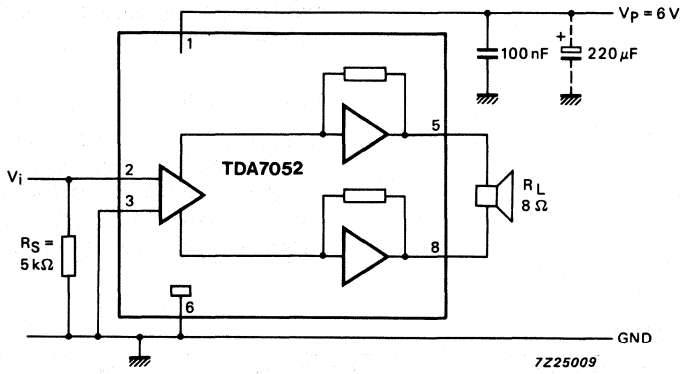


Fig. 3 Application diagram.

1 Watt BTL mono audio amplifier with DC volume control

TDA7052A/AT

FEATURES

- DC volume control
- Few external components
- Mute mode
- Thermal protection
- Short-circuit proof
- No switch-on and off clicks
- Good overall stability
- Low power consumption
- Low HF radiation
- ESD protected on all pins

GENERAL DESCRIPTION

The TDA7052A/AT are mono BTL output amplifiers with DC volume control. They are designed for use in TV and monitors, but also suitable for battery-fed portable recorders and radios.

Missing Current Limiter (MCL)

A MCL protection circuit is built-in. The MCL circuit is activated when the difference in current between the output terminal of each amplifier exceeds 100 mA (typical 300 mA). This level of 100 mA allows for headphone applications (single-ended).

QUICK REFERENCE DATA

SYMBOL	PARAMETERS	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	positive supply voltage range		4.5	–	18	V
P_O	output power					
	TDA7052A	R_L = 8 Ω; V_P = 6 V	1.0	1.1	–	W
	TDA7052AT	R_L = 16 Ω; V_P = 6 V	0.5	0.55	–	W
G_v	maximum total voltage gain		34.5	35.5	36.5	dB
ϕ	gain control range		75	80	–	dB
I_P	total quiescent current	V_P = 6 V; R_L = ∞	–	7	12	mA
THD	total harmonic distortion					
	TDA7052A	P_O = 0.5 W	–	0.3	1	%
	TDA7052AT	P_O = 0.25 W	–	0.3	1	%

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA7052A	8	DIL	plastic	SOT97
TDA7052AT	8	mini-pack	plastic	SOT96A

1 Watt BTL mono audio amplifier with DC volume control

TDA7052A/AT

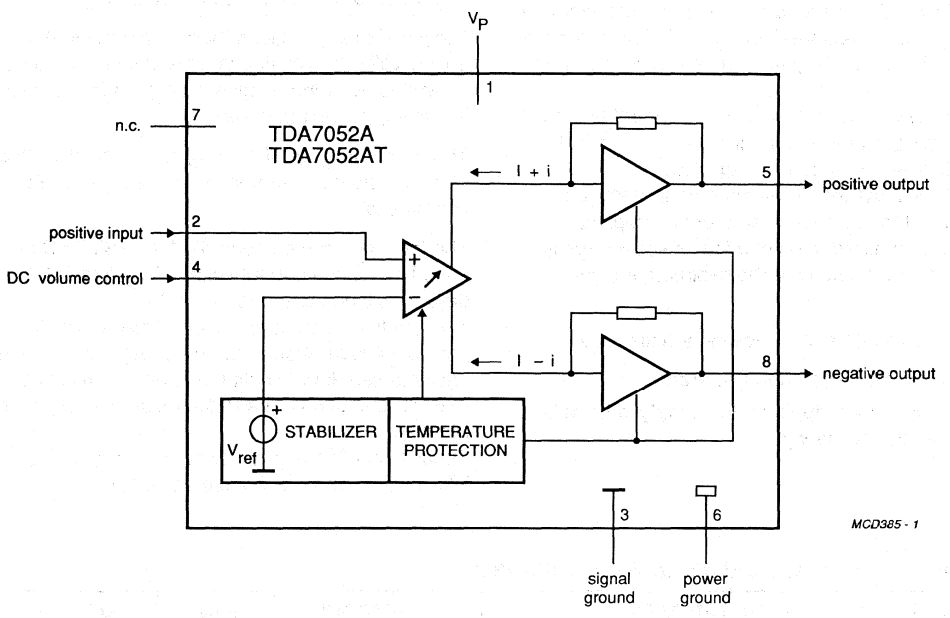


Fig.1 Block diagram.

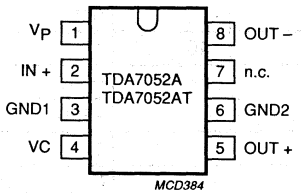


Fig.2 Pin configuration.

PINNING

SYMBOL	PIN	DESCRIPTION
V_P	1	positive supply voltage
IN+	2	positive input
GND1	3	signal ground
VC	4	DC volume control
OUT+	5	positive output
GND2	6	power ground
n.c	7	not connected
OUT−	8	negative output

FUNCTIONAL DESCRIPTION

The TDA7052A/AT are mono BTL output amplifiers with DC volume control, designed for use in TV and monitors but also suitable for battery fed portable recorders and radios.
In conventional DC volume circuits the control or input stage is AC coupled to the output stage via external capacitors to keep the offset voltage low.
In the TDA7052A/AT the DC volume control stage is integrated into the input stage so that no coupling capacitors are required and yet a low offset voltage is maintained. At the same time the minimum supply remains low.

The BTL principle offers the following advantages:

- Lower peak value of the supply current
- The frequency of the ripple on the supply voltage is twice the signal frequency.

Thus a reduced power supply with smaller capacitors can be used which results in cost savings.

For portable applications there is a trend to decrease the supply voltage, resulting in a reduction of output power at conventional output stages. Using the BTL principle increases the output power.

The maximum gain of the amplifier is fixed at 35.5 dB. The DC volume control stage has a logarithmic control characteristic.

The total gain can be controlled from 35.5 dB to –44 dB. If the DC volume control voltage is below 0.3 V, the device switches to the mute mode.
The amplifier is short-circuit proof to ground, V_P and across the load. Also a thermal protection circuit is implemented. If the crystal temperature rises above +150 °C the gain will be reduced, so the output power is reduced.
Special attention is given to switch on and off clicks, low HF radiation and a good overall stability.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_P	supply voltage range		–	18	V
I_{ORM}	repetitive peak output current		–	1.25	A
I_{OSM}	non-repetitive peak output current		–	1.5	A
P_{tot}	total power dissipation	$T_{amb} \leq 25$ °C			
	TDA7052A		–	1.25	W
	TDA7052AT		–	0.8	W
T_{amb}	operating ambient temperature range		–40	+85	°C
T_{stg}	storage temperature range		–55	+150	°C
T_{vj}	virtual junction temperature		–	+150	°C
T_{sc}	short-circuit time		–	1	hr
V_2	input voltage pin 2		–	8	V
V_4	input voltage pin 4		–	8	V

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient in free air	
	TDA7052A	100 K/W
	TDA7052AT	155 K/W

Note to the thermal resistance

TDA7052A: V_P = 6 V; R_L = 8 Ω. The maximum sine-wave dissipation is 0.9 W. Therefore $T_{amb(max)}$ = 150 - 100 x 0.9 = 60 °C.
TDA7052AT: V_P = 6 V; R_L = 16 Ω. The maximum sine-wave dissipation is 0.46 W. Therefore $T_{amb(max)}$ = 150 - 155 x 0.46 = 78 °C.

CHARACTERISTICS

V_P = 6 V; T_{amb} = 25 °C; f = 1 kHz; TDA7052A: R_L = 8 Ω; TDA7052AT: R_L = 16 Ω; unless otherwise specified (see Fig.6).

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	positive supply voltage range		4.5	–	18	V
I_P	total quiescent current	V_P = 6 V; R_L = ∞ note 1	–	7	12	mA
Maximum gain; V_4 = 1.4 V						
P_O	output power	THD = 10%				
	TDA7052A		1.0	1.1	–	W
	TDA7052AT		0.5	0.55	–	W
THD	total harmonic distortion					
	TDA7052A	P_O = 0.5 W	–	0.3	1	%
	TDA7052AT	P_O = 0.25 W	–	0.3	1	%
G_v	voltage gain		34.5	35.5	36.5	dB
V_I	input signal handling	V_4 = 0.8 V; THD < 1%	0.5	0.65	–	V
$V_{no(rms)}$	noise output voltage (RMS value)	f = 500 kHz; note 2	–	210	–	μV
B	bandwidth	−1 dB	–	20 Hz to 300 kHz	–	
SVRR	supply voltage ripple rejection	note 3	38	46	–	dB
$\lvert V_{off}\rvert$	DC output offset voltage		–	0	150	mV
Z_I	input impedance (pin 2)		15	20	25	kΩ
Minimum gain; V_4 = 0.5 V						
G_v	voltage gain		–	−44	–	dB
$V_{no(rms)}$	noise output voltage (RMS value)	note 4	–	20	30	μV
Mute position						
V_O	output voltage in mute position	$V_4 \leq 0.3$ V; V_I = 600 mV	–	–	30	μV
DC volume control						
ϕ	gain control range		75	80	–	dB
I_4	control current	V_4 = 0.4 V	60	70	80	μA

Notes to the characteristics

1. With a load connected to the outputs the quiescent current will increase, the maximum value of this increase being equal to the DC output offset voltage dividend by R_L.
2. The noise output voltage (RMS value) at f = 500 kHz is measured with R_S = 0 Ω and bandwidth = 5 kHz.
3. The ripple rejection is measured with R_S = 0 Ω and f = 100 Hz to 10 kHz. The ripple voltage of 200 mV, (RMS value) is applied to the positive supply rail.
4. The noise output voltage (RMS value) is measured with R_S = 5 kΩ unweighted.

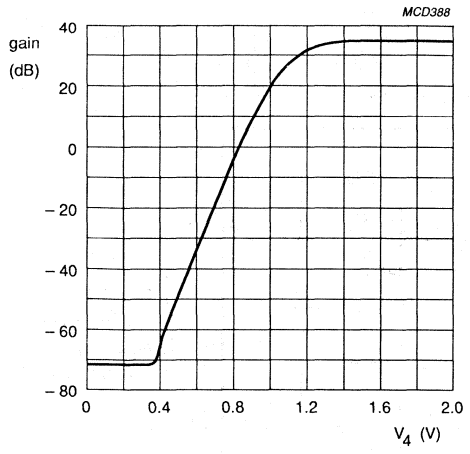


Fig.3 Gain control as a function of DC volume control.

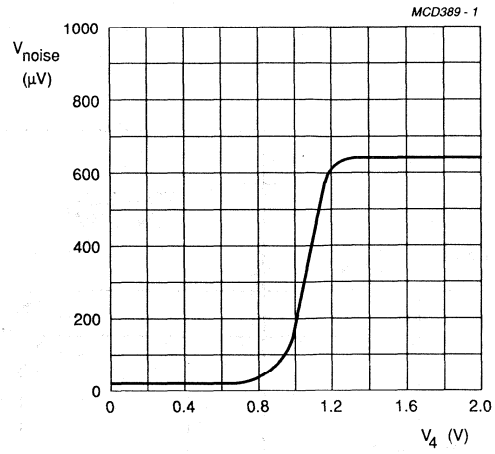


Fig.4 Noise output voltage as a function of DC volume control.

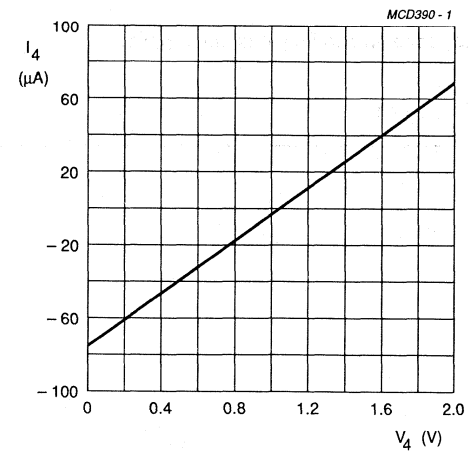
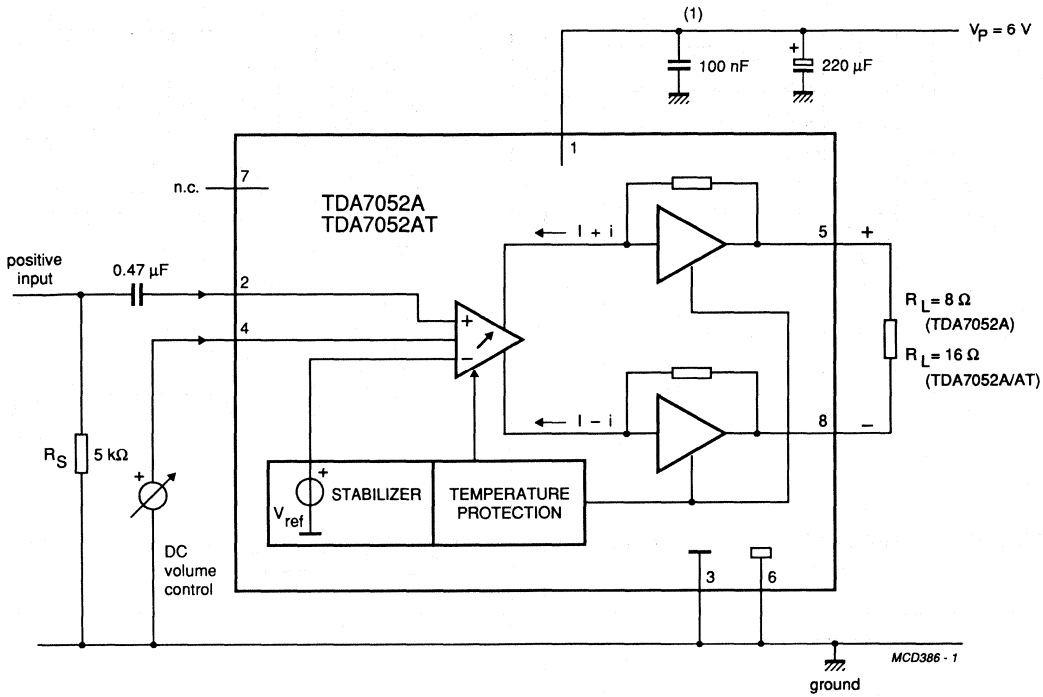


Fig.5 Control current as a function of DC volume control.

APPLICATION INFORMATION



(1) This capacitor can be omitted if the 220 µF electrolytic capacitor is connected close to pin 1.

Fig.6 Test and application diagram.

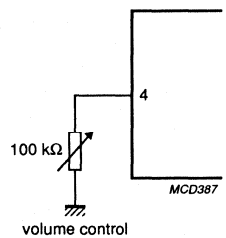


Fig.7 Application with potentiometer as volume control; maximum gain = 30 dB.

Mono BTL audio amplifier with DC volume control

TDA7052B; TDA7052BT

FEATURES

- DC volume control
- Few external components
- Mute mode
- Thermal protection
- Short-circuit proof
- No switch-on and switch-off clicks
- Good overall stability
- Low power consumption
- Low HF radiation
- ESD protected on all pins.

GENERAL DESCRIPTION

The TDA7052B; BT are 1 W and 0.5 W mono BTL output amplifiers with DC volume control. They have been designed for use in TV and monitors, but are also suitable for use in battery-fed portable recorders and radios.

Missing Current Limiter (MCL)

A MCL protection circuit is built-in. The MCL circuit is activated when the difference in current between the output terminal of each amplifier exceeds 100 mA (typical 300 mA). This level of 100 mA allows for headphone applications (single-ended).

QUICK REFERENCE DATA

SYMBOL	PARAMETERS	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	positive supply voltage		4.5	–	18	V
P_O	output power					
	TDA7052B	R_L = 8 Ω; V_P = 6 V	0.9	1.0	–	W
	TDA7052BT	R_L = 16 Ω; V_P = 6 V	0.5	0.55	–	W
G_v	maximum total voltage gain		39.5	40.5	41.5	dB
ϕ	gain control		68	73.5	–	dB
I_P	total quiescent current	V_P = 6 V; R_L = ∞	–	9.2	13	mA
THD	total harmonic distortion					
	TDA7052B	P_O = 0.5 W	–	0.3	1	%
	TDA7052BT	P_O = 0.25 W	–	0.3	1	%

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA7052B	8	DIL	plastic	SOT97DE
TDA7052BT	8	SO8	plastic	SOT96AG

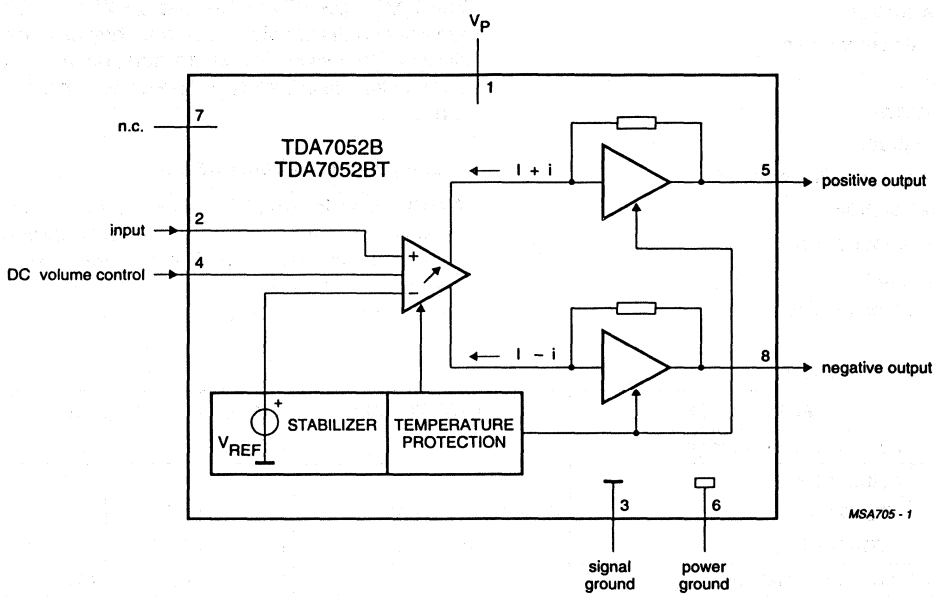


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
V_P	1	positive supply voltage
IN+	2	input
GND1	3	signal ground
VC	4	DC volume control
OUT+	5	positive output
GND2	6	power ground
n.c	7	not connected
OUT−	8	negative output

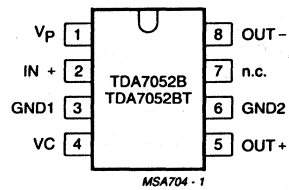


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The TDA7052B; BT are mono BTL output amplifiers with DC volume control which have been designed for use in TV and monitors but are also suitable for use in battery fed portable recorders and radios.
In conventional DC volume circuits the control or input stage is AC coupled to the output stage via external capacitors to keep the offset voltage low.
In the TDA7052B; BT the DC volume control stage is integrated into the input stage so that no coupling capacitors are required. With this configuration, a low offset voltage is maintained and the minimum supply voltage remains low.

The BTL principle offers the following advantages:

- Lower peak value of the supply current
- The frequency of the ripple on the supply voltage is twice the signal frequency.

Consequently, a reduced power supply with smaller capacitors can be used which results in cost reductions.

For portable applications there is a trend to decrease the supply voltage, resulting in a reduction of output power at conventional output stages. Using the BTL principle increases the output power.

The maximum gain of the amplifier is fixed at 40.5 dB. The DC volume control stage has a logarithmic control characteristic. Therefore, the total gain can be controlled from 40.5 dB to −33 dB.
If the DC volume control voltage falls below 0.4 V, the device will switch to the mute mode.

The amplifier is short-circuit proof to ground, V_P and across the load. Also a thermal protection circuit is implemented. If the crystal temperature rises above +150 °C the gain will be reduced, thereby reducing the output power.
Special attention is given to switch-on and switch-off clicks, low HF radiation and a good overall stability.

Power dissipation

Assume for the TDA7052B that V_P = 6 V; R_L = 8 Ω. The maximum sinewave dissipation is 0.9 W.
The $R_{th\ j\text{-}a}$ of the package is 100 K/W. Therefore
$T_{amb(max)}$ = 150 - 100 x 0.9 = 60 °C.

Assume for the TDA7052BT that V_P = 6 V; R_L = 16 Ω.
The maximum sinewave dissipation is 0.46 W.
The $R_{th\ j\text{-}a}$ of the package is 155 K/W. Therefore
$T_{amb(max)}$ = 150 - 155 x 0.46 = 78 °C.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_P	positive supply voltage		–	18	V
I_{ORM}	repetitive peak output current		–	1.25	A
I_{OSM}	non-repetitive peak output current		–	1.5	A
P_{tot}	total power dissipation	$T_{amb} \leq 25$ °C			
	TDA7052B		–	1.25	W
	TDA7052BT		–	0.8	W
T_{amb}	operating ambient temperature		−40	+85	°C
T_{stg}	storage temperature		−55	+150	°C
T_{vj}	virtual junction temperature		–	+150	°C
T_{sc}	short-circuit time		–	1	hr
$V_{2,4}$	input voltage pins 2 and 4		–	5	V

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient in free air	
	TDA7052B	100 K/W
	TDA7052BT	155 K/W

CHARACTERISTICS

V_P = 6 V; T_{amb} = 25 °C; f = 1 kHz; R_L = 8 Ω and 16 Ω; unless otherwise specified (see Fig.6).

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	positive supply voltage		4.5	–	18	V
I_P	total quiescent current	note 1; V_P = 6 V; R_L = ∞	–	9.2	13	mA
Maximum gain; $V_4 \geq 1.4$ V						
P_O	output power	THD = 10%				
	TDA7052B		0.9	1.0	–	W
	TDA7052BT		0.5	0.55	–	W
THD	total harmonic distortion					
	TDA7052B	P_O = 0.5 W	–	0.3	1	%
	TDA7052BT	P_O = 0.25 W	–	0.3	1	%
G_v	voltage gain		39.5	40.5	41.5	dB
$V_{I(RMS)}$	input signal handling (RMS value)	G_v = 0 dB; THD < 1%	1	–	–	V
V_{no}	noise output voltage	note 2; f = 500 kHz;	–	210	–	μV
B	bandwidth	at −1 dB	–	20 Hz to 300 kHz	–	Hz
SVRR	supply voltage ripple rejection	note 3	34	38	–	dB
$\lvert\Delta V_O\rvert$	DC output offset voltage	$\lvert V_8 - V_5\rvert$	–	0	200	mV
Z_I	input impedance (pin 3)		15	20	25	kΩ
Mute position						
V_O	output voltage in mute position	note 4; V_4 = 0.4 V ±30 mV; V_I = 1.0 V	–	30	40	μV
DC volume control						
ϕ	gain control		68	73.5	–	dB
I_4	control current	V_4 = 0 V	20	25	30	μA

Notes

1. With a load connected to the outputs the quiescent current will increase, the maximum value of this increase being equal to the DC output offset voltage divided by R_L.
2. The noise output voltage (RMS value) at f = 500 kHz is measured with R_S = 0 Ω and bandwidth = 5 kHz.
3. The ripple rejection is measured with R_S = 0 Ω and f = 100 Hz to 10 kHz. The ripple voltage of 200 mV (RMS value) is applied to the positive supply rail.
4. The noise output voltage (RMS value) is measured with R_S = 5 kΩ unweighted.

Quality specification

In accordance with SNW-FQ-611 part E, if this type is used as an audio amplifier.

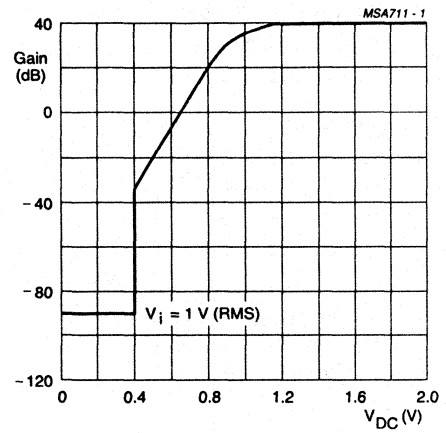
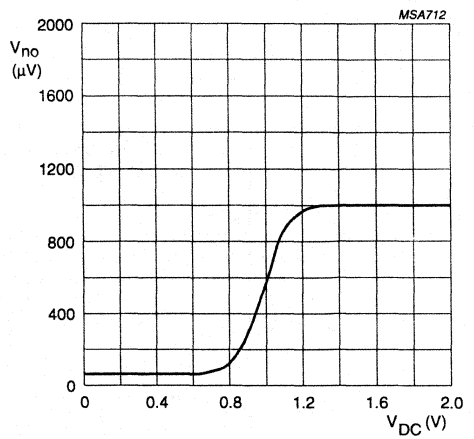


Fig.3 Gain control as a function of DC volume control.



(1) The noise output voltage (RMS value) is measured with R_S = 5 kΩ unweighted.

Fig.4 Noise output voltage as a function of DC volume control.

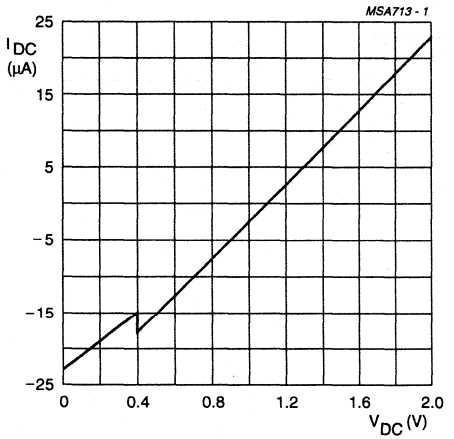
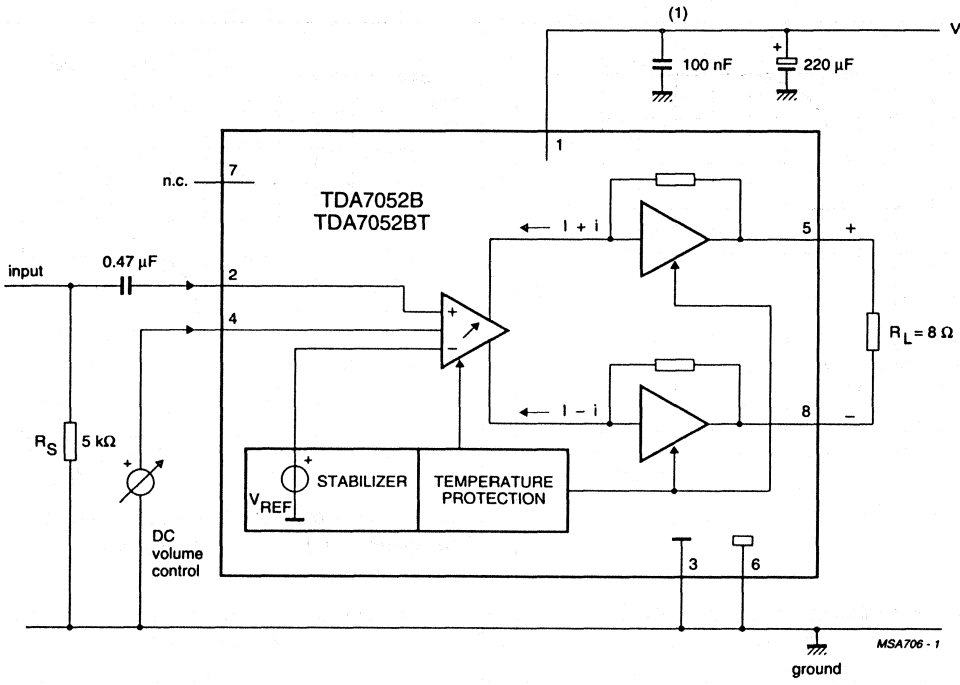


Fig.5 Control current as a function of DC volume control.

APPLICATION INFORMATION



(1) This capacitor can be omitted if the 220 µF electrolytic capacitor is connected close to pin 1.

Fig.6 Test and application diagram.

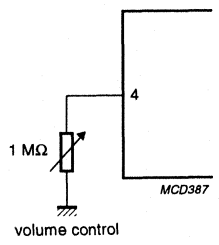


Fig.7 Application with potentiometer as volume control; maximum gain = 34 dB.

2 × 1 W PORTABLE/MAINS-FED STEREO POWER AMPLIFIER

GENERAL DESCRIPTION

The TDA7053 is an integrated class-B stereo power amplifier in a 16-lead dual-in-line (DIL) plastic package. The device, consisting of two BTL amplifiers, is primarily developed for portable audio applications but may also be used in mains-fed applications.

Features

- No external components
- No switch-ON/OFF clicks
- Good overall stability
- Low power consumption
- Short-circuit-proof

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage range		V_P	3	6	18	V
Total quiescent current	$R_L = \infty$	I_{tot}	–	9	16	mA
Output power	$R_L = 8\ \Omega$; $V_P = 6$ V	P_O	–	1.2	–	W
Internal voltage gain		G_v	38	39	40	dB
Total harmonic distortion	$P_O = 0.1$ W	THD	–	0.2	1.0	%

PACKAGE OUTLINE

16-lead DIL; plastic (SOT38).

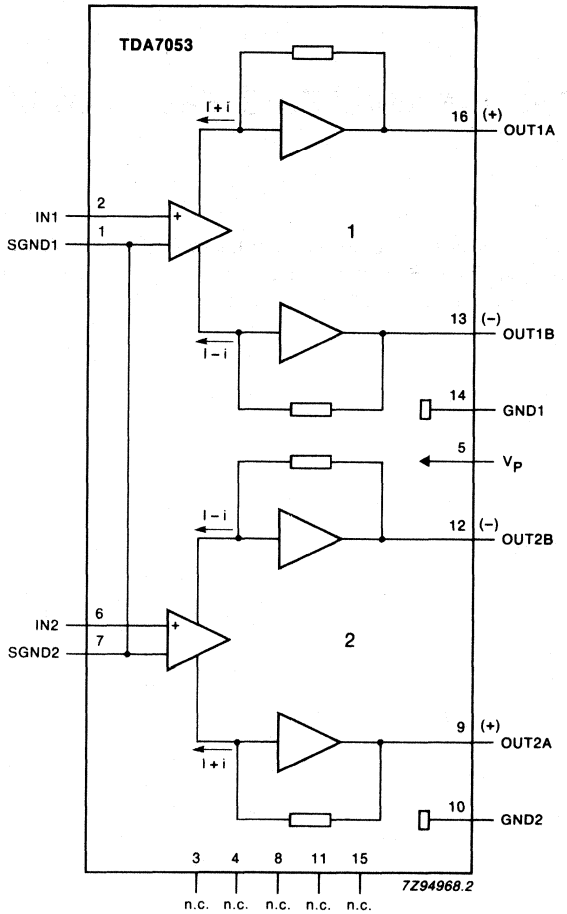


Fig. 1 Block diagram.

PINNING

1.	SGND1	signal ground 1	9.	OUT2A	output 2 (positive)
2.	IN1	input 1	10.	GND2	power ground 2
3.	n.c.	not connected	11.	n.c.	not connected
4.	n.c.	not connected	12.	OUT2B	output 2 (negative)
5.	V_P	supply voltage	13.	OUT1B	output 1 (negative)
6.	IN2	input 2	14.	GND1	power ground 1
7.	SGND2	signal ground 2	15.	n.c.	not connected
8.	n.c.	not connected	16.	OUT1A	output 1 (positive)

Note

The information contained within the parentheses refer to the polarity of the loudspeaker terminal to which the output must be connected.

FUNCTIONAL DESCRIPTION

The TDA7053 is a stereo output amplifier, with an internal gain of 39 dB, which is primarily for use in portable audio applications but may also be used in mains-fed applications. The current trends in portable audio application design is to reduce the number of batteries which results in a reduction of output power when using conventional output stages. The TDA7053 overcomes this problem by using the Bridge-Tied-Load (BTL) principle and is capable of delivering 1.2 W into an 8 Ω load (V_P = 6 V). The load can be short-circuited under all input conditions.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage		V_P	–	18	V
Non-repetitive peak output current		I_{OSM}	–	1.5	A
Total power dissipation		P_{tot}	see Fig. 2		
Crystal temperature		T_c	–	+150	°C
Storage temperature range		T_{stg}	−55	+150	°C

THERMAL RESISTANCE

From junction to ambient	$R_{th\ j\text{-}a}$	50	K/W

Power dissipation

Assuming: $V_P = 6$ V and $R_L = 8\ \Omega$:

The maximum sinewave dissipation is 1.8 W, therefore $T_{amb(max.)} = 150 - (50 \times 1.8) = 60$ °C.

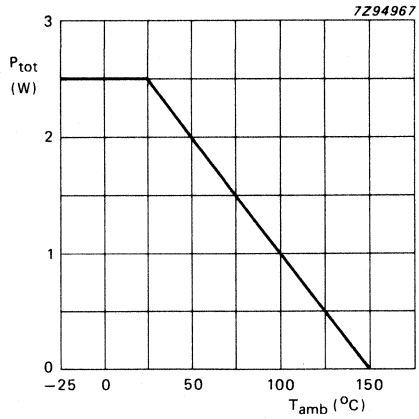


Fig. 2 Power derating curve.

CHARACTERISTICS

V_P = 6 V; R_L = 8 Ω; T_{amb} = 25 °C; unless otherwise specified; measured from test circuit, Fig. 7.

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage range		V_P	3	6	18	V
Total quiescent current	$R_L = \infty$; note 1	I_{tot}	–	9	16	mA
Input bias current		I_{bias}	–	100	300	nA
Supply voltage ripple rejection	note 2	SVRR	40	50	–	dB
Input impedance		Z_I	–	100	–	kΩ
DC output offset voltage	note 3	ΔV_{13-16}	–	–	100	mV
		ΔV_{12-9}	–	–	100	mV
Noise output voltage (RMS value)	note 4	$V_{no(rms)}$	–	150	300	μV
	note 5	$V_{no(rms)}$	–	60	–	μV
Output power	THD = 10%	P_O	–	1.2	–	W
Total harmonic distortion	P_O = 0.1 W	THD	–	0.2	1.0	%
Internal voltage gain		G_v	38	39	40	dB
Channel balance		ΔG_v	–	–	1	dB
Channel separation	note 3	α	40	–	–	dB
Frequency response		f	–	0.02 to 20	–	kHz

Notes to the characteristics

1. With a practical load the total quiescent current depends on the offset voltage.
2. Ripple rejection measured at the output with R_S = 0 Ω and f = 100 Hz to 10 kHz. The ripple voltage (200 mV) is applied to the positive supply rail.
3. R_S = 5 kΩ.
4. The noise output voltage (RMS value) is measured with R_S = 5 kΩ, unweighted and a bandwidth of 60 Hz to 15 kHz.
5. The noise output voltage (RMS value) is measured with R_S = 0 Ω and f = 500 kHz with 5 kHz bandwidth. If R_L = 8 Ω and L_L = 200 μH the noise output current is only 100 nA.

APPLICATION INFORMATION

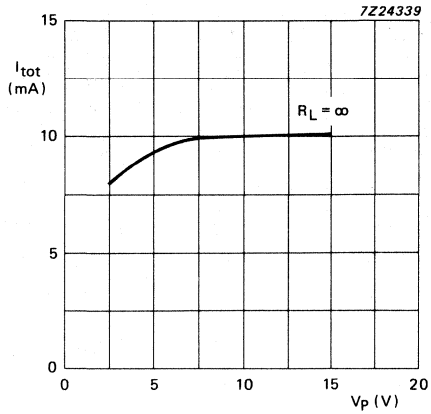


Fig. 3 Quiescent current as a function of voltage supply (V_P); T_{amb} = 60 °C.

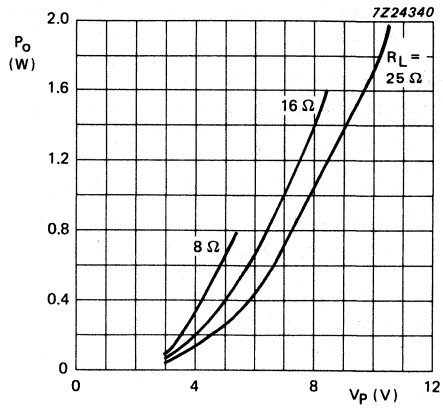
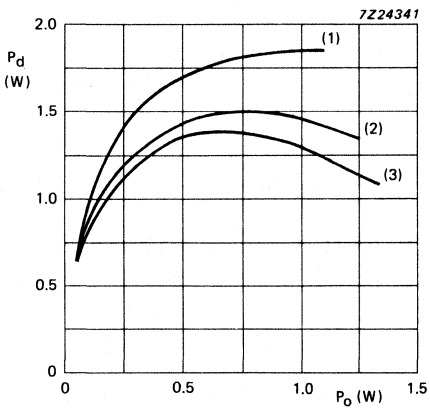
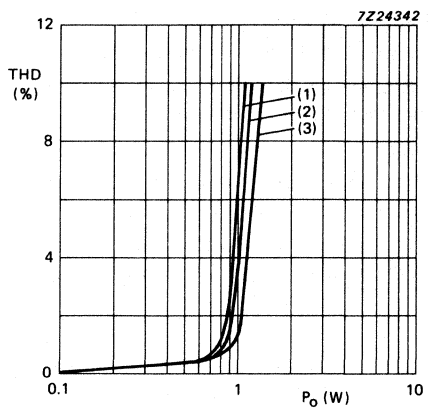


Fig. 4 Output power as a function of voltage supply (V_P); THD = 10%; f = 1 kHz; T_{amb} = 60 °C.



(1) V_P = 6.0 V; R_L = 8 Ω
(2) V_P = 7.5 V; R_L = 16 Ω
(3) V_P = 9.0 V; R_L = 25 Ω

Fig. 5 Power dissipation as a function of output power; f = 1 kHz; T_{amb} = 60 °C.



(1) V_P = 6.0 V; R_L = 8 Ω
(2) V_P = 7.5 V; R_L = 16 Ω
(3) V_P = 9.0 V; R_L = 25 Ω

Fig. 6 Total harmonic distortion as a function of output power; f = 1 kHz; T_{amb} = 60 °C.

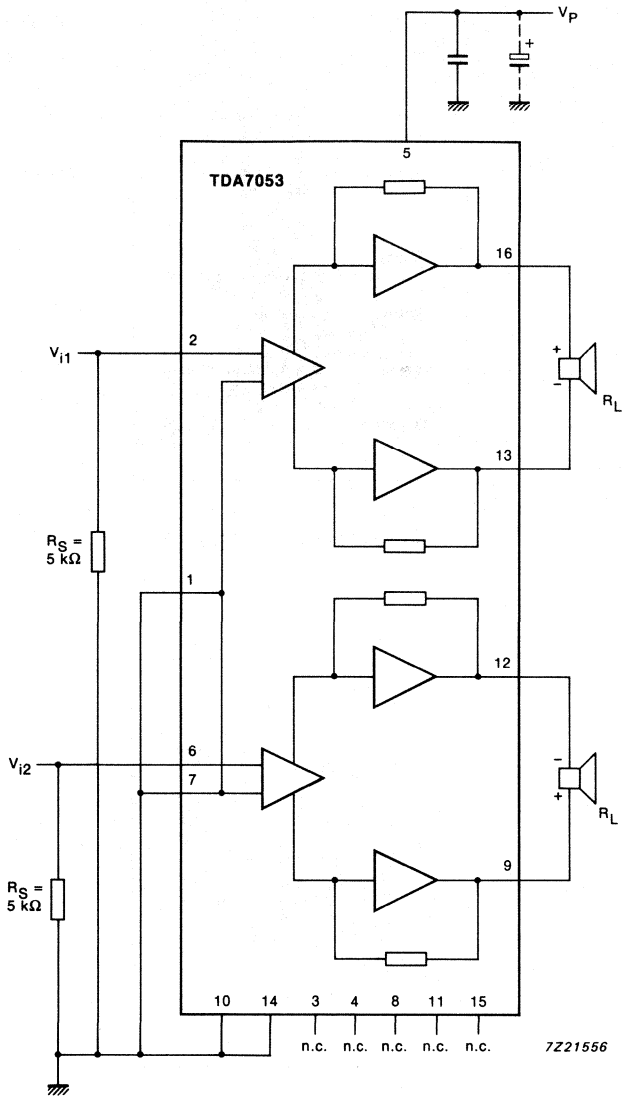


Fig. 7 Test and application circuit diagram.

APPLICATION INFORMATION (continued)

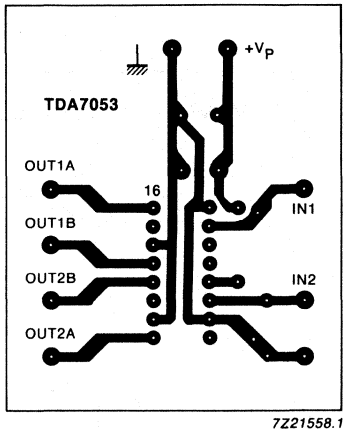


Fig. 8 Printed-circuit board, track side.

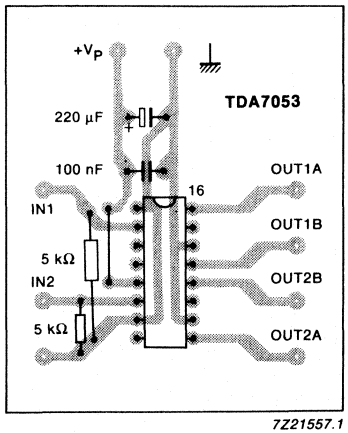


Fig. 9 Printed-circuit board, component side.

Stereo BTL audio output amplifiers with DC volume control

TDA7053A; TDA7053AT

FEATURES

- DC volume control
- Few external components
- Mute mode
- Thermal protection
- Short-circuit proof
- No switch-on and switch-off clicks
- Good overall stability
- Low power consumption
- Low HF radiation
- ESD protected on all pins.

GENERAL DESCRIPTION

The TDA7053A (2 x 1 W) and TDA7053AT (2 x 0.5 W) are stereo BTL output amplifiers wih DC volume control. The devices are designed for use in TV and monitors, but also suitable for battery-fed portable recorders and radios.

Missing Current Limiter (MCL)

A MCL protection circuit is built-in. The MCL circuit is activated when the difference in current between the output terminal of each amplifier exceeds 100 mA (typical 300 mA). This level of 100 mA allows for headphone applications (single-ended).

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	positive supply voltage		4.5	–	18	V
P_O	output power	V_P = 6 V				
	TDA7053A	R_L = 8 Ω	0.85	1.0	–	W
	TDA7053AT	R_L = 16 Ω	0.5	0.55	–	W
G_v	total voltage gain		39.5	40.5	41.5	dB
ϕ	gain control range		68	73.5	–	dB
I_P	total quiescent current	V_P = 6 V; R_L = ∞	–	15	25	mA
THD	total harmonic distortion					
	TDA7053A	P_O = 0.5 W	–	0.3	1	%
	TDA7053AT	P_O = 0.25 W	–	0.3	1	%

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA7053A	16	DIL	plastic	SOT38
TDA7053AT	16	mini-pack	plastic	SOT162A

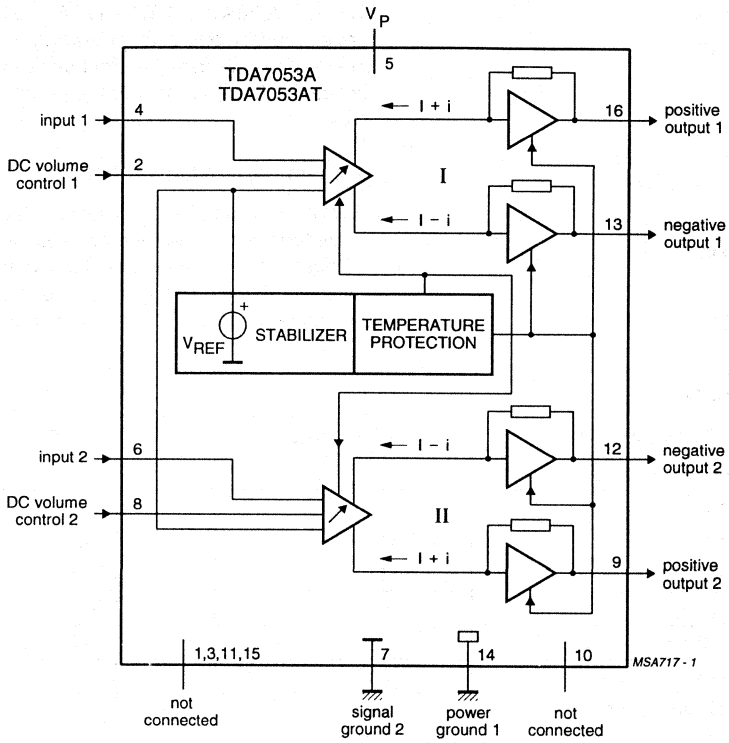


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
n.c.	1	not connected
VC1	2	DC volume control 1
n.c.	3	not connected
$V_{I(1)}$	4	voltage input 1
V_P	5	positive supply voltage
$V_{I(2)}$	6	voltage input 2
SGND	7	signal ground
VC2	8	DC volume control 2
OUT2+	9	positive output 2
n.c.	10	not connected
n.c.	11	not connected
OUT2–	12	negative output 2
OUT1–	13	negative output 1
PGND	14	power ground
n.c.	15	not connected
OUT1+	16	positive output 1

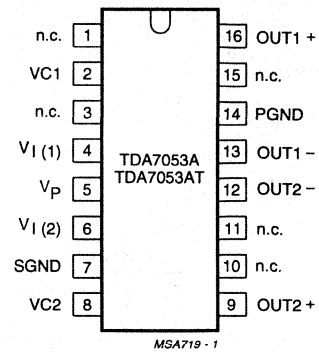


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The TDA7053A and TDA7053AT are stereo output amplifiers with two DC volume control stages, designed for TV and monitors, but also suitable for battery-fed portable recorders and radios.
In convential DC volume control circuits the control or input stage is AC coupled to the output stage via external capacitors to keep the offset voltage low.
The two DC volume control stages are integrated into the input stages so that no coupling capacitors are required and yet a low offset voltage is maintained. Also the minimum supply voltage remains low.
The BTL principle offers the following advantages:

- Lower peak value of the supply current
- The frequency of the ripple on the supply voltage is twice the signal frequency.

Consequently, a reduced power supply with smaller capacitors can be used which results in cost reductions.

For portable applications there is a trend to decrease the supply voltage, resulting in a reduction of output power at conventional output stages. Using the BTL principle increases the output power.

The maximum gain of the amplifier is fixed at 40.5 dB. The DC volume control stages have a logarithmic control characteristic. Therefore, the total gain can be controlled from 40.5 dB to –33 dB.
If the DC volume control voltage falls below 0.4 V, the device will switch to the mute mode.

The amplifier is short-circuit proof to ground, V_P and across the load. Also a thermal protection circuit is implemented. If the crystal temperature rises above +150 °C the gain will be reduced, thereby reducing the output power.
Special attention is given to switch-on and switch-off clicks, low HF radiation and a good overall stability.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_P	positive supply voltage		–	18	V
I_{ORM}	repetitive peak output current		–	1.25	A
I_{OSM}	non-repetitive peak output current		–	1.5	A
P_{tot}	total power dissipation	$T_{amb} \leq 25$ °C			
	TDA7053A		–	2.5	W
	TDA7053AT		–	1.32	W
T_{amb}	operating ambient temperature		–40	+85	°C
T_{stg}	storage temperature		–55	+150	°C
T_{vj}	virtual junction temperature		–	+150	°C
T_{sc}	short-circuit time		–	1	hr
V_n	input voltage pins 2, 4, 6 and 8		–	5	V

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient	
	TDA7053A	50 K/W
	TDA7053AT	95 K/W

Power dissipation

TDA7053A

Assume $V_P = 6$ V; $R_L = 8\ \Omega$.
The maximum sinewave dissipation is 2 x 0.9 W = 1.8 W.
The $R_{th\ j\text{-}a}$ of the package is 50 K/W;
So $T_{amb\ (max)} = 150 - (50 \times 1.8) = 60$ °C.

TDA7053AT

Assume $V_P = 6$ V; $R_L = 16\ \Omega$.
The maximum sinewave dissipation is 2 x 0.46 W = 0.92 W.
The $R_{th\ j\text{-}a}$ of the package is 95 K/W;
So $T_{amb\ (max)} = 150 - (95 \times 0.92) = 62.6$ °C.

CHARACTERISTICS

V_P = 6 V; T_{amb} = 25 °C; f = 1 kHz; TDA7053A: R_L = 8 Ω; TDA7053AT: R_L = 16 Ω; unless otherwise specified (see Fig.6).

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	positive supply voltage		4.5	–	18	V
I_P	total quiescent current	note 1; V_P = 6 V; R_L = ∞	–	15	25	mA
Maximum gain; $V_{2,8} \geq$ 1.4 V						
P_O	output power	THD = 10%				
	TDA7053A		0.85	1.0	–	W
	TDA7053AT		0.5	0.55	–	W
THD	total harmonic distortion					
	TDA7053A	P_O = 0.5 W	–	0.3	1	%
	TDA7053AT	P_O = 0.25 W	–	0.3	1	%
G_v	voltage gain		39.5	40.5	41.5	dB
$V_{I(RMS)}$	input signal handling (RMS value)	G_v = 0 dB; THD < 1%	1	–	–	V
V_{no}	noise output voltage	note 2; f = 500 kHz;	–	210	–	μV
B	bandwidth	at –1 dB	–	20 Hz to 300 kHz	–	Hz
SVRR	supply voltage ripple rejection	note 3	34	38	–	dB
$\lvert\Delta V_O\rvert$	DC output offset voltage	$\lvert V_{16}-V_{13}\rvert$ and $\lvert V_{12}-V_9\rvert$	–	0	200	mV
Z_I	input impedance (pins 4 and 6)		15	20	25	kΩ
α	channel separation	R_S = 5 kΩ	40	–	–	dB
$\lvert G_v\rvert$	channel unbalance	note 4	–	–	1	dB
$\lvert G_v\rvert$	channel unbalance at G_1 = 0 dB	note 5	–	–	tbf	dB
Mute position						
V_O	output voltage in mute position	note 6; $V_{2,8}$ = 0.4 V ±30 mV; V_I = 1.0 V	–	30	40	μV
DC volume control						
ϕ	gain control		68	73.5	–	dB
I_P	control current	V_2, V_8 = 0 V	20	25	30	μA

Notes

1. With a load connected to the outputs the quiescent current will increase, the maximum value of this increase being equal to the DC output offset voltage divided by R_L.
2. The noise output voltage (RMS value) at f = 500 kHz is measured with R_S = 0 Ω and bandwidth = 5 kHz.
3. The ripple rejection is measured with R_S = 0 Ω and f = 100 Hz to 10 kHz. The ripple voltage of 200 mV (RMS value) is applied to the positive supply rail.
4. The channel unbalance is measured with $V_{DC1} = V_{DC2}$.
5. The channel unbalance at G_1 = 0 dB is measured with $V_{DC1} = V_{DC2}$.
6. The noise output voltage (RMS value) is measured with R_S = 5 kΩ unweighted.

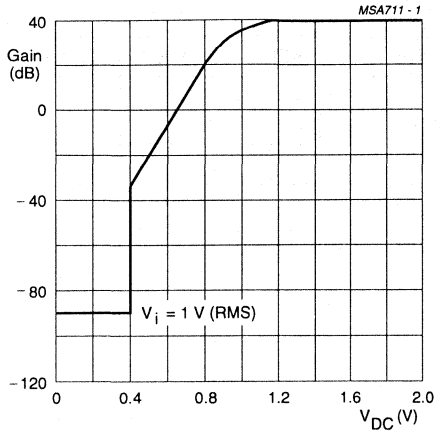
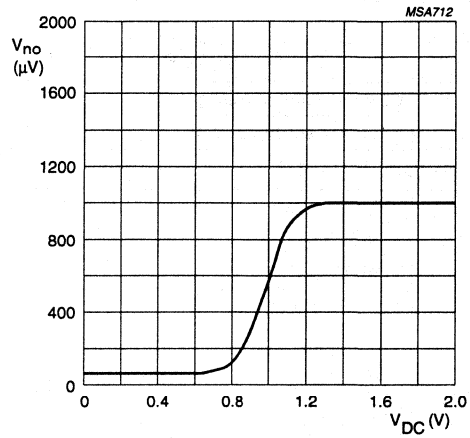


Fig.3 Gain control as a function of DC volume control.



The noise output voltage (RMS value) is measured with R_S = 5 kΩ unweighted.

Fig.4 Noise output voltage as a function of DC volume control.

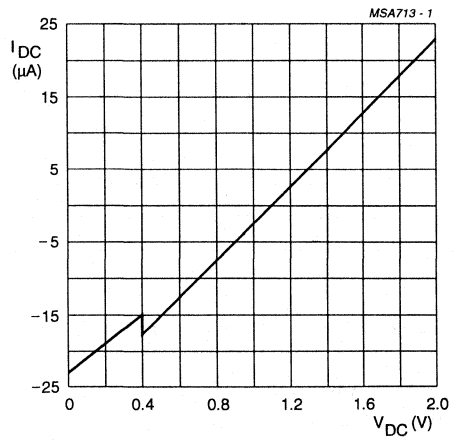
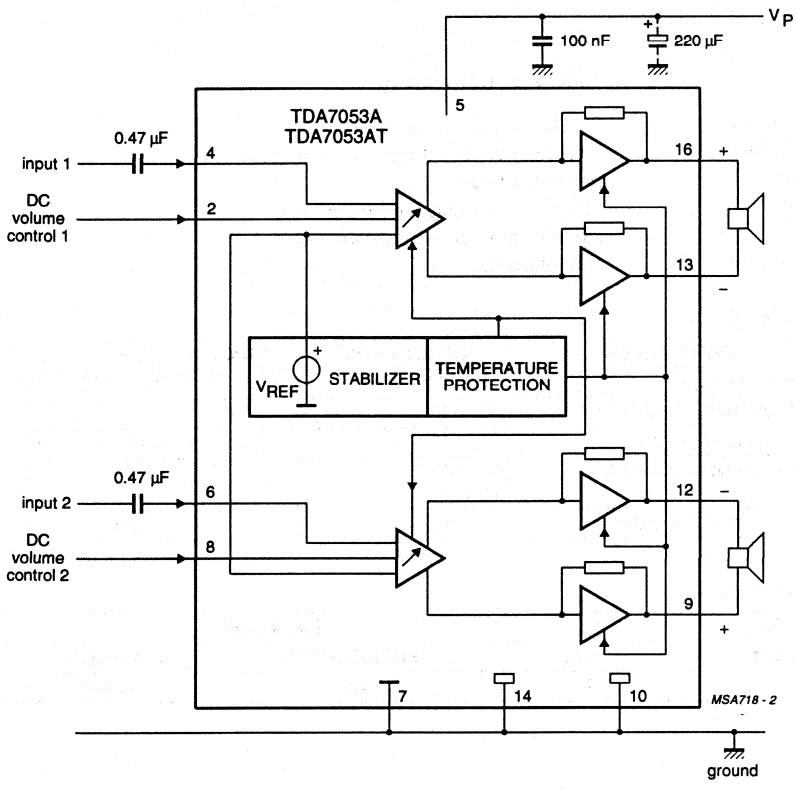


Fig.5 Control current as a function of DC volume control.

APPLICATION INFORMATION



(1) This capacitor can be omitted if the 220 µF electrolytic capacitor is connected close to pin 5.
(2) TDA7053AT: R_L = 16 Ω.

Fig.6 Test and application diagram.

Philips Semiconductors

Data sheet	
status	Product specification
date of issue	May 1992

TDA7056

3 Watt mono BTL audio output amplifier

FEATURES

- No external components
- No switch-on/off clicks
- Good overall stability
- Low power consumption
- Short circuit proof
- ESD protected on all pins

GENERAL DESCRIPTION

The TDA7056 is a mono output amplifier contained in a 9 pin medium power package.
The device is designed for battery-fed portable mono recorders, radios and television.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage		3	11	18	V
P_O	output power in 16 Ω	V_P = 11 V	2.5	3	-	W
G_V	internal voltage gain		39	40.5	42	dB
I_P	total quiescent current	V_P = 11 V; $R_L = \infty$	-	5	7	mA
THD	total harmonic distortion	P_O = 0.5 W	-	0.25	1	%

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA7056	9	SIL	plastic	SOT110

3 Watt mono BTL audio output amplifier TDA7056

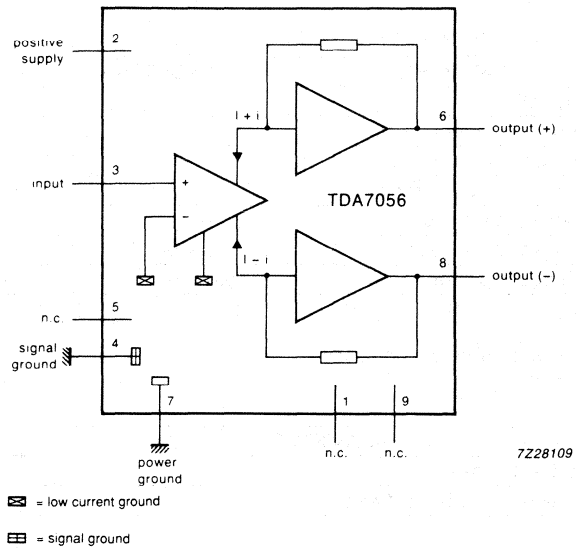


Fig.1 Block diagram.

PINNING

PIN	DESCRIPTION
1	n.c.
2	V_P
3	input (+)
4	signal ground
5	n.c.
6	output (+)
7	power ground
8	output (-)
9	n.c.

FUNCTIONAL DESCRIPTION

The TDA7056 is a mono output amplifier, designed for battery-fed portable radios and mains-fed equipment such as television.
For space reasons there is a trend to decrease the number of external components. For portable applications there is also a trend to decrease the number of battery cells, but still a reasonable output power is required.
The TDA7056 fulfills both of these requirements. It needs no peripheral components, because it makes use of the Bridge-Tied-Load (BTL) principle. Consequently it has, at the same supply voltage, a higher output power compared to a conventional Single Ended output stage. It delivers an output power of 1 W into a loudspeaker load of 8 Ω with 6 V supply or 3 W into 16 Ω loudspeaker at 11 V without need of an external heatsink. The gain is internally fixed at 40 dB. Special attention is given to switch-on/off click suppression, and it has a good overall stability. The load can be short circuited at all input conditions.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_P	supply voltage		-	18	V
I_{ORM}	Peak output current repetitive		-	1	A
I_{OSM}	Peak output current non-repetitive		-	1.5	A
T_{stg}	storage temperature range		–55	150	°C
T_j	junction temperature		-	150	°C
P_{tot}	total power dissipation	$T_{case} < 60$ °C	-	9	W
T_{sc}	short circuiting time	see note	-	1	hr

Note

The load can be short-circuited at all input conditions.

THERMAL RESISTANCE

SYMBOL	PARAMETER	NOM.	UNIT
$R_{th\ j\text{-}c}$	from junction to case	10	K/W
$R_{th\ j\text{-}a}$	from junction to ambient in free air	55	K/W

POWER DISSIPATION

Assume: $V_P = 11$ V; $R_L = 16\ \Omega$.

The maximum sine-wave dissipation is 1.52 W.

The $R_{th\ j\text{-}a}$ of the package is 55 K/W.

T_{amb} max = 150 - 55 x 1.52 = 66.4 °C.

CHARACTERISTICS

At T_{amb} = 25 °C; f = 1 kHz; V_P = 11 V; R_L = 16 Ω (see Fig.2)

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	operating supply voltage		3	11	18	V
I_{ORM}	repetitive peak output current		-	-	0.6	A
I_P	total quiescent current	note 1 $R_L = \infty$	-	5	7	mA
P_O	output power	THD = 10%	2.5	3	-	W
THD	total harmonic distortion	P_O = 0.5 W	-	0.25	1	%
G_v	voltage gain		39	40.5	42	dB
V_{no}	noise output voltage	note 2	-	180	300	μV
V_{no}	noise output voltage	note 3	-	60	-	μV
	frequency response		-	20 to 20.000	-	Hz
RR	ripple rejection	note 4	36	50	-	dB
ΔV	DC-output offset voltage	note 5	-	-	200	mV
$\|Z_i\|$	input impedance		-	100	-	kΩ
I_i	input bias current		-	100	300	nA

Notes to the characteristics

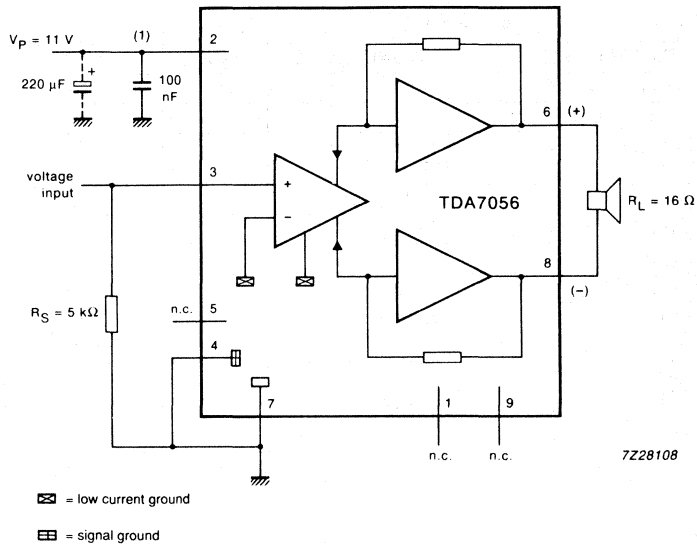
1. With a load connected to the outputs the quiescent current will increase, the maximum value of this increase being equal to the DC output offset voltage divided by R_L.

2. The noise output voltage (RMS value) is measured with R_S = 5 kΩ unweighted (20 Hz to 20 kHz).

3. The noise output voltage (RMS value) at f = 500 kHz is measured with R_S = 0 Ω and bandwidth = 5 kHz. With a practical load (R_L = 16 Ω, L_L = 200 μH) the noise output current is only 50 nA.

4. The ripple rejection is measured with R_S = 0 Ω and f = 100 Hz to 10 kHz. The ripple voltage (200 mV) is applied to the positive supply rail.

5. R_S = 5 kΩ



(1) This capacitor can be omitted if the supply electrolytic capacitor is placed closer to pin 2.

Fig.2 Test and application diagram.

3 W BTL mono audio output amplifier with DC volume control

TDA7056A

FEATURES

- DC volume control
- Few external components
- Mute mode
- Thermal protection
- Short-circuit proof
- No switch-on and off clicks
- Good overall stability
- Low power consumption
- Low HF radiation
- ESD protected on all pins.

GENERAL DESCRIPTION

The TDA7056A is a mono BTL output amplifier with DC volume control. It is designed for use in TV and monitors, but also suitable for battery-fed portable recorders and radios.

Missing Current Limiter (MCL)

A MCL protection circuit is built-in. The MCL circuit is activated when the difference in current between the output terminal of each amplifier exceeds 100 mA (typical 300 mA). This level of 100 mA allows for headphone applications (single-ended).

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	positive supply voltage range		4.5	–	18	V
P_O	output power	R_L = 16 Ω; V_P = 12 V	3	3.5	–	W
G_v	voltage gain		34.5	35.5	36.5	dB
ϕ	gain control range		75	80	–	dB
I_P	total quiescent current	V_P = 12 V; R_L = ∞	–	8	16	mA
THD	total harmonic distortion	V_P = 0.5 W	–	0.3	1	%

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA7056A	9	SIL	plastic	SOT110

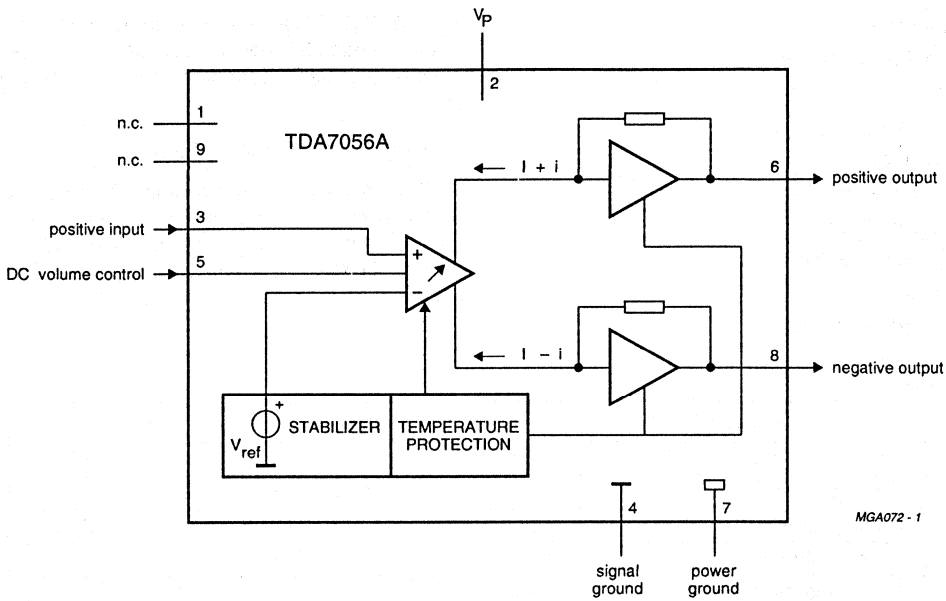


Fig.1 Block diagram.

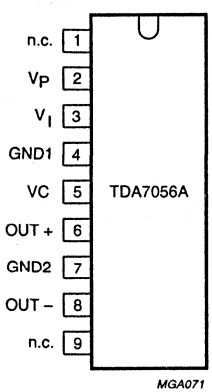


Fig.2 Pin configuration.

PINNING

SYMBOL	PIN	DESCRIPTION
n.c.	1	not connected
V_P	2	positive supply voltage
V_I	3	voltage input
GND1	4	signal ground
VC	5	DC volume control
OUT+	6	positive output
GND2	7	power ground
OUT−	8	negative output
n.c.	9	not connected

3 W BTL mono audio output amplifier with DC volume control

TDA7056A

FUNCTIONAL DESCRIPTION

The TDA7056A is a mono BTL output amplifier with DC volume control, designed for use in TV and monitor but also suitable for battery-fed portable recorders and radios.
In conventional DC volume circuits the control or input stage is AC coupled to the output stage via external capacitor to keep the offset voltage low.
In the TDA7056A the DC volume stage is integrated into the input stage so that coupling capacitors are not required and a low offset voltage is maintained.
At the same time the minimum supply voltage remains low.
The BTL principle offers the following advantages:

- lower peak value of the supply current
- the frequency of the ripple on the supply voltage is twice the signal frequency

Thus, a reduced power supply and smaller capacitors can be used which results in cost savings.
For portable applications there is a trend to decrease the supply voltage, resulting in a reduction of output power at conventional output stages. Using the BTL principle increases the output power.

The maximum gain of the amplifier is fixed at 35.5 dB.
The DC volume control stage has a logarithmic control characteristic.
The total gain can be controlled from 35.5 dB to –44 dB.
If the DC volume control voltage is below 0.3 V, the device switches to the mute mode.
The amplifier is short-circuit proof to ground, V_P and across the load. A thermal protection circuit is also implemented. If the crystal temperature rises above +150 °C the gain will be reduced, thereby reducing the output power.
Special attention is given to switch-on and off clicks, low HF radiation and a good overall stability.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_P	supply voltage range		–	18	V
I_{ORM}	repetitive peak output current		–	1.25	A
I_{OSM}	non repetitive peak output current		–	1.5	A
P_{tot}	total power dissipation	T_{case} < 60 °C	–	9	W
T_{amb}	operating ambient temperature range		–40	+85	°C
T_{stg}	storage temperature range		–55	+150	°C
T_{vj}	virtual junction temperature		–	+150	°C
T_{sc}	short-circuit time		–	1	hr
V_3	input voltage pin 3		–	8	V
V_5	input voltage pin 5		–	8	V

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient in free air	55 K/W
$R_{th\ j\text{-}c}$	from junction to case	10 K/W

Note to the thermal resistance

V_P = 12 V; R_L = 16 Ω; The maximum sine-wave dissipation is = 1.8 W. The $R_{th\ vj\text{-}a}$ of the package is 55 K/W; $T_{amb\ (max)}$ = 150 – 55 x 1.8 = 51 °C

CHARACTERISTICS

V_P = 12 V; f = 1 kHz; R_L = 16 Ω; T_{amb} = 25 °C; unless otherwise specified (see Fig.6)

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	positive supply voltage range		4.5	–	18	V
I_P	total quiescent current	V_P = 12 V; R_L = ∞; note 1	–	8	16	mA
Maximum gain (V_5 = 1.4 V)						
P_O	output power					
		THD = 10%; R_L = 16 Ω	3	3.5	–	W
		THD = 10%; R_L = 8 Ω	–	5.2	–	W
THD	total harmonic distortion	P_O = 0.5 W	–	0.3	1	%
G_v	voltage gain		34.5	35.5	36.5	dB
V_I	input signal handling	V_5 = 0.8 V;THD < 1%	0.5	0.65	–	V
$V_{no(rms)}$	noise output voltage (RMS value)	f = 500 kHz; note 2	–	210	–	μV
B	bandwidth	at –1 dB	–	20 Hz to 300 kHz	–	
SVRR	supply voltage ripple rejection	note 3	38	46	–	dB
$\lvert V_{off}\rvert$	DC output offset voltage		–	0	150	mV
Z_I	input impedance pin 3		15	20	25	kΩ
Minimum gain (V_5 = 0.5 V)						
G_v	voltage gain		–	–44	–	dB
$V_{no(rms)}$	noise output voltage (RMS value)	note 4	–	20	30	μV
Mute position						
V_O	output voltage in mute position	$V_5 \leq$ 0.3 V; V_I = 600 mV	–	–	30	μV
DC volume control						
ϕ	gain control range		75	80	–	dB
I_5	control current	V_5 = 0 V	60	70	80	μA

Notes to the characteristics

1. With a load connected to the outputs the quiescent current will increase, the maximum value of this increase being equal to the DC output offset voltage divided by R_L.
2. The noise output voltage (RMS value) at f = 500 kHz is measured with R_S = 0 Ω and bandwidth = 5 kHz.
3. The ripple rejection is measured with R_S = 0 Ω and f = 100 Hz to 10 kHz. The ripple voltage of 200 mV (RMS value) is applied to the positive supply rail.
4. The noise output voltage (RMS value) is measured with R_S = 5 kΩ unweighted.

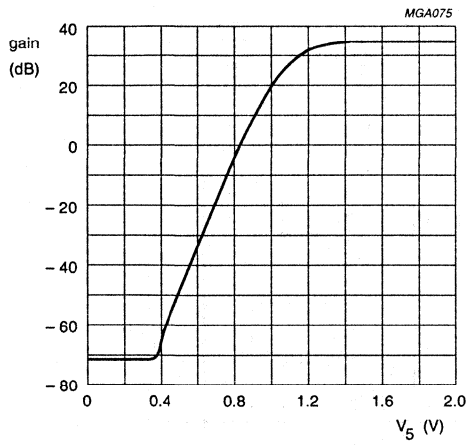


Fig.3 Gain as a function of DC volume control.

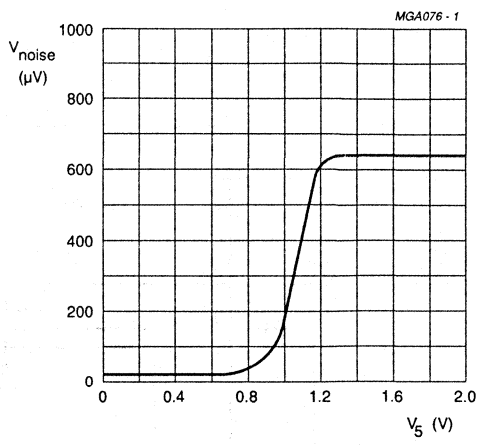


Fig.4 Noise output voltage as a function of DC volume control.

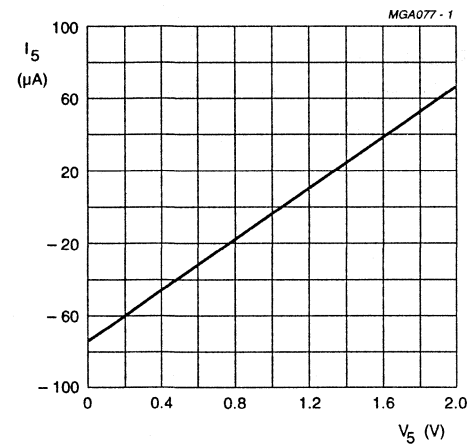
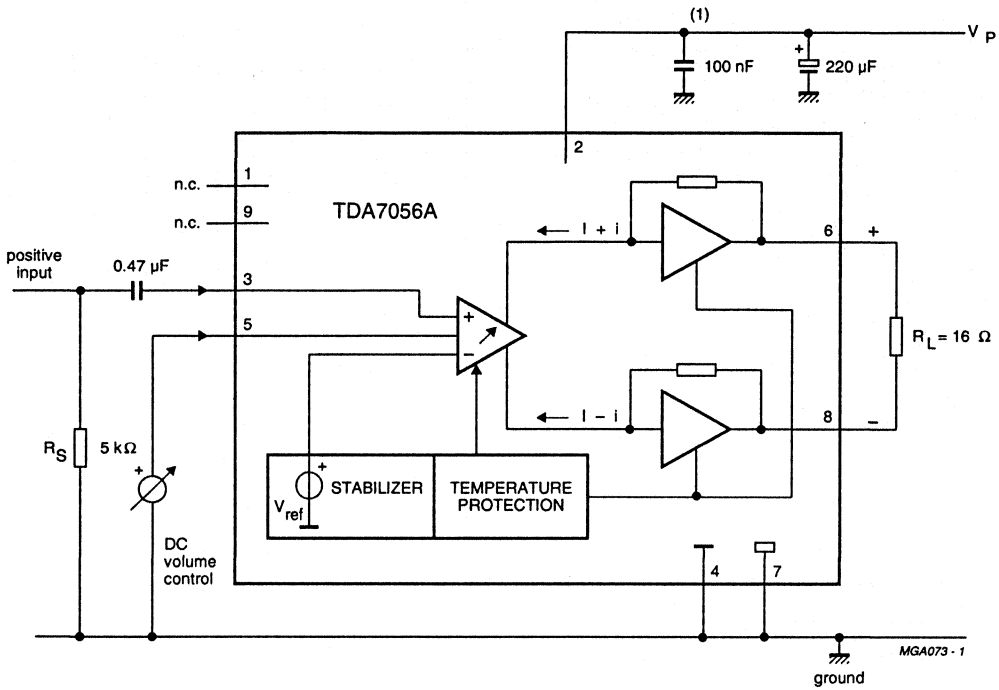


Fig.5 Control current as a function of DC volume control.

APPLICATION INFORMATION



(1) This capacitor can be omitted if the 220 µF electrolytic capacitor is connected close to pin 2.

Fig.6 Test and application diagram.

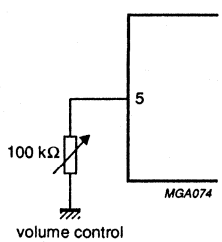


Fig.7 Application using a potentiometer for volume control; G_v = 30 dB.

5 W mono BTL audio amplifier with DC volume control

TDA7056B

FEATURES

- DC volume control
- Few external components
- Mute mode
- Thermal protection
- Short-circuit proof
- No switch-on and off clicks
- Good overall stability
- Low power consumption
- Low HF radiation
- ESD protected on all pins.

GENERAL DESCRIPTION

The TDA7056B is a mono BTL output amplifier with DC volume control. It is designed for use in TV and monitors, but is also suitable for battery-fed portable recorders and radios. The device is contained in a 9-pin medium power package.

Missing Current Limiter (MCL)

A MCL protection circuit is built-in. The MCL circuit is activated when the difference in current between the output terminal of each amplifier exceeds 100 mA (typical 300 mA). This level of 100 mA allows for headphone applications (single-ended).

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	positive supply voltage		4.5	–	18	V
P_O	output power	V_P = 12 V				
		R_L = 16 Ω	3	3.5	–	W
		R_L = 8 Ω	–	5	–	W
G_v	maximum voltage gain		39.5	40.5	41.5	dB
ϕ	gain control		68	73.5	–	dB
I_P	total quiescent current	V_P = 12 V; R_L = ∞	–	9.2	13	mA
THD	total harmonic distortion	P_O = 0.5 W	–	0.3	1	%

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA7056B	9	SIL	plastic	SOT110BE

5 W mono BTL audio amplifier with DC volume control

TDA7056B

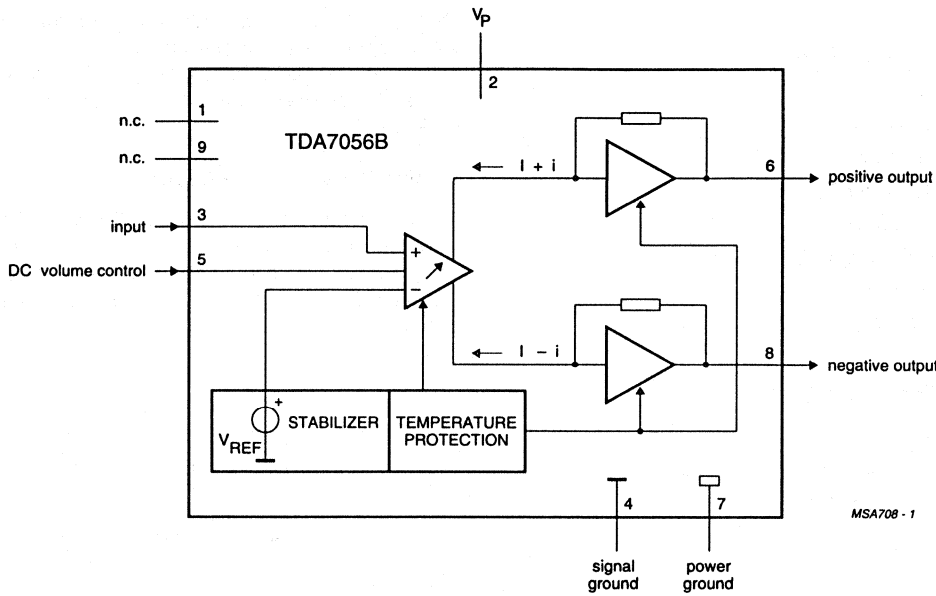


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
n.c.	1	not connected
V_P	2	positive supply voltage
V_I	3	voltage input
GND1	4	signal ground
VC	5	DC volume control
OUT+	6	positive output
GND2	7	power ground
OUT−	8	negative output
n.c.	9	not connected

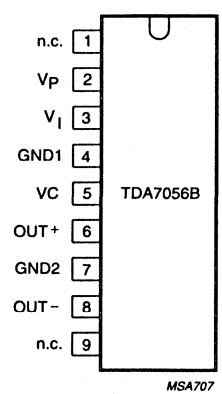


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The TDA7056B is a mono BTL output amplifier with DC volume control, designed for use in TV and monitor but is also suitable for battery-fed portable recorders and radios.

In conventional DC volume circuits the control or input stage is AC coupled to the output stage via external capacitor to keep the offset voltage low. In the TDA7056B the DC volume control stage is integrated into the input stage so that no coupling capacitors are required. With this configuration, a low offset voltage is still maintained and the minimum supply voltage remains low.

The BTL principle offers the following advantages:

- lower peak value of the supply current
- the frequency of the ripple on the supply voltage is twice the signal frequency

Consequently, a reduced power supply and smaller capacitors can be used which results in cost reductions. For portable applications there is a trend to decrease the supply voltage, resulting in a reduction of output power at conventional output stages. Using the BTL principle increases the output power.

The maximum gain of the amplifier is fixed at 40.5 dB. The DC volume control stage has a logarithmic control characteristic. Therefore, the total gain can be controlled from 40.5 dB to −33 dB.
If the DC volume control voltage falls below 0.4 V, the device will switch to the mute mode.

The amplifier is short-circuit proof to ground, V_P and across the load. A thermal protection circuit is also implemented. If the crystal temperature rises above +150 °C the gain will be reduced, thereby reducing the output power.
Special attention is given to switch-on and switch-off clicks, low HF radiation and a good overall stability.

Power dissipation

Assume V_P = 12 V; R_L = 16 Ω; The maximum sinewave dissipation is = 1.8 W.

The $R_{th\ vj\text{-}a}$ of the package is 55 K/W; $T_{amb\ (max)}$ = 150 − 55 x 1.8 = 51 °C.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_P	positive supply voltage		–	18	V
I_{ORM}	repetitive peak output current		–	1.25	A
I_{OSM}	non repetitive peak output current		–	1.5	A
P_{tot}	total power dissipation	T_{case} < 60 °C	–	9	W
T_{amb}	operating ambient temperature		−40	+85	°C
T_{stg}	storage temperature		−55	+150	°C
T_{vj}	virtual junction temperature		–	+150	°C
T_{sc}	short-circuit time		–	1	hr
$V_{3,\ 5}$	input voltage pins 3 and 5		–	5	V

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient in free air	55 K/W
$R_{th\ j\text{-}c}$	from junction to case	10 K/W

CHARACTERISTICS

V_P = 12 V; f = 1 kHz; R_L = 16 Ω; T_{amb} = 25 °C; unless otherwise specified (see Fig.6).

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_P	positive supply voltage		4.5	–	18	V
I_P	total quiescent current	note 1; V_P = 12 V; R_L = ∞	–	9.2	13	mA
Maximum gain ($V_5 \geq 1.4$ V)						
P_O	output power	THD = 10%; R_L = 16 Ω	3	3.5	–	W
		THD = 10%; R_L = 8 Ω	–	5	–	W
THD	total harmonic distortion	P_O = 0.5 W	–	0.3	1	%
G_v	voltage gain		39.5	40.5	41.5	dB
$V_{I(RMS)}$	input signal handling (RMS value)	G_v = 0 dB; THD < 1%	1.0	–	–	V
$V_{no(RMS)}$	noise output voltage (RMS value)	note 2; f = 500 kHz	–	210	–	μV
B	bandwidth	at −1 dB	–	20 Hz to 300 kHz	–	
SVRR	supply voltage ripple rejection	note 3	34	38	–	dB
$\lvert\Delta V_O\rvert$	DC output offset voltage	$\lvert V_8 - v_6\rvert$	–	0	200	mV
Z_I	input impedance pin 3		15	20	25	kΩ
Mute position						
V_O	output voltage in mute position	note 4; V_5 = 0.4 V ±30 mV; V_I = 1.0 V	–	30	40	μV
DC volume control						
ϕ	gain control		68	73.5	–	dB
I_5	control current	V_5 = 0 V	20	25	30	μA

Notes

1. With a load connected to the outputs the quiescent current will increase, the maximum value of this increase being equal to the DC output offset voltage divided by R_L.
2. The noise output voltage (RMS value) at f = 500 kHz is measured with R_S = 0 Ω and bandwidth = 5 kHz.
3. The ripple rejection is measured with R_S = 0 Ω and f = 100 Hz to 10 kHz. The ripple voltage of 200 mV (RMS value) is applied to the positive supply rail.
4. The noise output voltage (RMS value) is measured with R_S = 5 kΩ unweighted.

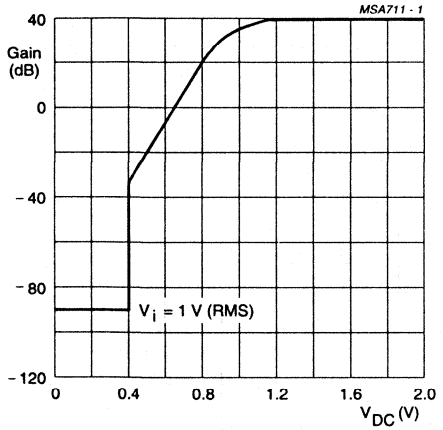
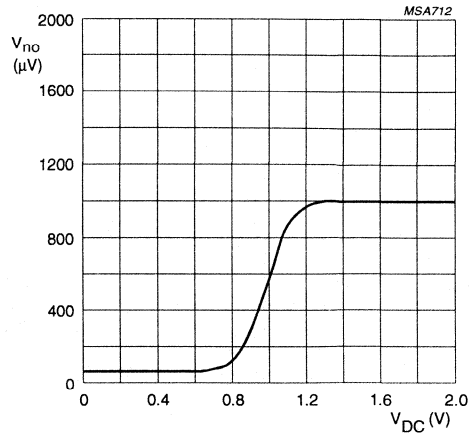


Fig.3 Gain as a function of DC volume control.



The noise output voltage (RMS value) is measured with R_S = 5 kΩ unweighted.

Fig.4 Noise output voltage as a function of DC volume control.

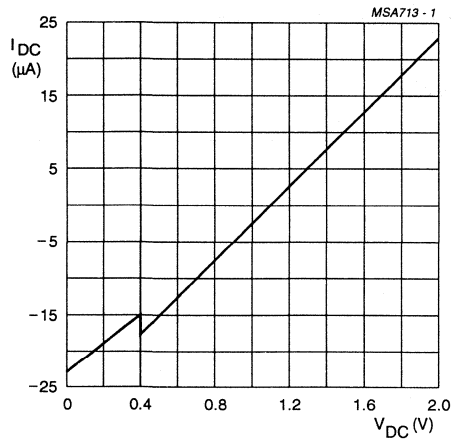
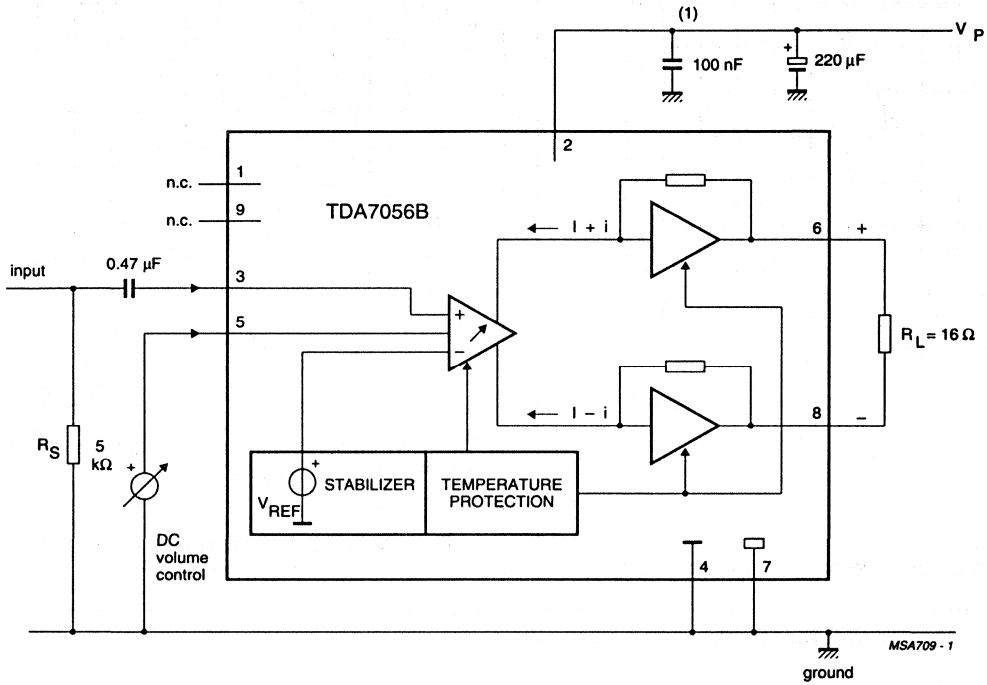


Fig.5 Control current as a function of DC volume control.

TEST AND APPLICATION INFORMATION



(1) This capacitor can be omitted if the 220 µF electrolytic capacitor is connected close to pin 2.

Fig.6 Test and application diagram.

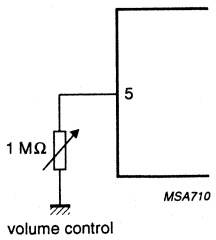


Fig.7 Application using a potentiometer for volume control; G_v = 34 dB.

2 x 5 W stereo BTL audio output amplifier with DC volume control

TDA7057AQ

FEATURES

- DC volume control
- Few external components
- Mute mode
- Thermal protection
- Short-circuit proof
- No switch-on and switch-off clicks
- Good overall stability
- Low power consumption
- Low HF radiation
- ESD protected on all pins.

GENERAL DESCRIPTION

The TDA7057AQ is a stereo BTL output amplifier wih DC volume control in a 13-pin medium power package. The device is designed for use in TV and monitors, but also suitable for battery-fed portable recorders and radios.

Missing Current Limiter (MCL)

A MCL protection circuit is built-in. The MCL circuit is activated when the difference in current between the output terminal of each amplifier exceeds 100 mA (typical 300 mA). This level of 100 mA allows for headphone applications (single-ended).

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	positive supply voltage		4.5	–	18	V
P_O	output power	V_P = 12 V				
	R_L = 16 Ω		3	3.5	–	W
	R_L = 8 Ω		–	5	–	W
G_v	total voltage gain		39.5	40.5	41.5	dB
ϕ	gain control range		68	73.5	–	dB
I_P	total quiescent current	V_P = 12 V; R_L = ∞	–	15	25	mA
THD	total harmonic distortion	P_O = 0.5 W	–	0.3	1	%

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA7057AQ	13	SBD	plastic	SOT141

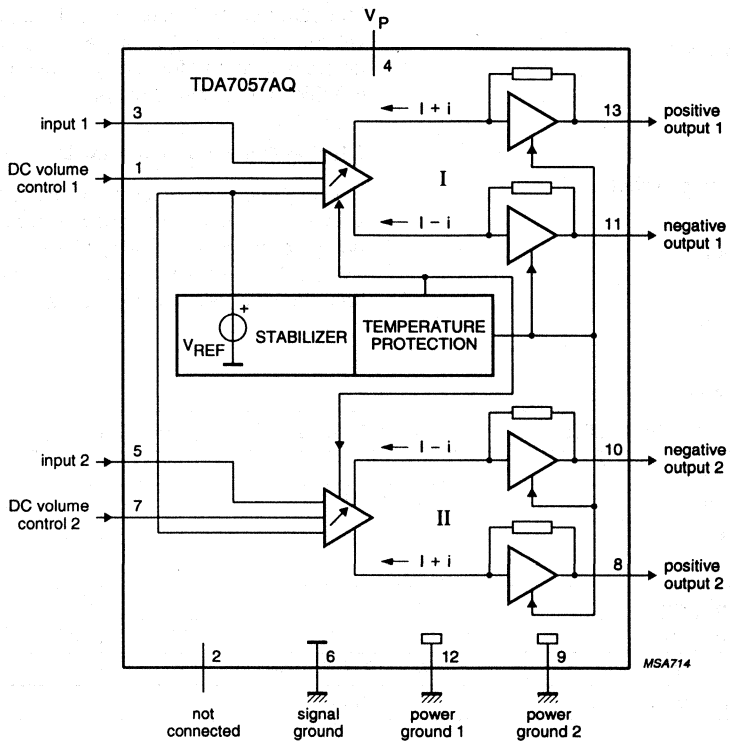


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
VC1	1	DC volume control 1
n.c.	2	not connected
$V_{I(1)}$	3	voltage input 1
V_P	4	positive supply voltage
$V_{I(2)}$	5	voltage input 2
SGND	6	signal ground
VC2	7	DC volume control 2
OUT2+	8	positive output 2
PGND2	9	power ground 2
OUT2–	10	negative output 2
OUT1–	11	negative output 1
PGND1	12	power ground 1
OUT1+	13	positive output 1

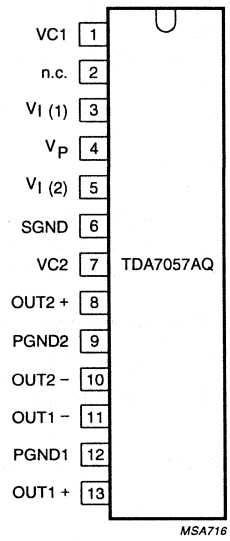


Fig.2 Pin configuration.

2 x 5 W stereo BTL audio output amplifier with DC volume control

TDA7057AQ

FUNCTIONAL DESCRIPTION

The TDA7057AQ is a stereo output amplifier wih two DC volume control stages, designed for TV and monitors, but also suitable for battery-fed portable recorders and radios.
In convential DC volume control circuits the control or input stage is AC coupled to the output stage via external capacitors to keep the offset voltage low.
In the TDA7057AQ the two DC volume control stages are integrated into the input stages so that no coupling capacitors are required and yet a low offset voltage is maintained. Also the minimum supply voltage remains low.
The BTL principle offers the following advantages:

- Lower peak value of the supply current
- The frequency of the ripple on the supply voltage is twice the signal frequency.

Consequently, a reduced power supply with smaller capacitors can be used which results in cost reductions.

For portable applications there is a trend to decrease the supply voltage, resulting in a reduction of output power at conventional output stages. Using the BTL principle increases the output power.

The maximum gain of the amplifier is fixed at 40.5 dB. The DC volume control stages have a logarithmic control characteristic. Therefore, the total gain can be controlled from 40.5 dB to −33 dB.
If the DC volume control voltage falls below 0.4 V, the device will switch to the mute mode.

The amplifier is short-circuit proof to ground, V_P and across the load. Also a thermal protection circuit is implemented. If the crystal temperature rises above +150 °C the gain will be reduced, thereby reducing the output power.
Special attention is given to switch-on and switch-off clicks, low HF radiation and a good overall stability.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_P	positive supply voltage		–	18	V
I_{ORM}	repetitive peak output current		–	1.25	A
I_{OSM}	non-repetitive peak output current		–	1.5	A
P_{tot}	total power dissipation	T_{case} < 60 °C	–	22.5	W
T_{amb}	operating ambient temperature		−40	+85	°C
T_{stg}	storage temperature		−55	+150	°C
T_{vj}	virtual junction temperature		–	+150	°C
T_{sc}	short-circuit time		–	1	hr
V_n	input voltage pins 1, 3, 5 and 7		–	5	V

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}c}$	from junction to case	4 K/W
$R_{th\ j\text{-}a}$	from junction to ambient	40 K/W

Power dissipation

Assume V_P = 12 V; R_L = 16 Ω.
The maximum sinewave dissipation is 2 x 1.8 W = 3.6 W.
At $T_{amb\ (max)}$ = 60 °C;
$R_{th\ tot}$ = (150 − 60)/3.6 = 25 K/W
$R_{th\ tot} = R_{th\ j\text{-}c} + R_{th\ c\text{-}hs} + R_{th\ hs}$
$R_{th\ c\text{-}hs} + R_{th\ hs}$ = 25 − 4 = 21 K/W

CHARACTERISTICS

V_P = 12 V; T_{amb} = 25 °C; f = 1 kHz; R_L = 16 Ω; unless otherwise specified (see Fig.6).

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	positive supply voltage		4.5	–	18	V
I_P	total quiescent current	note 1; V_P = 12 V; R_L = ∞	–	15	25	mA
Maximum gain; $V_{1,7} \geq$ 1.4 V						
P_O	output power	THD = 10%				
	R_L = 16 Ω		3.0	3.5	–	W
	R_L = 8 Ω		–	5	–	W
THD	total harmonic distortion	P_O = 0.5 W	–	0.3	1	%
G_v	voltage gain		39.5	40.5	41.5	dB
$V_{I(RMS)}$	input signal handling (RMS value)	G_v = 0 dB; THD < 1%	1	–	–	V
V_{no}	noise output voltage	note 2; f = 500 kHz;	–	210	–	μV
B	bandwidth	at –1 dB	–	20 Hz to 300 kHz	–	Hz
SVRR	supply voltage ripple rejection	note 3	34	38	–	dB
$\lvert\Delta V_O\rvert$	DC output offset voltage	$\lvert V_{13}-V_{11}\rvert$ and $\lvert V_{10}-V_8\rvert$	–	0	200	mV
Z_I	input impedance (pins 3 and 5)		15	20	25	kΩ
α	channel separation	R_S = 5 kΩ	40	–	–	dB
$\lvert G_v\rvert$	channel unbalance	note 4	–	–	1	dB
$\lvert G_v\rvert$	channel unbalance at G_1 = 0 dB	note 5	–	–	tbf	dB
Mute position						
V_O	output voltage in mute position	note 6; $V_{1,7}$ = 0.4 V ±30 mV; V_I = 1.0 V	–	30	40	μV
DC volume control						
ϕ	gain control		68	73.5	–	dB
I_P	control current	V_1, V_7 = 0 V	20	25	30	μA

Notes

1. With a load connected to the outputs the quiescent current will increase, the maximum value of this increase being equal to the DC output offset voltage divided by R_L.
2. The noise output voltage (RMS value) at f = 500 kHz is measured with R_S = 0 Ω and bandwidth = 5 kHz.
3. The ripple rejection is measured with R_S = 0 Ω and f = 100 Hz to 10 kHz. The ripple voltage of 200 mV (RMS value) is applied to the positive supply rail.
4. The channel unbalance is measured with $V_{DC1} = V_{DC2}$.
5. The channel unbalance at G_1 = 0 dB is measured with $V_{DC1} = V_{DC2}$.
6. The noise output voltage (RMS value) is measured with R_S = 5 kΩ unweighted.

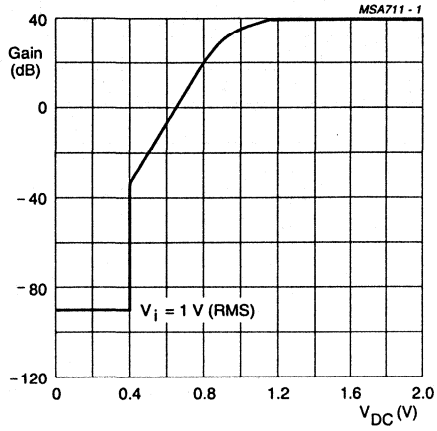
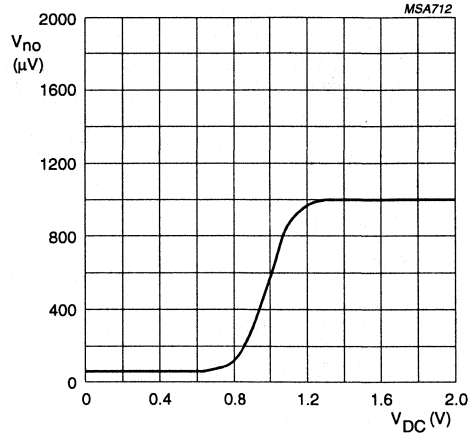


Fig.3 Gain control as a function of DC volume control.



The noise output voltage (RMS value) is measured with R_S = 5 kΩ unweighted.

Fig.4 Noise output voltage as a function of DC volume control.

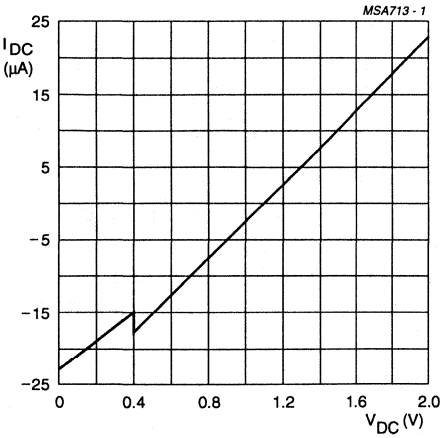
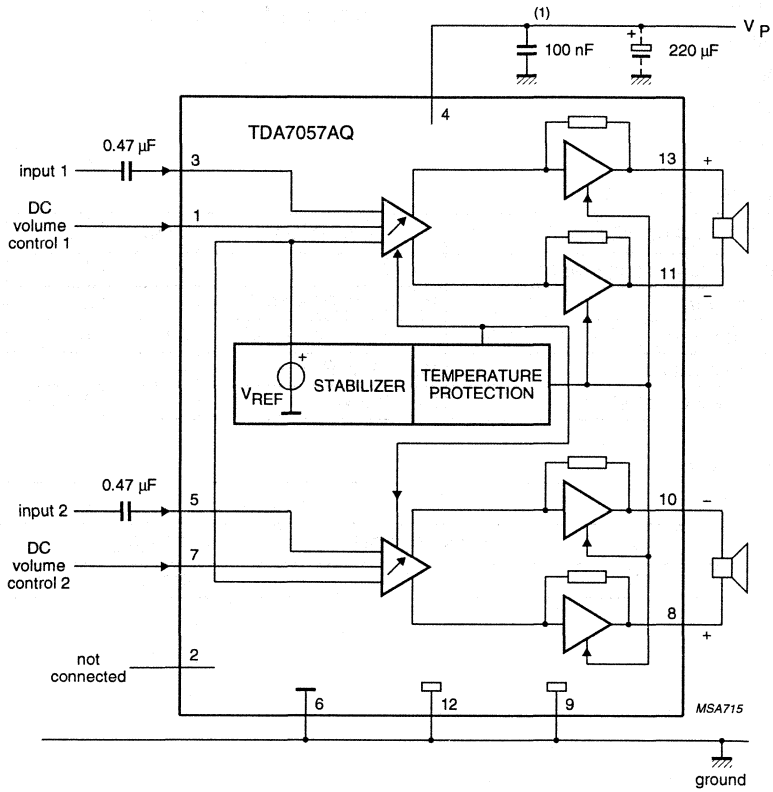


Fig.5 Control current as a function of DC volume control.

APPLICATION INFORMATION



(1) This capacitor can be omitted if the 220 µF electrolytic capacitor is connected close to pin 4.

Fig.6 Test and application diagram.

2 x 3 W stereo BTL audio output amplifier

TDA7057Q

FEATURES

- No external components
- No switch-on and off clicks
- Good overall stability
- Low power consumption
- Short-circuit proof
- Low HF radiation
- ESD protected on all pins.

GENERAL DESCRIPTION

The TDA7057Q is a stereo output amplifier in a 13 pin power package. The device is designed for battery-fed portable stereo recorders and radios, but also suitable for mains-fed applications.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	positive supply voltage range		3.0	11	18	V
P_O	output power	V_P = 11 V; R_L = 16 Ω	–	3	–	W
G_v	voltage gain		39	40	41	dB
I_P	total quiescent current	V_P = 11 V; R_L = ∞	–	10	14	mA
THD	total harmonic distortion	P_O = 0.5 W	–	0.25	1	%

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA7057Q	13	SBD	plastic	SOT141

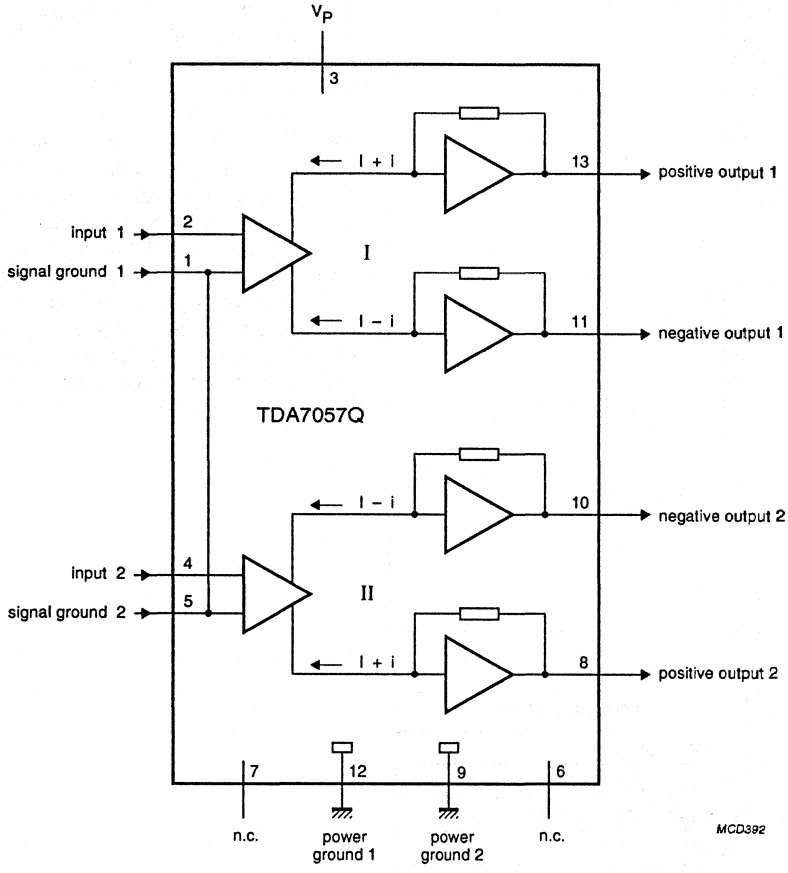


Fig.1 Block diagram.

2 x 3 W stereo BTL audio output amplifier

TDA7057Q

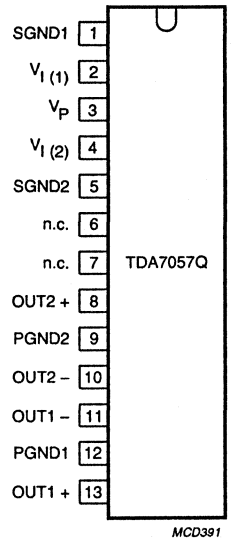


Fig.2 Pin configuration.

PINNING

SYMBOL	PIN	DESCRIPTION
SGND1	1	signal ground 1
$V_{I(1)}$	2	voltage input 1
V_P	3	positive supply voltage
$V_{I(2)}$	4	voltage input 2
SGND2	5	signal ground 2
n.c.	6	not connected
n.c.	7	not connected
OUT2+	8	positive output 2
PGND2	9	power ground 2
OUT2–	10	negative output 2
OUT1–	11	negative output 1
PGND1	12	power ground 1
OUT1+	13	positive output 1

FUNCTIONAL DESCRIPTION

The TDA7057Q is a stereo output amplifier, designed for battery-fed applications e.g. portable radios, but also suitable for mains fed applications. The gain is internally fixed at 40 dB.

For space reason there is a trend to decrease the number of battery cells. This means a decrease in supply voltage, resulting in a reduction of output power at conventional output stages. The latter is not preferred. Using the BTL principle increases the output power.

The TDA7057Q can deliver an output power of 3 W in a speaker load of 16 Ω with 11 V supply.

The circuit is designed such that no external components are required. Special attention is given to switch-on and off clicks, low HF radiation and a good overall stability. The load can be short-circuited at all input conditions.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_P	positive supply voltage range		–	18	V
I_{ORM}	repetitive peak output current		–	1	A
I_{OSM}	non repetitive peak output current		–	1.5	A
P_{tot}	total power dissipation	$T_{case} < 60$ °C	–	9	W
T_{stg}	storage temperature range		–55	+150	°C
T_{vj}	virtual junction temperature		–	+150	°C
T_{sc}	short-circuit time	see note	–	1	hr

Note to the limiting values

The load can be short-circuited at all input conditions.

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient in free air	45 K/W
$R_{th\ j\text{-}c}$	from junction to case	8 K/W

Note to the thermal resistance

$V_P = 11$ V; $R_L = 16\ \Omega$; The maximum sine-wave dissipation is = 3 W; $T_{amb\ (max)} = 60$ °C; $R_{th\ vj\text{-}a} = (150 - 60)/3 = 30$ K/W

$R_{th\ vj\text{-}a} = R_{th\ vj\text{-}c} + R_{th\ c\text{-}HS} + R_{th\ HS}$

$R_{th\ c\text{-}HS} + R_{th\ HS} = 30 - 8 = 22$ K/W

CHARACTERISTICS

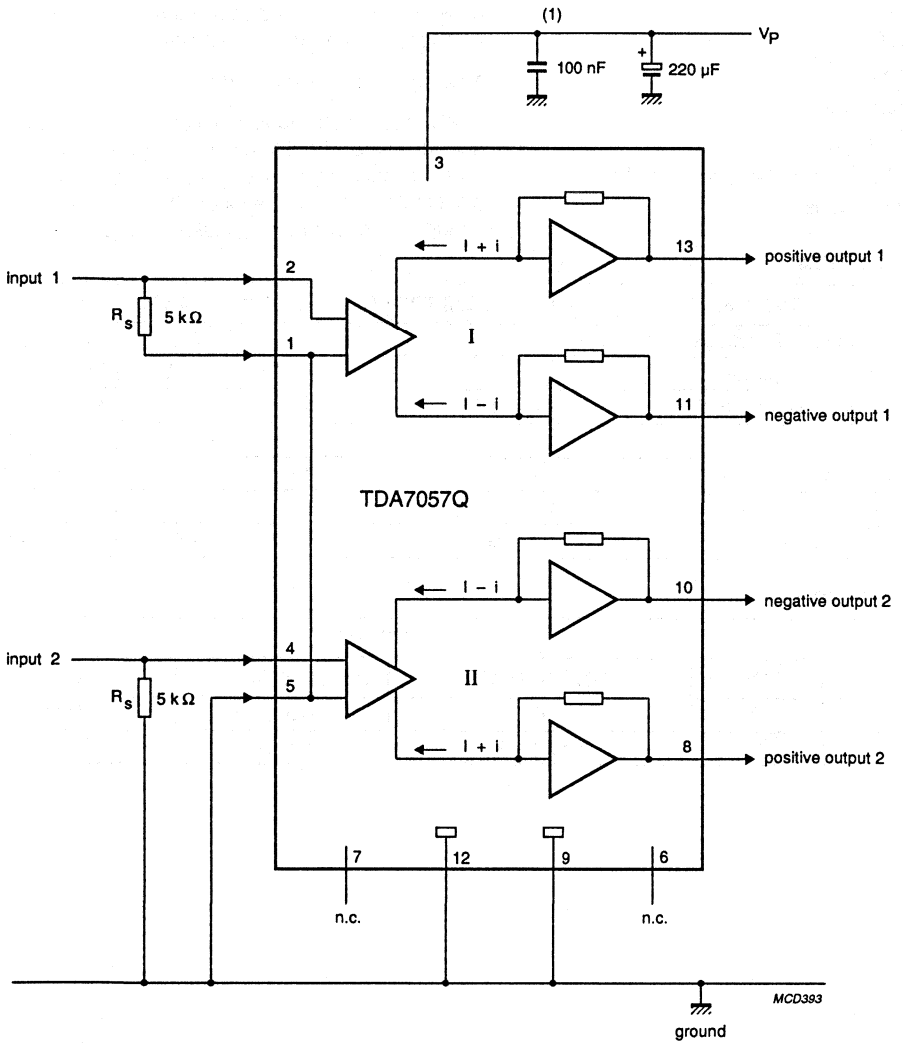
V_P = 11 V; f = 1 kHz; R_L = 16 Ω; T_{amb} = 25 °C; unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	positive supply voltage range		3.0	11	18	V
I_{ORM}	repetitive peak output current		–	–	0.6	A
Operating position						
I_P	total quiescent current	R_L = ∞; note 1	–	10	14	mA
P_O	output power	THD = 10%	2.5	3	–	W
THD	total harmonic distortion	P_O = 0.5 W	–	0.25	1	%
G_v	voltage gain		39	40	41	dB
$V_{no(rms)}$	noise output voltage (RMS value)	note 2	–	180	300	μV
$V_{no(rms)}$	noise output voltage (RMS value)	note 3	–	60	–	μV
B	bandwidth		–	20 Hz to 20 kHz	–	
SVRR	supply voltage ripple rejection	note 4	36	60	–	dB
$\lvert V_{off}\rvert$	DC output offset voltage	R_S = 5 kΩ	–	–	200	mV
Z_I	input impedance		–	100	–	kΩ
I_{bias}	input bias current		–	100	300	nA
α	channel separation	R_S = 5 kΩ	40	–	–	dB
$\lvert G_v\rvert$	channel balance		–	–	1	dB

Notes to the characteristics

1. With a load connected to the outputs the quiescent current will increase, the maximum value of this increase being equal to the DC output offset voltage divided by R_L.
2. The noise output voltage (RMS value) is measured with R_S = 5 kΩ unweighted (20 Hz to 20 kHz).
3. The noise output voltage RMS value) at f = 500 kHz is measured with R_S = 0 Ω and bandwidth = 5 kHz.
   With a practical load (R_L = 16 Ω, L = 200 μH) the noise output current is only 50 nA.
4. The ripple rejection is measured with R_S = 0 Ω and f = 100 Hz to 10 kHz.
   The ripple voltage of 200 mV (RMS value) is applied to the positive supply rail.

APPLICATION INFORMATION



(1) This capacitor can be omitted if the 220 µF electrolytic capacitor is connected close to pin 3.

Fig.3 Test and application diagram.

Single BTL power driver TDA7072A/AT

FEATURES

- No external components
- Very high slew rate
- Single power supply
- Short-circuit proof
- High output current (0.6 A)
- Wide supply voltage range
- Low output offset voltage
- Suited for handling PWM signals up to 176 kHz
- ESD protected on all pins

GENERAL DESCRIPTION

The TDA7072A/AT are single power driver circuits in a BTL configuration, intended for use as a power driver for servo systems with a single supply. They are specially designed for compact disc players and are capable of driving focus, tracking, sled functions and spindle motors.

Missing Current Limiter (MCL)

A MCL protection circuit is built-in. The MCL circuit is activated when the difference in current between the output terminal of each amplifier exceeds 100 mA (typical 300 mA). This level of 100 mA allows for headphone applications (single-ended).

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	positive supply voltage range		3.0	5.0	18	V
G_v	internal voltage gain		32.5	33.5	34.5	dB
I_P	total quiescent current	$V_P = 5$ V; $R_L = \infty$	–	4	8	mA
SR	slew rate		–	12	–	V/µs
I_O	output current		–	–	0.6	A
I_{bias}	input bias current		–	100	300	nA
f_{co}	cut-off frequency	–3 dB	–	1.5	–	MHz

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA7072A	8	DIL	plastic	SOT97
TDA7072AT	8	mini-pack	plastic	SOT96A

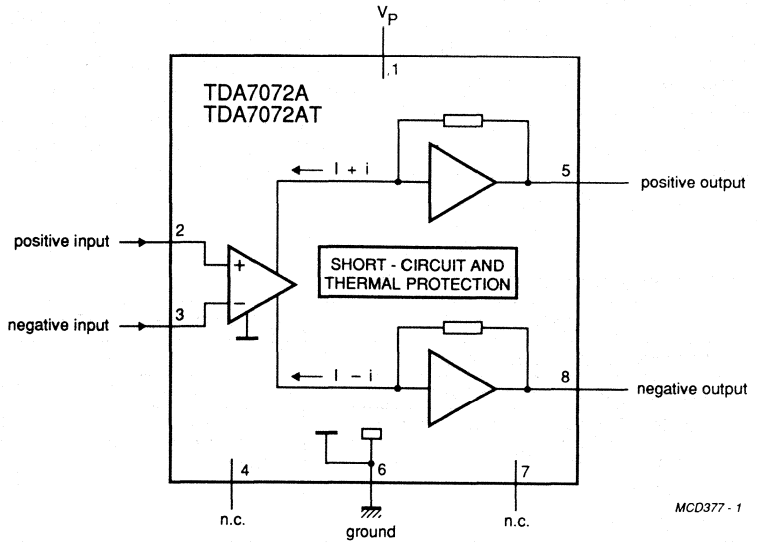


Fig.1 Block diagram.

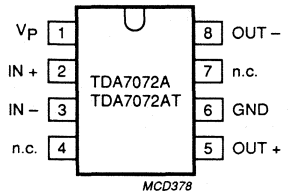


Fig.2 Pin configuration.

PINNING

SYMBOL	PIN	DESCRIPTION
V_P	1	positive supply voltage
IN+	2	positive input
IN–	3	negative input
n.c.	4	not connected
OUT+	5	positive output
GND	6	ground
n.c.	7	not connected
OUT–	8	negative output

FUNCTIONAL DESCRIPTION

The TDA7072A/AT are single power driver circuits in a BTL configuration, intended for use as a power driver for servo systems with a single supply. They are particular designed for compact disc players and are capable of driving focus, tracking, sled functions and spindle motors.

Because of the BTL configuration, the devices can supply a bi-directional DC current in the load, with only a single supply voltage. The voltage gain is fixed by internal feedback at 33.5 dB and the devices operate in a wide supply voltage range (3 to 18 V). The devices can supply a maximum output current of 0.6 A. The outputs can be short-circuited over the load, to the supply and to ground at all input conditions. The differential inputs can handle common mode input voltages from ground level up to (V_P –2.2 V). The devices have a very high slew rate. Due to the large bandwidth, they can handle PWM signals up to 176 kHz.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_P	positive supply voltage range		–	18	V
I_{ORM}	repetitive peak output current		–	1	A
I_{OSM}	non repetitive peak output current		–	1.5	A
P_{tot}	total power dissipation	T_{amb} < 25 °C			
	TDA7072A		–	1.25	W
	TDA7072AT		–	0.54	W
T_{stg}	storage temperature range		–55	+150	°C
T_{vj}	virtual junction temperature		–	+150	°C
T_{sc}	short-circuit time	see note	–	1	hr

Note to the limiting values

The outputs can be short-circuited over the load, to the supply and to ground at all input conditions.

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient in free air	
	TDA7072A	100 K/W
	TDA7072AT	155 K/W

note to the thermal resistance

TDA7072A: V_P = 5 V; R_L = 8 Ω; The typical voltage swing = 5.8 V and V_{loss} is 2.1 V therefore I_O = 0.36 A and P_{tot} = 0.76 W; $T_{amb\ (max)}$ = 150 – 0.76 x 100 = 74 °C
TDA7072AT: V_P = 5 V; R_L = 16 typical voltage swing = 5.8 V and V_{loss} is 2.1 V therefore I_O = 0.18 A and P_{tot} = 0.38 W; $T_{amb\ (max)}$ = 150 – 0.38 x 155 = 91 °C

CHARACTERISTICS

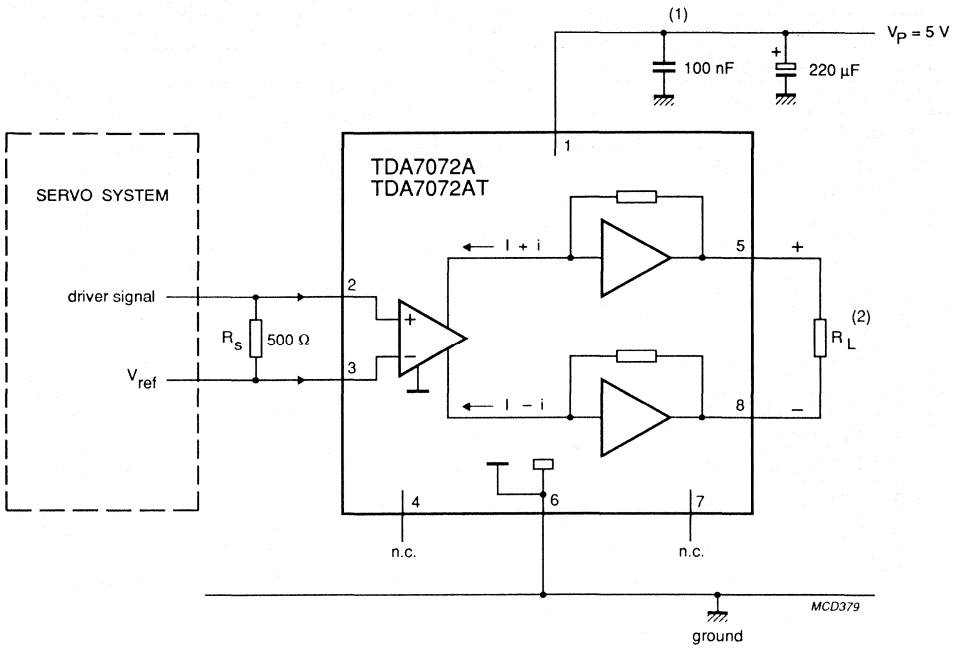
V_P = 5 V; f = 1 kHz; T_{amb} = 25 °C; unless otherwise specified (see Fig.3]). TDA7072A: R_L = 8 Ω; TDA7072AT: R_L = 16 Ω.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	positive supply voltage range		3.0	5.0	18	V
I_{ORM}	repetitive peak output current		–	–	0.6	A
I_P	total quiescent current	R_L = ∞; note 1	–	4	8	mA
ΔV_{OUT}	output voltage swing	note 2	5.2	5.8	–	V
THD	total harmonic distortion	V_{OUT} = 1 V (RMS)				
	TDA7072A		–	0.3	–	%
	TDA7072AT		–	0.1	–	%
G_v	voltage gain		32.5	33.5	34.5	dB
$V_{no(rms)}$	noise output voltage (RMS value)	note 3	–	75	150	μV
B	bandwidth		–	–	1.5	MHz
SVRR	supply voltage ripple rejection	note 4	40	55	–	dB
$\lvert\Delta V_{5-8}\rvert$	DC output offset voltage	R_S = 500 Ω	–	–	100	mV
$V_{I(CM)}$	DC common mode voltage range	note 5	0	–	2.8	V
CMRR	DC common mode rejection ratio	note 6	–	100	–	dB
Z_I	input impedance		–	100	–	kΩ
I_{bias}	input bias current		–	100	300	nA
SR	slew rate		–	12	–	V/μs

Notes to the characteristics

1. With a load connected to the outputs the quiescent current will increase, the maximum value of this increase being equal to the DC output offset voltage divided by R_L.
2. The output voltage swing is typically limited to 2 x (V_P –2.1 V) (see Fig.4).
3. The noise output voltage (RMS value), unweighted (20 Hz to 20 kHz) is measured with R_S = 500 Ω.
4. The ripple rejection is measured with R_S = 0 Ω and f = 100 Hz to 10 kHz. The ripple voltage of 200 mV (RMS value) is applied to the positive supply rail.
5. The DC common mode voltage range is limited to (V_P –2.2 V).
6. The common mode rejection ratio is measured at V_{ref} = 1.4 V, $V_{I(CM)}$ = 200 mV and f = 1 kHz.

APPLICATION INFORMATION



(1) This capacitor can be omitted if the 220 µF electrolytic capacitor is connected close to pin 1.

(2) R_L can be: focus, tracking, sled function or spindle motor.

Fig.3 Test and application diagram.

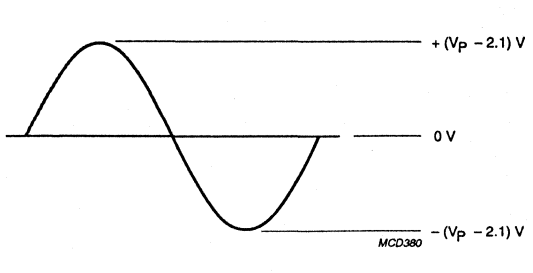


Fig.4 Typical output voltage swing over R_L.

Dual BTL power driver TDA7073A/AT

FEATURES

- No external components
- Very high slew rate
- Single power supply
- Short-circuit proof
- High output current (0.6 A)
- Wide supply voltage range
- Low output offset voltage
- Suited for handling PWM signals up to 176 kHz
- ESD protected on all pins

GENERAL DESCRIPTION

The TDA7073A/AT are dual power driver circuits in a BTL configuration, intended for use as a power driver for servo systems with a single supply. They are specially designed for compact disc players and are capable of driving focus, tracking, sled functions and spindle motors.

Missing Current Limiter (MCL)

A MCL protection circuit is built-in. The MCL circuit is activated when the difference in current between the output terminal of each amplifier exceeds 100 mA (typical 300 mA). This level of 100 mA allows for headphone applications (single-ended).

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	positive supply voltage range		3.0	5.0	18	V
G_v	internal voltage gain		32.5	33.5	34.5	dB
I_P	total quiescent current	V_P = 5 V; R_L = ∞	–	8	16	mA
SR	slew rate		–	12	–	V/µs
I_O	output current		–	–	0.6	A
I_{bias}	input bias current		–	100	300	nA
f_{co}	cut-off frequency	–3 dB	–	1.5	–	MHz

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA7073A	16	DIL	plastic	SOT38
TDA7073AT	16	mini-pack	plastic	SOT162A

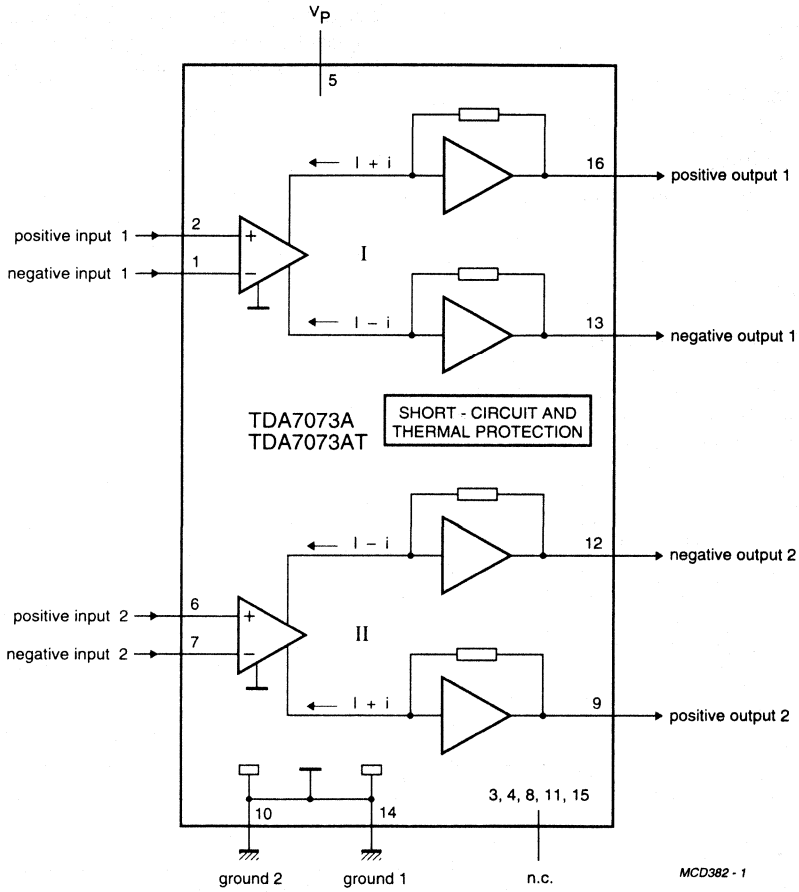


Fig.1 Block diagram.

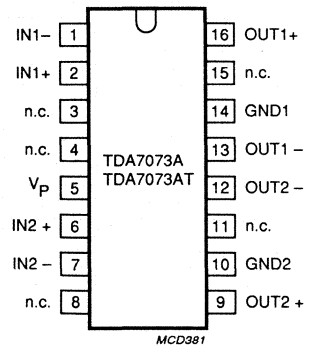


Fig.2 Pin configuration.

PINNING

SYMBOL	PIN	DESCRIPTION
IN1–	1	negative input 1
IN1+	2	positive input 1
n.c.	3	not connected
n.c.	4	not connected
V_P	5	positive supply voltage
IN2+	6	positive input 2
IN2–	7	negative input 2
n.c.	8	not connected
OUT2+	9	positive output 2
GND2	10	ground 2
n.c.	11	not connected
OUT2–	12	negative output 2
OUT1–	13	negative output 1
GND1	14	ground 1
n.c.	15	not connected
OUT1+	16	positive output 1

FUNCTIONAL DESCRIPTION

The TDA7073A/AT are dual power driver circuits in a BTL configuration, intended for use as a power driver for servo systems with a single supply. They are particular designed for compact disc players and are capable of driving focus, tracking, sled functions and spindle motors.

Because of the BTL configuration, the devices can supply a bi-directional DC current in the load, with only a single supply voltage. The voltage gain is fixed by internal feedback at 33.5 dB and the devices operate in a wide supply voltage range (3 to 18 V). The devices can supply a maximum output current of 0.6 A. The outputs can be short-circuited over the load, to the supply and to ground at all input conditions. The differential inputs can handle common mode input voltages from ground level up to (V_P –2.2 V with a maximum of 10 V). The devices have a very high slew rate. Due to the large bandwidth, they can handle PWM signals up to 176 kHz.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_P	positive supply voltage range		–	18	V
I_{ORM}	repetitive peak output current		–	1	A
I_{OSM}	non repetitive peak output current		–	1.5	A
P_{tot}	total power dissipation	T_{amb} < 25 °C			
	TDA7073A		–	2.5	W
	TDA7073AT		–	1.32	W
T_{stg}	storage temperature range		–55	+150	°C
T_{vj}	virtual junction temperature		–	+150	°C
T_{sc}	short-circuit time	see note	–	1	hr

Note to the limiting values

The outputs can be short-circuited over the load, to the supply and to ground at all input conditions.

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient in free air	
	TDA7073A	50 K/W
	TDA7073AT	95 K/W

Note to the thermal resistance

TDA7073A: V_P = 5 V; R_L = 8 Ω; The typical voltage swing = 5.8 V and V_{loss} is 2.1 V therefore I_O = 0.36 A and P_{tot} = 2 x 0.76 W = 1.52 W; $T_{amb\ (max)}$ = 150 – 1.52 x 50 = 74 °C
TDA7073AT: V_P = 5 V; R_L = 16 Ω; typical voltage swing = 5.8 V and V_{loss} is 2.1 V therefore I_O = 0.18 A and P_{tot} = 2 x 0.38 W = 0.76 W; $T_{amb\ (max)}$ = 150 – 0.76 x 95 = 77 °C

CHARACTERISTICS

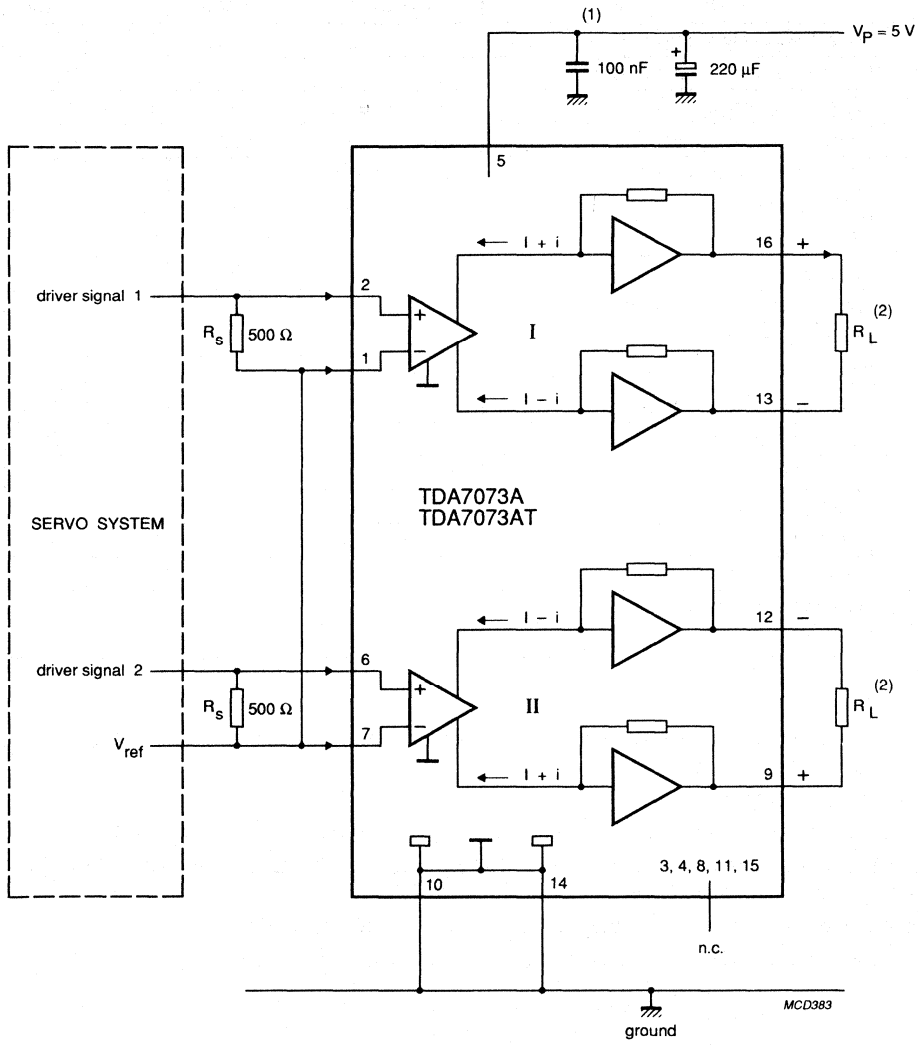
V_P = 5 V; f = 1 kHz; T_{amb} = 25 °C; unless otherwise specified (see Fig.3]).
TDA7073A: R_L = 8 Ω; TDA7073AT: R_L = 16 Ω.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	positive supply voltage range		3.0	5.0	18	V
I_{ORM}	repetitive peak output current		–	–	0.6	A
I_P	total quiescent current	$R_L = \infty$; note 1	–	8	16	mA
ΔV_{OUT}	output voltage swing	note 2	5.2	5.8	–	V
THD	total harmonic distortion	V_{OUT} = 1 V (RMS)				
	TDA7073A		–	0.3	–	%
	TDA7073AT		–	0.1	–	%
G_v	voltage gain		32.5	33.5	34.5	dB
$V_{no(rms)}$	noise output voltage (RMS value)	note 3	–	75	150	μV
B	bandwidth		–	–	1.5	MHz
SVRR	supply voltage ripple rejection	note 4	40	55	–	dB
$\lvert\Delta V_{16\text{-}13,\ 12\text{-}9}\rvert$	DC output offset voltage	R_S = 500 Ω	–	–	100	mV
$V_{I(CM)}$	DC common mode voltage range	note 5	0	–	2.8	V
CMRR	DC common mode rejection ratio	note 6	–	100	–	dB
Z_I	input impedance		–	100	–	kΩ
I_{bias}	input bias current		–	100	300	nA
α	channel separation		40	50	–	dB
$\lvert\Delta G V\rvert$	channel unbalance		–	–	1	dB
SR	slew rate		–	12	–	V/μs

Notes to the characteristics

1. With a load connected to the outputs the quiescent current will increase, the maximum value of this increase being equal to the DC output offset voltage divided by R_L
2. The output voltage swing is typically limited to 2 x (V_P –2.1 V) (see Fig.4)
3. The noise output voltage (RMS value), unweighted (20 Hz to 20 kHz) is measured with R_S = 500 Ω
4. The ripple rejection is measured with R_S = 0 Ω and f = 100 Hz to 10 kHz. The ripple voltage of 200 mV (RMS value) is applied to the positive supply rail
5. The DC common mode voltage range is limited to (V_P –2.2 V with a maximum of 10 V).
6. The common mode rejection ratio is measured at V_{ref} = 1.4 V, $V_{I(CM)}$ = 200 mV and f = 1 kHz

APPLICATION INFORMATION



(1) This capacitor can be omitted if the 220 µF electrolytic capacitor is connected close to pin 5.

(2) R_L can be: focus, tracking, sled function or spindle motor.

Fig.3 Test and application diagram.

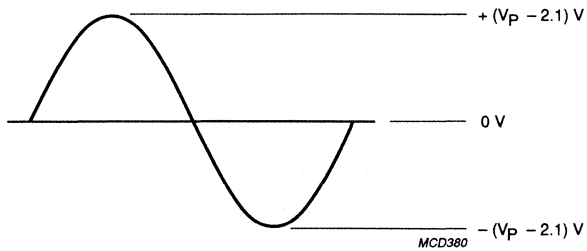


Fig.4 Typical output voltage swing over R_L.

Philips Semiconductors

Data sheet	
status	Preliminary specification
date of issue	January 1991

TDA7088T
FM receiver circuit for battery supply

FEATURES

- Provided with all stages of a mono receiver from antenna to audio output
- Mute circuit
- Search tuning applicable with a single varicap diode
- Mechanical tuning with integrating AFC applicable
- AM application supported
- Power supply polarity protection
- Power supply voltage down to 1.8 V

GENERAL DESCRIPTION

The TDA7088T is a monolithic bipolar integrated circuit for mono portable and pocket radios, wherein a minimum of peripheral components (of small dimensions and low costs) are needed. The circuit is performed with a FLL system (frequency locked loop) and has an FM-IF of about 70 kHz. Selectivity is obtained by active RC-filters. Detuning referred to the IF and too weak input signals is suppressed by muting.

The circuit is applicable for mechanical as well as for electrical tuned radios. Whereas mechanical tuning is possible with or without integrating AFC circuit; electrical tuning is realized by one directional (band-up) search tuning facility, including RESET to the lower band limit.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage (pin 4)	1.8	3	5	V
I_P	supply current	4.2	5.2	6.6	mA
f_{iRF}	radio input frequency range	0.5	-	110	MHz
$V_{i\ (rms)}$	input sensitivity for –3 dB limiting (RMS value, mute disable)	- -	 3	 6	 µV
	signal handling	100	200	-	mV
$V_{o\ (rms)}$	AF output signal (R_L = 22 kΩ)	-	85	-	mV
T_{amb}	operating ambient temperature	–10	-	+70	°C

ORDERING AND PACKAGE INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA7088T	16	mini-pack	plastic	SOT109A

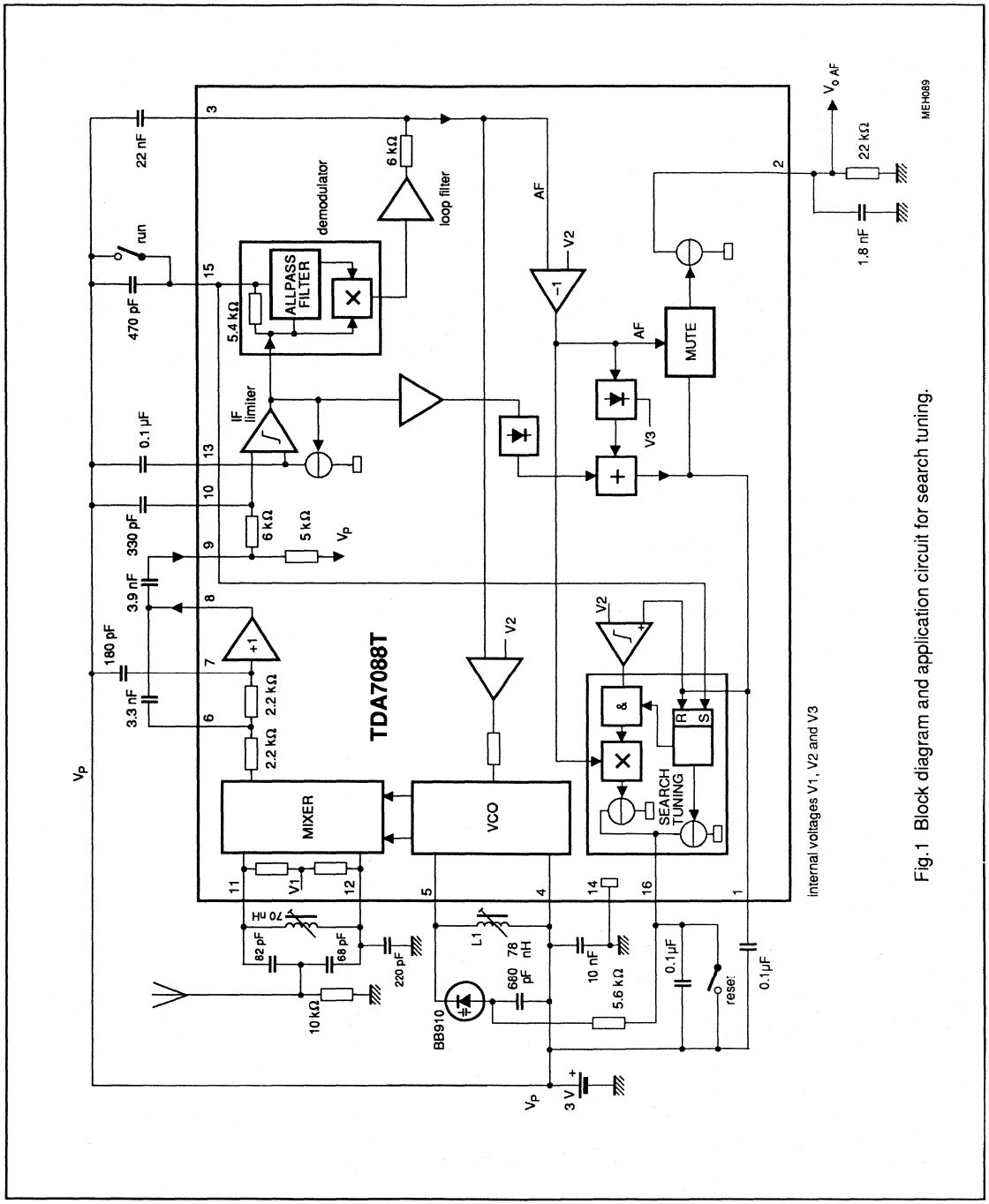


Fig.1 Block diagram and application circuit for search tuning.

PINNING

SYMBOL	PIN	DESCRIPTION
MUTE	1	mute output
V_{oAF}	2	audio frequency output signal
LOOP	3	AF loop filter
V_P	4	+3 V supply voltage
OSC	5	oscillator resonant circuit
IFFB	6	IF feedback
C_{LP1}	7	low-pass capacitor of 1 dB amplifier
V_{oIF}	8	IF output to external coupling capacitor (high-pass)
V_{iIF}	9	IF input to limiter amplifier
C_{LP2}	10	low-pass capacitor of IF limitter amplifier
V_{iRF}	11	radio frequency input
V_{iRF}	12	radio frequency input
C_{LIM}	13	limiter offset voltage capacitor
GND	14	ground (0 V)
C_{AP}	15	all-pass filter capacitor / input for search tuning
TUNE	16	electrical tuning respectively AFC output

PIN CONFIGURATION

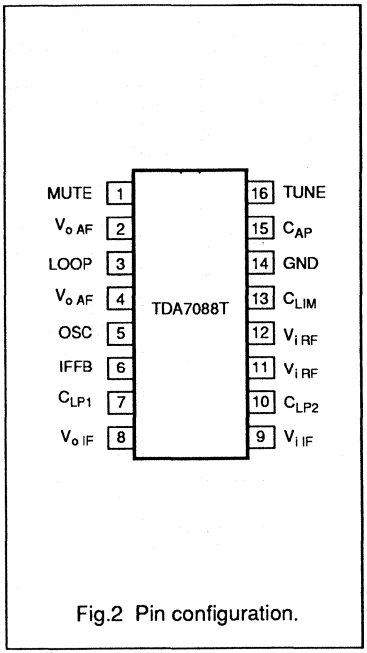


Fig.2 Pin configuration.

LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_P	supply voltage (pin 4)	0	5	V
T_{stg}	storage temperature range	–55	150	°C
T_{amb}	operating ambient temperature range	–10	+70	°C
V_{ESD}	electrostatic handling*		-	

* There is no special ESD protection circuit built in; ESD data on request.

DC CHARACTERISTICS

V_P = 3 V and T_{amb} = 25 °C, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage range (pin 4)		1.8	3	5	V
I_P	supply current		4.2	5.2	6.6	mA
V_1	DC voltage		2.50	2.55	2.60	V
V_3	DC voltage		2.64	2.69	2.74	V
$V_{6,7}$	DC voltage		2.38	2.44	2.50	V
V_8	DC voltage		1.60	1.67	1.74	V
$V_{9,10,13}$	DC voltage		2.42	2.47	2.52	V
$V_{11,12}$	DC voltage		0.91	0.94	0.98	V
V_{15}	DC voltage		2.06	2.12	2.18	V
V_{16}	DC voltage		t.b.n.	-	-	V
I_2	AF output current		45	60	80	µA
I_5	oscillator current		275	375	500	µA

AC CHARACTERISTICS

V_P = 3 V; T_{amb} = 25 °C ; f_{iRF} = 96 MHz modulated with f_{mod} = 1 kHz and ±22.5 kHz deviation; EMF = 400 µV (R_S = 75 Ω) and measurements taken in Fig.3, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{i\,RF}$	input sensivity at –3 dB before limiting					
	(RMS value, pins 11–12, Fig.4)	mute-off	-	3	6	µV
	input sensivity	–3 dB muting	3	6	12	µV
		S/N = 26 dB	-	5	10	µV
	signal handling (RMS value, pins 11–12)	Δf = ±75 kHz; THD < 10%	100	200	-	mV
S/N	signal-to-noise ratio	Fig.4	52	56	-	dB
THD	total harmonic distortion	Δf = ±22.5 kHz	-	1	1.4	%
		Δf = ±75 kHz	-	2.4	3.3	%
α_{AM}	AM suppression:	FM: 1 kHz; ±75 kHz				
		AM: 1 kHz; m = 0.8	47	52	-	dB
RR_{1000}	ripple rejection, measurements taken with 100 mV (RMS) ripple on V_P	f = 1 kHz	7	10	-	dB
V_o	audio output signal (RMS value, pin 2)	R_L = 22 kΩ	60	85	120	mV

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Search tuning with BB910 (Fig.1)		C_{16} = 0.1 µF				
V_{16}	minimum output voltage	limiting point	-	V_P–1.85	-	V
$\Delta V/\Delta t$	tuning steepness	voltage pin 16	95	210	420	mV/s
$\Delta f_{osc}/\Delta t$	oscillator steepness		1.25	2.83	5.6	MHz/s
$\Delta I_{AFC}/\Delta V_3$	AFC steepness	voltage pin 3	4.75	9.5	19	µA/V

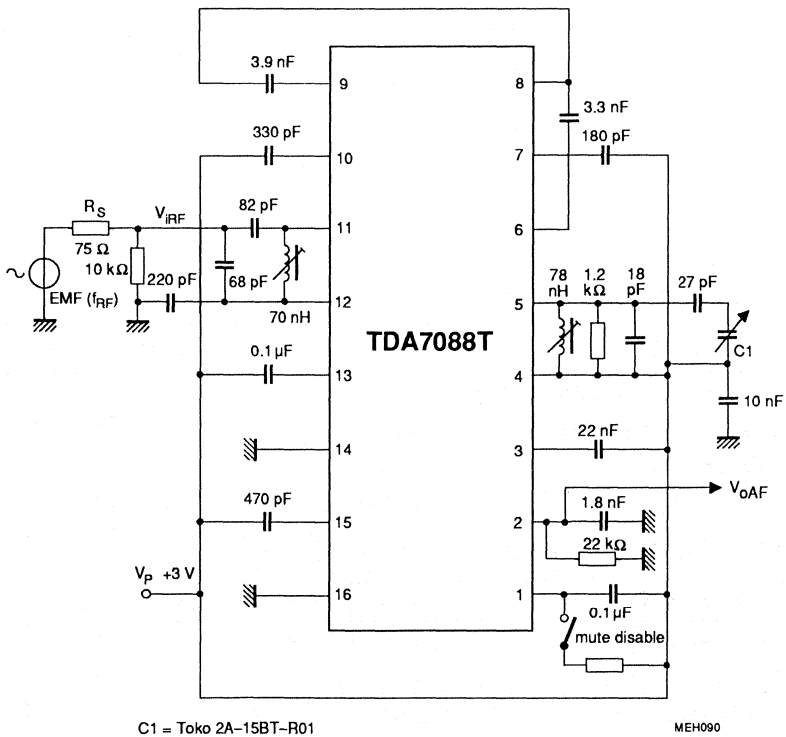


Fig.3 Test circuit and application for mechanical tuning.

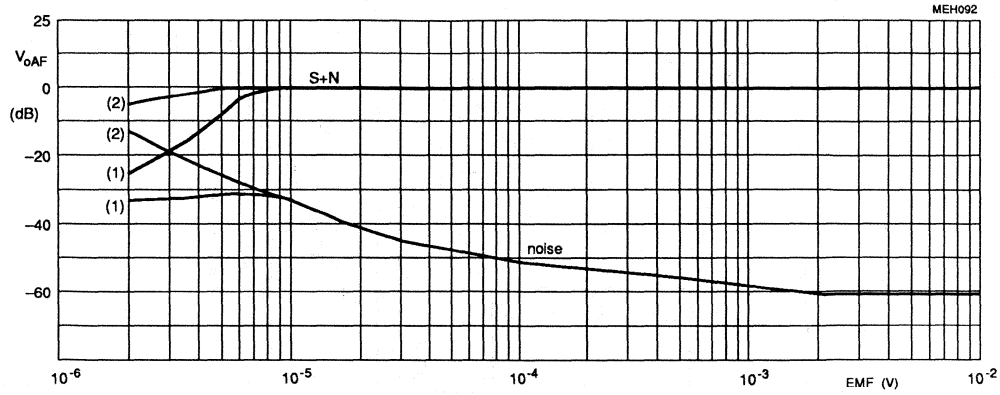


Fig.4 Input sensitivity: (1) mute-on; (2) mute-off.

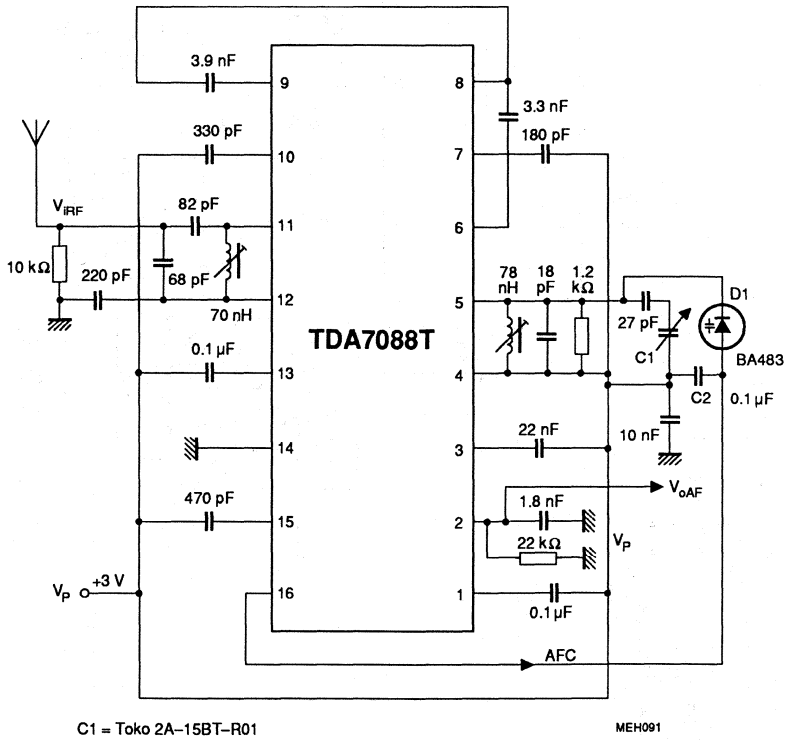


Fig.5 Application circuit with AFC for mechanical tuning.

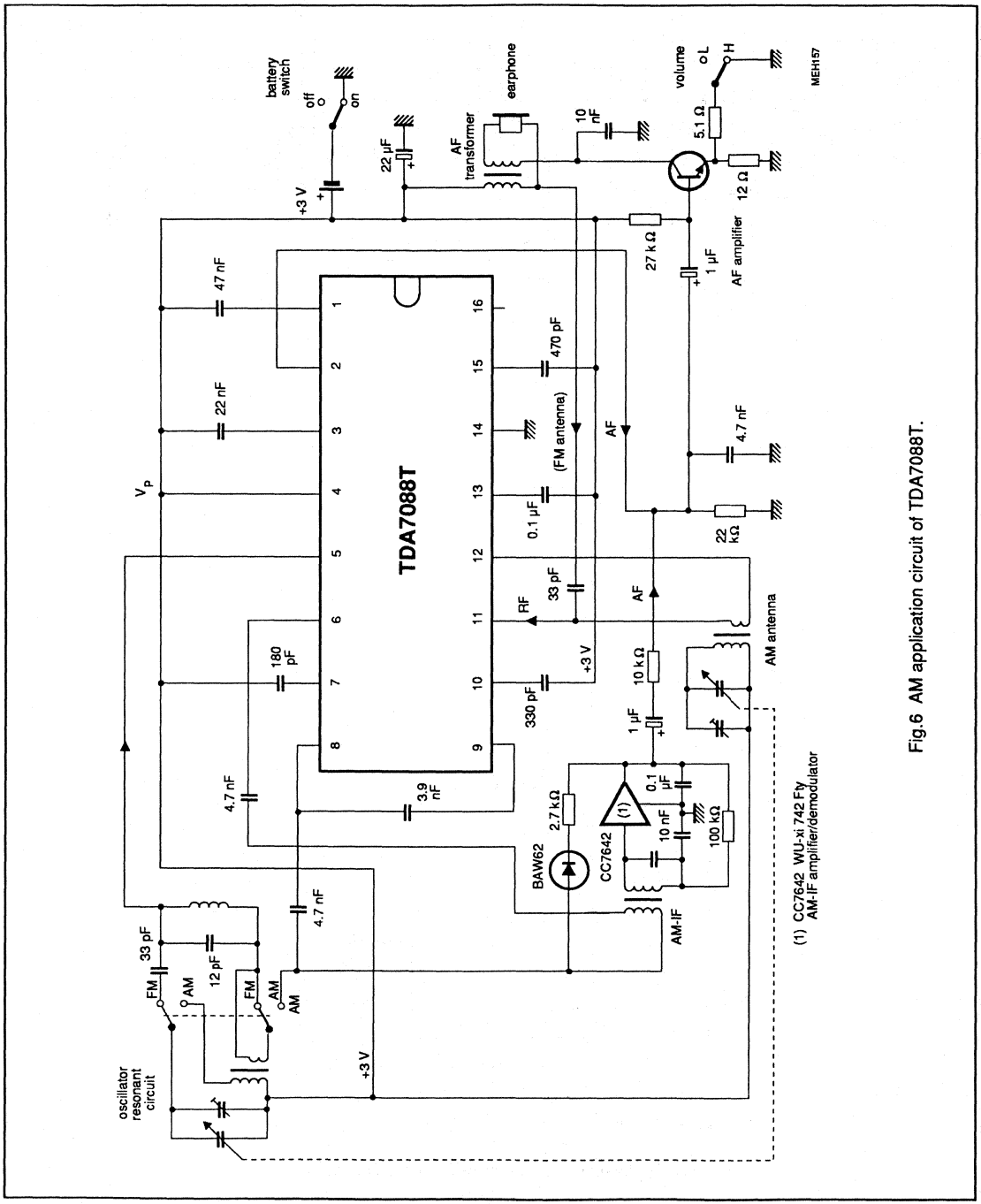


Fig.6 AM application circuit of TDA7088T.

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC02 OR DATASHEET

I²C-BUS INTERFACE FOR COLOUR DECODERS

GENERAL DESCRIPTION

The TDA8442 provides control of four analogue functions and has one high-current and two switching outputs. Control of the IC is performed via the two-line, bidirectional I²C-bus.

Features

- Four analogue control outputs
- One high-current output port (npn open emitter)
- Two switching output ports (npn collector with internal pull-up resistor)
- I²C-bus slave receiver
- Power-down reset

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage (pin 9)		V_P	10.8	12.0	13.2	V
Supply current	no outputs loaded	I_P	8	13	18	mA
Total power dissipation	no outputs loaded	P_{tot}	–	–	1	W
Operating ambient temperature range		T_{amb}	−20	–	+ 70	°C

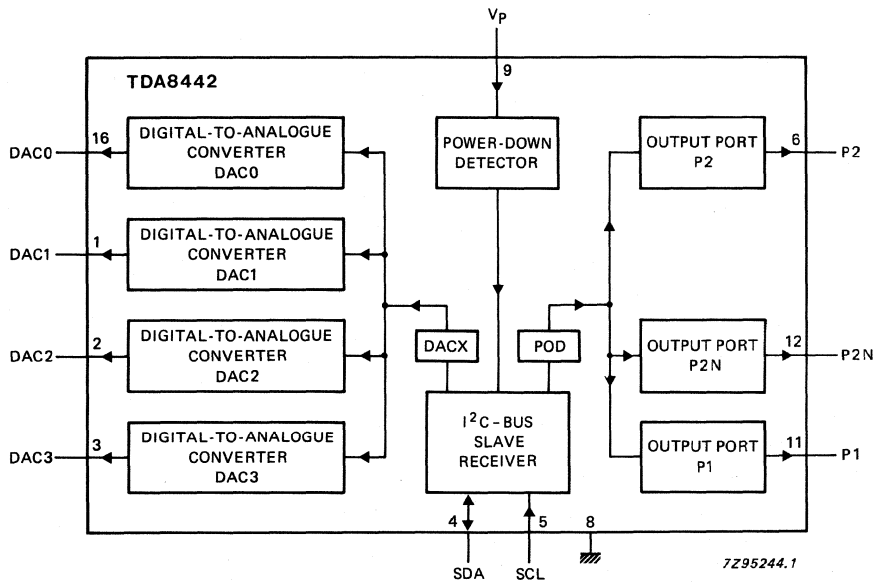


Fig. 1 Block diagram.

PACKAGE OUTLINE

16-lead DIL; plastic (SOT38).

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC12 OR DATASHEET

OCTUPLE 6-BIT DAC WITH I²C-BUS

GENERAL DESCRIPTION

The TDA8444 comprises eight digital-to-analogue converters (DACs) each controlled via the two-wire I²C-bus. The DACs are individually programmed using a 6-bit word to select an output from one of 64 voltage steps. The maximum output voltage of all DACs is set by the input V_{max} and the resolution is approximately $V_{max}/64$. At power-on all DAC outputs are set to their lowest value. The I²C-bus slave receiver has a 7-bit address of which 3 bits are programmable via pins A0, A1 and A2.

Features

- Eight discrete DACs
- I²C-bus slave receiver
- 16-pin DIL package

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage		V_P	10.8	12.0	13.2	V
Supply current	no loads; $V_{max} = V_P$; all data = 00	I_{CC}	8	12	15	mA
Total power dissipation	no loads; $V_{max} = V_P$; all data = 00	P_{tot}	–	150	–	mW
Effective range of V_{max} input	V_P = 12 V	V_{max}	1	–	10.5	V
DAC output voltage range		V_O	0.1	–	V_P–0.5	V
Step value of 1 LSB	$V_{max} = V_P$; I_O = –2 mA	V_{LSB}	70	160	250	mV

PACKAGE OUTLINE

16-lead DIL; plastic (SOT38).

2 x 40 W/2 Ω stereo BTL car radio power amplifier with diagnostic facility

TDA8560Q

FEATURES

- Requires very few external components
- High output power
- 4 Ω and 2 Ω load impedance
- Low output offset voltage
- Fixed gain
- Diagnostic facility (distortion, short-circuit and temperature detection)
- Good ripple rejection
- Mode select switch (operating, mute and stand-by)
- Load dump protection
- Short-circuit safe to ground, to V_P and across the load
- Low power dissipation in any short-circuit condition
- Thermally protected
- Reverse polarity safe
- Electrostatic discharge protection
- No switch-on/switch-off plop
- Flexible leads
- Low thermal resistance.

GENERAL DESCRIPTION

The TDA8560Q is an integrated class-B output amplifier in a 13-lead single-in-line (SIL) power package.
It contains 2 × 40 W/2 Ω amplifiers in BTL configuration.

The device is primarily developed for car radio applications.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	operating supply voltage		6.0	14.4	18	V
I_{ORM}	repetitive peak output current		–	–	7.5	A
$I_{q(tot)}$	total quiescent current		–	115	–	mA
I_{sb}	stand-by current		–	0.1	100	μA
I_{sw}	switch-on current		–	–	40	μA
$\|Z_I\|$	input impedance		25	30	–	kΩ
P_o	output power	R_L = 4 Ω; THD = 10%	–	25	–	W
		R_L = 2 Ω; THD = 10%	–	40	–	W
SVRR	supply voltage ripple rejection	R_s = 0 Ω	–	45	–	dB
α_{cs}	channel separation	R_s = 10 kΩ	–	50	–	dB
G_v	closed loop voltage gain		39	40	41	dB
V_{no}	noise output voltage	R_s = 0 Ω	–	–	250	μV
$\|\Delta V_O\|$	DC output offset voltage		–	–	200	mV

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA8560Q	13	DBS	plastic	SOT141R

2 x 40 W/2 Ω stereo BTL car radio power amplifier with diagnostic facility

TDA8560Q

BLOCK DIAGRAM

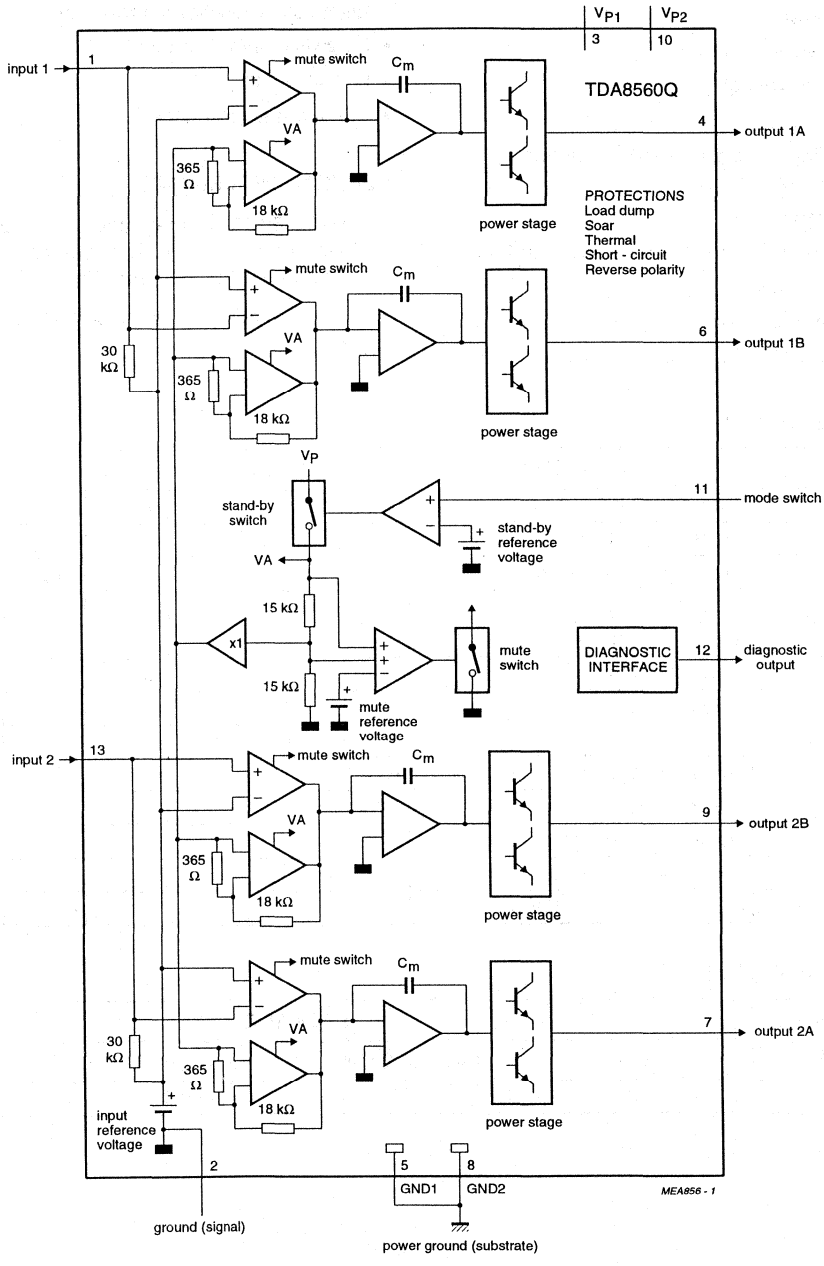


Fig.1 Block diagram.

2 x 40 W/2 Ω stereo BTL car radio power amplifier with diagnostic facility

TDA8560Q

PINNING

SYMBOL	PIN	DESCRIPTION
IN 1	1	input 1
GND(S)	2	signal ground
V_{P1}	3	supply voltage 1
OUT 1A	4	output 1A
GND1	5	power ground 1
OUT 1B	6	output 1B
OUT 2A	7	output 2A
GND2	8	power ground 2
OUT 2B	9	output 2B
V_{P2}	10	supply voltage 2
MODE	11	mode switch input
V_{DIAG}	12	diagnostic output
IN 2	13	input 2

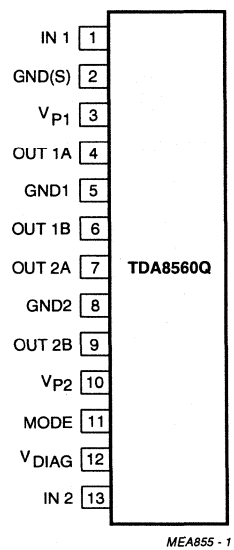


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The TDA8560Q contains two identical amplifiers and can be used for bridge applications. The gain of each amplifier is fixed at 40 dB. Special features of the device are as follows.

Mode select switch (pin 11)

- Stand-by: low supply current (<100 μA)
- Mute: input signal suppressed
- Operating: normal on condition.

Since this pin has a very low input current (<40 μA), a low cost supply switch can be applied.

To avoid switch-on plops, it is advised to keep the amplifier in the mute mode during ≥100 ms (charging of the input capacitors at pin 1 and pin 13).

This can be achieved by:

- Microprocessor control
- External timing circuit (see Fig.7).

Diagnostic output (pin 12)

DYNAMIC DISTORTION DETECTOR (DDD)

At the onset of clipping of one or more output stages, the dynamic distortion detector becomes active and pin 12 goes low. This information can be used to drive a sound processor or DC volume control to attenuate the input signal and thus limit the distortion. The output level of pin 12 is independent of the number of channels that are clipping (see Fig.3).

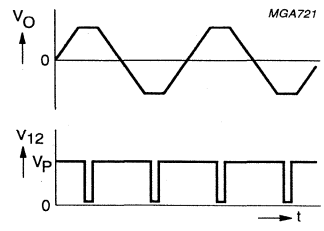


Fig.3 Distortion detector waveform.

SHORT-CIRCUIT PROTECTION

When a short-circuit occurs at one or more outputs to ground or to the supply voltage, the output stages are switched off until the short-circuit is removed and the device is switched on again, with a delay of approximately 20 ms, after removal of the short-circuit. During this short-circuit condition, pin 12 is continuously low.

When a short-circuit across the load of one or both channels occurs the output stages are switched off during approximately 20 ms. After that time it is checked during approximately 50 µs to see whether the short-circuit is still present. Due to this duty cycle of 50 µs/20 ms the average current consumption during this short-circuit condition is very low (approximately 40 mA).

During this short-circuit condition, pin 12 is low for 20 ms and high for 50 µs (see Fig. 4).

The power dissipation in any short-circuit condition is very low.

TEMPERATURE DETECTION

When the virtual junction temperature T_{vj} reaches 150 °C, pin 12 will become continuously low.

OPEN COLLECTOR OUTPUT

Pin 12 is an open collector output, which allows pin 12 of more devices being tied together.

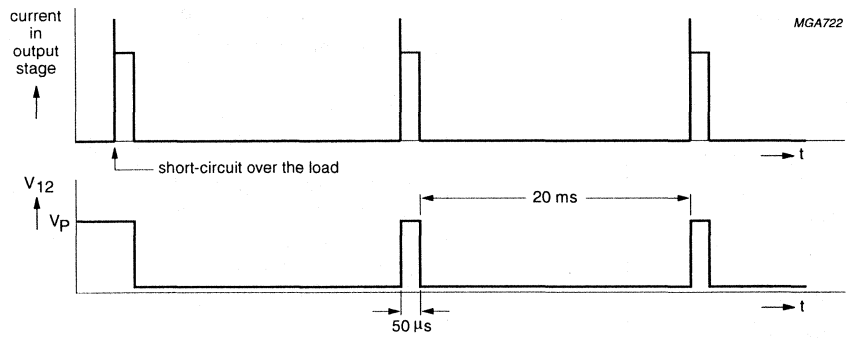


Fig.4 Short-circuit waveform.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_P	supply voltage				
	operating		–	18	V
	non-operating		–	30	V
	load dump protection	during 50 ms; $t_r \geq 2.5$ ms	–	45	V
V_{psc}	AC and DC short-circuit safe voltage		–	18	V
V_{pr}	reverse polarity		–	6	V
I_{OSM}	non-repetitive peak output current		–	10	A
I_{ORM}	repetitive peak output current		–	7.5	A
P_{tot}	total power dissipation		–	60	W
T_{stg}	storage temperature		–55	+150	°C
T_{amb}	operating ambient temperature		–40	+85	°C
T_{vj}	virtual junction temperature		–	150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient in free air	40 K/W
$R_{th\ j\text{-}c}$	from junction to case (see Fig.5)	1.3 K/W

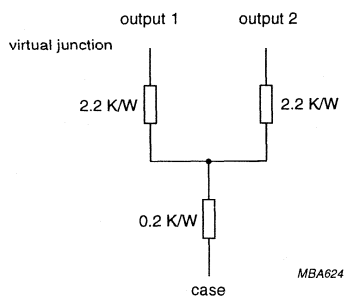


Fig.5 Equivalent thermal resistance network.

DC CHARACTERISTICS

V_P = 14.4 V; T_{amb} = 25 °C; measured in Fig.6; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_P	supply voltage	note 1	6.0	14.4	18	V
I_q	quiescent current	$R_L = \infty$	–	115	180	mA
Operating condition						
V_{11}	mode switch voltage level		8.5	–	V_P	V
I_{11}	mode switch current	V_{11} = 14.4 V	–	15	40	μA
V_O	DC output voltage	note 2	–	7.0	–	V
$\lvert\Delta V_O\rvert$	DC output offset voltage		–	–	200	mV
Mute condition						
V_{11}	mode switch voltage level		3.3	–	6.4	V
V_O	DC output voltage	note 2	–	7.0	–	V
$\lvert\Delta V_O\rvert$	DC output offset voltage		–	–	200	mV
Stand-by condition						
V_{11}	mode switch voltage level		0	–	2	V
I_{sb}	stand-by current		–	0.1	100	μA
Diagnostic output						
V_{12}	diagnostic output voltage	any short-circuit or clipping	–	–	0.6	V

Notes

1. The circuit is DC adjusted at V_P = 6 to 18 V and AC operating at V_P = 8.5 to 18 V.
2. At 18 V < V_P < 30 V the DC output voltage $\leq \frac{1}{2}V_P$.

AC CHARACTERISTICS

V_P = 14.4 V; R_L = 2 Ω; f = 1 kHz; T_{amb} = 25 °C; measured in Fig.6; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
P_o	output power	THD = 0.5%	25	30	–	W
		THD = 10%	33	40	–	W
		THD = 30%	45	55	–	W
P_o	output power	V_P = 13.2 V				
		THD = 0.5%	–	25	–	W
		THD = 10%	–	35	–	W
THD	total harmonic distortion	P_o = 1 W	–	0.1	–	%
		$V_{12} \leq$ 0.6 V; note 1	–	10	–	%
B	power bandwidth	THD = 0.5%; P_o = −1 dB with respect to 25 W	–	20 to 20000	–	Hz
f_{lr}	low frequency roll-off	at −1 dB; note 2	–	25	–	Hz
f_{hr}	high frequency roll-off	at −1 dB	20	–	–	kHz
G_v	closed loop voltage gain		39	40	41	dB
SVRR	supply voltage ripple rejection					
	on	note 3	40	–	–	dB
	mute	note 3	50	–	–	dB
	stand-by	note 3	80	–	–	dB
$\|Z_i\|$	input impedance		25	30	38	kΩ
V_{no}	noise output voltage					
	on	note 4	–	200	250	μV
	on	note 5	–	250	–	μV
	mute	note 6	–	135	–	μV
α_{cs}	channel separation	note 7	45	–	–	dB
$\|\Delta G_v\|$	channel unbalance		–	–	1	dB
V_o	output voltage in mute	note 8	–	–	5	mV

Notes

1. Dynamic distortion detector active.
2. Frequency response externally fixed.
3. $V_{ripple} = V_{ripple(max)}$ = 2 V (p-p); R_s = 0 Ω.
4. B = 20 Hz to 20 kHz; R_s = 0 Ω.
5. B = 20 Hz to 20 kHz; R_s = 10 kΩ.
6. B = 20 Hz to 20 kHz; independent of R_s.
7. P_o = 25 W; R_s = 10 kΩ.
8. $V_i = V_{i(max)}$ = 1 V (RMS).

AC CHARACTERISTICS

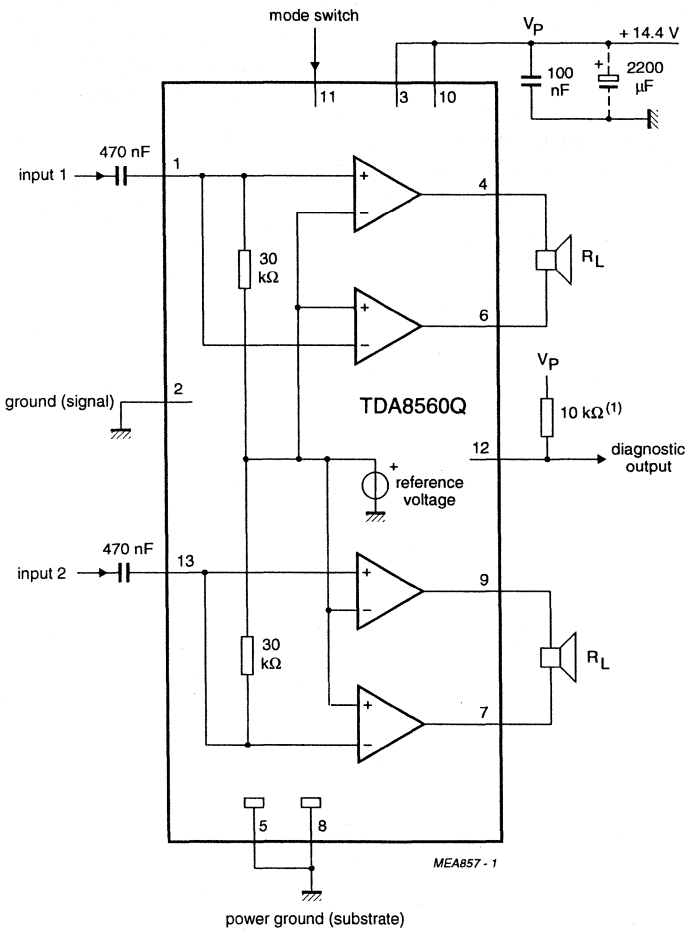
V_P = 14.4 V; R_L = 4 Ω; f = 1 kHz; T_{amb} = 25 °C; measured in Fig.6; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
P_o	output power	THD = 0.5%	16	19	–	W
		THD = 10%	21	25	–	W
		THD = 30%	28	35	–	W
P_o	output power	V_P = 13.2 V				
		THD = 0.5%	–	15	–	W
		THD = 10%	–	21	–	W
THD	total harmonic distortion	P_o = 1 W	–	0.1	–	%

QUALITY SPECIFICATION

Quality in accordance with *"Quality reference pocketbook UZW-BO/FQ-0601"*, if this type used as an audio amplifier.

TEST/APPLICATION INFORMATION



(1) To avoid high energy switching pulses which can feedback to the inputs it is advisable to ensure that the value of the resistor at pin 12 is ≥10 kΩ.

Fig.6 Stereo BTL test/application diagram.

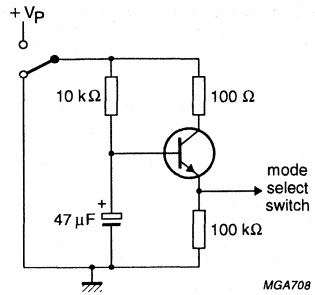


Fig.7 Mode select switch circuitry.

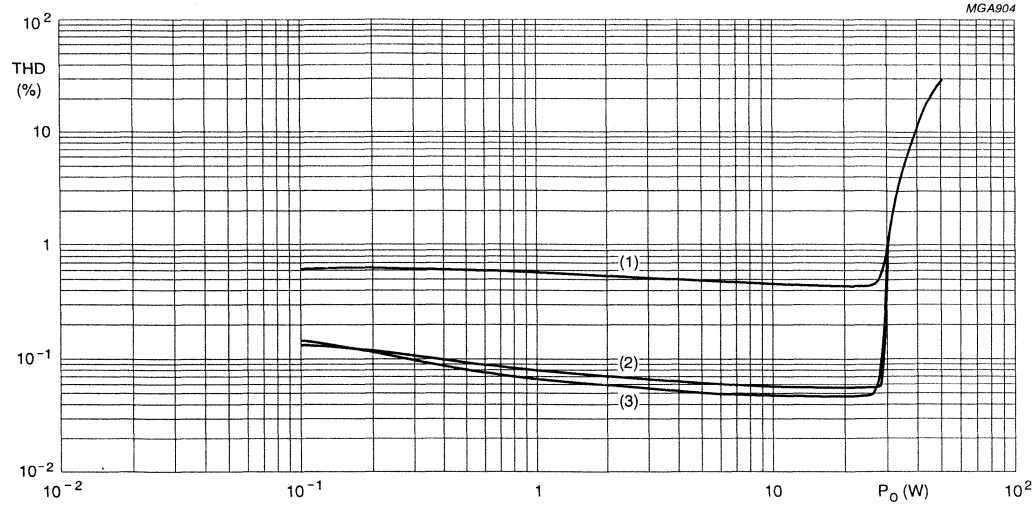
Diagnostic output

Special care must be taken in the printed-circuit board layout to separate pin 12 from pin 1 and pin 13, to minimize the crosstalk between the diagnostic output and the inputs.

Mode select switch

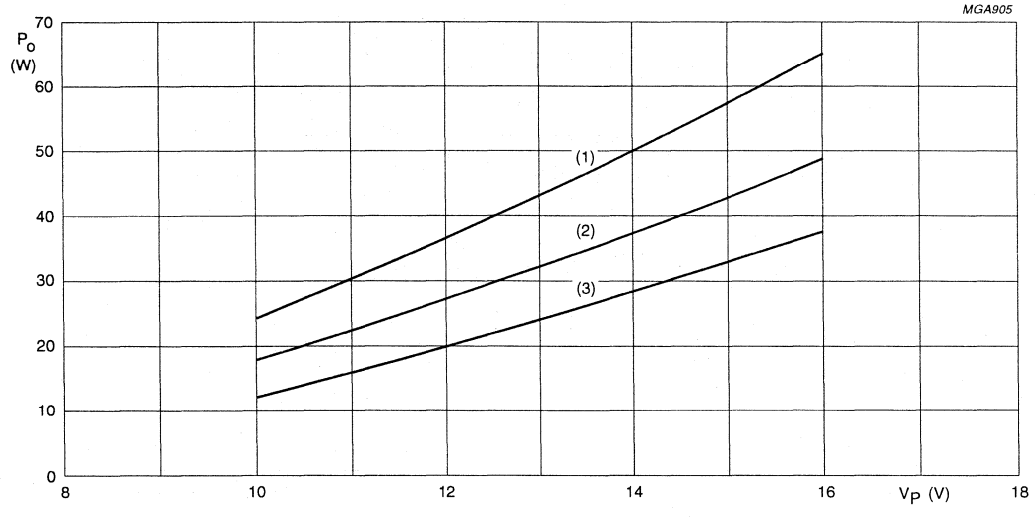
To avoid switch-on plops, it is advised to keep the amplifier in the mute mode during >100 ms (charging of the input capacitors at pin 1 and pin 13).

The circuit in Fig.7 slowly ramps up the voltage at the mode select switch pin when switching on and results in fast muting when switching off.



(1) f = 10 kHz.
(2) f = 1 Hz.
(3) f = 100 Hz.

Fig.8 Total harmonic distortion as a function of output power; V_P = 14.4 V; R_L = 2 Ω.



(1) THD = 30%.
(2) THD = 10%.
(3) THD = 0.5%.

Fig.9 Output power as a function of supply voltage; f = 1 kHz; R_L = 2 Ω.

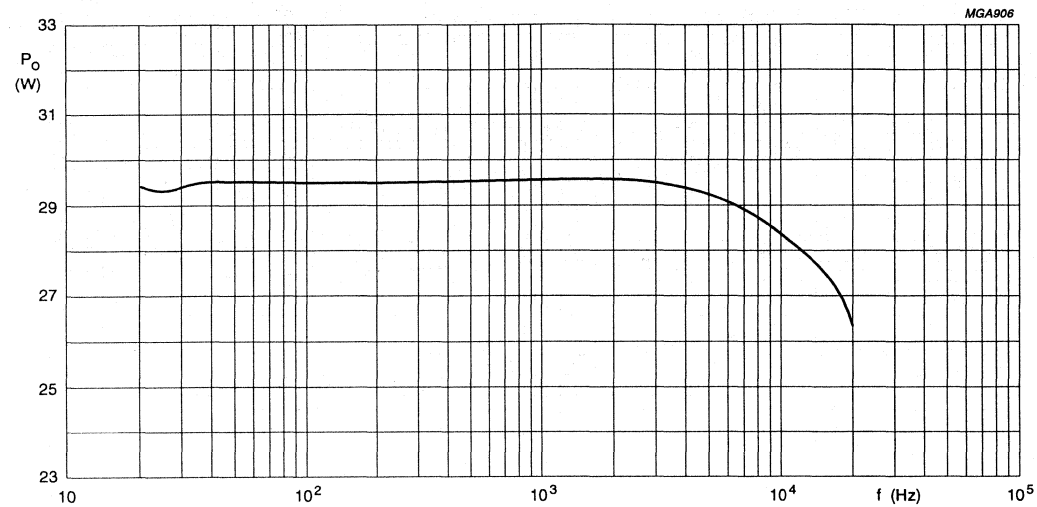
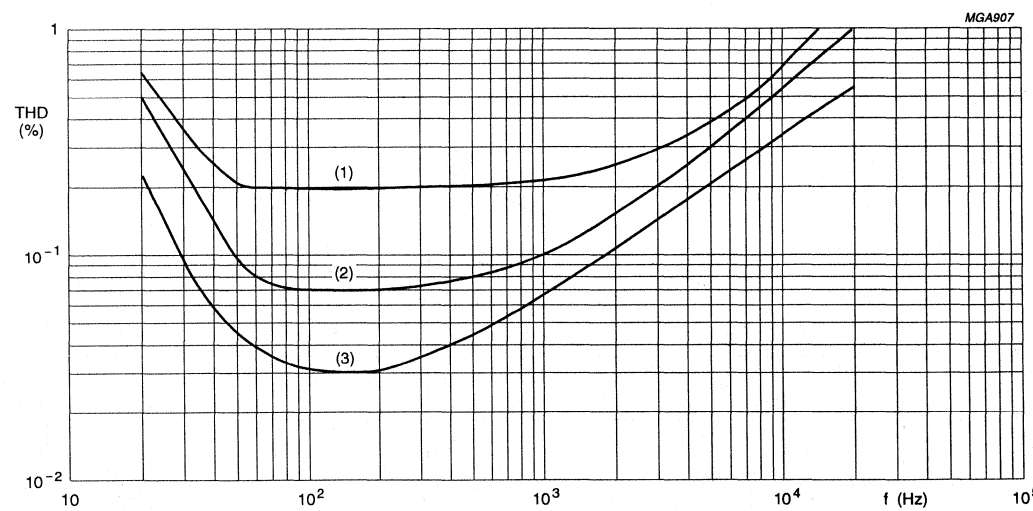
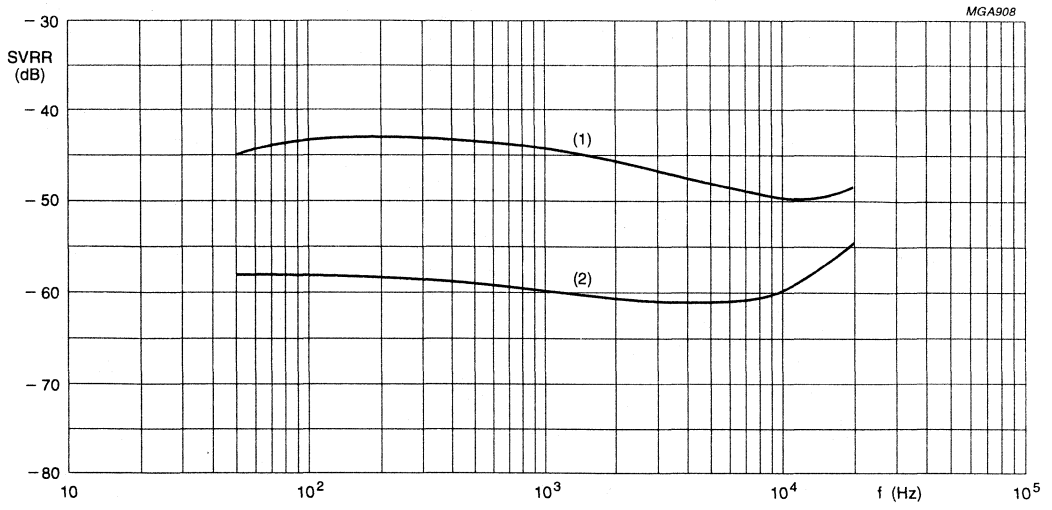


Fig.10 Output power as a function of frequency; THD = 0.5%; V_P = 14.4 V; R_L = 2 Ω.



(1) P_o = 0.1 W.
(2) P_o = 1 W.
(3) P_o = 10 W.

Fig.11 Total harmonic distortion as a function of frequency; V_P = 14.4 V; R_L = 2 Ω.



(1) On condition.
(2) Mute condition.

Fig.12 Ripple rejection as a function of frequency; V_P = 14.4 V; V_{ripple} = 2 V (p-p); R_s = 0 Ω.

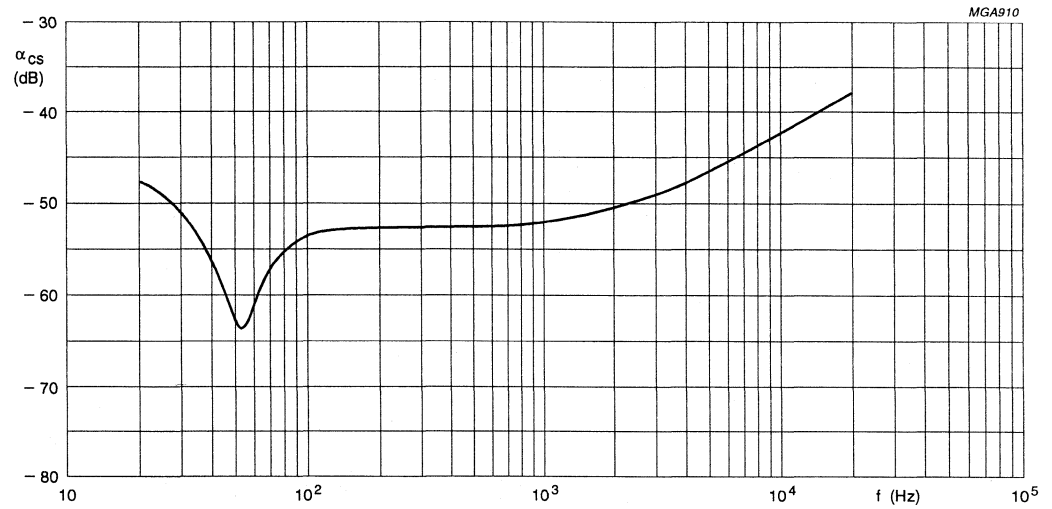


Fig.13 Channel separation as a function of frequency; V_P = 14.4 V; P_o = 25 W; R_L = 2 Ω; R_s = 10 kΩ.

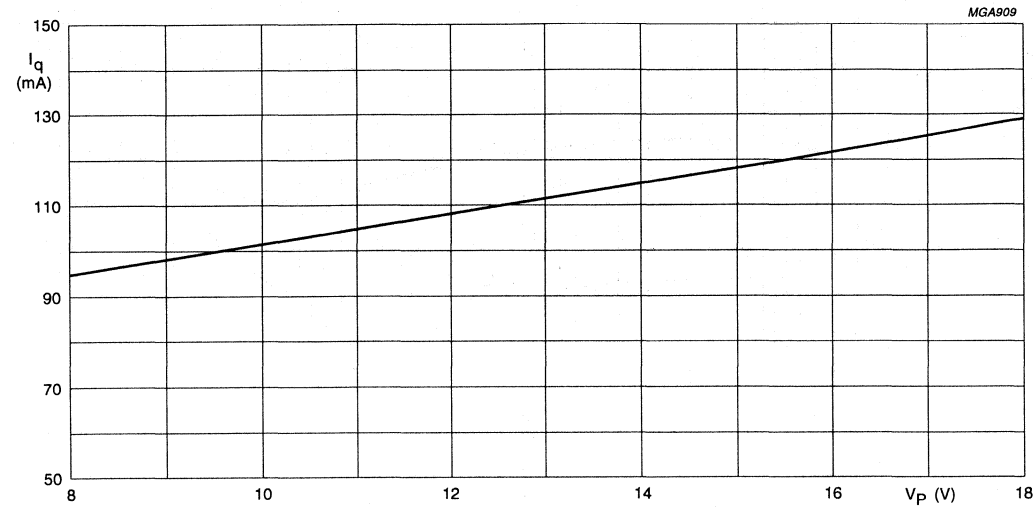


Fig.14 Quiescent current as a function of supply voltage; $R_L = \infty$.

2 x 24 W BTL or 4 x 12 W single-ended car radio power amplifier

TDA8561Q

FEATURES

- Requires very few external components
- High output power
- Flexibility in use - Quad single-ended or stereo BTL
- Low output offset voltage
- Fixed gain
- Diagnostic facility (distortion, short-circuit and temperature detection)
- Good ripple rejection
- Mode select switch (operating, mute and stand-by)
- Load dump protection
- AC and DC short-circuit safe to ground and to V_P
- Low power dissipation in any short-circuit condition
- Thermally protected
- Reverse polarity safe
- Electrostatic discharge protection
- No switch-on/switch-off plop
- Flexible leads
- Low thermal resistance
- Identical inputs (inverting and non-inverting).

GENERAL DESCRIPTION

The TDA8561Q is an integrated class-B output amplifier in a 17-lead single-in-line (SIL) power package. It contains 4 x 12 W single-ended or 2 x 24 W bridge amplifiers.
The device is primarily developed for car radio applications.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	positive operating supply voltage		6	14.4	18	V
I_{ORM}	repetitive peak output current		–	–	4	A
I_P	total quiescent current		–	80	–	mA
I_{sb}	stand-by current		–	0.1	100	μA
Stereo BTL application						
P_O	output power	4 Ω; THD = 10%	–	24	–	W
RR	supply voltage ripple rejection		48	–	–	dB
V_{no}	noise output voltage	R_s = 0 Ω	–	70	–	μV
$\|Z_I\|$	input impedance		25	–	–	kΩ
$\|\Delta V_O\|$	DC output offset voltage		–	–	150	mV
Quad single-ended application						
P_O	output power	THD = 10%				
		4 Ω	–	7	–	W
		2 Ω	–	12	–	W
RR	supply voltage ripple rejection		48	–	–	dB
V_{no}	noise output voltage	R_s = 0 Ω	–	50	–	μV
$\|Z_I\|$	input impedance		50	–	–	kΩ

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA8561Q	17	DBS	plastic	SOT243R

2 x 24 W BTL or 4 x 12 W single-ended car radio power amplifier

TDA8561Q

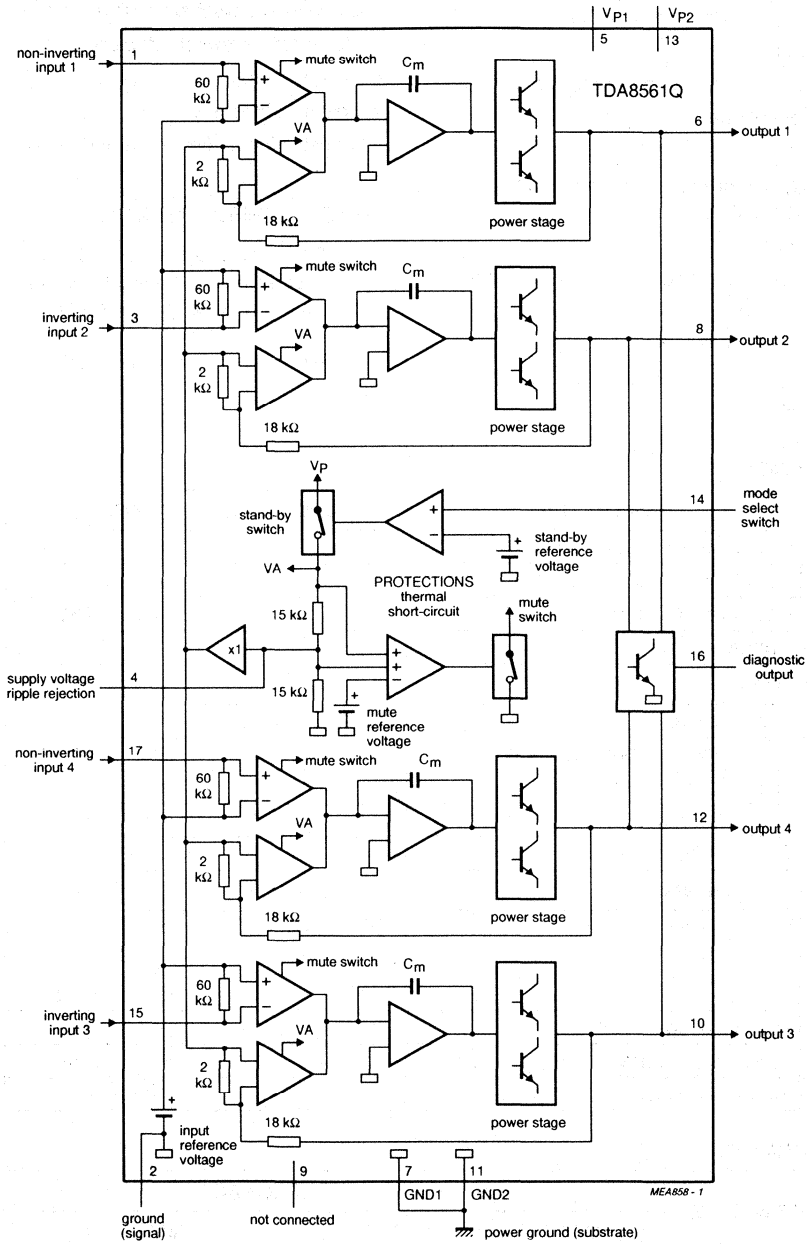


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
–INV 1	1	non-inverting input 1
GND(S)	2	signal ground
INV 2	3	inverting input 2
RR	4	supply voltage ripple rejection
V_{P1}	5	supply voltage
OUT 1	6	output 1
GND1	7	power ground 1
OUT 2	8	output 2
n.c.	9	not connected
OUT 3	10	output 3
GND2	11	power ground 2
OUT 4	12	output 4
V_{P2}	13	supply voltage
MODE	14	mode select switch input
INV 3	15	inverting input 3
V_{DIAG}	16	diagnostic output
–INV 4	17	non-inverting input 4

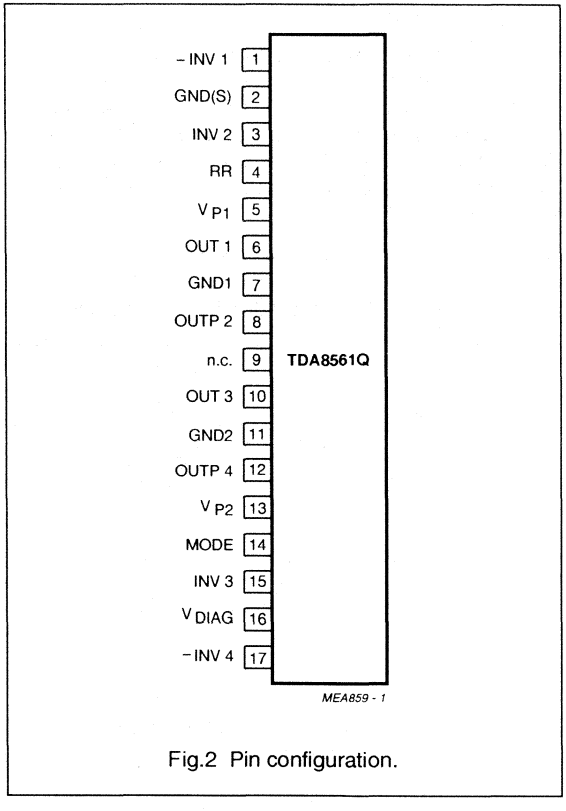


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The TDA8561Q contains four identical amplifiers and can be used for single-ended or bridge applications. The gain of each amplifier is fixed at 20 dB (26 dB in BTL). Special features of the device are:

Mode select switch (pin 14)

- low stand-by current (< 100 μA)
- low switching current (low cost supply switch)
- mute facility

To avoid switch-on plops, it is advised to keep the amplifier in the mute mode during ≥ 100 ms (charging of the input capacitors at pin 1, 3, 15 and pin 17).
This can be achieved by:

- microprocessor control
- external timing circuit (see Fig.11)

Diagnostic output (pin 16)

DYNAMIC DISTORTION DETECTOR (DDD)

At the onset of clipping of one or more output stages, the dynamic distortion detector becomes active and pin 16 goes low. This information can be used to drive a sound processor or DC volume control to attenuate the input signal and thus limit the distortion. The output level of pin 16 is independent of the number of channels that are clipping (see Fig.3 and Fig.4).

SHORT-CIRCUIT PROTECTION

When a short-circuit occurs at one or more outputs to ground or to the supply voltage, the output stages are switched off until the short-circuit is removed and the device is switched on again, with a delay of approximately 20 ms, after removal of the short-circuit. During this short-circuit condition, pin 16 is continuously low.

When a short-circuit across the load of one or both channels occurs the output stages are switched off during approximately 20 ms. After that time it is checked during approximately 50 µs to see whether the short-circuit is still present. Due to this duty cycle of 50 µs/20 ms the average current consumption during this short-circuit condition is very low (approximately 40 mA).
During this short-circuit condition, pin 16 is low for 20 ms and high for 50 µs (see Fig.5).

The power dissipation in any short-circuit condition is very low.

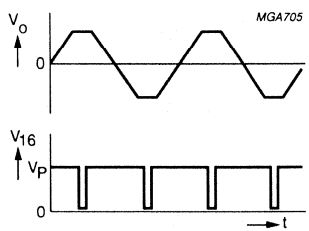


Fig.3 Distortion detector waveform; BTL application.

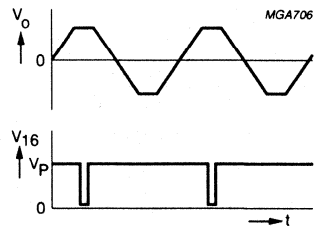


Fig.4 Distortion detector waveform; single-ended application.

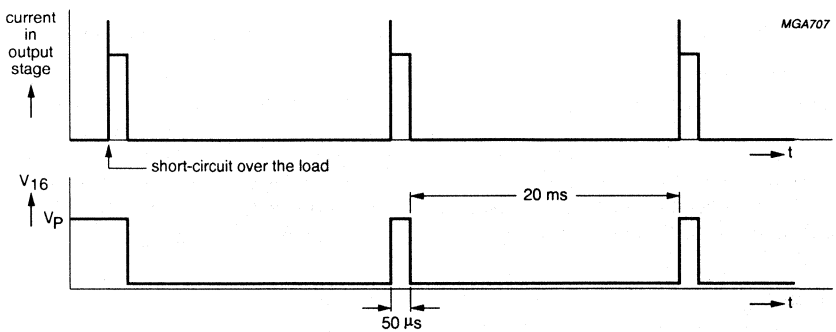


Fig.5 Short-circuit waveform.

TEMPERATURE DETECTION

When the virtual junction temperature T_{vj} reaches 150 °C, pin 16 will be active LOW.

OPEN COLLECTOR OUTPUT

Pin 16 is an open collector output, which allows pin 16 of more devices being tied together.

LIMITING VALUES

In accordance with the absolute maximum system (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_P	positive supply voltage				
	operating		–	18	V
	non-operating		–	30	V
	load dump protection	during 50 ms; $t_r \geq 2.5$ ms	–	45	V
I_{OSM}	non-repetitive peak output current		–	6	A
I_{ORM}	repetitive peak output current		–	4	A
T_{stg}	storage temperature		–55	+150	°C
T_{amb}	operating ambient temperature		–40	+85	°C
T_{vj}	virtual junction temperature		–	150	°C
V_{psc}	AC and DC short-circuit safe voltage		–	18	V
V_{pr}	reverse polarity		–	6	V
P_{tot}	total power dissipation		–	60	W

THERMAL RESISTANCE

In accordance with IEC 747-1.

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient in free air	40 K/W
$R_{th\ j\text{-}c}$	from junction to case (see Fig.6 and Fig.7)	1.3 K/W

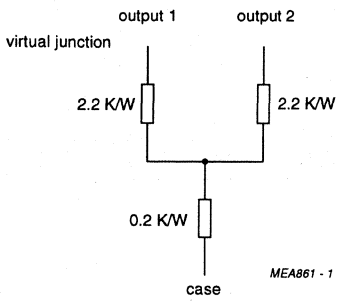


Fig.6 Equivalent thermal resistance network; BTL application.

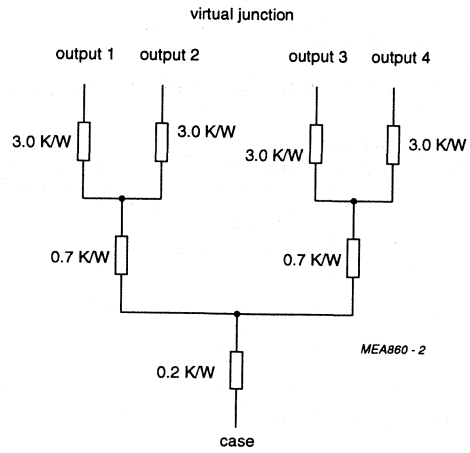


Fig.7 Equivalent thermal resistance network; single-ended application.

DC CHARACTERISTICS

V_P = 14.4 V; T_{amb} = 25 °C; measured in Fig.8; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_P	positive supply voltage	note 1	6	14.4	18	V
I_P	quiescent current		–	80	160	mA
V_O	DC output voltage	note 2	–	6.9	–	V
$\lvert\Delta V_O\rvert$	DC output offset voltage		–	–	150	mV
Mode select switch						
V_{on}	switch-on voltage level		8.5	–	–	V
MUTE CONDITION						
V_{mute}	mute voltage		3.3	–	6.4	V
V_O	output voltage in mute position	V_{Imax} = 1 V; f = 1 kHz	–	–	2	mV
$\lvert\Delta V_O\rvert$	DC output offset voltage (between pins 6-8 and 10-12)		–	–	150	mV
STAND-BY CONDITION						
V_{sb}	stand-by voltage		0	–	2	V
I_{sb}	stand-by current		–	–	100	µA
I_{sw}	switch-on current		–	12	40	µA
Diagnostic output (pin 16)						
V_{DIAG}	diagnostic output voltage	any short-circuit or clipping	–	–	0.6	V

AC CHARACTERISTICS

V_P = 14.4 V; R_L = 4 Ω; f = 1 kHz; T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Stereo BTL application (measured in Fig.8)						
P_O	output power	note 7				
		THD = 0.5%	15	19	–	W
		THD = 10%	20	24	–	W
THD	total harmonic distortion	P_O = 1 W	–	0.1	–	%
P_O	output power	V_P = 13.2 V				
		THD = 0.5%	–	16	–	W
		THD = 10%	–	20	–	W
B	power bandwidth	THD = 0.5%; P_O = −1 dB; with respect to 15 W	–	20 to 15000	–	Hz
f_l	low frequency roll-off	at −1 dB; note 3	–	45	–	Hz
f_h	high frequency roll-off	at −1 dB	20	–	–	kHz
G_v	closed loop voltage gain		25	26	27	dB
RR	supply voltage ripple rejection	note 4				
	on		48	–	–	dB
	mute		48	–	–	dB
	stand-by		80	–	–	dB
$\|Z_I\|$	input impedance		25	30	38	kΩ
V_{no}	noise output voltage					
	on	R_s = 0 Ω; note 5	–	70	–	μV
	on	R_s = 10 kΩ; note 5	–	100	200	μV
	mute	notes 5 and 6	–	60	–	μV
α	channel separation	R_s = 10 kΩ	40	–	–	dB
$\|\Delta G_v\|$	channel unbalance		–	–	1	dB
DYNAMIC DISTORTION DETECTOR						
THD	total harmonic distortion	$V_{16} \leq$ 0.6 V; no short-circuit	–	10	–	%
Quad single-ended application (measured in Fig.9)						
P_O	output power	note 7				
		THD = 0.5%	4	5	–	W
		THD = 10%	5.5	7	–	W
THD	total harmonic distortion	P_O = 1 W	–	0.1	–	%
P_O	output power	R_L = 2 Ω; note 7				
		THD = 0.5%	7.5	10	–	W
		THD = 10%	10	12	–	W
f_l	low frequency roll-off	at −3 dB; note 3	–	45	–	Hz
f_h	high frequency roll-off	at −1 dB	20	–	–	kHz

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Quad single-ended application (measured in Fig.9)						
G_v	closed loop voltage gain		19	20	21	dB
RR	supply voltage ripple rejection	note 4				
	on		48	–	–	dB
	mute		48	–	–	dB
	stand-by		80	–	–	dB
$\|Z_I\|$	input impedance		50	60	75	kΩ
V_{no}	noise output voltage					
	on	R_s = 0 Ω; note 5	–	50	–	μV
	on	R_s = 10 kΩ; note 5	–	70	100	μV
	mute	notes 5 and 6	–	50	–	μV
α	channel separation	R_s = 10 kΩ	40	–	–	dB
$\|\Delta G_v\|$	channel unbalance		–	–	1	dB
DYNAMIC DISTORTION DETECTOR						
THD	total harmonic distortion	$V_{16} \leq 0.6$ V; no short-circuit	–	10	–	%

Notes

1. The circuit is DC adjusted at V_P = 6 to 18 V and AC operating at V_P = 8.5 to 18 V.
2. At 18 V < V_P < 30 V the DC output voltage ≤ $V_P/2$.
3. Frequency response externally fixed.
4. Ripple rejection measured at the output with a source impedance of 0 Ω, maximum ripple amplitude of 2 V (p-p) and at a frequency of between 100 Hz and 10 kHz.
5. Noise measured in a bandwidth of 20 Hz to 20 kHz.
6. Noise output voltage independent of R_s (V_I = 0 V).
7. Output power is measured directly at the output pins of the IC.

TEST/APPLICATION INFORMATION

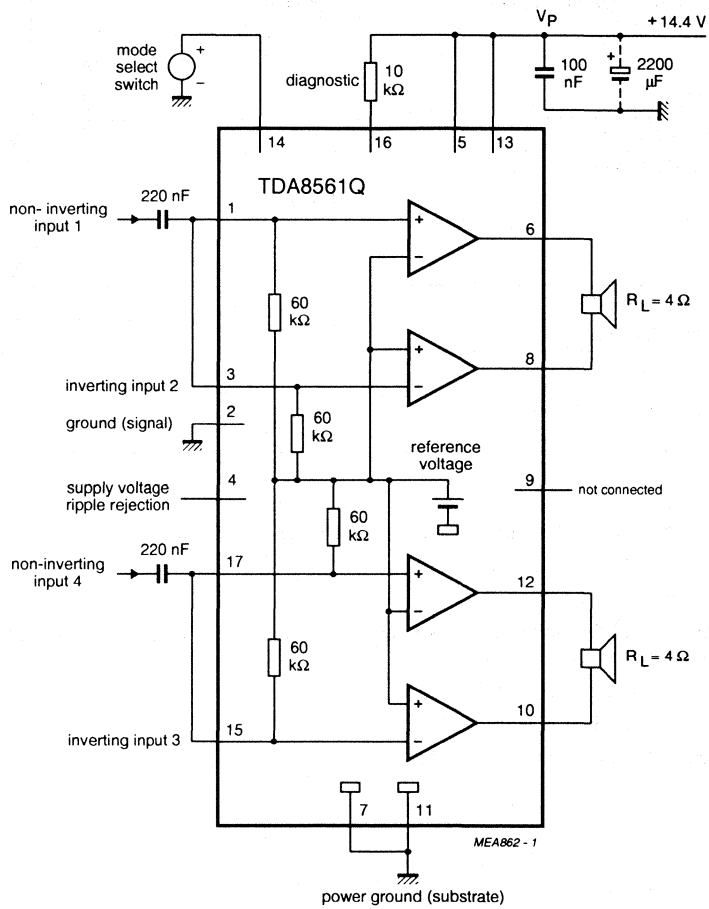


Fig.8 Stereo BTL application diagram.

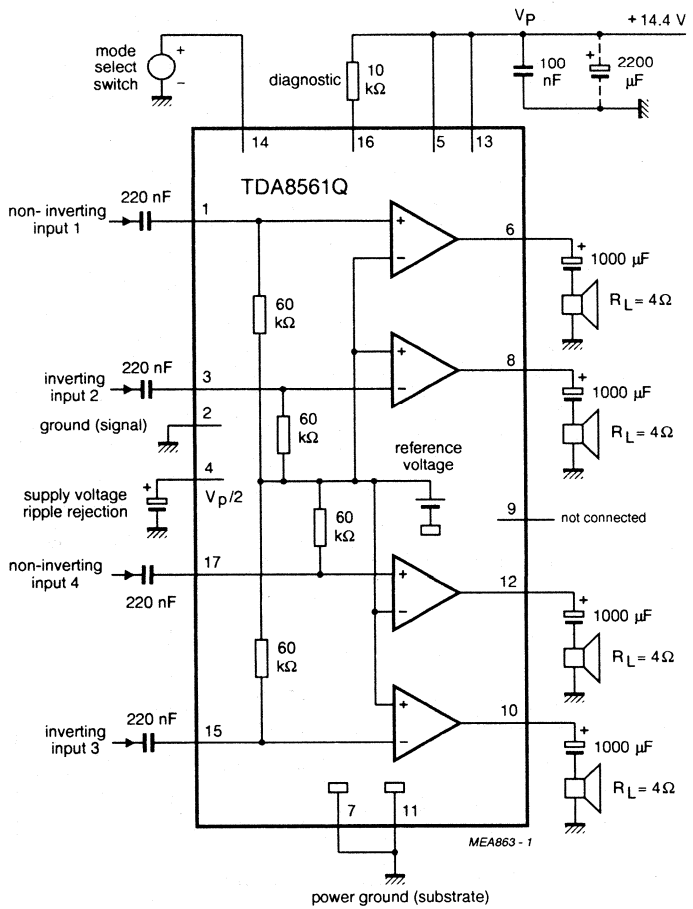
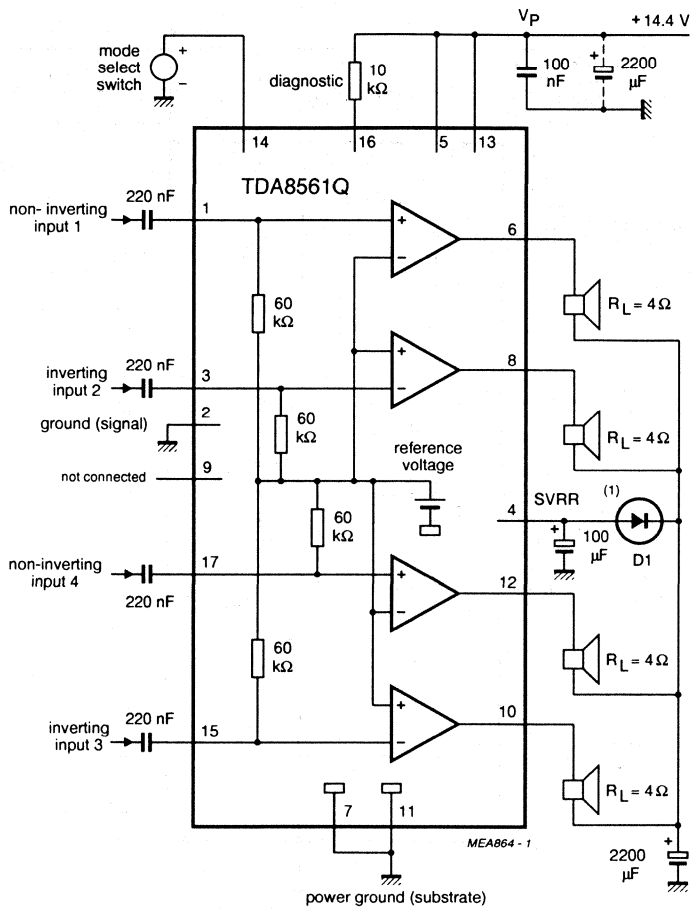


Fig.9 Quad single-ended application diagram 1.



(1) When short-circuiting the single-ended capacitor, the dissipation will be reduced due to diode D1.

Fig.10 Quad single-ended application diagram 2.

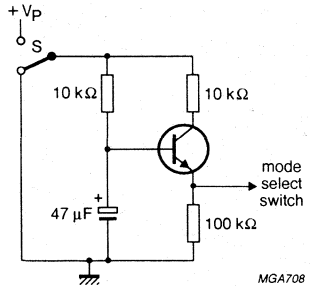
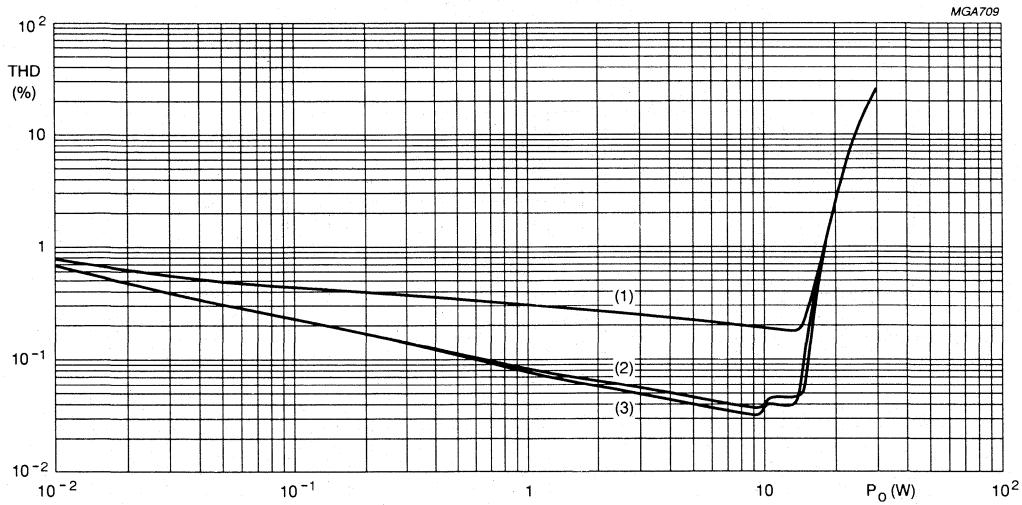


Fig.11 Mode select switch circuitry.

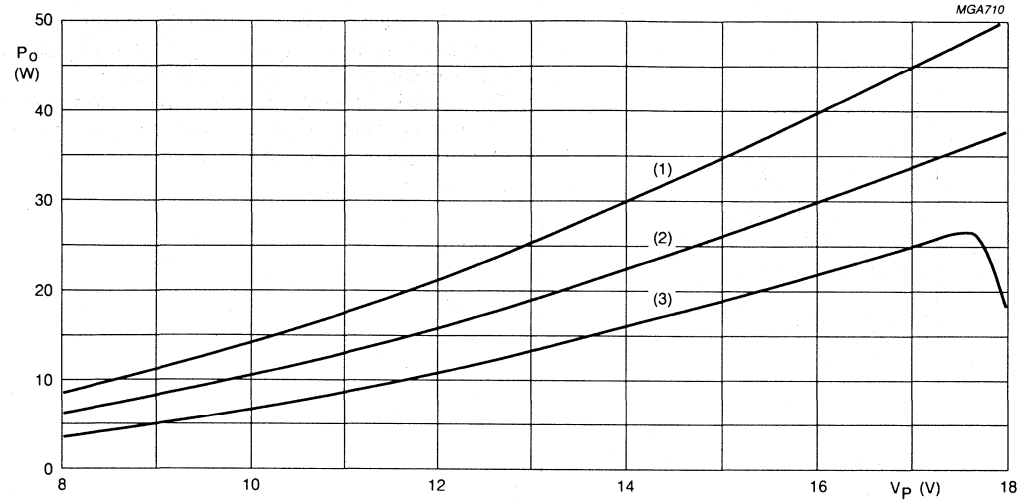
Mode select switch

To avoid switch-on plops, it is advised to keep the amplifier in the mute mode during > 100 ms (charging of the input capacitors at pins 1, 3, 15 and 17.
The circuit in Fig.11 slowly ramps up the voltage at the mode select switch pin when switching on and results in fast muting when switching off.



(1) f = 10 kHz.
(2) f = 1 kHz.
(3) f = 100 Hz.

Fig.12 Total harmonic distortion as a function of output power; V_P = 14.4 V, R_L = 4 Ω.



(1) THD = 30%.
(2) THD = 10%.
(3) THD = 0.5%.

Fig.13 Output power as a function of supply voltage.

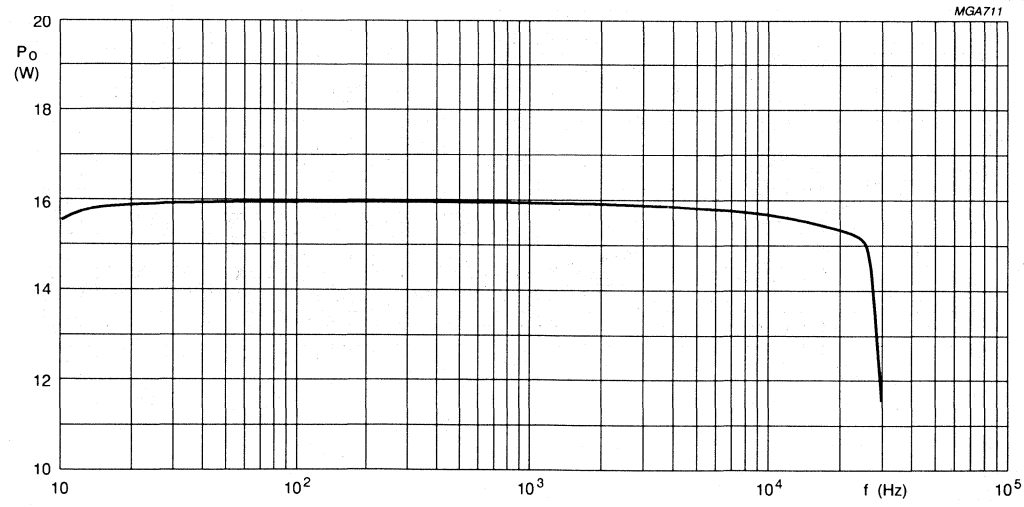
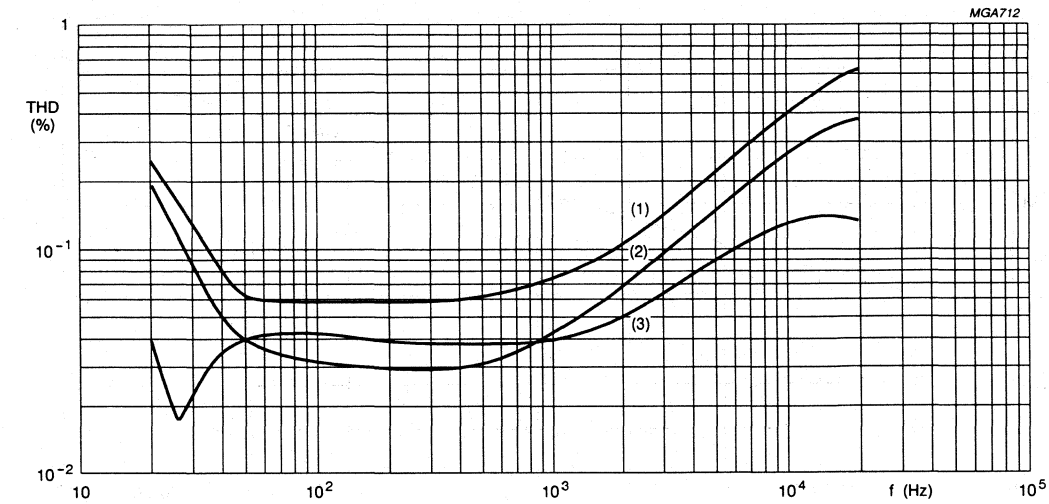
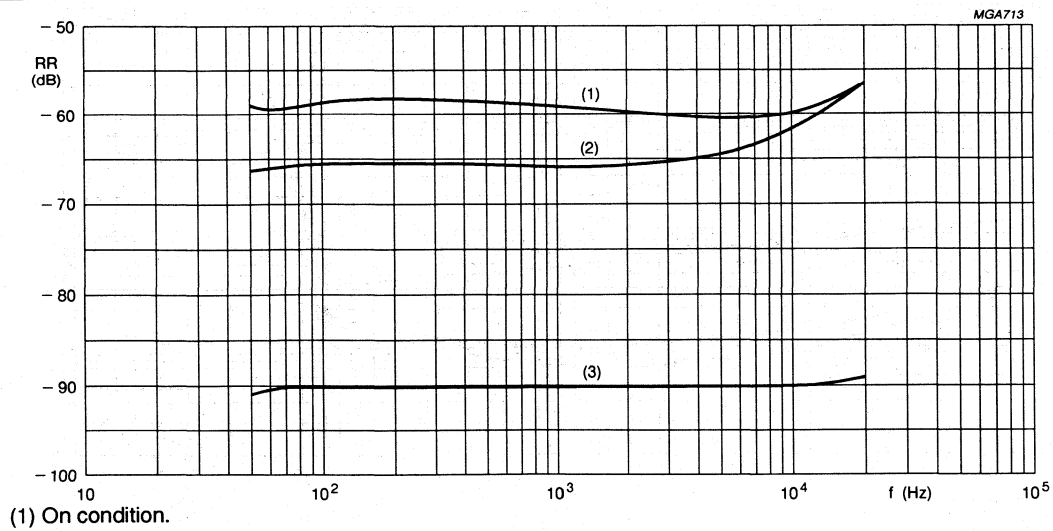


Fig.14 Power bandwidth as a function of frequency; THD = 0.5%, V_P = 14.4 V, R_L = 4 Ω.



(1) P_O = 0.1 W.
(2) P_O = 1 W.
(3) P_O = 10 W.

Fig.15 Total harmonic distortion as a function of frequency; V_P = 14.4 V, R_L = 4 Ω.



(1) On condition.
(2) Mute condition.
(3) Stand-by condition.

Fig.16 Ripple rejection as a function of frequency.

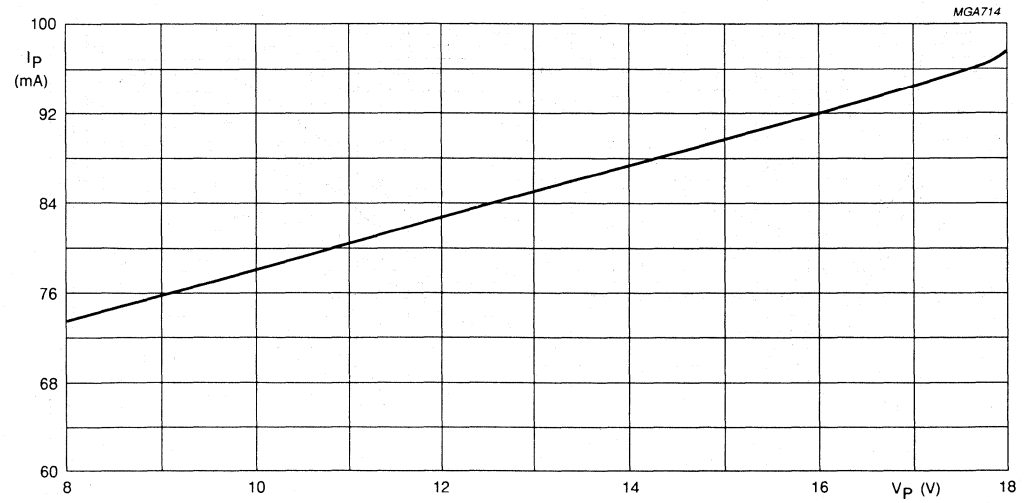
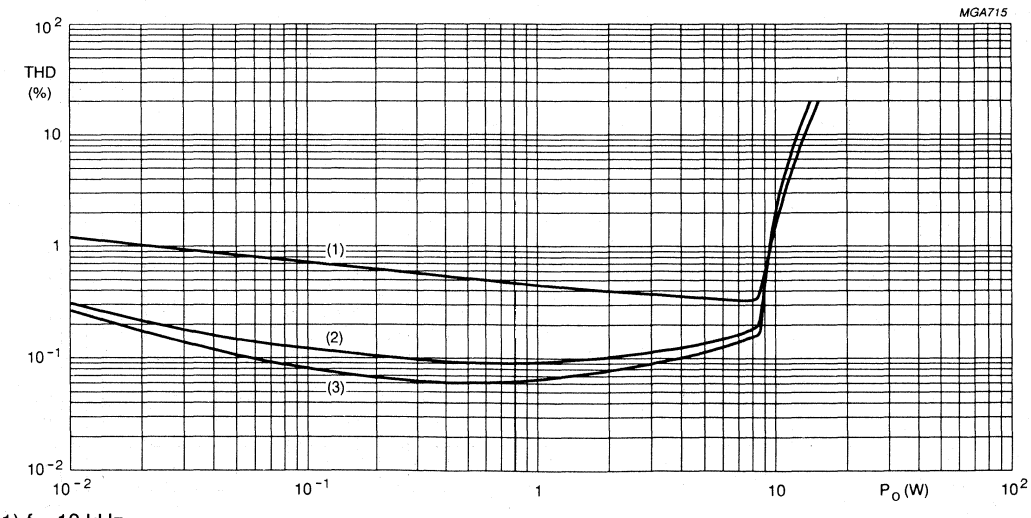


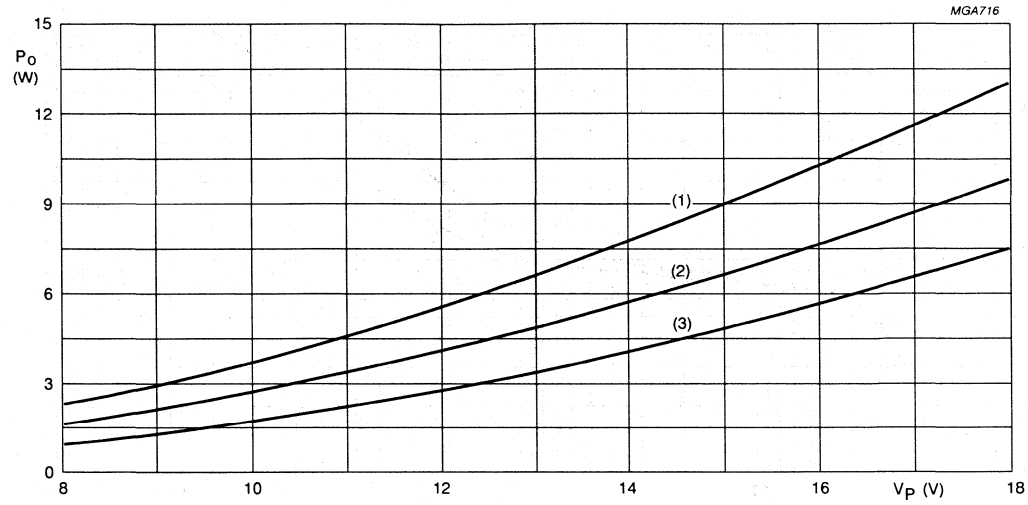
Fig.17 Quiescent current as a function of supply voltage; $R_L = \infty$.

SINGLE-ENDED APPLICATION



(1) f = 10 kHz.
(2) f = 1 kHz.
(3) f = 100 Hz.

Fig.18 Total harmonic distortion as a function of output power; $V_P = 14.4$ V, $R_L = 2\ \Omega$.



(1) THD = 30%.
(2) THD = 10%.
(3) THD = 0.5%.

Fig.19 Output power as a function of supply voltage.

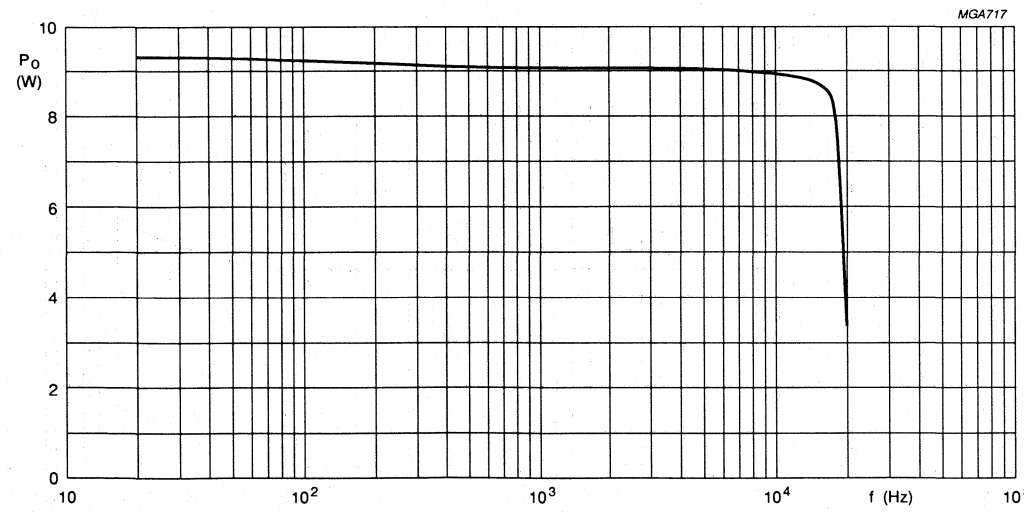
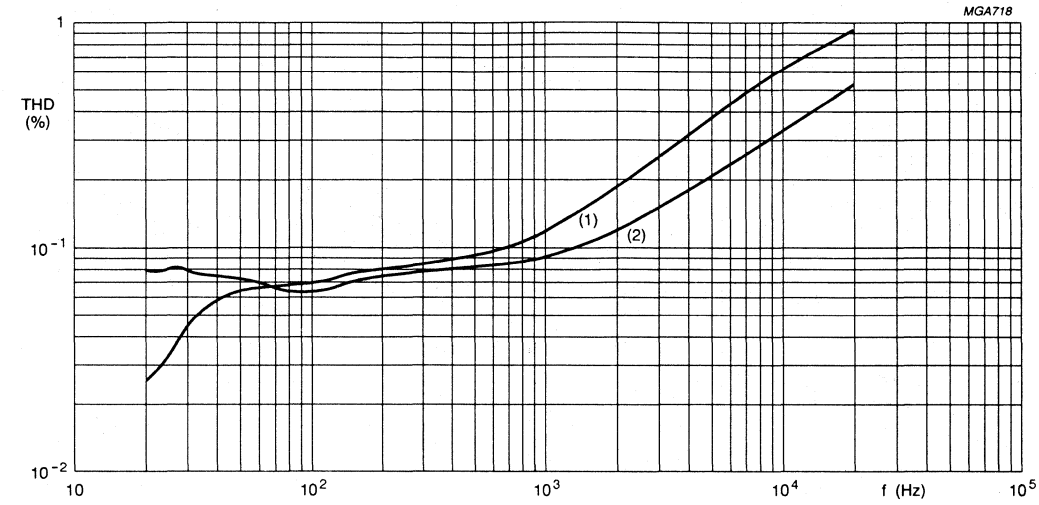


Fig.20 Power bandwidth as a function of frequency; THD = 0.5%, V_P = 14.4 V, R_L = 2 Ω.



(1) P_O = 0.1 W.
(2) P_O = 1 W.

Fig.21 Total harmonic distortion as a function of frequency; V_P = 14.4 V, R_L = 2 Ω.

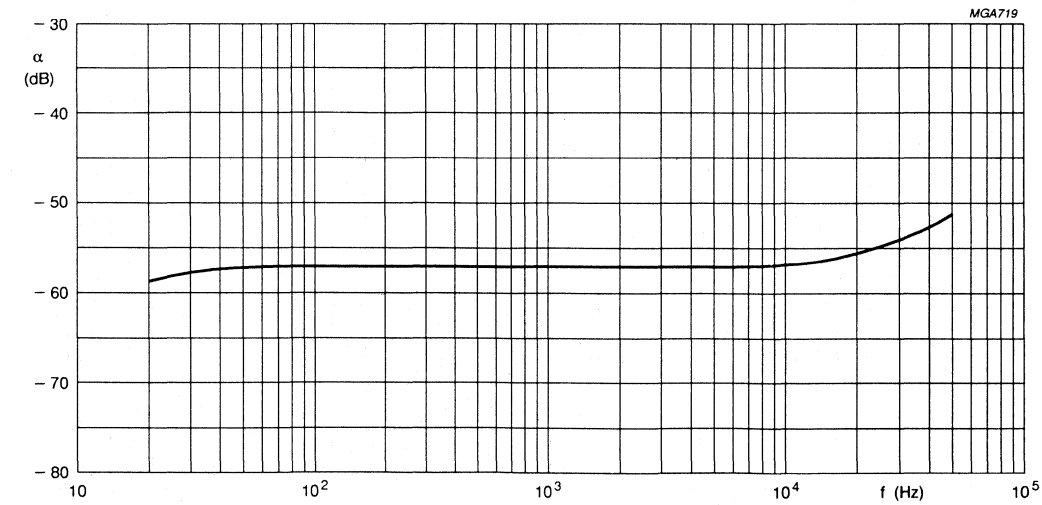


Fig.22 Channel separation as a function of frequency.

BTL APPLICATION

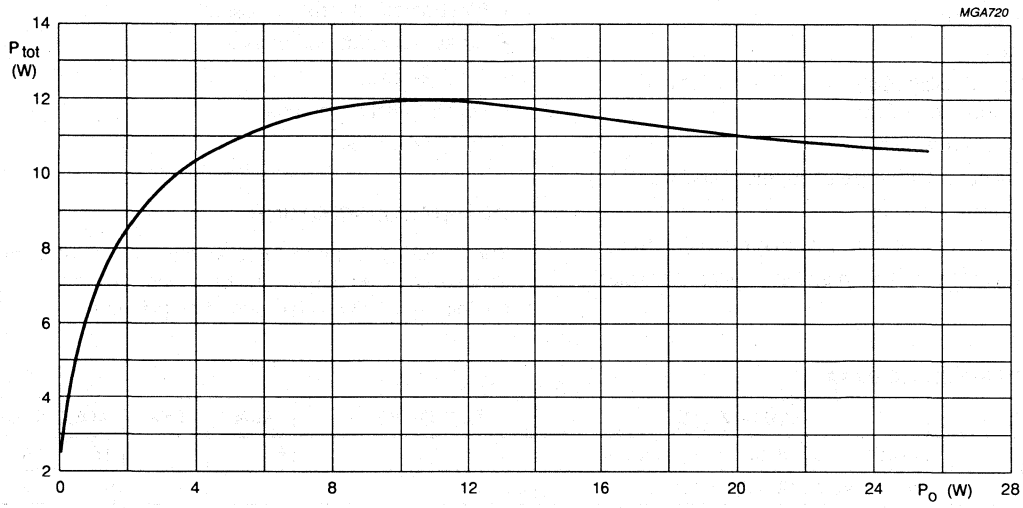


Fig.23 Total power dissipation as a function of output power; V_P = 14.4 V, R_L = 4 Ω (1 channel driven BTL or 4 channels in single-ended mode).

4 x 12 W single-ended car radio power amplifier with dynamic distortion detector and diagnostic interface

TDA8562Q

FEATURES

- Requires very few external components
- High output power
- Fixed gain
- Diagnostic facility (distortion, short-circuit and temperature detection)
- Good ripple rejection
- Mode select switch (operating, mute and stand-by)
- Load dump protection
- AC and DC short-circuit safe to ground and to V_P
- Low power dissipation in any short-circuit condition
- Thermally protected
- Reverse polarity safe
- Electrostatic discharge protection
- No switch-on/switch-off plop
- Flexible leads
- Low thermal resistance
- Identical inputs.

GENERAL DESCRIPTION

The TDA8562Q is an integrated class-B output amplifier in a 17-lead single-in-line (SIL) power package. It contains 4 x 12 W single-ended amplifiers.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	positive operating supply voltage		6	14.4	18	V
I_{ORM}	repetitive peak output current		–	–	4	A
I_P	total quiescent current		–	80	–	mA
I_{sb}	stand-by current		–	0.1	100	μA
P_O	output power	THD = 10%				
		4 Ω	–	7	–	W
		2 Ω	–	12	–	W
RR	supply voltage ripple rejection		48	–	–	dB
V_{no}	noise output voltage	R_s = 0 Ω	–	50	–	μV
$\|Z_i\|$	input impedance		50	–	–	kΩ

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA8562Q	17	DBS	plastic	SOT243R

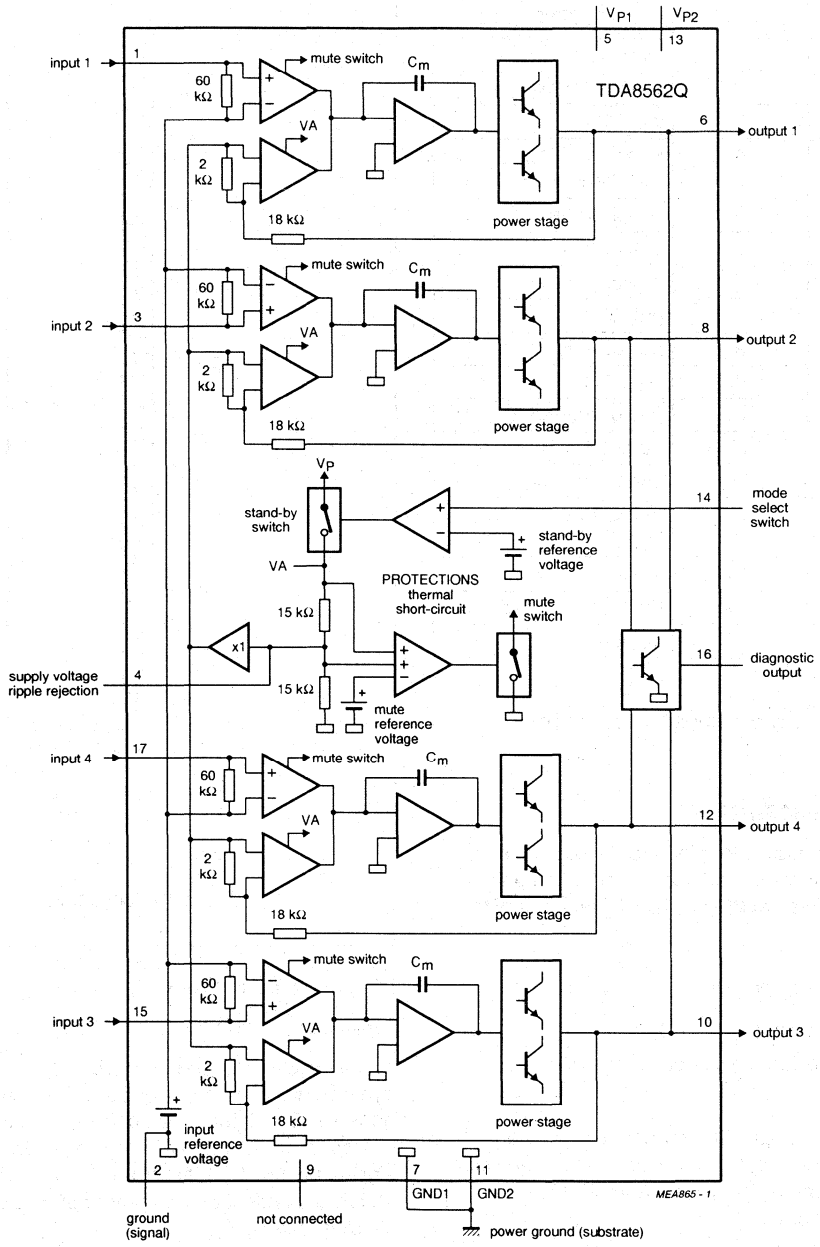


Fig.1 Block diagram.

4 x 12 W single-ended car radio power amplifier with dynamic distortion detector and diagnostic interface

TDA8562Q

PINNING

SYMBOL	PIN	DESCRIPTION
IN 1	1	input 1
GND(S)	2	signal ground
IN 2	3	input 2
RR	4	supply voltage ripple rejection
V_{P1}	5	supply voltage
OUT 1	6	output 1
GND1	7	power ground 1
OUT 2	8	output 2
n.c.	9	not connected
OUT 3	10	output 3
GND2	11	power ground 2
OUT 4	12	output 4
V_{P2}	13	supply voltage
MODE	14	mode select switch input
IN 3	15	input 3
V_{DIAG}	16	diagnostic output
IN 4	17	input 4

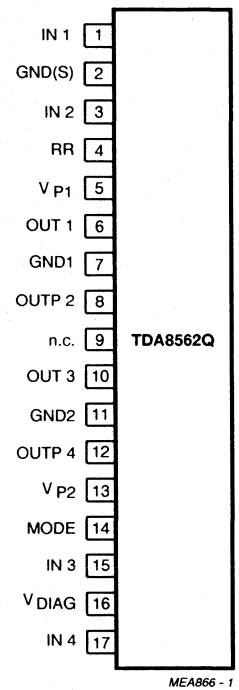


Fig.2 Pin configuration.

The device is primarily developed for car radio applications.

FUNCTIONAL DESCRIPTION

The TDA8562Q contains four identical amplifiers and can be used for single-ended applications. The gain of each amplifier is fixed at 20 dB. Special features of the device are:

Mode select switch (pin 14)

- low stand-by current (< 100 μA)
- low switching current (low cost supply switch)
- mute facility

To avoid switch-on plops, it is advised to keep the amplifier in the mute mode during ≥ 100 ms (charging of the input capacitors at pin 1, 3, 15 and pin 17). This can be achieved by:

- microprocessor control
- external timing circuit (see Fig.7)

Diagnostic output (pin 16)

DYNAMIC DISTORTION DETECTOR (DDD)

At the onset of clipping of one or more output stages, the dynamic distortion detector becomes active and pin 16 goes low. This information can be used to drive a sound processor or DC volume control to attenuate the input signal and thus limit the distortion. The output level of pin 16 is independent of the number of channels that are clipping (see Fig.3).

SHORT-CIRCUIT PROTECTION

When a short-circuit occurs at one or more outputs to ground or to the supply voltage, the output stages are switched off until the short-circuit is removed and the device is switched on again, with a delay of approximately 20 ms, after removal of the short-circuit. During this short-circuit condition, pin 16 is continuously low.

When a short-circuit across the load of one or more channels occurs the output stages are switched off during approximately 20 ms. After that time it is checked during approximately 50 µs to see whether the short-circuit is still present. Due to this duty cycle of 50 µs/20 ms the average current consumption during this short-circuit condition is very low (approximately 40 mA).
During this short-circuit condition, pin 16 is low for 20 ms and high for 50 µs (see Fig.4).

The power dissipation in any short-circuit condition is very low.

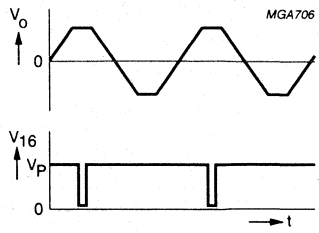


Fig.3 Distortion detector waveform.

TEMPERATURE DETECTION

When the virtual junction temperature T_{vj} reaches 150 °C, pin 16 will be active LOW.

OPEN COLLECTOR OUTPUT

Pin 16 is an open collector output, which allows pin 16 of more devices being tied together.

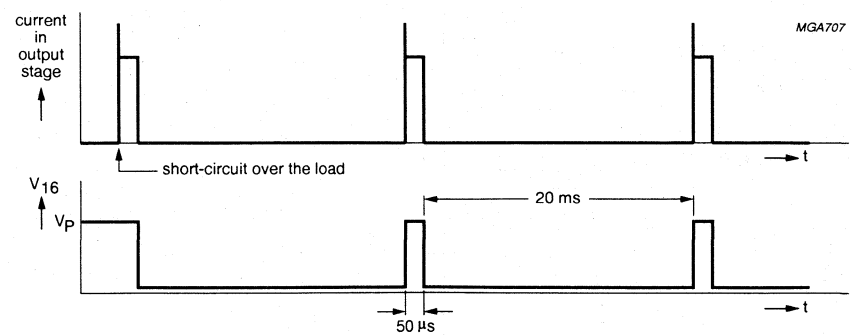


Fig.4 Short-circuit waveform.

LIMITING VALUES

In accordance with the absolute maximum system (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_P	positive supply voltage				
	operating		–	18	V
	non-operating		–	30	V
	load dump protection	during 50 ms; $t_r \geq 2.5$ ms	–	45	V
I_{OSM}	non-repetitive peak output current		–	6	A
I_{ORM}	repetitive peak output current		–	4	A
T_{stg}	storage temperature		–55	+150	°C
T_{amb}	operating ambient temperature		–40	+85	°C
T_{vj}	virtual junction temperature		–	150	°C
V_{psc}	AC and DC short-circuit safe voltage		–	18	V
V_{pr}	reverse polarity		–	6	V
P_{tot}	total power dissipation		–	60	W

THERMAL RESISTANCE

In accordance with IEC 747-1.

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient in free air	40 K/W
$R_{th\ j\text{-}c}$	from junction to case (see Fig.5)	1.3 K/W

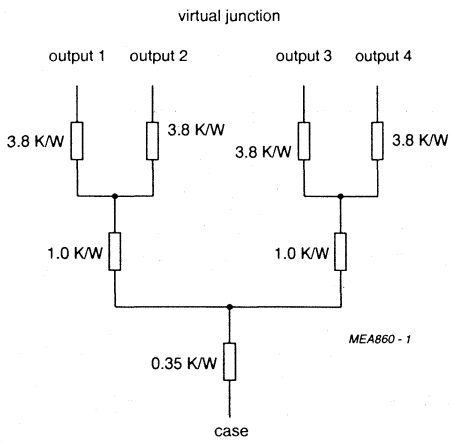


Fig.5 Equivalent thermal resistance network.

DC CHARACTERISTICS

V_P = 14.4 V; T_{amb} = 25 °C; measured in Fig.6; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_P	positive supply voltage	note 1	6	14.4	18	V
I_P	quiescent current		–	80	160	mA
V_O	DC output voltage	note 2	–	6.9	–	V
Mute select switch						
V_{on}	switch-on voltage level		8.5	–	–	V
MUTE CONDITION						
V_{mute}	mute voltage		3.3	–	6.4	V
V_O	output voltage in mute position	V_{Imax} = 1 V; f = 1 kHz	–	–	2	mV
STAND-BY CONDITION						
V_{sb}	stand-by voltage		0	–	2	V
I_{sb}	stand-by current		–	–	100	µA
I_{sw}	switch-on current		–	12	40	µA
Diagnostic output (pin 16)						
V_{DIAG}	diagnostic output voltage	any short-circuit or clipping	–	–	0.6	V

AC CHARACTERISTICS

V_P = 14.4 V; R_L = 4 Ω; f = 1 kHz; T_{amb} = 25 °C; measured in Fig.6; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
P_O	output power	note 3				
		THD = 0.5%	4	5	–	W
		THD = 10%	5.5	7	–	W
THD	total harmonic distortion	P_O = 1 W	–	0.1	–	%
P_O	output power	R_L = 2 Ω; note 3				
		THD = 0.5%	–	10	–	W
		THD = 10%	–	12	–	W
f_l	low frequency roll-off	at −3 dB; note 4	–	45	–	Hz
f_h	high frequency roll-off	at −1 dB	20	–	–	kHz
G_v	closed loop voltage gain		19	20	21	dB
RR	supply voltage ripple rejection	note 5				
	on		48	–	–	dB
	mute		48	–	–	dB
	stand-by		80	–	–	dB
$\|Z_I\|$	input impedance		50	60	75	kΩ
V_{no}	noise output voltage					
	on	R_s = 0 Ω; note 6	–	50	–	μV
	on	R_s = 10 kΩ; note 6	–	70	100	μV
	mute	notes 6 and 7	–	50	–	μV
α	channel separation	R_s = 10 kΩ	40	–	–	dB
$\|\Delta G_v\|$	channel unbalance		–	–	1	dB
Dynamic distortion detector						
THD	total harmonic distortion	$V_{16} \leq 0.6$ V; no short-circuit	–	10	–	%

Notes

1. The circuit is DC adjusted at V_P = 6 to 18 V and AC operating at V_P = 8.5 to 18 V.
2. At 18 V < V_P < 30 V the DC output voltage ≤ $V_P/2$.
3. Output power is measured directly at the output pins of the IC.
4. Frequency response externally fixed.
5. Ripple rejection measured at the output with a source-impedance of 0 Ω, maximum ripple amplitude of 2 V (p-p) and at a frequency of between 100 Hz and 10 kHz.
6. Noise measured in a bandwidth of 20 Hz to 20 kHz.
7. Noise output voltage independent of R_s (V_I = 0 V).

TEST/APPLICATION INFORMATION

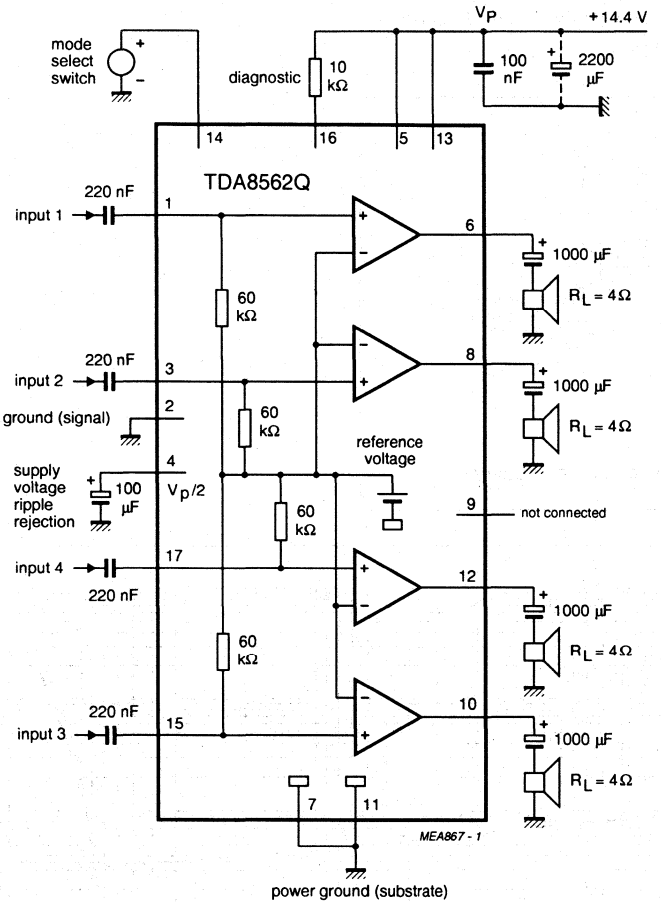


Fig.6 Application diagram.

Mode select switch

To avoid switch-on plops, it is advised to keep the amplifier in the mute mode during > 100 ms (charging of the input capacitors at pins 1, 3, 15 and 17.
The circuit in Fig.7 slowly ramps up the voltage at the mode select switch pin when switching on and results in fast muting when switching off.

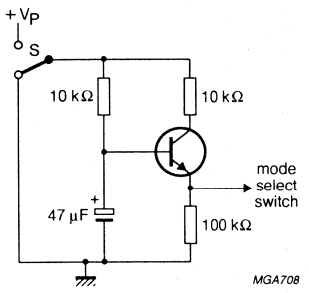
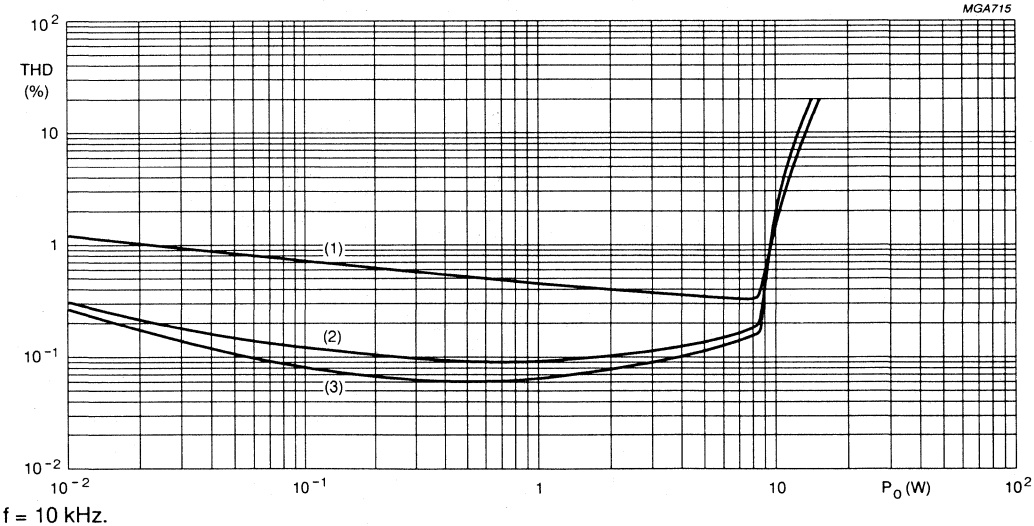
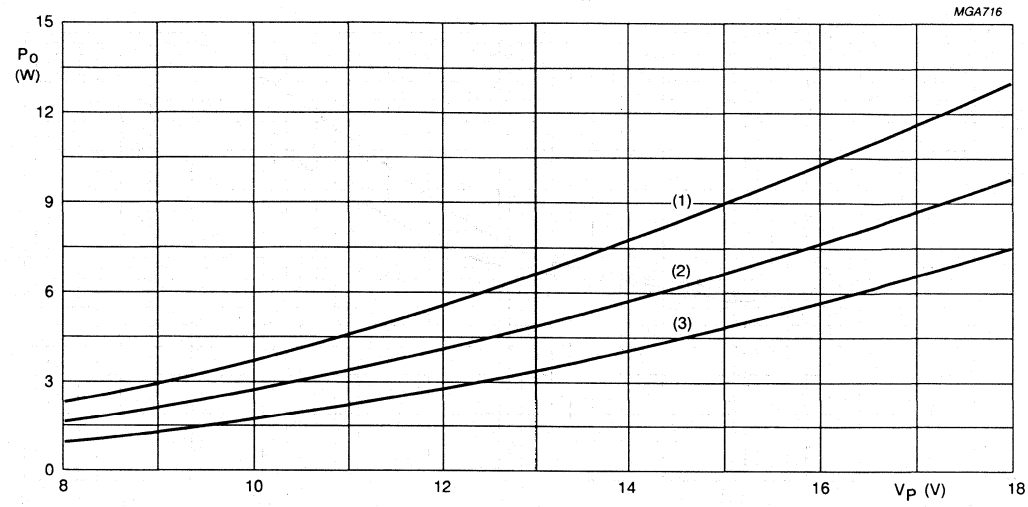


Fig.7 Mode select switch circuitry.



(1) f = 10 kHz.
(2) f = 1 kHz.
(3) f = 100 Hz.

Fig.8 Total harmonic distortion as a function of output power; V_P = 14.4 V, R_L = 2 Ω.



(1) THD = 30%.
(2) THD = 10%.
(3) THD = 0.5%.

Fig.9 Output power as a function of supply voltage.

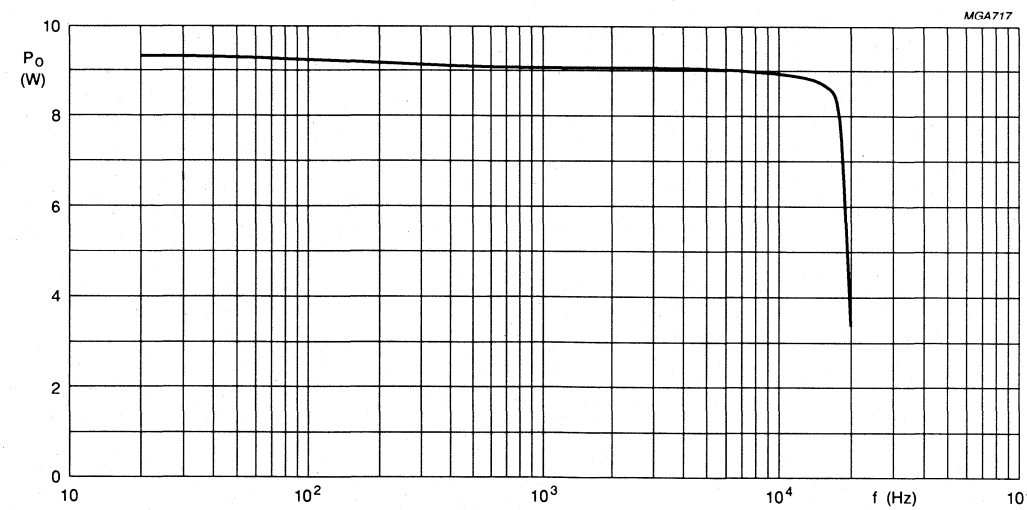
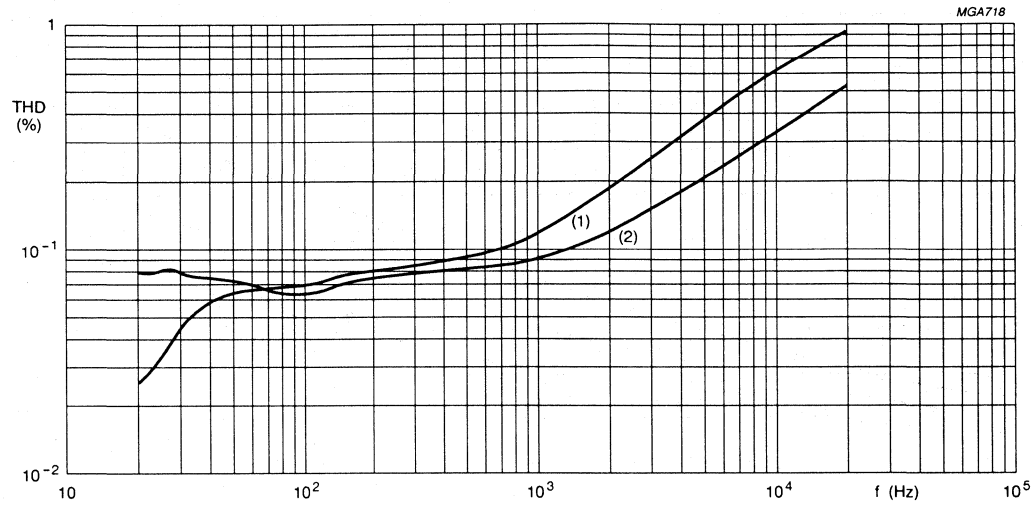
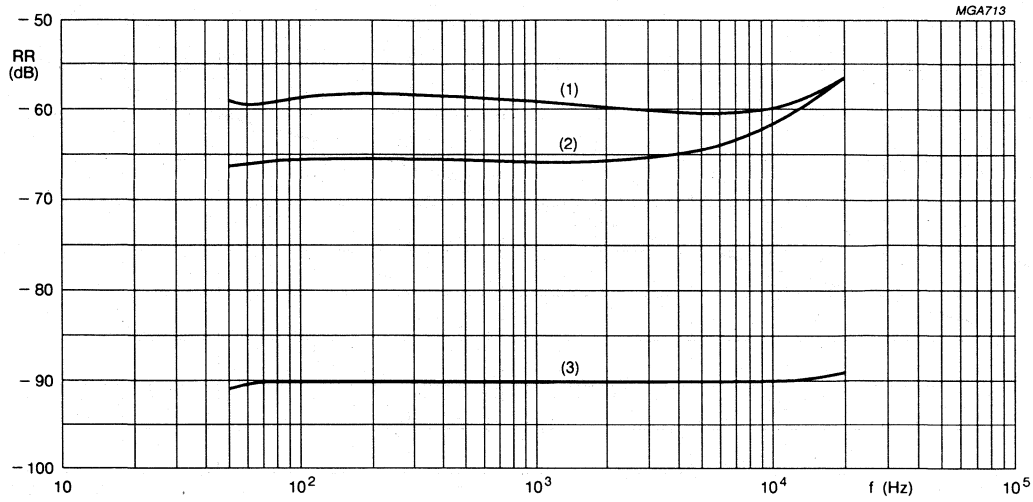


Fig.10 Power bandwidth as a function of frequency; THD = 0.5%, V_P = 14.4 V, R_L = 2 Ω.



(1) P_O = 0.1 W.
(2) P_O = 1 W.

Fig.11 Total harmonic distortion as a function of frequency; V_P = 14.4 V, R_L = 2 Ω.



(1) On condition.
(2) Mute condition.
(3) Stand-by condition.

Fig.12 Ripple rejection as a function of frequency.

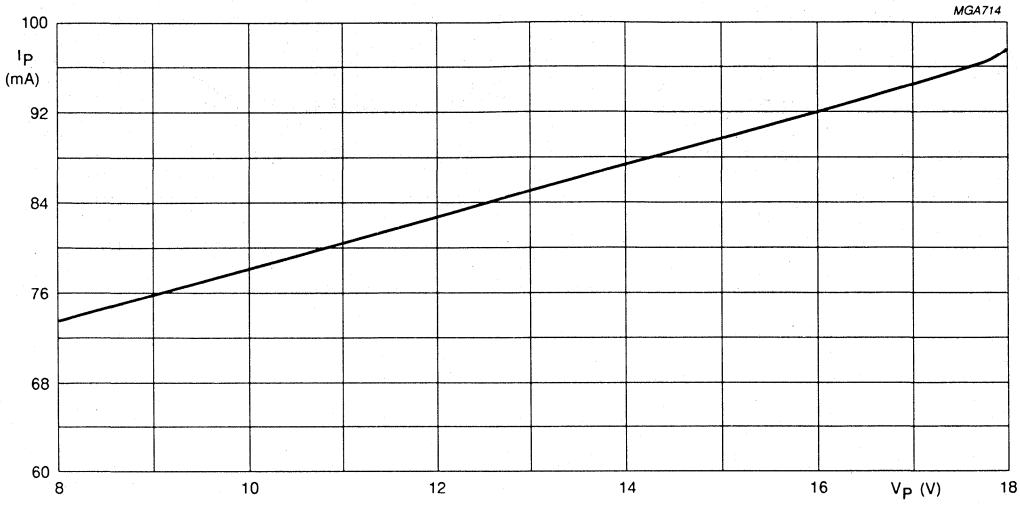


Fig.13 Quiescent current as a function of supply voltage; $R_L = \infty$.

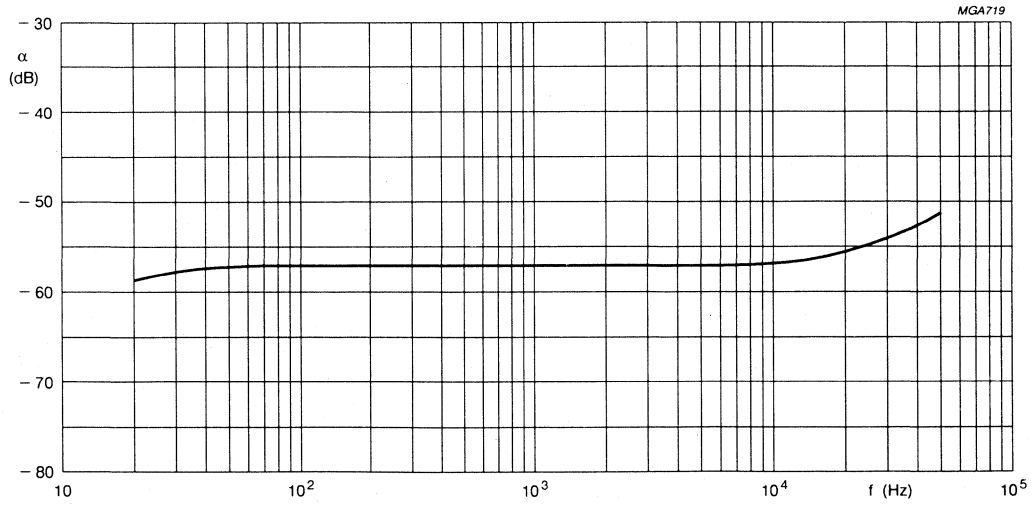


Fig.14 Channel separation as a function of frequency.

2 x 40 W/2 Ω stereo BTL car radio power amplifier with diagnostic facility

TDA8563Q

FEATURES

- Requires very few external components
- High output power
- 4 Ω and 2 Ω load impedance
- Low output offset voltage
- Fixed gain
- Diagnostic facility (distortion, short-circuit and temperature detection)
- Good ripple rejection
- Mode select switch (operating, mute and stand-by)
- Load dump protection
- Short-circuit safe to ground, to V_P and across the load
- Low power dissipation in any short-circuit condition
- Thermally protected
- Reverse polarity safe
- Electrostatic discharge protection
- No switch-on/switch-off plop
- Flexible leads
- Low thermal resistance.

GENERAL DESCRIPTION

The TDA8563Q is an integrated class-B output amplifier in a 13-lead single-in-line (SIL) power package. It contains 2 × 40 W/2 Ω amplifiers in BTL configuration.

The device is primarily developed for car radio applications.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	operating supply voltage		6.0	14.4	18	V
I_{ORM}	repetitive peak output current		–	–	7.5	A
$I_{q(tot)}$	total quiescent current		–	115	–	mA
I_{sb}	stand-by current		–	0.1	100	μA
I_{sw}	switch-on current		–	–	40	μA
$\|Z_I\|$	input impedance		25	30	–	kΩ
P_o	output power	R_L = 4 Ω; THD = 10%	–	25	–	W
		R_L = 2 Ω; THD = 10%	–	40	–	W
SVRR	supply voltage ripple rejection	R_s = 0 Ω	–	60	–	dB
α_{cs}	channel separation	R_s = 10 kΩ	–	50	–	dB
G_v	closed loop voltage gain		25	26	27	dB
V_{no}	noise output voltage	R_s = 0 Ω	–	–	120	μV
$\|\Delta V_O\|$	DC output offset voltage		–	–	150	mV

ORDERING INFORMATION

TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA8563Q	13	DBS	plastic	SOT141R

2 x 40 W/2 Ω stereo BTL car radio power amplifier with diagnostic facility

TDA8563Q

BLOCK DIAGRAM

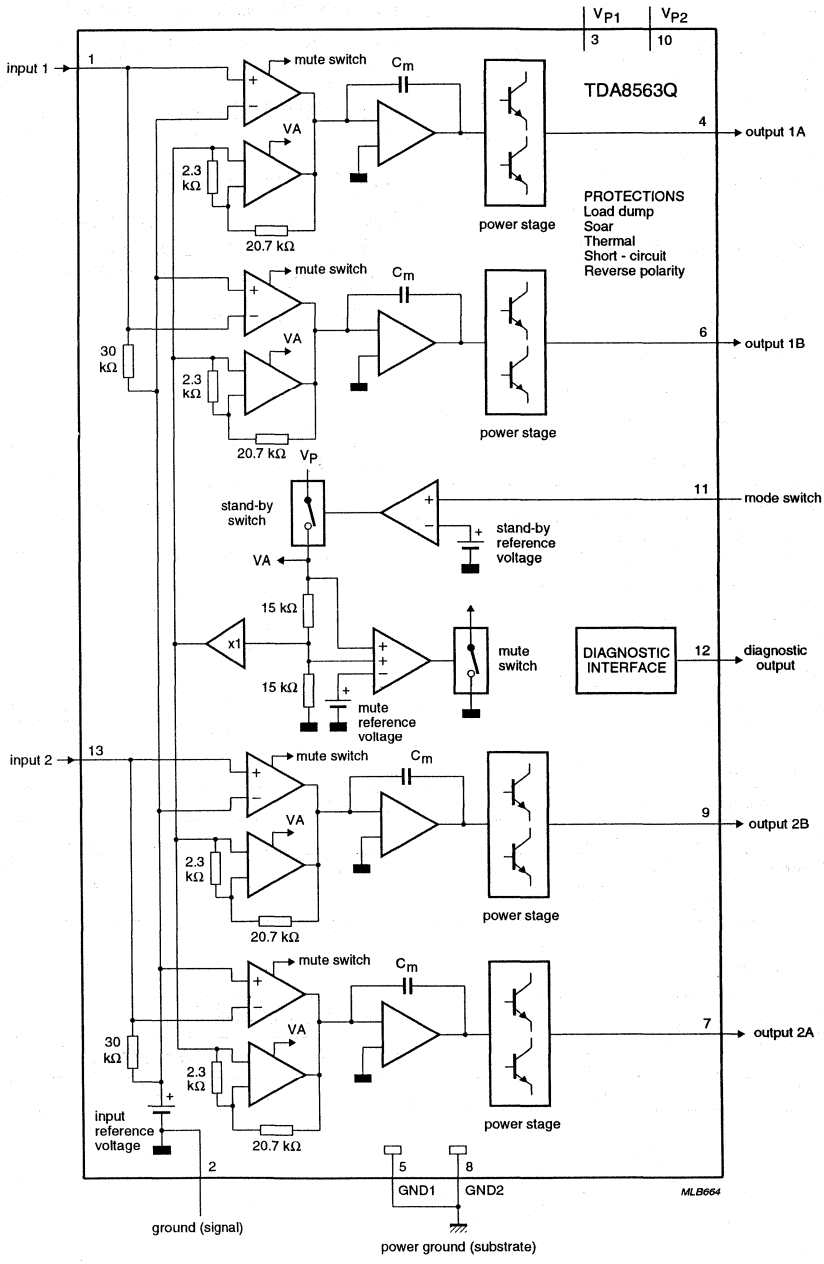


Fig.1 Block diagram.

2 x 40 W/2 Ω stereo BTL car radio power amplifier with diagnostic facility

TDA8563Q

PINNING

SYMBOL	PIN	DESCRIPTION
IN 1	1	input 1
GND(S)	2	signal ground
V_{P1}	3	supply voltage 1
OUT 1A	4	output 1A
GND1	5	power ground 1
OUT 1B	6	output 1B
OUT 2A	7	output 2A
GND2	8	power ground 2
OUT 2B	9	output 2B
V_{P2}	10	supply voltage 2
MODE	11	mode switch input
V_{DIAG}	12	diagnostic output
IN 2	13	input 2

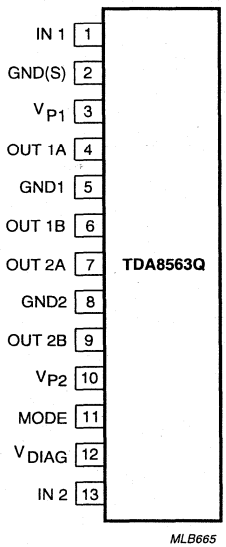


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The TDA8563Q contains two identical amplifiers and can be used for bridge applications. The gain of each amplifier is fixed at 26 dB. Special features of the device are as follows.

Mode select switch (pin 11)

- Stand-by: low supply current (<100 μA)
- Mute: input signal suppressed
- Operating: normal on condition.

Since this pin has a very low input current (<40 μA), a low cost supply switch can be applied.

To avoid switch-on plops, it is advised to keep the amplifier in the mute mode during ≥100 ms (charging of the input capacitors at pin 1 and pin 13).

This can be achieved by:

- Microprocessor control
- External timing circuit (see Fig.7).

Diagnostic output (pin 12)

DYNAMIC DISTORTION DETECTOR (DDD)

At the onset of clipping of one or more output stages, the dynamic distortion detector becomes active and pin 12 goes low. This information can be used to drive a sound processor or DC volume control to attenuate the input signal and thus limit the distortion. The output level of pin 12 is independent of the number of channels that are clipping (see Fig.3).

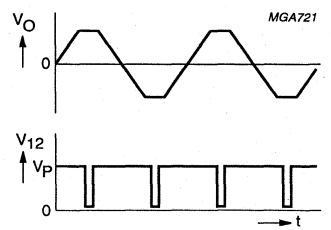


Fig.3 Distortion detector waveform.

SHORT-CIRCUIT PROTECTION

When a short-circuit occurs at one or more outputs to ground or to the supply voltage, the output stages are switched off until the short-circuit is removed and the device is switched on again, with a delay of approximately 20 ms, after removal of the short-circuit. During this short-circuit condition, pin 12 is continuously low.

When a short-circuit across the load of one or both channels occurs the output stages are switched off during approximately 20 ms. After that time it is checked during approximately 50 µs to see whether the short-circuit is still present. Due to this duty cycle of 50 µs/20 ms the average current consumption during this short-circuit condition is very low (approximately 40 mA).

During this short-circuit condition, pin 12 is low for 20 ms and high for 50 µs (see Fig. 4).

The power dissipation in any short-circuit condition is very low.

TEMPERATURE DETECTION

When the virtual junction temperature T_{vj} reaches 150 °C, pin 12 will become continuously low.

OPEN COLLECTOR OUTPUT

Pin 12 is an open collector output, which allows pin 12 of more devices being tied together.

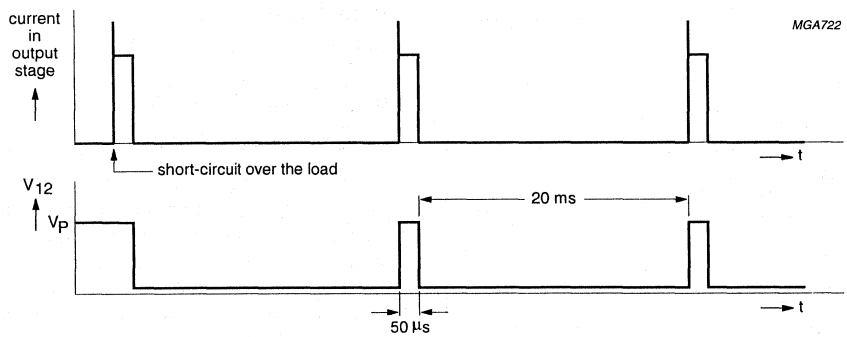


Fig.4 Short-circuit waveform.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_P	supply voltage				
	operating		–	18	V
	non-operating		–	30	V
	load dump protection	during 50 ms; $t_r \geq 2.5$ ms	–	45	V
V_{psc}	AC and DC short-circuit safe voltage		–	18	V
V_{pr}	reverse polarity		–	6	V
I_{OSM}	non-repetitive peak output current		–	10	A
I_{ORM}	repetitive peak output current		–	7.5	A
P_{tot}	total power dissipation		–	60	W
T_{stg}	storage temperature		–55	+150	°C
T_{amb}	operating ambient temperature		–40	+85	°C
T_{vj}	virtual junction temperature		–	150	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air	40 K/W
$R_{th\ j\text{-}c}$	thermal resistance from junction to case (see Fig.5)	1.3 K/W

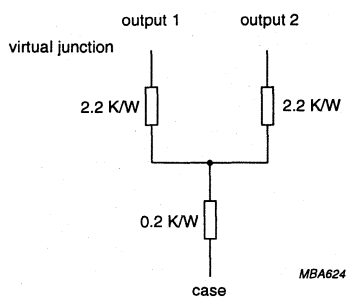


Fig.5 Equivalent thermal resistance network.

DC CHARACTERISTICS

V_P = 14.4 V; T_{amb} = 25 °C; measured in Fig.6; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_P	supply voltage	note 1	6.0	14.4	18	V
I_q	quiescent current	$R_L = \infty$	–	115	180	mA
Operating condition						
V_{11}	mode switch voltage level		8.5	–	V_P	V
I_{11}	mode switch current	V_{11} = 14.4 V	–	15	40	μA
V_O	DC output voltage	note 2	–	7.0	–	V
$\lvert\Delta V_O\rvert$	DC output offset voltage		–	–	150	mV
Mute condition						
V_{11}	mode switch voltage level		3.3	–	6.4	V
V_O	DC output voltage	note 2	–	7.0	–	V
$\lvert\Delta V_O\rvert$	DC output offset voltage		–	–	150	mV
Stand-by condition						
V_{11}	mode switch voltage level		0	–	2	V
I_{sb}	stand-by current		–	0.1	100	μA
Diagnostic output						
V_{12}	diagnostic output voltage	any short-circuit or clipping	–	–	0.6	V

Notes

1. The circuit is DC adjusted at V_P = 6 to 18 V and AC operating at V_P = 8.5 to 18 V.
2. At 18 V < V_P < 30 V the DC output voltage $\leq \frac{1}{2}V_P$.

AC CHARACTERISTICS

V_P = 14.4 V; R_L = 2 Ω; f = 1 kHz; T_{amb} = 25 °C; measured in Fig.6; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
P_o	output power	THD = 0.5%	25	30	–	W
		THD = 10%	33	40	–	W
		THD = 30%	45	55	–	W
P_o	output power	THD = 0.5%; V_P = 13.2 V	–	25	–	W
		THD = 10%; V_P = 13.2 V	–	35	–	W
THD	total harmonic distortion	P_o = 1 W	–	0.1	–	%
		$V_{12} \leq$ 0.6 V; note 1	–	10	–	%
B	power bandwidth	THD = 0.5%; P_o = −1 dB with respect to 25 W	–	20 to 20000	–	Hz
f_{lr}	low frequency roll-off	at −1 dB; note 2	–	25	–	Hz
f_{hr}	high frequency roll-off	at −1 dB	20	–	–	kHz
G_v	closed loop voltage gain		25	26	27	dB
SVRR	supply voltage ripple rejection					
	on	note 3	50	–	–	dB
	mute	note 3	50	–	–	dB
	stand-by	note 3	80	–	–	dB
$\|Z_i\|$	input impedance		25	30	38	kΩ
V_{no}	noise output voltage					
	on	note 4	–	85	120	μV
	on	note 5	–	100	–	μV
	mute	note 6	–	60	–	μV
α_{cs}	channel separation	note 7	45	–	–	dB
$\|\Delta G_v\|$	channel unbalance		–	–	1	dB
V_o	output voltage in mute	note 8	–	–	2	mV

Notes

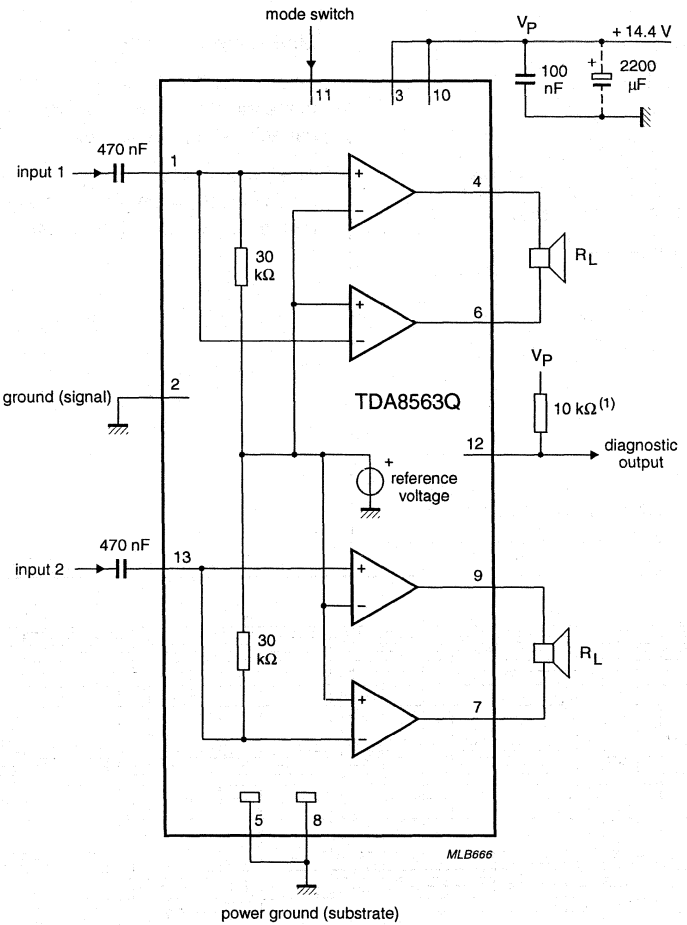
1. Dynamic distortion detector active.
2. Frequency response externally fixed.
3. $V_{ripple} = V_{ripple(max)}$ = 2 V (p-p); R_s = 0 Ω.
4. B = 20 Hz to 20 kHz; R_s = 0 Ω.
5. B = 20 Hz to 20 kHz; R_s = 10 kΩ.
6. B = 20 Hz to 20 kHz; independent of R_s.
7. P_o = 25 W; R_s = 10 kΩ.
8. $V_i = V_{i(max)}$ = 1 V (RMS).

AC CHARACTERISTICS

V_P = 14.4 V; R_L = 4 Ω; f = 1 kHz; T_{amb} = 25 °C; measured in Fig.6; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
P_o	output power	THD = 0.5%	16	19	–	W
		THD = 10%	21	25	–	W
		THD = 30%	28	35	–	W
P_o	output power	THD = 0.5%; V_P = 13.2 V	–	15	–	W
		THD = 10%; V_P = 13.2 V	–	21	–	W
THD	total harmonic distortion	P_o = 1 W	–	0.1	–	%

TEST/APPLICATION INFORMATION



(1) To avoid high energy switching pulses which can feedback to the inputs it is advisable to ensure that the value of the resistor at pin 12 is ≥10 kΩ.

Fig.6 Stereo BTL test/application diagram.

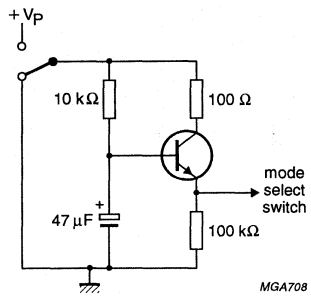


Fig.7 Mode select switch circuitry.

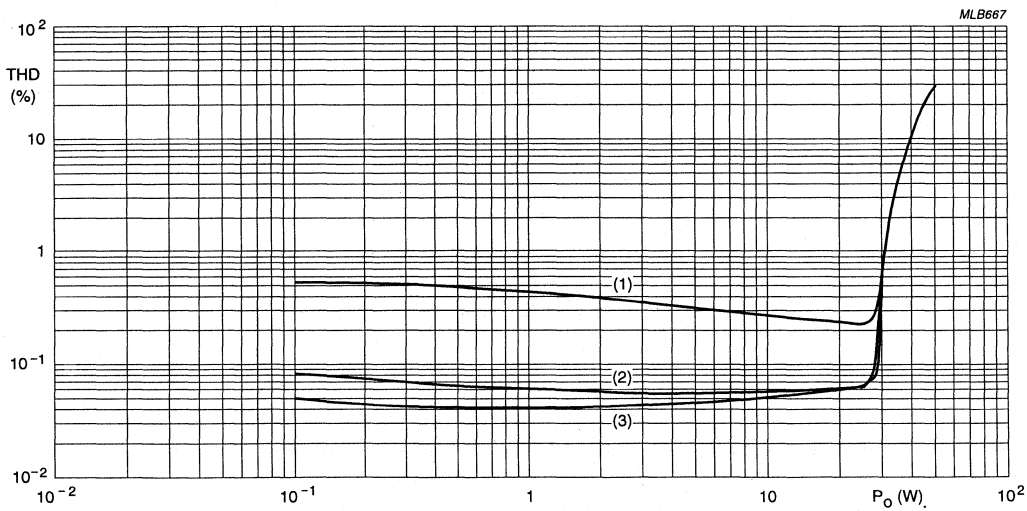
Diagnostic output

Special care must be taken in the printed-circuit board layout to separate pin 12 from pin 1 and pin 13, to minimize the crosstalk between the diagnostic output and the inputs.

Mode select switch

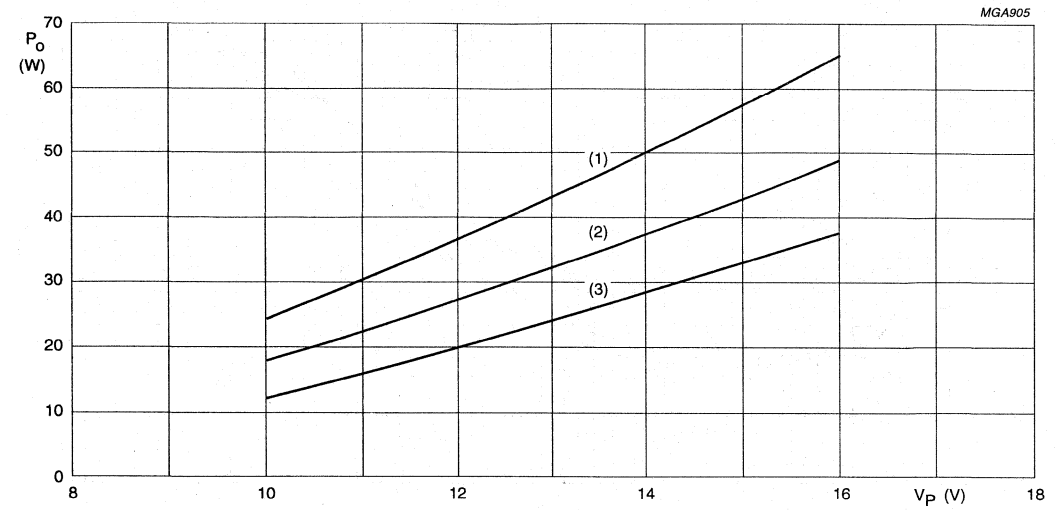
To avoid switch-on plops, it is advised to keep the amplifier in the mute mode during >100 ms (charging of the input capacitors at pin 1 and pin 13).

The circuit in Fig.7 slowly ramps up the voltage at the mode select switch pin when switching on and results in fast muting when switching off.



(1) f = 10 kHz.
(2) f = 1 Hz.
(3) f = 100 Hz.

Fig.8 Total harmonic distortion as a function of output power; V_P = 14.4 V; R_L = 2 Ω.



(1) THD = 30%.
(2) THD = 10%.
(3) THD = 0.5%.

Fig.9 Output power as a function of supply voltage; f = 1 kHz; R_L = 2 Ω.

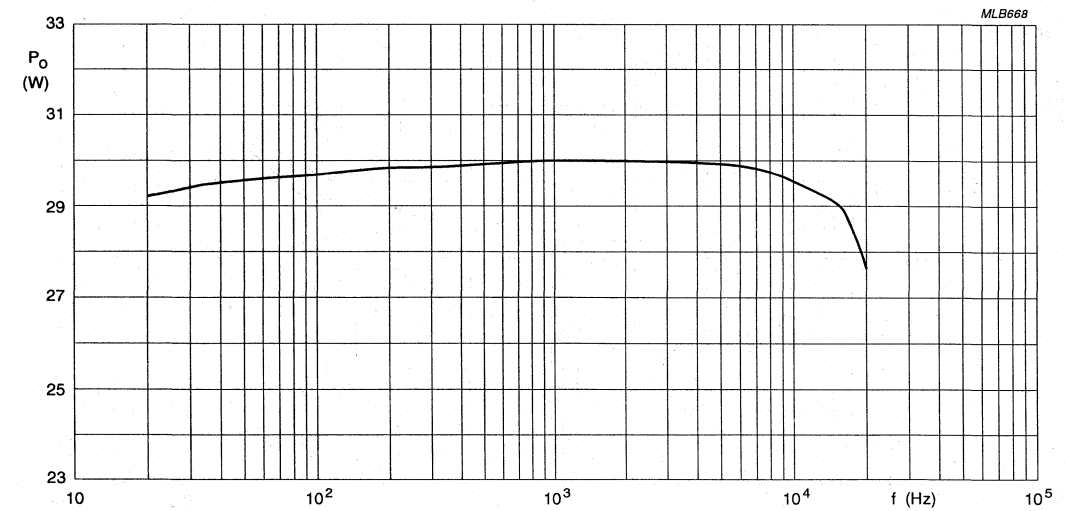
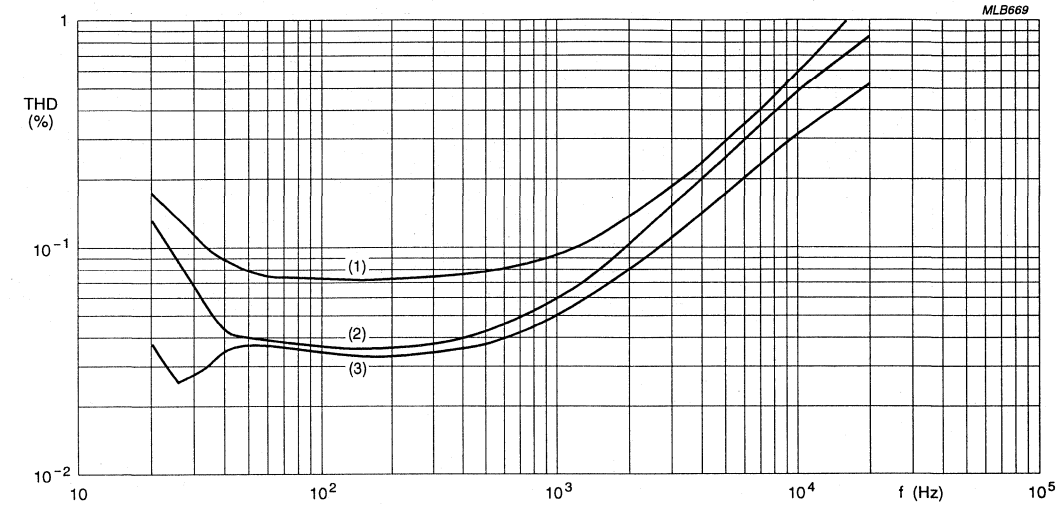
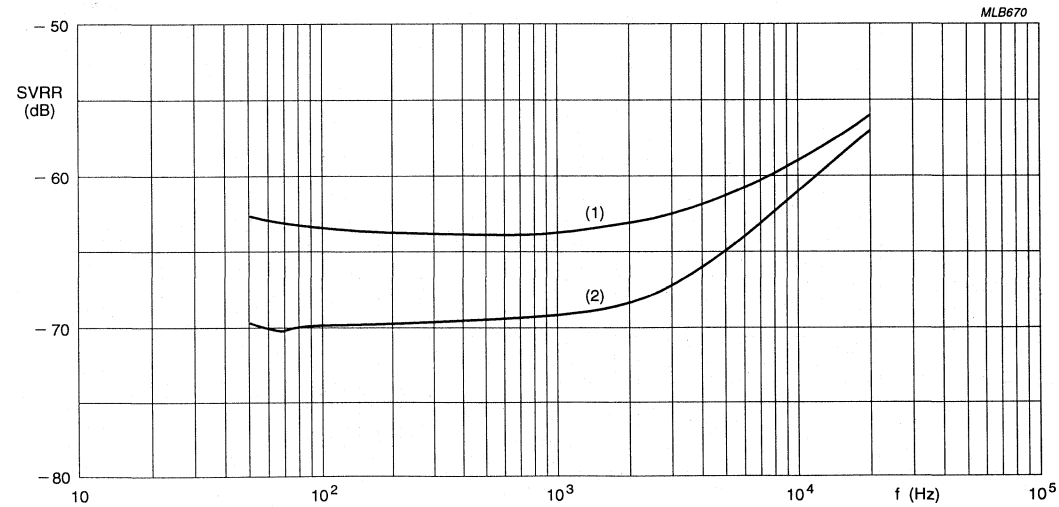


Fig.10 Output power as a function of frequency; THD = 0.5%; V_P = 14.4 V; R_L = 2 Ω.



(1) P_o = 0.1 W.
(2) P_o = 1 W.
(3) P_o = 10 W.

Fig.11 Total harmonic distortion as a function of frequency; V_P = 14.4 V; R_L = 2 Ω.



(1) On condition.
(2) Mute condition.

Fig.12 Ripple rejection as a function of frequency; V_P = 14.4 V; V_{ripple} = 2 V (p-p); R_s = 0 Ω.

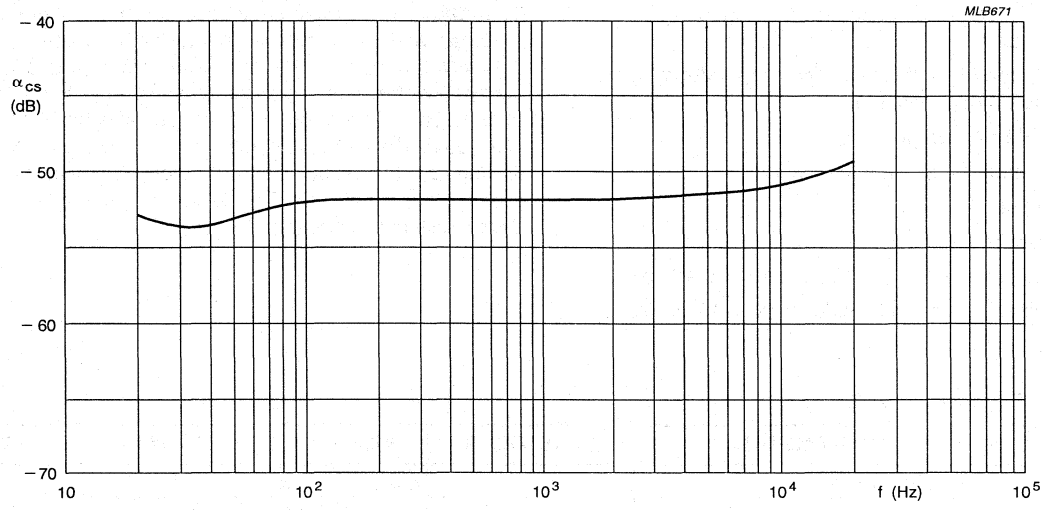


Fig.13 Channel separation as a function of frequency; V_P = 14.4 V; P_o = 25 W; R_L = 2 Ω; R_s = 10 kΩ.

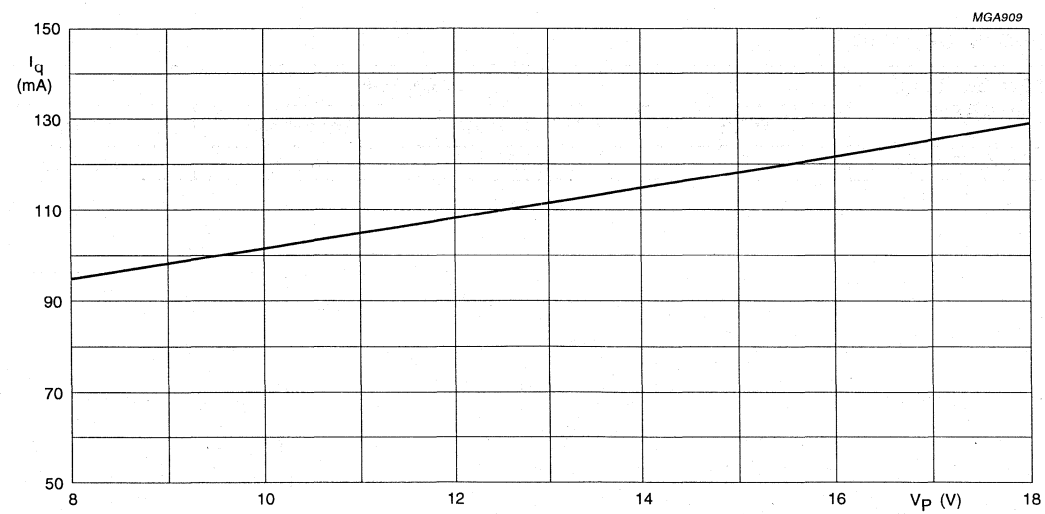


Fig.14 Quiescent current as a function of supply voltage; $R_L = \infty$.

Dual common-mode rejection differential line receiver

TDA8577

FEATURES

- Excellent common-mode rejection, up to high frequencies
- Elimination of source resistance dependency in the common-mode rejection
- Few external components
- High supply voltage ripple rejection
- Low noise
- Low distortion
- All pins protected against electrostatic discharge
- AC and DC short-circuit safe to ground and V_{CC}
- Fast DC settling.

GENERAL DESCRIPTION

The TDA8577 is a two channel differential amplifier with 0 dB gain and low distortion. The device has been primarily developed for car radio applications where long connections between signal sources and amplifiers (or boosters) are necessary and where ground noise has to be eliminated. The device is intended to be used to receive line inputs in audio applications that require a high level of common-mode rejection. The device is contained in a 9-pin single in-line package.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage		5.0	8.5	18	V
I_{CC}	supply current	V_{CC} = 8.5	–	11	14	mA
G_v	voltage gain		–0.5	0	+0.5	dB
SVRR	supply voltage ripple rejection		55	60	–	dB
V_{no}	noise output voltage		–	3.7	5.0	μV
$\|Z_i\|$	input impedance		100	240	–	kΩ
CMRR	common-mode rejection ratio	R_s = 0 Ω	–	80	–	dB

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA8577	9	SIL9	plastic	SOT142

Dual common-mode rejection differential line receiver

TDA8577

BLOCK DIAGRAM

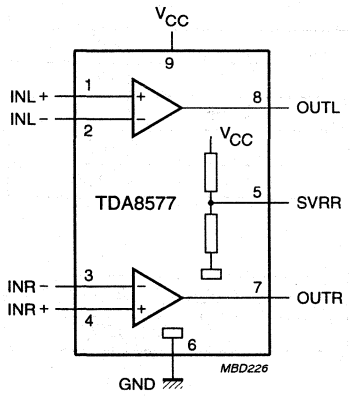


Fig.1 Block diagram.

FUNCTIONAL DESCRIPTION

The TDA8577 contains two identical differential amplifiers with a voltage gain of 0 dB. The device is intended to receive line input signals for audio applications. The TDA8577 has a very high level of common-mode rejection and thus eliminates ground noise. The common-mode rejection remains constant up to high frequencies (the amplifier gain is fixed at 0 dB). The inputs have a high input impedance. The output stage is a class AB stage with a low output impedance. For a large common-mode rejection, also at low frequencies, an electrolytic capacitor connected to the negative input is advised. Because the input impedance is relatively high, this results in a large settling time of the DC input voltage. Therefore a quick-charge circuit is included to charge the input capacitor within 0.2 seconds.

PINNING

SYMBOL	PIN	DESCRIPTION
INL+	1	positive input left
INL−	2	negative input left
INR−	3	negative input right
INR+	4	positive input right
SVRR	5	half supply voltage
GND	6	ground
OUTR	7	output right
OUTL	8	output left
V_{CC}	9	supply voltage

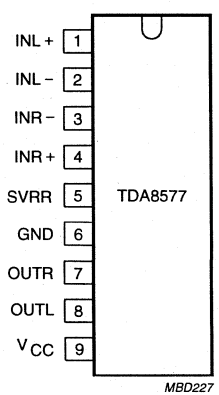


Fig.2 Pin configuration.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	supply voltage	operating	–	18	V
I_{ORM}	repetitive peak output current		–	40	mA
V_{sc}	AC and DC short-circuit safe voltage		–	18	V
T_{stg}	storage temperature		–55	+150	°C
T_{amb}	operating ambient temperature		–40	+85	°C
T_j	maximum junction temperature		–	+150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient in free air	80 K/W

CHARACTERISTICS

V_{CC} = 8.5 V; T_{amb} = 25 °C; f = 1 kHz; measured in test circuit of Fig.3; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage		5.0	8.5	18	V
I_{CC}	supply current		–	11	14	mA
V_O	DC output voltage	note 1	–	4.3	–	V
t_{set}	DC input voltage settling time		–	0.2	–	s
G_v	voltage gain		–0.5	0	+0.5	dB
α_{cs}	channel separation	R_s = 5 kΩ	70	80	–	dB
$\lvert\Delta G_v\rvert$	channel unbalance		–	–	0.5	dB
f_L	low frequency roll-off	–1 dB; note 2	20	–	–	Hz
f_H	high frequency roll-off	–1 dB	20	–	–	kHz
$\lvert Z_i\rvert$	input impedance		100	240	–	kΩ
$\lvert Z_o\rvert$	output impedance		–	–	10	Ω
$V_{i(max)}$	maximum input voltage	THD = 1%	–	2	–	V
V_{no}	noise output voltage	R_s = 0 Ω; note 3	–	3.7	5.0	μV
$V_{CM(rms)}$	common-mode input voltage (RMS value)		–	–	1	V
CMRR	common-mode rejection ratio	R_s = 5 kΩ	66	70	–	dB
		R_s = 0 Ω; note 4	–	80	–	dB
SVRR	supply voltage ripple rejection	note 5	55	65	–	dB
		note 6	–	60	–	dB
THD	total harmonic distortion	V_i = 1 V;	–	0.02	–	%
		V_i = 1 V; f = 20 Hz to 20 kHz	–	–	0.1	%
THD_{max}	total harmonic distortion at maximum output current	V_i = 1 V; R_L = 150 Ω	–	–	1	%

Notes

1. The DC output voltage with respect to ground is approximately $0.5V_{CC}$.
2. The frequency response is externally fixed by the input coupling capacitors.
3. The noise output voltage is measured in a bandwidth of 20 Hz to 20 kHz (unweighted).
4. The common-mode rejection ratio is measured at the output with a voltage source of 1 V (RMS) in accordance with the test circuit (see Fig.3) while V_{INL} and V_{INR} are shorted-circuited. Frequencies between 100 Hz and 100 kHz.
5. The ripple rejection is measured at the output, with R_s = 2 kΩ, f = 1 kHz and a ripple amplitude of 2 V (p-p).
6. The ripple rejection is measured at the output, with R_s = 0 to 2 kΩ, f = 100 Hz to 20 kHz and a maximum ripple amplitude of 2 V (p-p).

Dual common-mode rejection differential line receiver

TDA8577

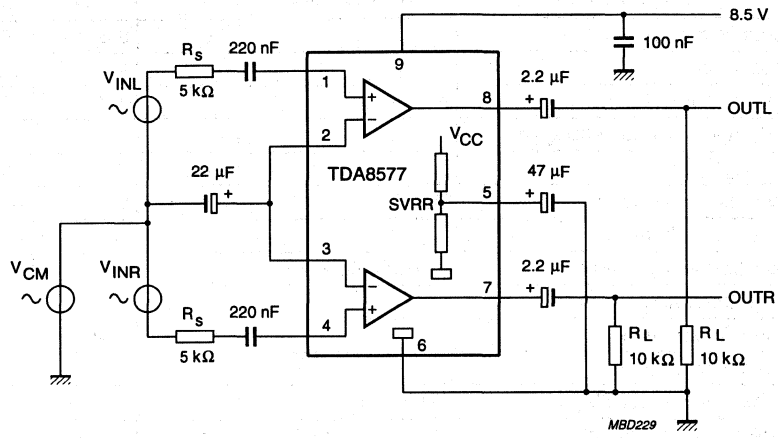


Fig.3 Test circuit.

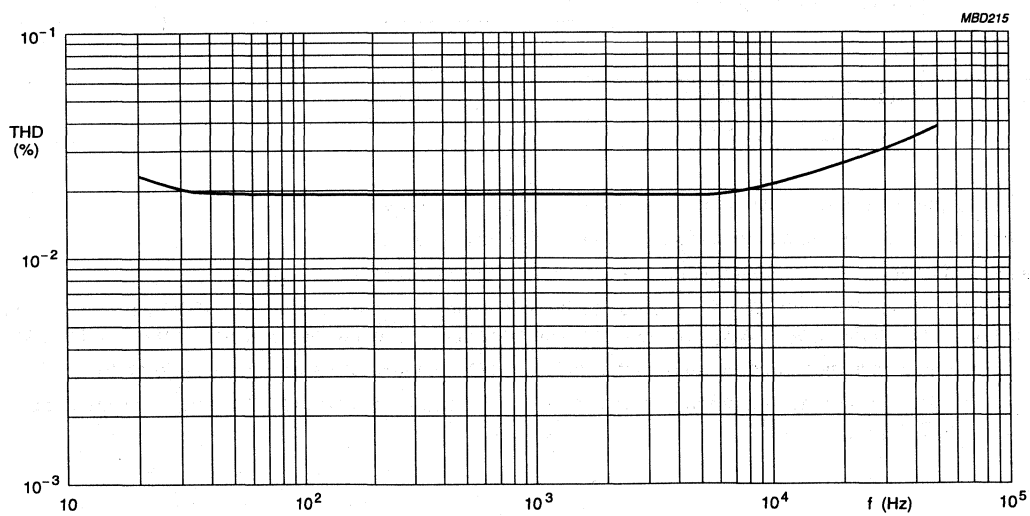
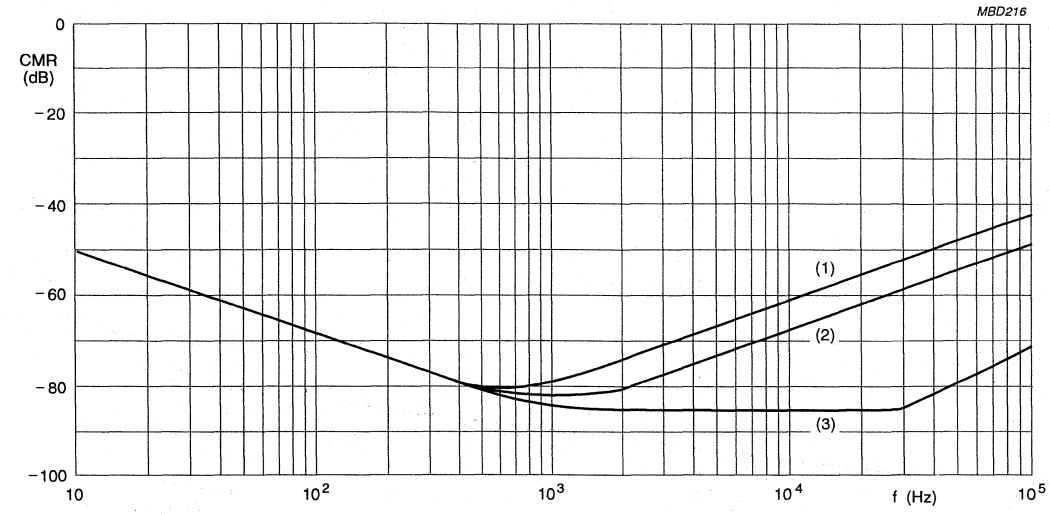


Fig.4 Total harmonic distortion as a function of frequency; V_i = 1V (RMS).



(1) R_s = 5 kΩ
(2) R_s = 2 kΩ
(3) R_s = 0 kΩ

Fig.5 Common-mode rejection ratio as a function of frequency; V_{CM} = 1 V (RMS).

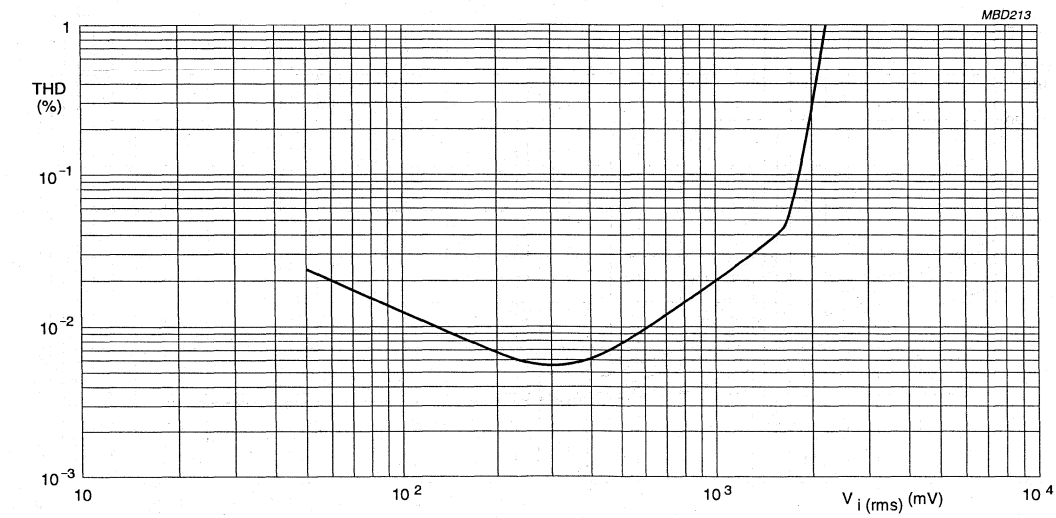


Fig.6 Total harmonic distortion as a function of input voltage; f = 1 kHz.

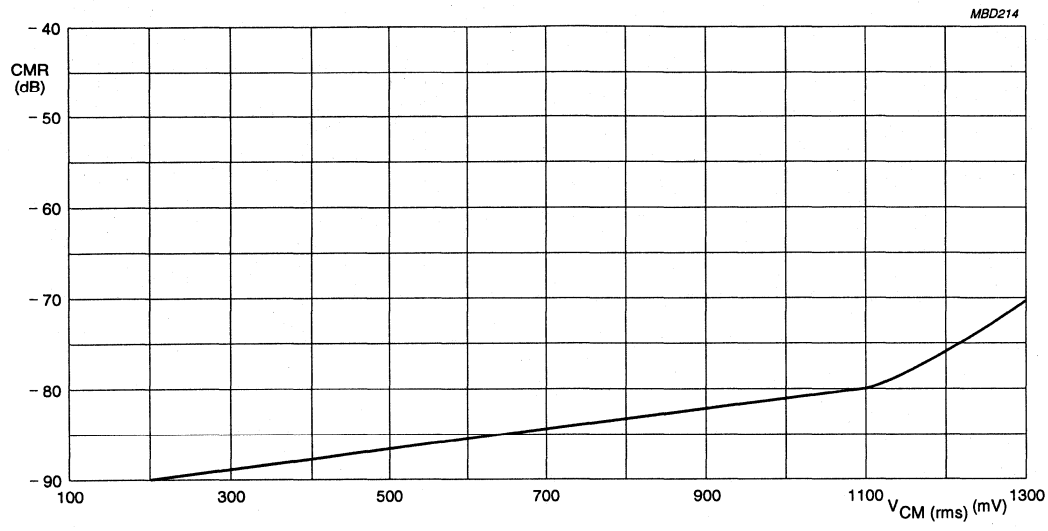
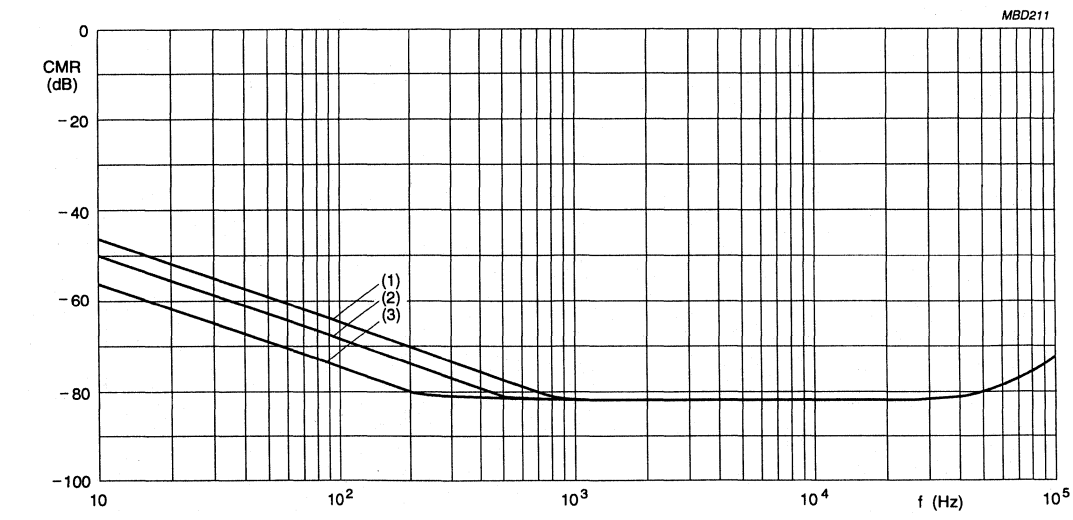


Fig.7 Common-mode rejection ratio as a function of common-mode input voltage; f = 1 kHz (R_s = 0 Ω).



(1) C2 = 22 μF
(2) C2 = 47 μF
(3) C2 = 100 μF

Fig.8 Common-mode rejection ratio as a function of frequency; V_{CM} = 1 V (RMS).

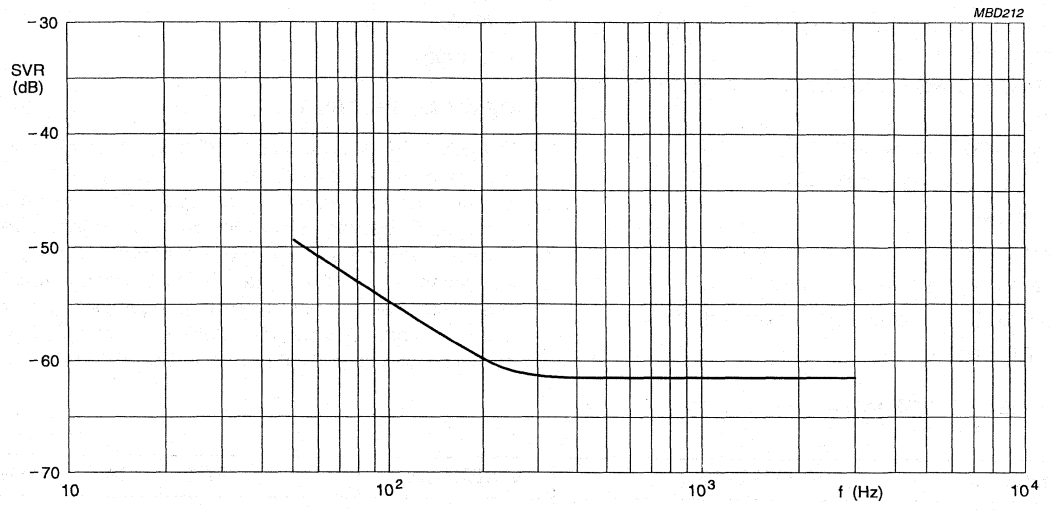


Fig.9 Supply voltage ripple rejection as a function of frequency; V_{ripple} = 2 V (p-p), R_s = 2 kΩ.

APPLICATION INFORMATION

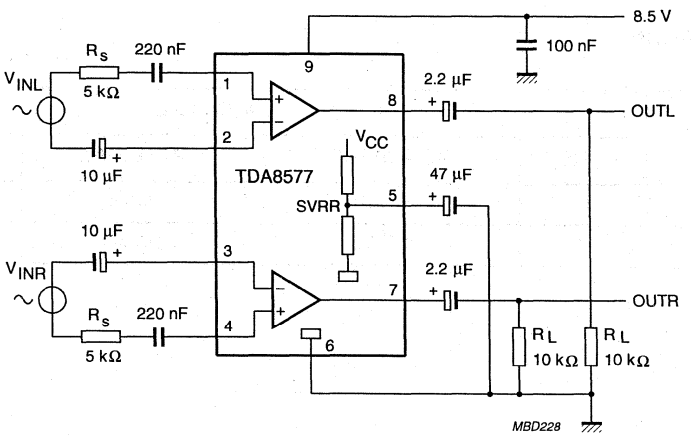


Fig.10 Application circuit with balanced signal source

Dual common-mode rejection differential line receiver

TDA8578

FEATURES

- Excellent common-mode rejection up to high frequencies
- Elimination of source resistance in the common-mode rejection
- Few external components
- High supply voltage ripple rejection
- Low noise
- Low distortion
- Protected against electrostatic discharge
- AC and DC short circuit safe to ground and V_{CC}
- Fast DC settling.

APPLICATIONS

- Audio
- Car radio.

GENERAL DESCRIPTION

The TDA8578 is a two channel differential amplifier with 0 dB gain and low distortion. The device has been primarily developed for car radio applications where long connections between signal sources and amplifiers (or boosters) are necessary and where ground noise has to be eliminated. The device is intended to be used to receive line inputs in audio applications that require a high level of common-mode rejection. The device is contained in an 16-pin small outline (SO) or dual in-line (DIL) package.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage		5	8.5	18	V
I_{CC}	supply current	V_{CC} = 8.5 V	–	11	14	mA
G_v	voltage gain		–0.5	0	+0.5	dB
SVRR	supply voltage ripple rejection		–55	–60	–	dB
V_{no}	noise output voltage		–	3.7	5	μV
$\|Z_i\|$	input impedance		100	240	–	kΩ
CMRR	common-mode rejection ratio	R_s = 0 Ω	–	80	–	dB

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA8578	16	DIL16	plastic	SOT38
TDA8578T	16	SO16	plastic	SOT109A

Dual common-mode rejection differential line receiver

TDA8578

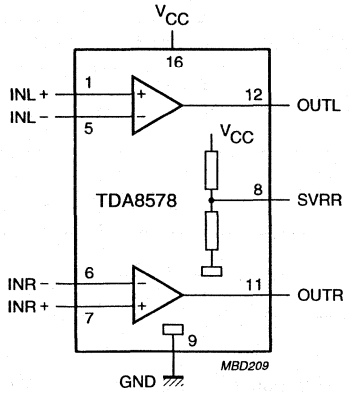


Fig.1 Block diagram.

FUNCTIONAL DESCRIPTION

The TDA8578 contains two identical differential amplifiers with a voltage gain of 0 dB. The device is intended to receive line input signals for audio applications. The TDA8578 has a very high level of common-mode rejection and thus eliminates ground noise. The common-mode rejection remains constant up to high frequencies (the amplifier gain is fixed at 0 dB). The inputs have a high input impedance. The output stage is a class AB stage with a low output impedance. For a large common-mode rejection, also at low frequencies, an electrolytic capacitor connected to the negative input is advised. Because the input impedance is relatively high, this results in a large settling time of the DC input voltage. Therefore a quick-charge circuit is included to charge the input capacitor within 0.2 seconds.

PINNING

SYMBOL	PIN	DESCRIPTION
INL+	1	positive input left
n.c.	2	not connected
n.c.	3	not connected
n.c.	4	not connected
INL−	5	negative input left
INR−	6	negative input right
INR+	7	positive input right
SVRR	8	half supply voltage
GND	9	ground
n.c.	10	not connected
OUTR	11	output right
OUTL	12	output left
n.c.	13	not connected
n.c.	14	not connected
n.c.	15	not connected
V_{CC}	16	supply voltage

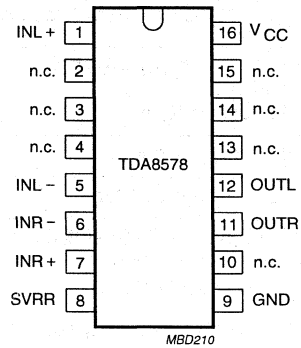


Fig.2 Pin configuration.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	supply voltage	operating	–	18	V
I_{ORM}	repetitive peak output current		–	40	mA
V_{sc}	AC and DC short-circuit safe voltage		–	18	V
T_{stg}	storage temperature		–55	+150	°C
T_{amb}	operating ambient temperature		–40	+85	°C
T_j	junction temperature		–	+150	°C

HANDLING

Inputs and outputs are protected against electrostatic discharges in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling integrated circuits.

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient in free air	
	TDA8578 (DIL16)	75 K/W
	TDA8578T (SO16)	120 K/W

DC CHARACTERISTICS

V_{CC} = 8.5 V; T_{amb} = 25 °C; in accordance with test circuit (see Fig.3); unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage		5	8.5	18	V
I_{CC}	supply current		–	11	14	mA
V_O	DC output voltage	note (1)	–	4.3	–	V
t_{set}	DC input voltage settling time		–	0.2	–	s

Note to the DC characteristics

1. The DC output voltage with respect to ground is approximately $0.5V_{CC}$.

AC CHARACTERISTICS

V_{CC} = 8.5 V; f = 1 kHz; T_{amb} = 25 °C; in accordance with test circuit (see Fig.3); unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
G_v	voltage gain		−0.5	0	+0.5	dB
α_{cs}	channel separation	R_s = 5 kΩ	70	80	–	dB
$\lvert\Delta G_v\rvert$	channel unbalance		–	–	0.5	dB
f_L	low frequency roll-off	−1 dB; note (1)	20	–	–	Hz
f_H	high frequency roll-off	−1 dB	20	–	–	kHz
$\lvert Z_i\rvert$	input impedance		100	240	–	kΩ
$\lvert Z_o\rvert$	output impedance		–	–	10	Ω
$V_{i(max)}$	maximum input voltage	THD = 1%	–	2	–	V
V_{no}	noise output voltage	R_s = 0 Ω; note (2)	–	3.7	5	μV
$V_{CM(rms)}$	common-mode input voltage (RMS value)		–	–	1	V
CMRR	common-mode rejection ratio	R_s = 5 kΩ	66	70	–	dB
		R_s = 0 Ω; note (3)	–	80	–	dB
SVRR	supply voltage ripple rejection	note (4)	55	65	–	dB
		note (5)	–	60	–	dB
THD	total harmonic distortion	V_i = 1 V	–	0.02	–	%
		V_i = 1 V; f = 20 Hz to 20 kHz	–	–	0.1	%
THD_{max}	total harmonic distortion at maximum output current	V_i = 1 V; R_L = 150 Ω	–	–	1	%

Notes to the AC characteristics

1. Frequency response externally fixed by the input coupling capacitors.
2. Noise output voltage is measured in a bandwidth of 20 Hz to 20 kHz (unweighted).
3. The common-mode rejection ratio is measured at the output, with a voltage source of 1 V (RMS), in accordance with test circuit (see Fig.3), while V_{INL} and V_{INR} are short-circuited. Frequencies between 100 Hz and 100 kHz.
4. Ripple rejection is measured at the output, with R_s = 2 kΩ; f = 1 kHz and a ripple amplitude of 2 V (p-p).
5. Ripple rejection is measured at the output, with R_s = 0 Ω up to 2 kΩ and f = 100 Hz to 20 kHz; maximum ripple amplitude of 2V (p-p).

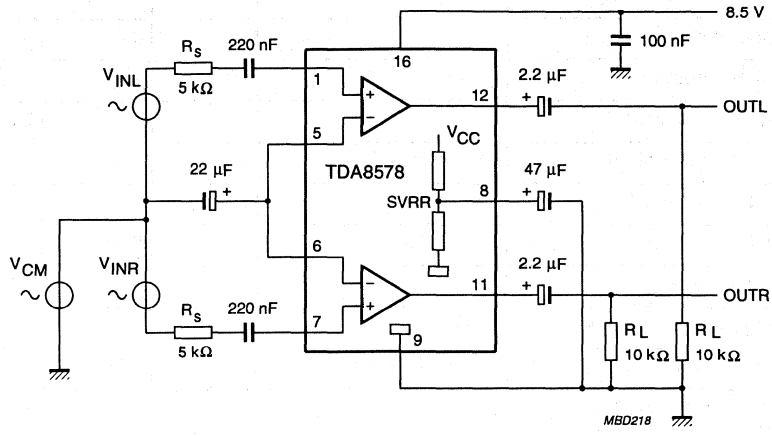


Fig.3 Test circuit.

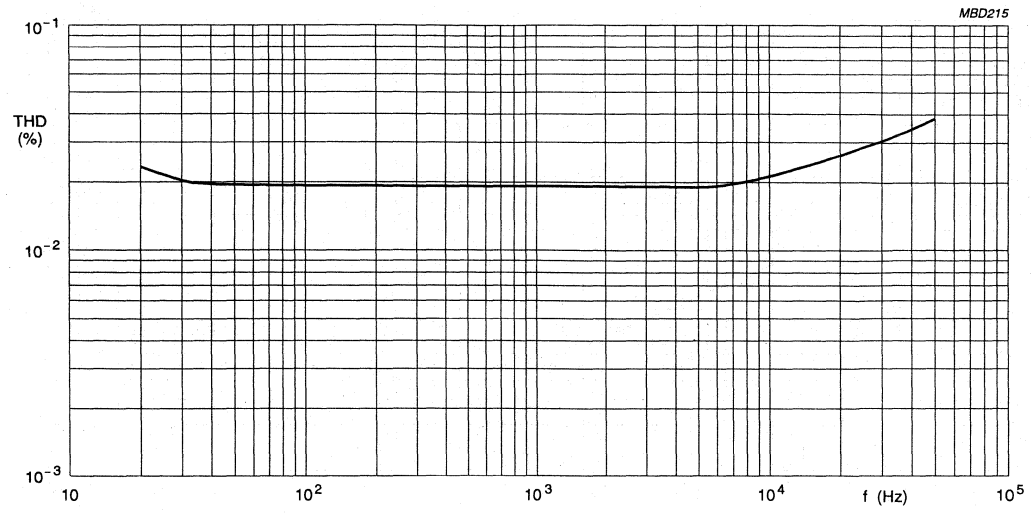
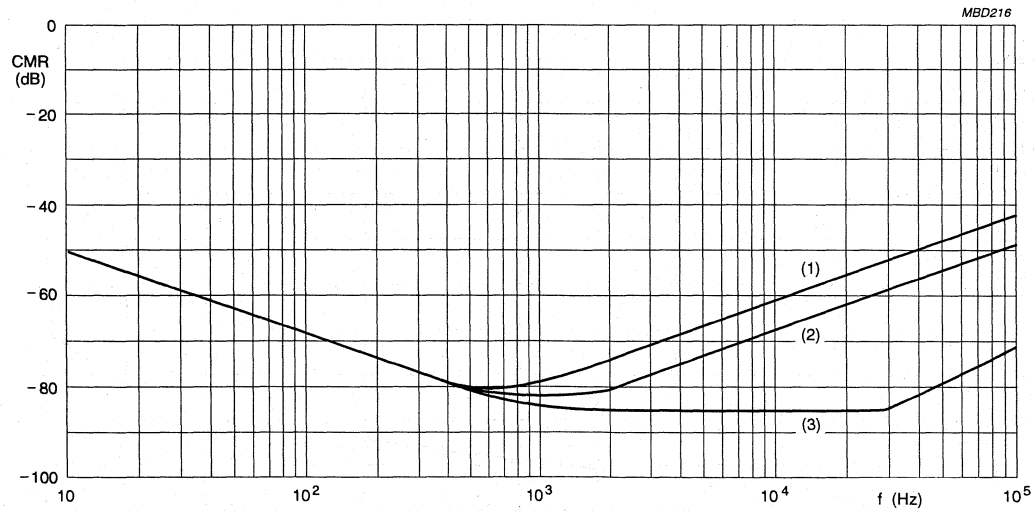


Fig.4 Total harmonic distortion as a function of frequency; V_i = 1.0 V (RMS).



(1) R_s = 5 kΩ.
(2) R_s = 2 kΩ.
(3) R_s = 0 Ω.

Fig.5 Common-mode rejection as function of frequency; V_{CM} = 1.0 V (RMS).

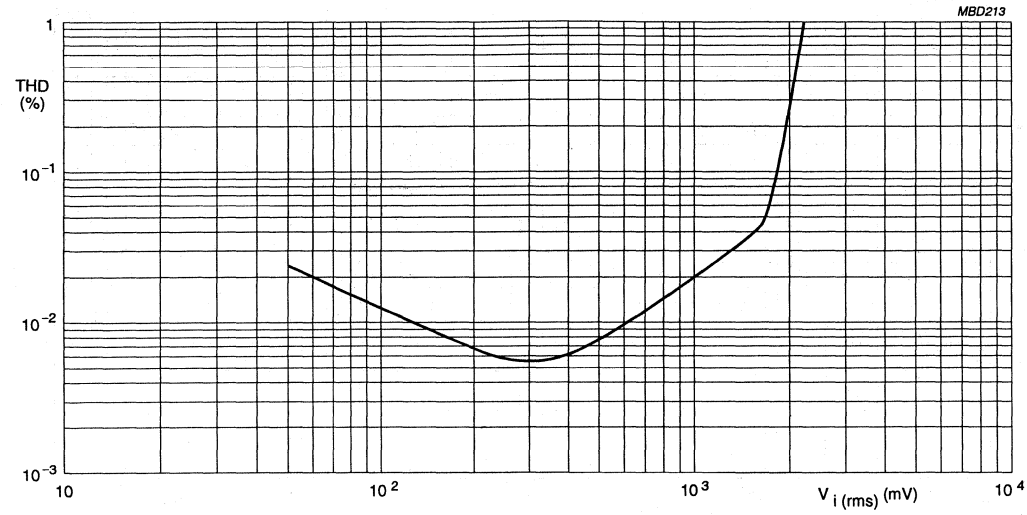


Fig.6 Total harmonic distortion as a function of input voltage; f = 1 kHz.

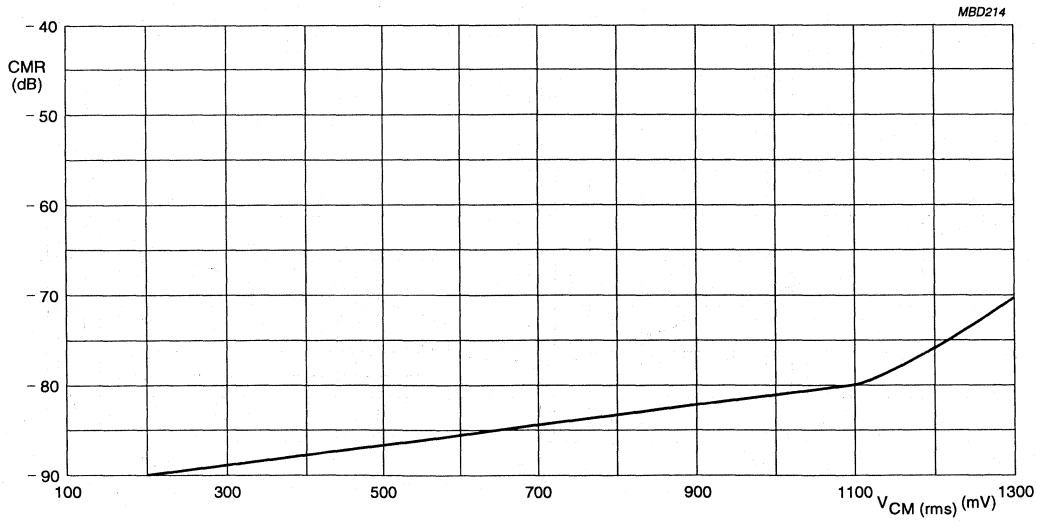
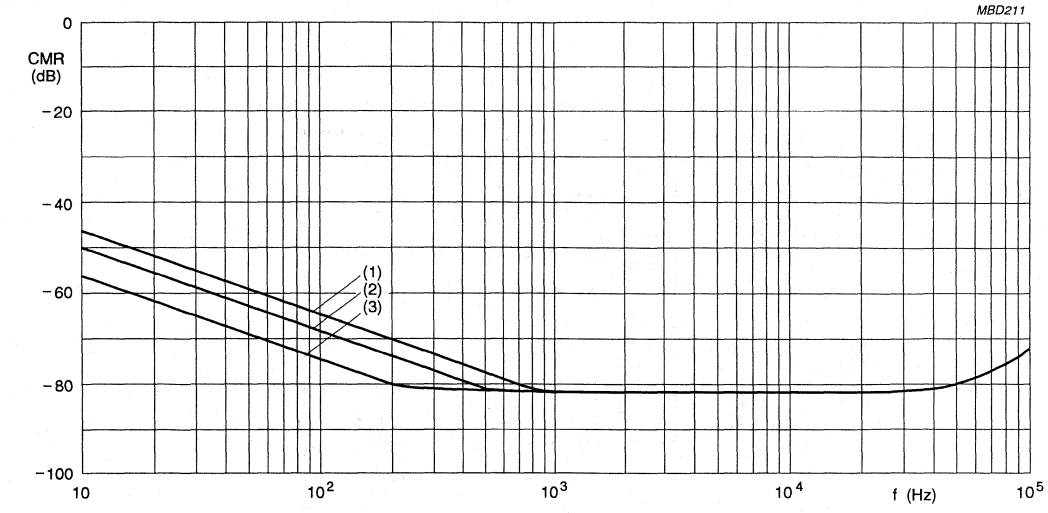
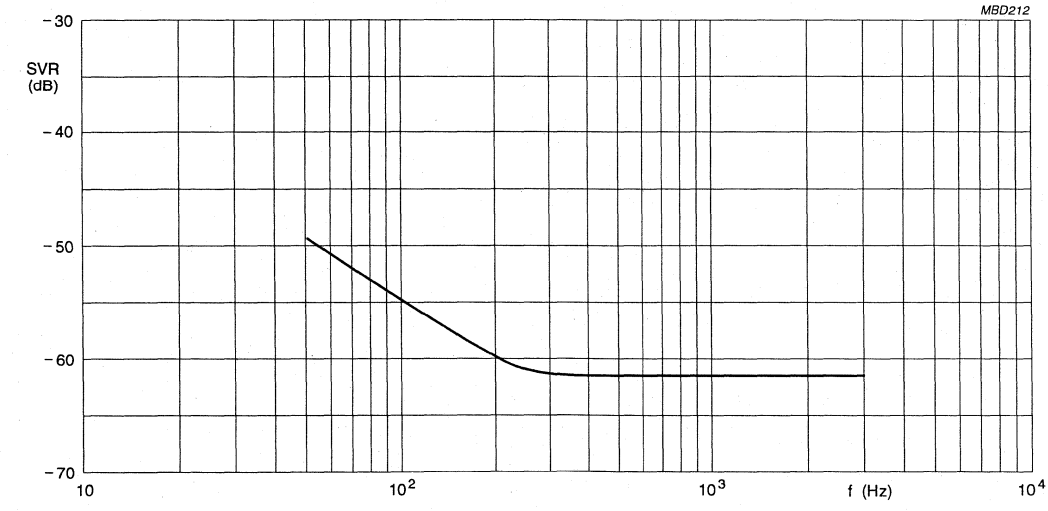


Fig.7 Common-mode rejection as a function of common-mode input voltage; f = 1 kHz; $R_s = 0\ \Omega$.



(1) C2 = 22 µF.
(2) C2 = 47 µF.
(3) C2 = 100 µF.

Fig.8 Common-mode rejection as a function of frequency; V_{CM} = 1.0V.



V_{ripple} = 2 V (p-p); R_s = 2 kΩ.

Fig.9 Supply voltage ripple rejection as a function of frequency.

APPLICATION INFORMATION

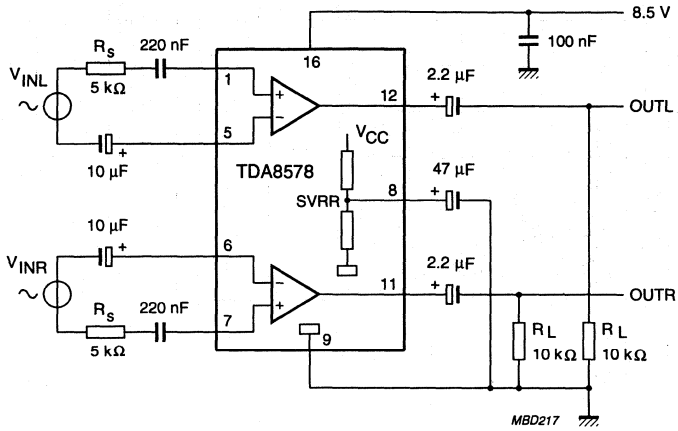


Fig.10 Application circuit balanced signal source.

Dual common-mode rejection differential line receiver

TDA8579

FEATURES

- Excellent common-mode rejection, up to high frequencies
- Elimination of source resistance dependency in the common-mode rejection
- Few external components
- High supply voltage ripple rejection
- Low noise
- Low distortion
- All pins protected against electrostatic discharge
- AC and DC short-circuit safe to ground and V_{CC}
- Fast DC settling.

GENERAL DESCRIPTION

The TDA8579 is a two channel differential amplifier with 0 dB gain and low distortion. The device has been primarily developed for car radio applications where long connections between signal sources and amplifiers (or boosters) are necessary and where ground noise has to be eliminated. The device is intended to be used to receive line inputs in audio applications that require a high level of common-mode rejection. The device is contained in an 8-pin small outline (SO) or dual in-line (DIL) package.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage		5.0	8.5	18	V
I_{CC}	supply current	V_{CC} = 8.5 V	–	11	14	mA
G_v	voltage gain		−0.5	0	+0.5	dB
SVRR	supply voltage ripple rejection		55	60	–	dB
V_{no}	noise output voltage		–	3.7	5.0	μV
$\|Z_i\|$	input impedance		100	240	–	kΩ
CMRR	common-mode rejection ratio	R_s = 0 Ω	–	80	–	dB

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA8579	8	DIL8	plastic	SOT97
TDA8579T	8	SO8	plastic	SOT96

Dual common-mode rejection differential line receiver

TDA8579

BLOCK DIAGRAM

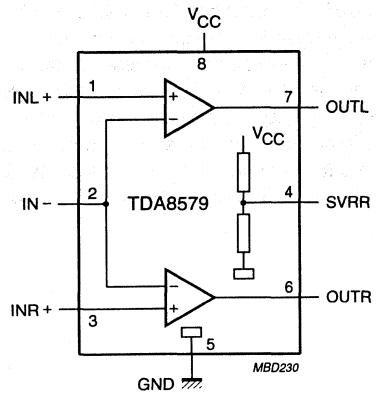


Fig.1 Block diagram.

FUNCTIONAL DESCRIPTION

The TDA8579 contains two identical differential amplifiers with a voltage gain of 0 dB. The device is intended to receive line input signals for audio applications. The TDA8579 has a very high level of common-mode rejection and thus eliminates ground noise. The common-mode rejection remains constant up to high frequencies (the amplifier gain is fixed at 0 dB). The inputs have a high input impedance. The output stage is a class AB stage with a low output impedance. For a large common-mode rejection, also at low frequencies, an electrolytic capacitor connected to the negative input is advised. Because the input impedance is relatively high, this results in a large settling time of the DC input voltage. Therefore a quick-charge circuit is included to charge the input capacitor within 0.2 seconds.

PINNING

SYMBOL	PIN	DESCRIPTION
INL+	1	positive input left
IN−	2	common negative input
INR+	3	positive input right
SVRR	4	half supply voltage
GND	5	ground
OUTR	6	output right
OUTL	7	output left
V_{CC}	8	supply voltage

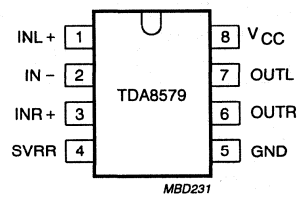


Fig.2 Pin configuration.

LIMITING VALUES

in accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	supply voltage	operating	–	18	V
I_{ORM}	repetitive peak output current		–	40	mA
V_{sc}	AC and DC short-circuit safe voltage		–	18	V
T_{stg}	storage temperature		–55	+150	°C
T_{amb}	operating ambient temperature		–40	+85	°C
T_j	maximum junction temperature		–	+150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient in free air	
	TDA8579	110 K/W
	TDA8579T	160 K/W

CHARACTERISTICS

V_{CC} = 8.5 V; T_{amb} = 25 °C; f = 1 kHz; measured in test circuit of Fig.3; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage		5.0	8.5	18	V
I_{CC}	supply current		–	11	14	mA
V_O	DC output voltage	note 1	–	4.3	–	V
t_{set}	DC input voltage settling time		–	0.2	–	s
G_v	voltage gain		−0.5	0	+0.5	dB
α_{cs}	channel separation	R_s = 5 kΩ	70	80	–	dB
$\lvert\Delta G_v\rvert$	channel unbalance		–	–	0.5	dB
f_L	low frequency roll-off	−1 dB; note 2	20	–	–	Hz
f_H	high frequency roll-off	−1 dB	20	–	–	kHz
$\lvert Z_i\rvert$	input impedance		100	240	–	kΩ
$\lvert Z_o\rvert$	output impedance		–	–	10	Ω
$V_{i(max)}$	maximum input voltage	THD = 1%	–	2.0	–	V
V_{no}	noise output voltage	R_s = 0 Ω; note 3	–	3.7	5.0	μV
$V_{CM(RMS)}$	common-mode input voltage (RMS value)		–	–	1.0	V
CMRR	common-mode rejection ratio	R_s = 5 kΩ	66	70	–	dB
		R_s = 0 Ω; note 4	–	80	–	dB
SVRR	supply voltage ripple rejection	note 5	55	65	–	dB
		note 6	–	60	–	dB
THD	total harmonic distortion	V_i = 1 V;	–	0.02	–	%
		V_i = 1 V; f = 20 Hz to 20 kHz	–	–	0.1	%
THD_{max}	total harmonic distortion at maximum output current	V_i = 1 V; R_L = 150 Ω	–	–	1	%

Notes

1. The DC output voltage with respect to ground is approximately $0.5V_{CC}$.
2. The frequency response is externally fixed by the input coupling capacitors.
3. The noise output voltage is measured in a bandwidth of 20 Hz to 20 kHz (unweighted).
4. The common-mode rejection ratio is measured at the output with a voltage source of 1 V (RMS) in accordance with the test circuit (see Fig.3) while V_{INL} and V_{INR} are shorted-circuited. Frequencies between 100 Hz and 100 kHz.
5. The ripple rejection is measured at the output, with R_s = 2 kΩ, f = 1 kHz and a ripple amplitude of 2 V (p-p).
6. The ripple rejection is measured at the output, with R_s = 0 to 2 kΩ, f = 100 Hz to 20 kHz and a maximum ripple amplitude of 2 V (p-p).

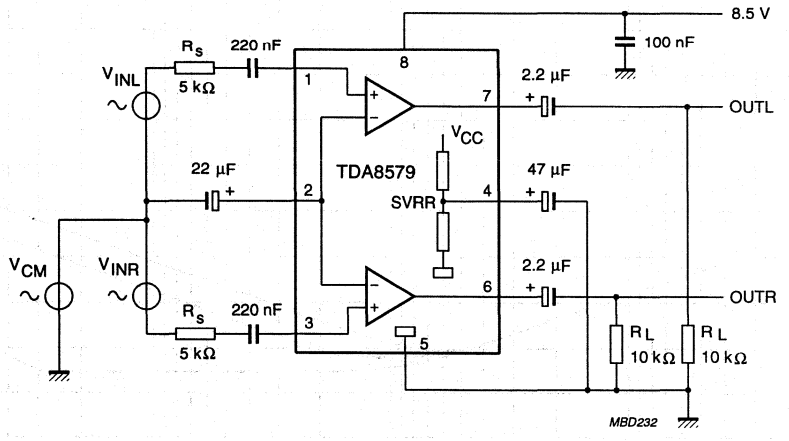


Fig.3 Test and application circuit.

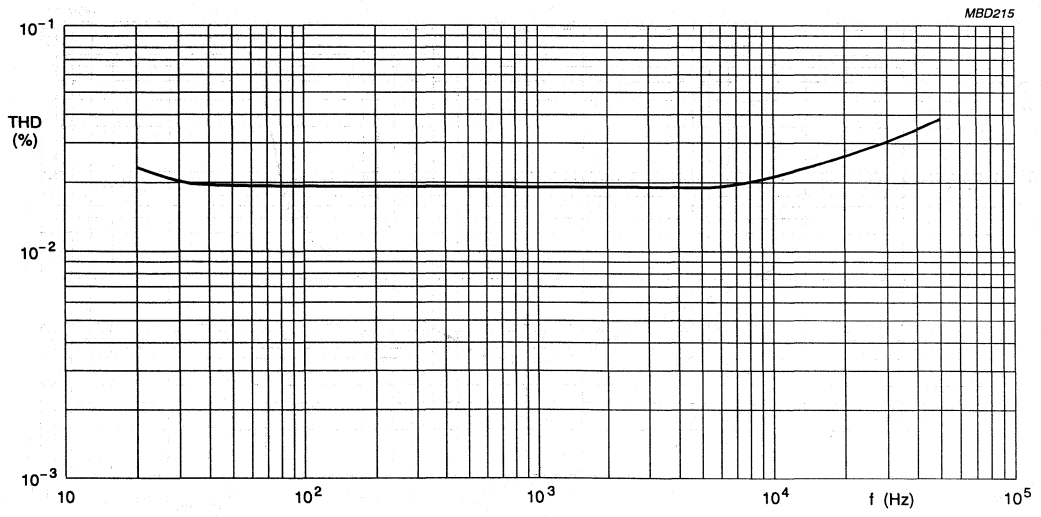
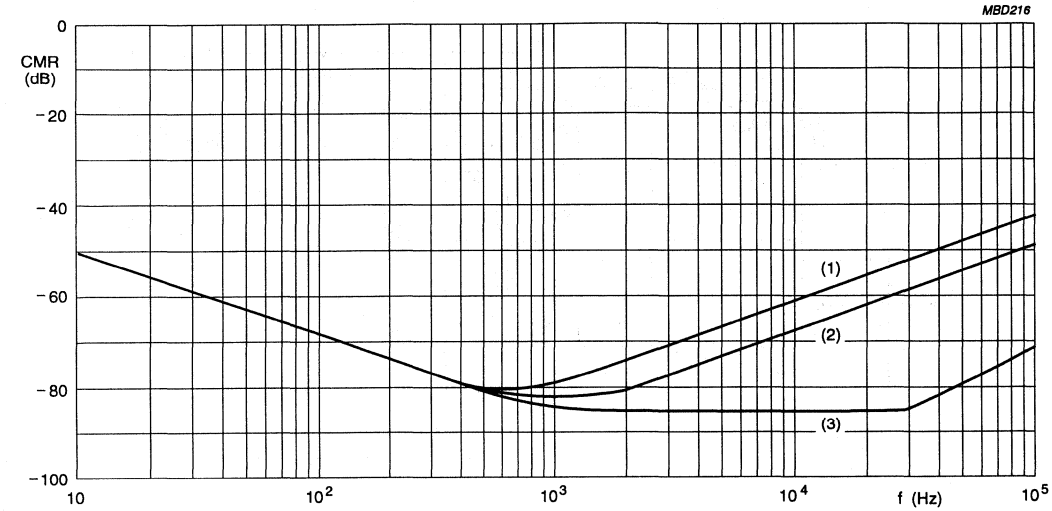


Fig.4 Total harmonic distortion as a function of frequency; V_i = 1 V (RMS).



(1) $R_s = 5\ k\Omega$
(2) $R_s = 2\ k\Omega$
(3) $R_s = 0\ k\Omega$

Fig.5 Common-mode rejection ratio as a function of frequency; $V_{CM} = 1$ V (RMS).

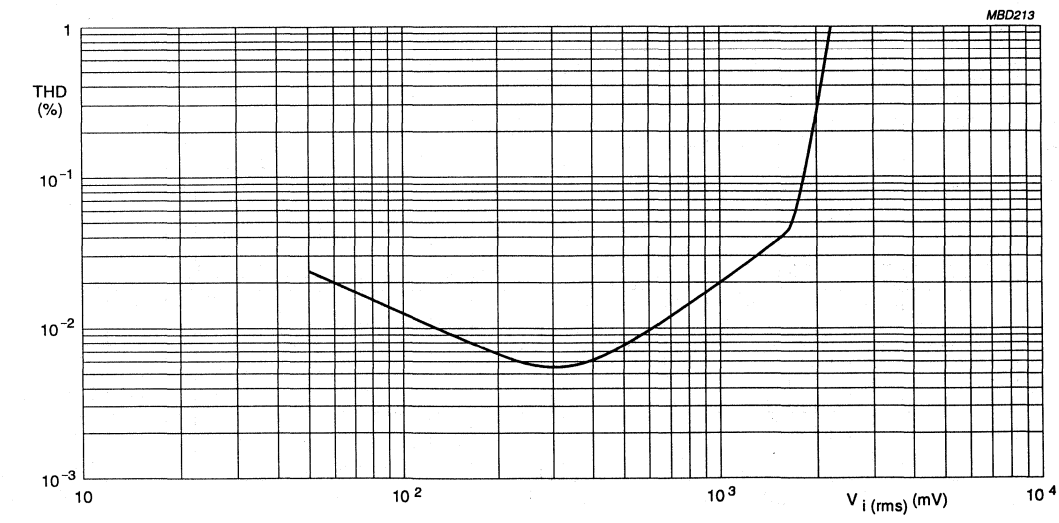


Fig.6 Total harmonic distortion as a function of input voltage; f = 1 kHz.

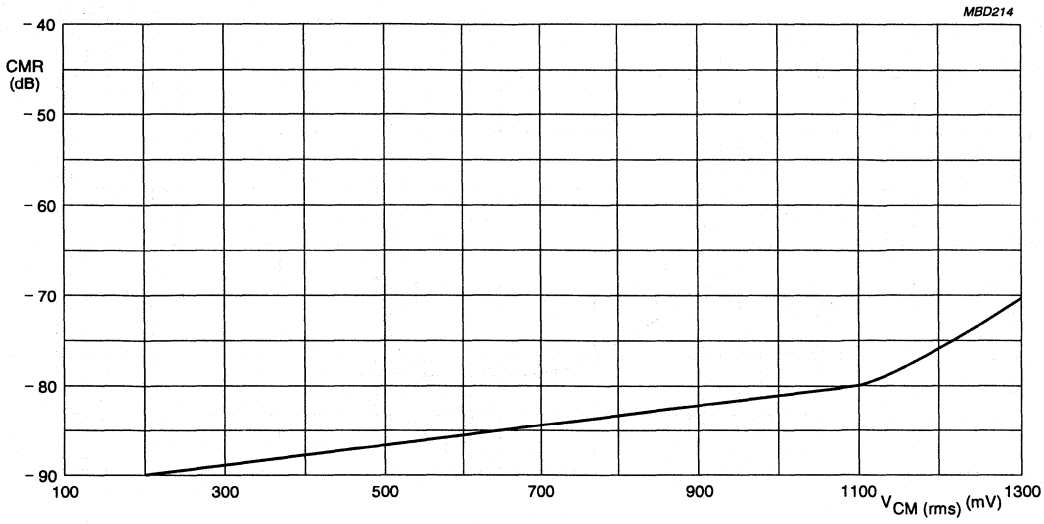
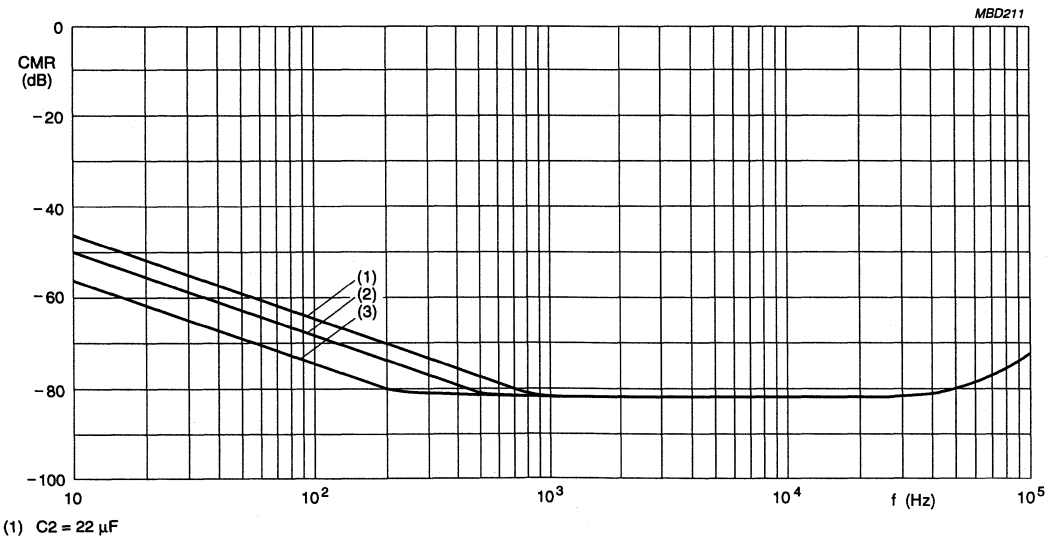


Fig.7 Common-mode rejection ratio as a function of common-mode input voltage; f = 1 kHz (R_s = 0 Ω).



(1) C2 = 22 µF
(2) C2 = 47 µF
(3) C2 = 100 µF

Fig.8 Common-mode rejection ratio as a function of frequency; V_{CM} = 1 V (RMS).

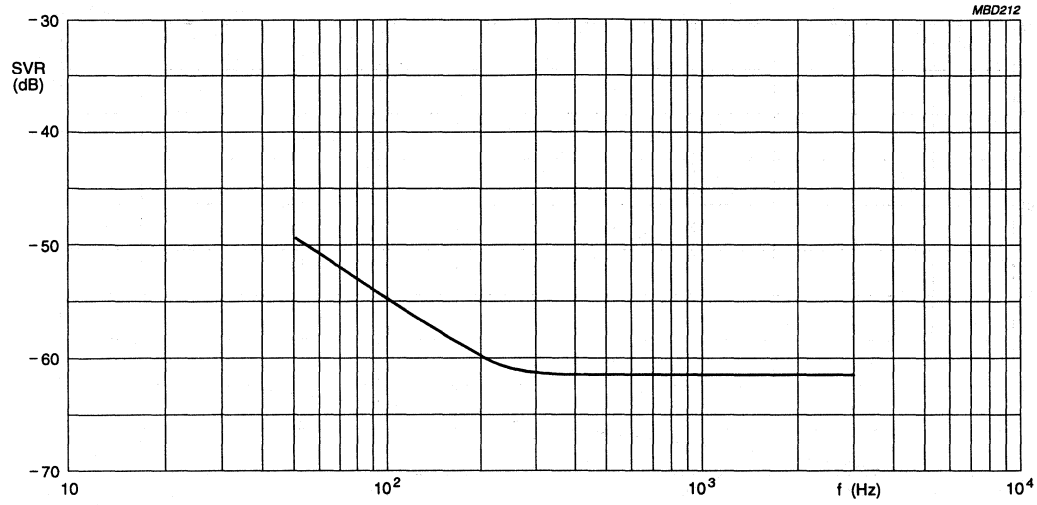


Fig.9 Supply voltage ripple rejection as a function of frequency; V_{ripple} = 2 V (p-p), R_s = 2 kΩ.

PLL frequency synthesizer TDA8735

FEATURES

- Complete 30 MHz single-chip tuning system
- Loop amplifier included
- 2-level current amplifier (charge pump) for adjusting the loop gain
- A powerful digital memory phase detector
- Programmable reference frequencies of 1 kHz, 10 kHz or 25 kHz
- I²C-bus interface
- Programmable address select input
- Software controlled switch output.

APPLICATIONS

- Satellite sound receiver
- Radio receiver: LW, MW and SW.

GENERAL DESCRIPTION

The TDA8735 is a single-chip PLL synthesizer designed for satellite receivers. The device can be set to two different addresses which can be used in applications where independently tuned VCOs are required.

To adapt to different frequency accuracy, 3 reference frequencies are selectable via the I²C-bus. The charge pump current can be set to 2 values with a ratio of 1 : 100 via the I²C-bus.

A programmable switch (open collector) is integrated to enable mode or normal switching, or other types of application.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC1}	supply voltage (pin 3)		4.5	5.0	5.5	V
V_{CC2}	supply voltage (pin 16)		V_{CC1}	8.5	12	V
I_{CC1}	supply current (pin 3)	outputs unloaded	12	20	28	mA
I_{CC2}	supply current (pin 16)	outputs unloaded	0.2	0.5	1	mA
$f_{i(max)}$	maximum input frequency		30	–	–	MHz
$f_{i(min)}$	minimum input frequency		–	–	512	kHz
$V_{i(rms)}$	input voltage (RMS value)		30	–	500	mV
P_{tot}	total power dissipation		–	0.14	–	W
T_{amb}	operating ambient temperature		–30	–	+85	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8735	DIP16	plastic dual in-line package; 16 leads (300 mil)	SOT38-1
TDA8735T	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1

BLOCK DIAGRAM

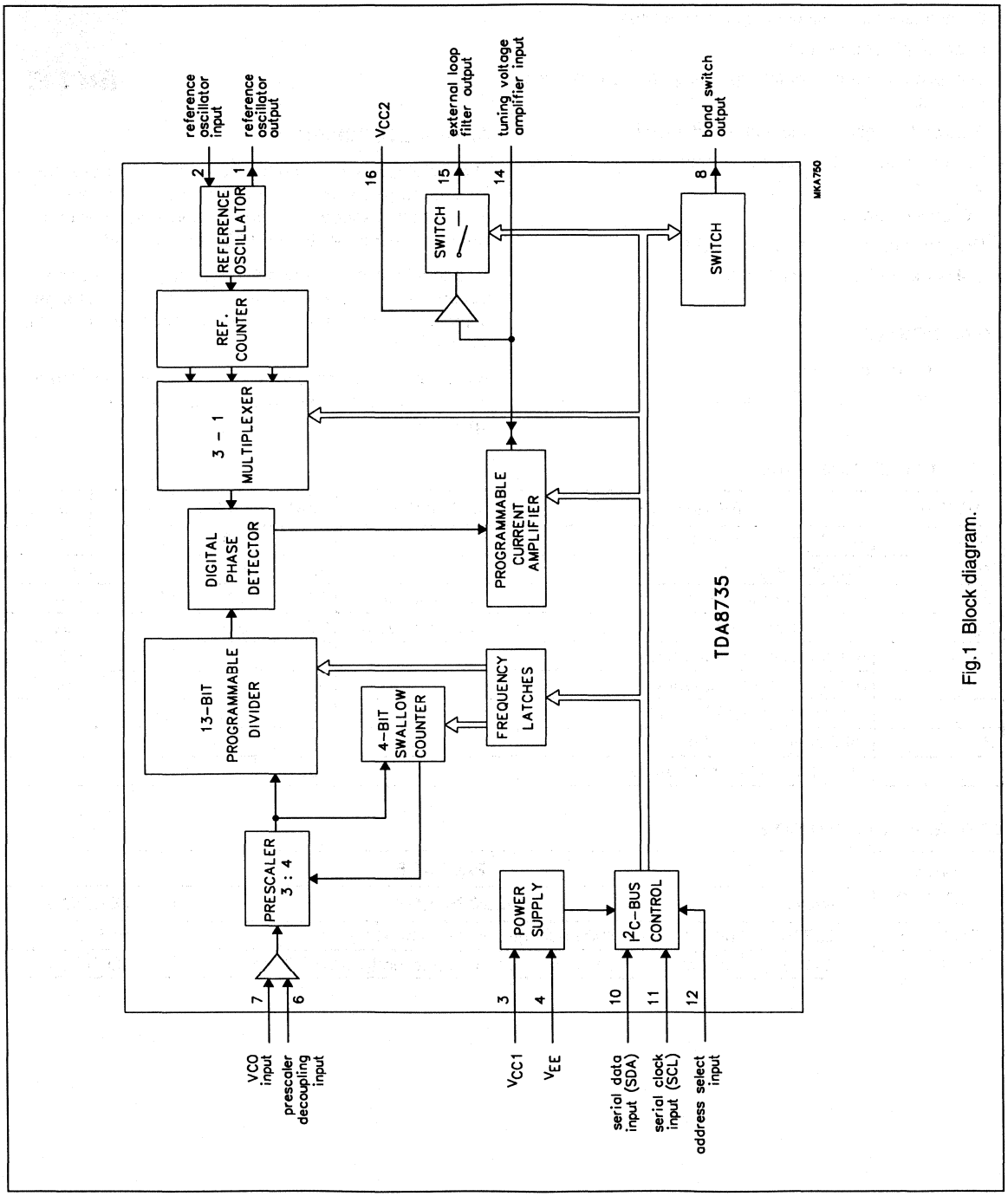


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
XTAL1	1	reference oscillator output
XTAL2	2	reference oscillator input
V_{CC1}	3	supply voltage 1
V_{EE}	4	ground
n.c.	5	not connected
DEC	6	prescaler decoupling
VCOFI	7	VCO input frequency
BS	8	band switch output
n.c.	9	not connected
SDA	10	serial data input (I^2C-bus)
SCL	11	serial clock input (I^2C-bus)
AS	12	address select input (I^2C-bus)
n.c.	13	not connected
$LOOP_I$	14	tuning voltage amplifier input
$LOOP_O$	15	external loop filter output
V_{CC2}	16	supply voltage 2

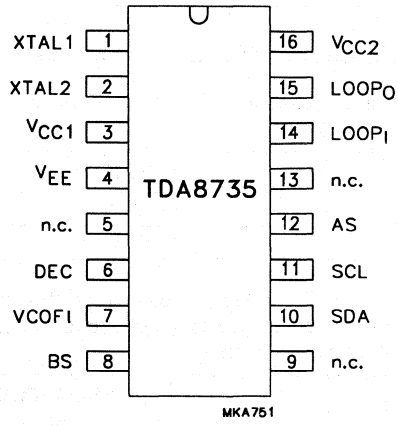


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The TDA8735 contains the following parts and facilities:

- Input amplifier VCO-signal.
- A prescaler with the divisors 3 : 4 and a 2-bit programmable swallow counter.
- A 13-bit programmable counter.
- A digital memory phase detector.
- A reference frequency channel comprised of a 4 MHz crystal oscillator followed by a reference counter; the reference frequency can be 1 kHz, 10 kHz or 25 kHz and is applied to the digital memory phase detector.
- An I^2C-bus interface with data latches and control logic; the I^2C-bus is intended for communication between microcontrollers and different ICs or modules. Detailed information on the I^2C-bus specification is available on request.
- A software-controlled switch output.
- A programmable current amplifier (charge pump) which consists of a 5 μA and a 500 μA current source, this allows adjustment of loop gain, thus providing high-current high-speed tuning and low current-stable tuning. The output at the loop amplifier can deliver a tuning voltage of up to 10.5 V (V_{CC2} – 1.5 V).

Controls

The TDA8735 is controlled via the 2-wire I^2C-bus. As slave receiver for programming there is one module address, a logic 0 ($R/\overline{W}$ bit), a subaddress byte and four data bytes. The subaddress determines which one of the four data bytes is transmitted first. The module address contains a programmable address bit (D1) which with address select input AS (pin 12) makes it possible to operate two TDA8735 in one system.

The auto increment facility of the I^2C-bus allows programming of the TDA8735 within one transmission (address + subaddress + 4 data bytes).

The TDA8735 can also be partially programmed. Transmission must then be ended by a stop condition.

The bit organization of the 4 data bytes is illustrated in Fig.3 and is described below.

The divider number is defined by 15-bit words, bits S0 to S14. To calculate the lock frequency, the divider number has to be multiplied by the selected reference frequency.

Table 1 Divider number setting.

$\overline{ON}$	DIVIDER NUMBER SETTING	INPUT
0	$(S0 + S1) \times 2^1 .... + S13 \times 2^{13} + S14 \times 2^{14}$	ON

Where the minimum divider ratio is: $2^6 = 64$ to $2^{15} - 1 = 32761$.

Table 2 Bit CP (used to control the charge pump; DB0: D0).

CP	CURRENT
0	LOW
1	HIGH

Table 3 Bits REF1 and REF2 (used to set the reference frequency applied to the phase detector; DB2: D7 and D6).

REF1	REF2	FREQUENCY (kHz)
0	0	1
0	1	10
1	0	25
1	1	0

Table 4 Bit OPAMP (used to control the switch in the tuning voltage amplifier output circuitry; DB2: D4).

OPAMP	SWITCH
1	on
0	off

Table 5 Bit BS (used to control the open-collector switch output; DB2: D2).

BS	SWITCH OUTPUT
1	sink current
0	floating

The data byte DB3 must be set to 0....0. It is also used for test purposes (see Fig.3).

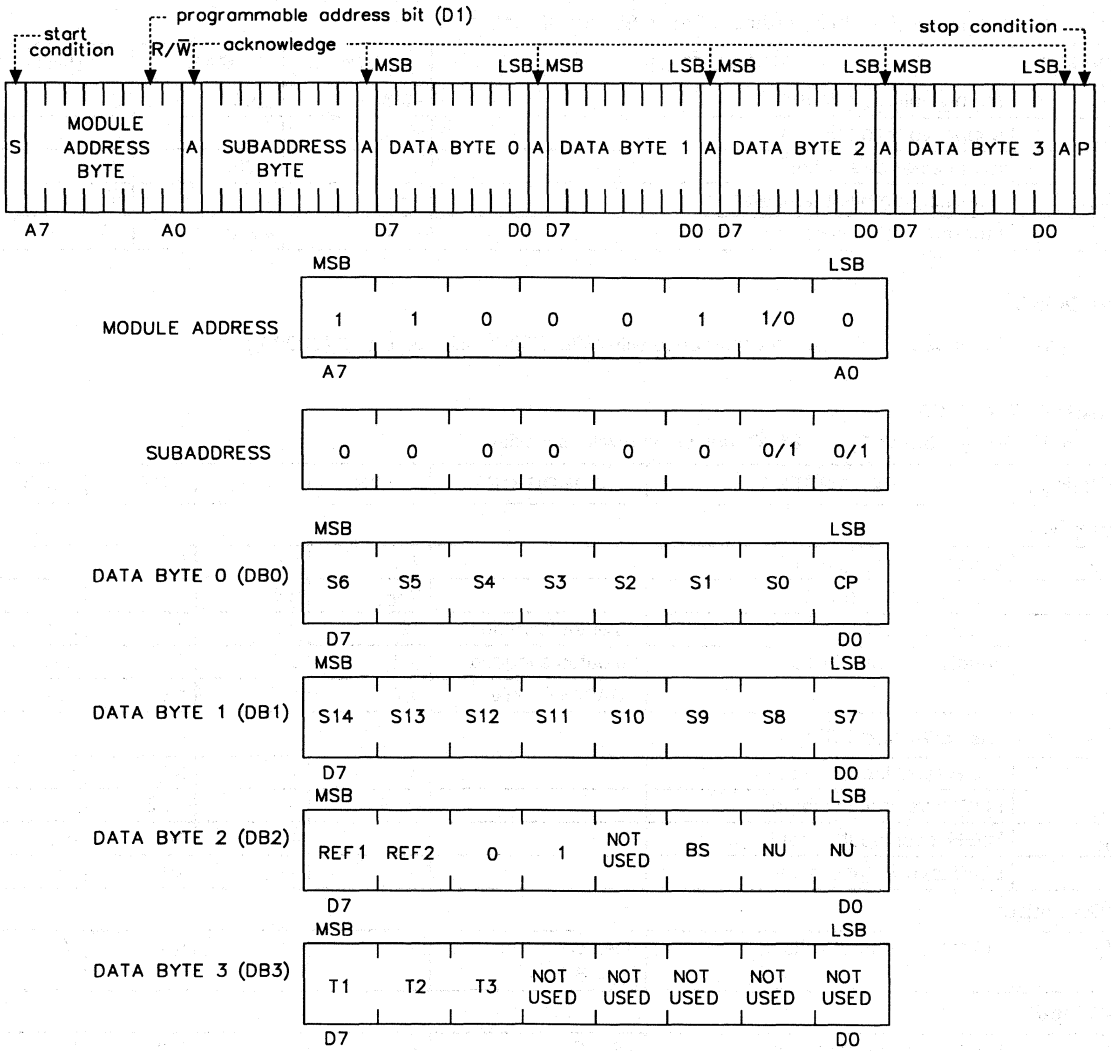


Fig.3 Bit organization.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{CC1}	supply voltage (pin 3)	−0.3	+5.5	V
V_{CC2}	supply voltage (pin 16)	V_{CC1}	12.5	V
P_{tot}	total power dissipation	–	0.85	W
T_{amb}	operating ambient temperature	−30	+85	°C
T_{stg}	storage temperature	−65	+150	°C

HANDLING

Every pin withstands the ESD test in accordance with *"MIL-STD-883C category B"* (2000 V).

CHARACTERISTICS

V_{CC1} = 5 V; V_{CC2} = 8.5 V; T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{CC1}	supply voltage (pin 3)		4.5	5.0	5.5	V
V_{CC2}	supply voltage (pin 16)		V_{CC1}	8.5	12	V
I_{CC1}	supply current (pin 3)	no outputs loaded	12	20	28	mA
I_{CC2}	supply current (pin 16)	no outputs loaded	0.2	0.5	1	mA
		TDA8735T only	0.7	1	1.5	mA
I²C-bus inputs (SDA and SCL)						
V_{IH}	HIGH level input voltage		3.0	–	5.0	V
V_{IL}	LOW level input voltage		−0.3	–	+1.5	V
I_{IH}	HIGH level input current		–	–	10	µA
I_{IL}	LOW level input current		–	–	10	µA
SDA output						
V_{OL}	LOW level output voltage	open collector; I_{OL} = 3.0 mA	–	–	0.4	V
AS input						
V_{IH}	HIGH level input voltage	AS = C6	3.0	–	5.0	V
V_{IL}	LOW level input voltage	AS = C4	−0.3	–	+1.0	V
I_{IH}	HIGH level input current		–	–	10	µA
I_{IL}	LOW level input current		–	–	10	µA
RF input						
$f_{i(max)}$	maximum input frequency		30	–	–	MHz
$f_{i(min)}$	minimum input frequency		–	–	512	kHz
$V_{i(rms)}$	input voltage (RMS value)	measured in Fig.4	30	–	500	mV
R_i	input resistance		–	5.9	–	kΩ
C_i	input capacitance		–	2	–	pF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Oscillator (XTAL1 and XTAL2)						
R_{xtal}	crystal resonance resistance (4 MHz)	see Fig.5	–	–	150	Ω
Programmable charge pump						
I_{CHP}	output current to loop filter	bit CP = logic 0	3	5	7	μA
		bit CP = logic 1	400	500	600	μA
		bit CP = logic 0; TDA8735T only	3	5	9	μA
Ripple rejection						
RR	$20 \log \frac{\Delta V_{CC1}}{\Delta V_O}$	f_{ripple} = 100 Hz	40	50	–	dB
	$20 \log \frac{\Delta V_{CC2}}{\Delta V_O}$	f_{ripple} = 100 Hz	40	50	–	dB
Band switch output (pin 8)						
V_{OH}	HIGH level output voltage		–	–	12	V
V_{OL}	LOW level output voltage	I_{OL} = 3 mA	–	–	0.8	V
$\|I_{LO}\|$	output leakage current	V_{OH} = 12 V	–	–	10	μA
Tuning voltage amplifier output (pin 15)						
$V_{O(max)}$	maximum output voltage	I_{source} = 0.5 mA	V_{CC2} – 1.5	–	–	V
$V_{O(min)}$	minimum output voltage	I_{sink} = 1 mA	–	–	0.8	V
I_{source}	maximum output source current		0.5	–	–	mA
I_{sink}	maximum output sink current		1.0	–	–	mA
$Z_{o(off)}$	impedance of switched-off output		5	–	–	MΩ
$\|I_{bias}\|$	input bias current (absolute value)		–	1	5	nA

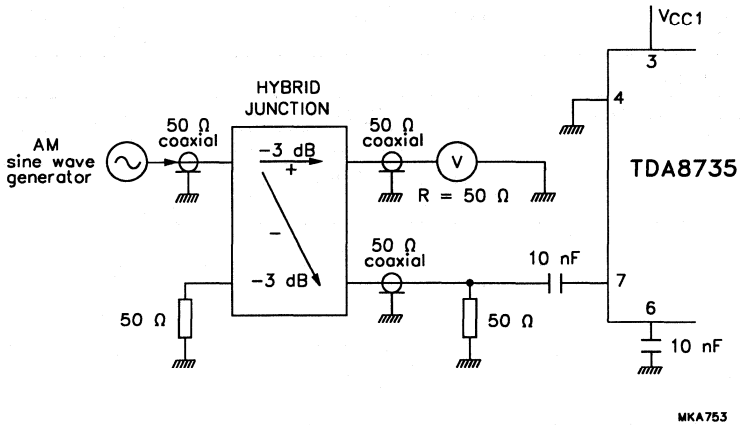


Fig.4 Prescaler input sensitivity (set-up measurement).

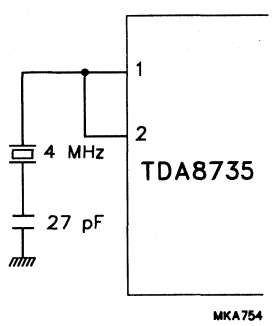
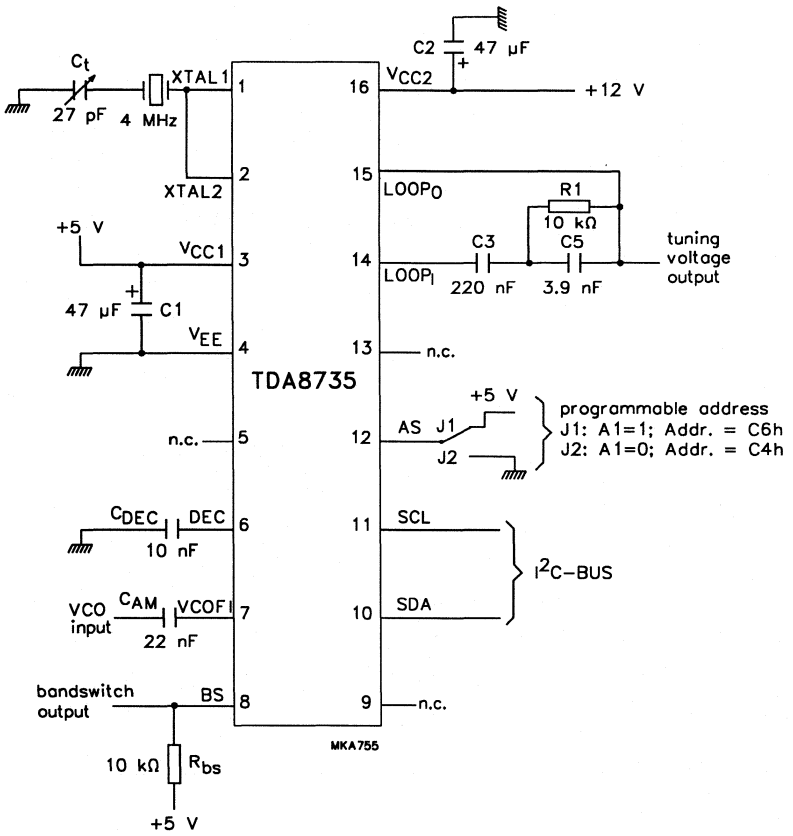


Fig.5 Crystal connection (4 MHz).

APPLICATION INFORMATION



Loop filter depends on VCO parameters.

Fig.6 Application example.

PHOTO DIODE SIGNAL PROCESSOR FOR COMPACT DISC PLAYERS

GENERAL DESCRIPTION

The TDA8808 is a bipolar integrated circuit designed for use in compact disc players with a single spot read-out system. It amplifies the photo-diode signals and processes the error signals for the focus- and radial control network.

Features

- Data amplifier with equalizer and AGC
- Offset-free pre-amplifier with AGC for the servo signals
- Trackloss and drop-out detection
- Start-up procedure for focus
- Normalizing focus error output signal to minimize radial error interference
- Laser supply amplifier and reference source
- Both TDA8808T and TDA8808AT versions suitable for car, portable and home applications
- Single and dual supply application
- Focus in-lock signal; ready signal output (RD)

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage range		V_P	4,5	5,0	5,5	V
External voltage range						
TDA8808T		V_{ext}	−5,5	−5,0	0	V
TDA8808AT		V_{ext}	V_P	10	12	V
Quiescent supply current	Si/$\overline{RD}$ = 0 V	I_Q	7,5	10	12,5	mA
HF input current (peak-to-peak value)	f_{HFin} = 100 kHz	$I_{HFin(p-p)}$	3	–	10	μA
LF input current (for each diode input)		I_D	0	–	6	μA
Laser supply output current	Si/$\overline{RD}$ = HIGH Z	I_{LO}	−8	−4	−2	mA
Operating ambient temperature range		T_{amb}	−30	–	+85	°C

PACKAGE OUTLINE

28-lead mini-pack; plastic (SO28; SOT136A).

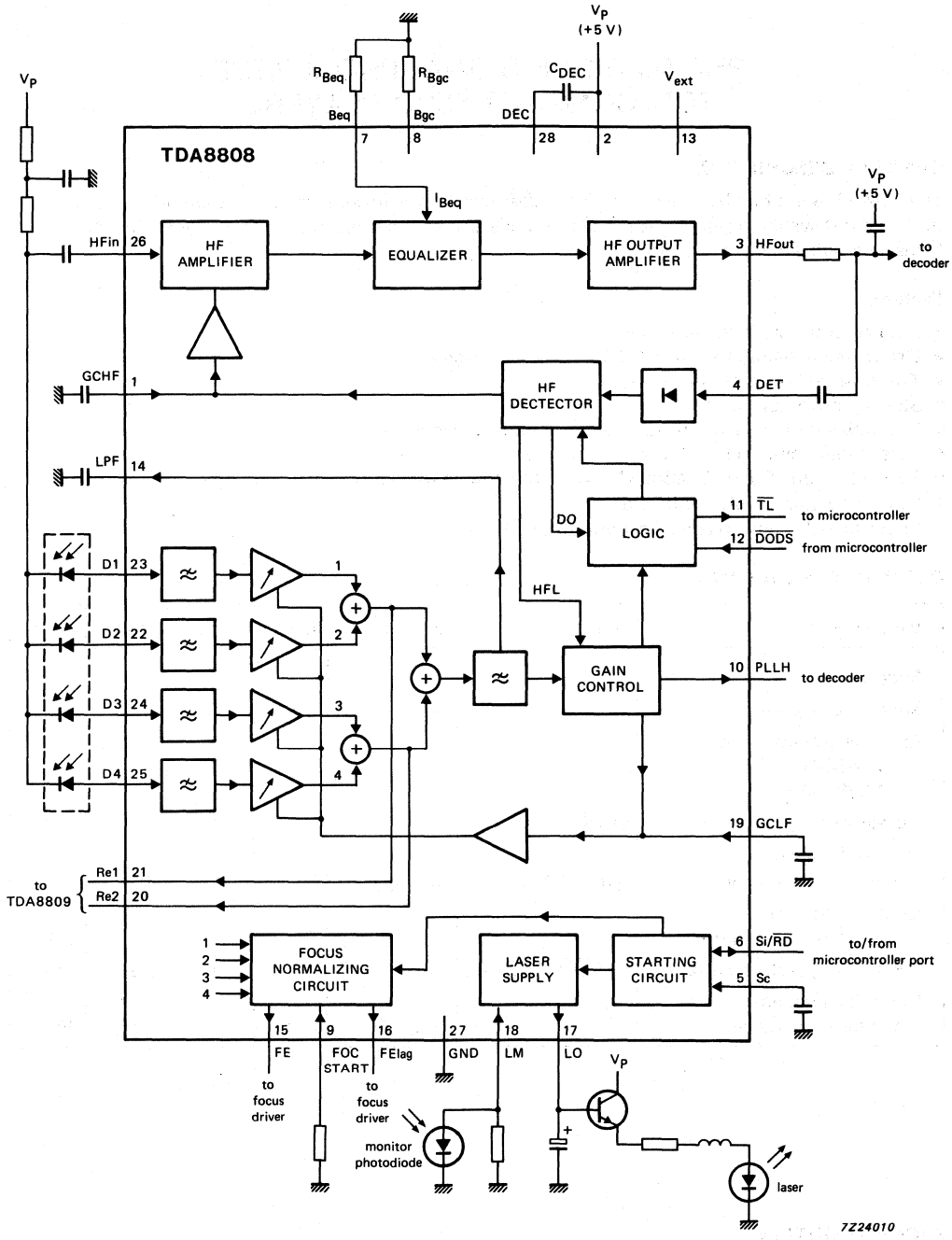


Fig. 1 Block diagram.

PINNING

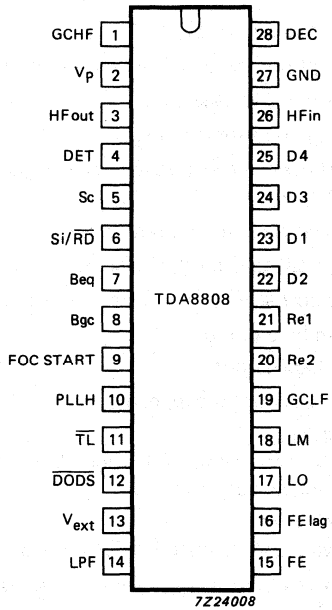


Fig. 2 Pinning diagram.

Pin functions

pin	mnemonic	description
1	GCHF	Gain control input of HF amplifier. Current output from HF amplitude detector
2	Vp	Positive supply voltage
3	HFout	HF amplifier and equalizer voltage output
4	DET	HF detector voltage input
5	Sc	Starting up capacitor input
6	Si/$\overline{RD}$	On/off control (start input); ready signal output (starting up procedure successful)
7	Beq	Equalizer reference current input
8	Bgc	DC and LF gain control reference current input
9	FOC START	Focus normalizing circuit starting current
10	PLLH	PLL on hold output
11	$\overline{TL}$	Track loss output
12	$\overline{DODS}$	Drop out detector suppression input
13	V_{ext}	TDA8808T Negative supply connection for FE and FElag output stage; also substrate connection TDA8808AT Positive supply connection for FE and FElag output stage
14	LPF	Low pass filter for I_{ret}, used in track loss ($\overline{TL}$) detector and LF gain control
15	FE	Current output of normalized, switched focus error signal
16	FElag	Current output of switched focus error signal, intended for lag network.
17	LO	Laser amplifier current output
18	LM	Laser monitor diode input
19	GCLF	Gain control input for AC and LF amplifiers. Current output from LF amplitude detector
20	Re2	Summation of amplified currents from D3 and D4
21	Re1	Summation of amplified currents from D1 and D2
23, 22	D1, D2	Current inputs to DC and LF photo diode amplifier
24, 25	D3, D4	Current inputs to DC and LF photo diode amplifier
26	HFin	Current input to HF amplifier
27	GND	Ground connection of device; also substrate connection for TDA8808AT
28	DEC	Decoupling input (internal bypass)

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage ranges (see Fig. 3)				
TDA8808T				
pin 2 to pin 13	$V_P - V_{(ext)}$	−0,3	13	V
pin 27 to pin 13	$V_{GND} - V_{(ext)}$	−0,3	13	V
TDA8808AT				
pin 13 to 27	$V_{ext} - V_{GND}$	−0,3	13	V
pin 2 to pin 27	$V_P - V_{GND}$	−0,3	13	V
Output voltage ranges				
except FE and FE_{lag}	V_O	0	V_P	V
FE and FE_{lag} (TDA8808T)	V_O	V_{ext}	V_P	V
FE and FE_{lag} (TDA8808AT)	V_O	V_{GND}	V_{ext}	V
LM (open loop)	V_O	V_{GND}	V_P	V
Total power dissipation	P_{tot}	see Fig. 4		
Storage temperature range	T_{stg}	−55	+ 150	°C
Operating ambient temperature range	T_{amb}	−30	+ 85	°C
Operating junction temperature	T_j	−	150	°C

THERMAL RESISTANCE

From junction to ambient $R_{th\ j\text{-}a}$ = 140 K/W

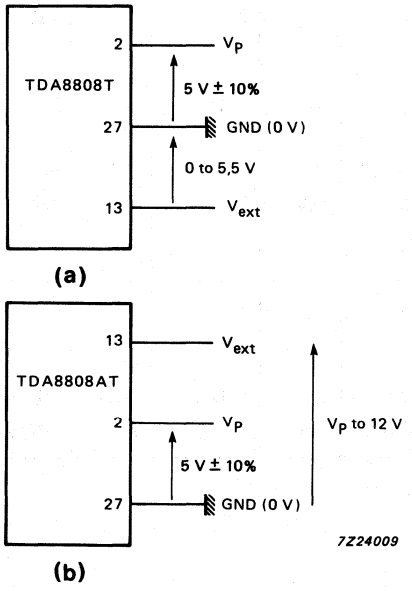


Fig. 3 Supply voltages; (a) TDA8808T, (b) TDA8808AT.

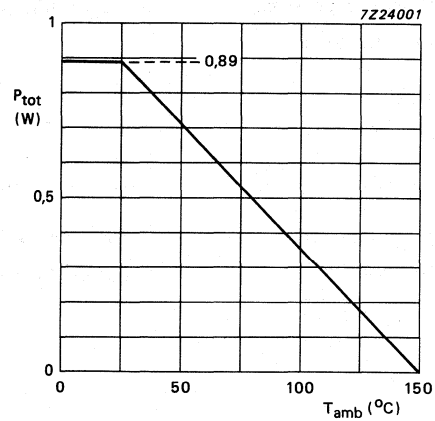


Fig. 4 Power derating curve.

CHARACTERISTICS

V_P = + 5 V; V_{GND} = 0 V; V_{ext} = –5 V (TDA8808T); V_{ext} = + 10 V (TDA8808AT); $V_{RE1} = V_{RE2}$ = 3,5 V; $V_{FE} = V_{FElag}$ = 0 V (TDA8808T); $V_{FE} = V_{FElag}$ = 5 V (TDA8808AT); $R_{FOC\ START}$ = 3,3 kΩ; $I_{Beq} = I_{Bgc}$ = 50 μA (current sources); T_{amb} = 25 °C; all voltages measured with respect to V_{GND}, unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage range		V_P	4,5	5,0	5,5	V
External voltage range						
TDA8808T		V_{ext}	–5,5	–5,0	0	V
TDA8808AT		V_{ext}	V_P	10	12	V
Quiescent supply current	$V_{Si/\overline{RD}}$ = 0 V	I_Q	7,5	10	12,5	mA
Reference input (Beq)						
Input voltage level		V_{Beq}	500	560	620	mV
Input current		I_{Beq}	–	–50	–	μA
Reference input (Bgc)						
Input voltage level		V_{Bgc}	1,15	1,25	1,35	V
Input current		I_{Bgc}	–	–50	–	μA
Decoupling input (DEC)						
Input voltage level		V_{DEC}	–	V_P–1,4	–	V
Input impedance		$\lvert Z_{DEC}\rvert$	–	2	–	kΩ
HF input (HFin)						
Input voltage level		V_{HFin}	–	1,4	–	V
HF input current (peak-to-peak value)	f_{HFin} = 100 kHz	$I_{HFin(p-p)}$	3	–	10	μA
Input impedance		$\lvert Z_{HFin}\rvert$	0,5	1	2	kΩ
HF part						
DC characteristics						
Gain (G1) = $\frac{\Delta V_{HFout}}{\Delta I_{HFin}}$	I_{HFin} = ± 1 μA					
Maximum gain	V_{GCHF} = 4 V	G1(max)	390	480	570	mV/μA
Minimum gain	V_{GCHF} = 1,5 V	G1(min)	–5	0	5	mV/μA

parameter	conditions	symbol	min.	typ.	max.	unit
HF part (continued)						
AC characteristics						
Gain (G2) = 20 log $\frac{V_{O1}}{V_{O2}}$	note 1	G2	2	3,5	5	dB
Gain (G3) = 20 log $\frac{V_{O1}}{V_{O2}}$	note 2	G3	4	5,5	7	dB
Phase of input/output signal at 1 MHz	note 3	ϕ	–	$\pi/2$	–	rad.
Group delay at f_{HFin} = 300 kHz + Δf	note 3	$\tau 300$	–	290	–	ns
Flatness between 0,1 and 1 MHz	note 3	$\Delta\tau$	*	9	*	ns
HF output (HFout)						
Output voltage at I_{HFin} = 0	V_{GCHF} = 4 V	V_{HFout}	1,5	2,4	3,3	V
Output voltage (peak-to-peak value)						
at $I_{HFin(p-p)}$ = 7 μA	note 4	$V_{O1(p-p)}$	1	1,20	–	V
at $I_{HFin(p-p)}$ = 4 to 10 μA	note 5	$V_{O(p-p)}$	–20%	M_1	+20%	V
Output impedance		$\lvert Z_{HFout}\rvert$	–	60	–	Ω
HF detector input (DET)	see Fig. 5					
DC voltage level	I_{DET} = 0	V_{DET0}	–	2,2	–	V
Positive reference voltage V_{DET} to V_{DET0}		V_{refp}	–10%	540	+10%	mV
Negative reference voltage V_{DET} to V_{DET0}		V_{refn}	–5%	$-V_{refp}$	+5%	mV
Input impedance		$\lvert Z_{DET}\rvert$	–	9	–	kΩ

* Value to be fixed.

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Gain control (GCHF)						
Input voltage for:						
minimum HF gain		V_{GCHF}	–	1,8	–	V
maximum HF gain		V_{GCHF}	–	3,4	–	V
Input impedance						
at V_{GCHF} = 1,5 to 4 V		$\lvert Z_{GCHF}\rvert$	–	25	–	MΩ
Output current (see Fig. 5)						
$\Delta V_{DET} < V_{refn}$ or $\Delta V_{DET} > V_{refp}$	$\overline{DODS}$ = LOW	I_{GCHF}	90	100	110	μA
$\Delta V_{DET} < V_{refn}$ or $\Delta V_{DET} > V_{refp}$	$\overline{DODS}$ = HIGH	I_{GCHF}	86	96	106	μA
$V_{refn} < \Delta V_{DET} < V_{DETn1}$ or $V_{DETp1} < \Delta V_{DET} < V_{refp}$	$\overline{DODS}$ = LOW	I_{GCHF}	−0,65	−0,35	−0,2	μA
$V_{refn} < \Delta V_{DET} < V_{DETn1}$ or $V_{DETp1} < \Delta V_{DET} < V_{refp}$	$\overline{DODS}$ = HIGH	I_{GCHF}	−5,0	−4,4	−3,8	μA
$V_{DETn1} < \Delta V_{DET} < V_{DETp1}$	$\overline{DODS}$ = X*	I_{GCHF}	−0,65	−0,35	−0,2	μA
V_{DETp1}/V_{refp}; V_{DETn1}/V_{refn}			10	12,5	15	%
PLLH output (pin 10)						
Output voltage LOW						
I_{PLLH} = 400 μA (sink current)		V_{PLLHL}	–	–	0,4	V
Output voltage HIGH						
I_{PLLH} = −50 μA (source current)		V_{PLLHH}	2,4	–	–	V
Output sink current		I_{PLLH}	0,5	1,5	–	mA
Output source current		I_{PLLH}	–	−100	−50	μA
Threshold total LF current	V_{GCLF} = 3,5 V	I_{DT1}	–	2,0	–	μA
V_{DETp2}/V_{refp}; V_{DETn2}/V_{refn}			57,5	62,5	67,5	%
LF photo diode inputs (pins 22 to 25)						
(values given for each input)						
DC voltage level		V_D	–	1,2	–	V
Input current range		I_D	0	–	6	μA
Input impedance at 1 MHz	I_D = 1 μA	$\lvert Z_D\rvert$	–	10	–	kΩ

* X = don't care.

parameter	conditions	symbol	min.	typ.	max.	unit
LF gain						
Maximum DC gain						
for: $A_1 = \left\lvert \frac{I_{Re1}}{I_{D1} + I_{D2}} \right\rvert$;						
$I_{D3} = I_{D4} = 0$	V_{GCLF} = 3,5 V					
at $I_{D1} = 0\ \mu A$; $I_{D2} = 1\ \mu A$		A_{11}	S_1–10%	S_1	S_1	
at $I_{D1} = 1\ \mu A$; $I_{D2} = 0\ \mu A$		A_{12}	S_1 or 55	S_1	S_1	
for: $A_2 = \left\lvert \frac{I_{Re2}}{I_{D3} + I_{D4}} \right\rvert$;						
$I_{D1} = I_{D2} = 0$	V_{GCLF} = 3,5 V					
at $I_{D3} = 0\ \mu A$; $I_{D4} = 1\ \mu A$		A_{21}	S_1–10%	S_1	S_1	
at $I_{D3} = 1\ \mu A$; $I_{D4} = 0\ \mu A$		A_{22}	S_1 or 55	S_1	S_1	
S_1 mean value of A_{11}, A_{12}, A_{21}, A_{22}			55	64	84	
Minimum DC gain						
for: $A_3 = \left\lvert \frac{I_{Re1}}{I_{D1} + I_{D2}} \right\rvert$;						
$I_{D3} = I_{D4} = 0$	V_{GCLF} = 0,8 V					
at $I_{D1} = 0\ \mu A$; $I_{D2} = 1\ \mu A$		A_{31}	S_2–1	S_2	S_2+1	
at $I_{D1} = 1\ \mu A$; $I_{D2} = 0\ \mu A$		A_{32}	S_2–1	S_2	S_2+1	
for: $A_4 = \left\lvert \frac{I_{Re2}}{I_{D3} + I_{D4}} \right\rvert$;						
$I_{D1} = I_{D2} = 0$	V_{GCLF} = 0,8 V					
at $I_{D3} = 0\ \mu A$; $I_{D4} = 1\ \mu A$		A_{41}	S_2–1	S_2	S_2+1	
at $I_{D3} = 1\ \mu A$; $I_{D4} = 0\ \mu A$		A_{42}	S_2–1	S_2	S_2+1	
S_2 mean value of A_{31}, A_{32}, A_{41}, A_{42}			–0,1	0,7	3	

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
LF gain (continued)						
AC gain for:						
$G_4 = 20 \log P_1$; $I_{D3} = I_{D4} = 0$						
at $I_{D1} = 0$; $I_{D2(p-p)} = 1\ \mu A + 2\ \mu ADC$	note 6	G_4	−4,5	−3	−1,5	dB
at $I_{D1(p-p)} = 1\ \mu A + 2\ \mu ADC$; $I_{D2} = 0$	note 6	G_4	−4,5	−3	−1,5	dB
$G_5 = 20 \log P_2$; $I_{D1} = I_{D2} = 0$						
at $I_{D3} = 0$; $I_{D4(p-p)} = 1\ \mu A + 2\ \mu ADC$	note 7	G_5	−4,5	−3	−1,5	dB
at $I_{D3(p-p)} = 1\ \mu A + 2\ \mu ADC$; $I_{D4} = 0$	note 7	G_5	−4,5	−3	−1,5	dB
Gain control (GCLF)						
Input voltage for:						
minimum LF gain		V_{GCLF}	–	1	–	V
maximum LF gain		V_{GCLF}	–	2,8	–	V
Input impedance		$\lvert Z_{GCLF} \rvert$	–	25	–	MΩ
Threshold total LF current	I_{DT3}		–	1,6	–	mA
Output current (see Fig. 7)						
$\Delta V_{DET} < V_{DETn2}$ or $\Delta V_{DET} > V_{DETp2}$	$I_{DT} < I_{DT3}$	I_{GCLF}	–	−0,6 I_{Bgc}	± 10	μA
	$I_{DT} > I_{DT3}$; note 8	I_{GCLF}	S_6−10	S_6	S_6+10	μA
$V_{DETn2} < \Delta V_{DET} < V_{DETp2}$		I_{GCLF}	–	−0,2 I_{Bgc}	± 2	μA
Re1, Re2 outputs (pin 21, pin 20)						
Output current	V_{GCLF} = 3,5 V					
at $I_{D1} = I_{D2} = 1\ \mu A$; $I_{D3} = I_{D4} = 0$		I_{Re1}	110	128	168	μA
at $I_{D1} = I_{D2} = I_{D3} = I_{D4} = 0$		I_{Re1}	–	0	–	μA
at $I_{D1} = I_{D2} = 0$; $I_{D3} = I_{D4} = 1\ \mu A$		I_{Re2}	110	128	168	μA
at $I_{D1} = I_{D2} = I_{D3} = I_{D4} = 0$		I_{Re2}	–	0	–	μA
Output voltage						
pin 21		V_{Re1}	1	–	V_P	V
pin 20		V_{Re2}	1	–	V_P	V
Output impedance						
pin 21		$\lvert Z_{Re1} \rvert$	–	1	–	MΩ
pin 20		$\lvert Z_{Re2} \rvert$	–	1	–	MΩ

parameter	conditions	symbol	min.	typ.	max.	unit
Reference current (I_{ret})						
$I_{ret} = I_{Re1} = I_{Re2}$	note	I_{ret}	200	220	240	μA
LPF output (pin 14)						
DC voltage level	note 9	V_{LPF}	$V_P-2,1$	$V_P-1,7$	$V_P-1,4$	V
Input impedance		$\lvert Z_{LPF}\rvert$	–	3	–	kΩ
FOC START input (pin 9)						
Start current (ST) for FE ($-I_{FOC\ START} = I_{ST}$)	Si/$\overline{RD}$ = HIGH Z	I_{ST}	75	150	500	μA
	Si/$\overline{RD}$ = LOW	I_{ST}	–	0	–	μA
Start voltage (ST) for FE ($V_{FOC\ START} = V_{ST}$)	Si/$\overline{RD}$ = HIGH Z	V_{ST}	430	530	630	mV
	Si/$\overline{RD}$ = LOW	V_{ST}	−20	0	20	mV
FElag output (pin 16)	see Fig. 8					
Output voltage						
TDA8808T		V_{FElag}	$V_{ext}+1,5$	–	$V_P-1,5$	V
TDA8808AT		V_{FElag}	+1,5	–	$V_{ext}-1,5$	V
Output impedance		$\lvert Z_{FElag}\rvert$	–	8	–	MΩ
Output current	Si/$\overline{RD}$ = HIGH Z; V_{GCLF} = 3,5 V					
$I_{D1} = I_{D2} = I_{D3} = I_{D4} = 1\ \mu A$	$V_{Sc} = V_P$	$I_{FElag} = I_O$	−10	0	+10	μA
$I_{D2} = I_{D3} = 1\ \mu A$; $I_{D1} = I_{D4} = 2\ \mu A$	$V_{Sc} = V_P$	I_{FElag}	−10%	$-2S_1 + I_O$	+10%	μA
$I_{D2} = I_{D3} = 2\ \mu A$; $I_{D1} = I_{D4} = 1\ \mu A$	$V_{Sc} = V_P$	I_{FElag}	−10%	$-2S_1 + I_O$	+10%	μA
$I_{D2} = I_{D3} = 2\ \mu A$; $I_{D1} = I_{D4} = 1\ \mu A$	V_{Sc} = 1,5 V	I_{FElag}	−5	0	+5	μA
$I_{D2} = I_{D3} = 1\ \mu A$; $I_{D1} = I_{D4} = 2\ \mu A$	V_{Sc} = 1,5 V	I_{FElag}	−5	0	+5	μA

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
FE output (pin 15)	see Fig. 8					
Output voltage						
TDA8808T		V_{FE}	$V_{ext}+1,5$	–	$V_P-1,5$	V
TDA8808AT		V_{FE}	+1,5	–	$V_{ext}-1,5$	V
Output impedance		$\|Z_{FE}\|$	–	8	–	MΩ
Output current	note 10					
$I_{D1} = I_{D4} = 2\ \mu A$; $I_{D2} = I_{D3} = 1\ \mu A$	$V_{Sc} = 0$	I_{FE}	−10%	$-2S_1-134-I_{ST}$	+10%	μA
$I_{D1} = I_{D4} = 1\ \mu A$; $I_{D2} = I_{D3} = 2\ \mu A$	$V_{Sc} = 0$	I_{FE}	−10%	$-4S_1-67-I_{ST}$	+10%	μA
$I_{D1} = I_{D4} = 2\ \mu A$; $I_{D2} = I_{D3} = 1\ \mu A$	$V_{Sc} = 1,25$ V	I_{FE}	−10%	$-2S_1-134+I_{ST}$	+20%	μA
$I_{D1} = I_{D4} = 1\ \mu A$; $I_{D2} = I_{D3} = 2\ \mu A$	$V_{Sc} = 1,25$ V	I_{FE}	−10%	$-4S_1-67+I_{ST}$	+20%	μA
$I_{D1} = I_{D4} = 2\ \mu A$; $I_{D2} = I_{D3} = 1\ \mu A$	$V_{Sc} = 1,75$ V	I_{FE}	−20%	$-2S_1+67+I_{ST}$	+10%	μA
$I_{D1} = I_{D4} = 1\ \mu A$; $I_{D2} = I_{D3} = 2\ \mu A$	$V_{Sc} = 1,75$ V	I_{FE}	−10%	$-4S_1-67+I_{ST}$	+20%	μA
$I_{D1} = I_{D4} = 2\ \mu A$; $I_{D2} = I_{D3} = 1\ \mu A$	$V_{Sc} = V_P$	$I_{FE} = S_6$	−20%	67	+20%	μA
$I_{D1} = I_{D4} = 1\ \mu A$; $I_{D2} = I_{D3} = 2\ \mu A$	$V_{Sc} = V_P$	I_{FE}	−15%	$-S_6$	+15%	μA
$I_{D1} = I_{D2} = I_{D3} = I_{D4} = 1\ \mu A$	$V_{Sc} = V_P$	I_{FE}	−10	0	+10	μA
$I_{D1} = I_{D2} = I_{D3} = I_{D4} = 0$	$V_{Sc} = V_P$	I_{FE}	−5	0	+5	μA

parameter	conditions	symbol	min.	typ.	max.	unit
$\overline{\text{DODS}}$ logic input (pin 12)						
Switching levels						
input voltage LOW		$V_{\overline{DODS}}$	–	–	+0,8	V
input voltage HIGH		$V_{\overline{DODS}}$	+2	–	–	V
Input source current		$I_{\overline{DODS}}$	–35	–25	–15	μA
Starting input (Sc)	see Fig. 9					
Output voltage	Si/$\overline{\text{RD}}$ = LOW	V_{Sc}	–	0	–	V
Output voltage	S1/$\overline{\text{RD}}$ = HIGH Z	V_{Sc}	–	–	V_P–0,5	V
Output impedance		$\lvert Z_{Sc} \rvert$	–	*	–	MΩ
Output source current	Si/$\overline{\text{RD}}$ = HIGH Z; V_{Sc} = 1,5 V	I_{Sc}	–1,2	–1	–0,8	μA
Output sink current	Si/$\overline{\text{RD}}$ = LOW	I_{Sc}	0,5	1,2	2,0	mA
Si/$\overline{\text{RD}}$ logic input/output (pin 20)	see Fig. 9					
Voltage "forced LOW"	$I_{Si/\overline{RD}}$ = 400 μA; V_{Sc} = 2,5 V; $V_{GCLF} < 2{,}8$ V	$V_{Si/\overline{RD}}$	–	0,15	0,4	V
Switching levels						
input voltage LOW		$V_{Si/\overline{RD}}$	–	–	+0,8	V
input voltage HIGH Z	$I_{Si/\overline{RD}}$ = –5 μA	$V_{Si/\overline{RD}}$	2,4	2,8	–	V
Input source current LOW		$I_{Si/\overline{RD}}$	–35	–25	–15	μA
$\overline{\text{TL}}$ logic output (pin 11)	see Fig. 6					
Output voltage level LOW	$I_{\overline{TL}}$ = 400 μA; (sink current)	$V_{\overline{TL}}$	–	0,15	0,4	V
Output voltage level HIGH	$I_{\overline{TL}}$ = –50 μA; (source current)	$V_{\overline{TL}}$	2,4	–	–	V
Threshold total LF current	I_{DT2}		–	3,9	–	μA
Output voltage	DODS = HIGH (≥ 2,4 V)					
$\Delta V_{DET} < V_{DETn2}$ or $\Delta V_{DET} > V_{DETp2}$	I_{DT} don't care	$V_{\overline{TL}}$	2,4	–	–	V
$V_{DETn1} < \Delta V_{DET} < V_{DETp1}$	I_{DT} don't care	$V_{\overline{TL}}$	2,4	–	–	V
$V_{DETn2} < V_{DET} < V_{DETn1}$ or $V_{DETp1} < \Delta V_{DET} < V_{DETp2}$	$I_{DT} < I_{DT2}$	$V_{\overline{TL}}$	2,4	–	–	V
$V_{DETn2} < V_{DET} < V_{DETn1}$ or $V_{DETp1} < V_{DET} < V_{DETp2}$	$I_{DT} > I_{DT2}$	$V_{\overline{TL}}$	–	0,15	0,4	V

* Value to be fixed.

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
$\overline{TL}$ logic output (continued)						
Output voltage	$\overline{DODS}$ = LOW ($\leqslant$ 0,8 V)					
$\Delta V_{DET} < V_{DETn2}$ or $\Delta V_{DET} > V_{DETp2}$	I_{DT} don't care	$V_{\overline{TL}}$	2,4	–	–	V
$V_{DETn2} < \Delta V_{DET} < V_{DETp2}$	$I_{DT} < I_{DT2}$	$V_{\overline{TL}}$	2,4	–	–	V
$V_{DETn2} < \Delta V_{DET} < V_{DETp2}$	$I_{DT} > I_{DT2}$	$V_{\overline{TL}}$	–	0,15	0,4	V
Output sink current	$V_{\overline{TL}}$ = LOW	$I_{\overline{TL}}$	1	2,2	–	mA
Output source current	$V_{\overline{TL}}$ = HIGH	$I_{\overline{TL}}$	–	–100	–50	μA
Delay times (see Fig. 10)	see Fig. 6	$\tau 1$	7	8,5	10	μs
		$\tau 2$	$\tau 1$–15% or 6,5	–	$\tau 1$+ 5% or 10	μs
		$\tau 3$	7	8,5	10	μs
		$\tau 4$	$\tau 3$–10% or 7	–	$\tau 3$+10% or 10	μs
LO output (pin 17)						
Output voltage		V_{LO}	–	–	V_P – 0,5	V
Output impedance		$\lvert Z_{LO} \rvert$	–	95	–	kΩ
Output leakage current	Si/$\overline{RD}$ = LOW	I_{LO}	–10	–0,1	0	μA
Maximum output current	Si/$\overline{RD}$ = HIGH Z	I_{LO}	–8	–4	–2	mA
LM input (pin 18)						
Input voltage	closed loop	V_{LM}	185	205	225	mV
Input bias current		I_{LM}	–2	–	–	μA
Laser supply						
Transconductance						
For DC (note 11)	Si/$\overline{RD}$ = HIGH Z	G_{LDC}	–	0,5	–	A/V
	Si/$\overline{RD}$ = LOW	G_{LDC}	–	0	–	A/V
For AC (note 12) delay time		τLO	–	*	–	ns

* Value to be fixed.

Notes to the characteristics

1. Voltage output signal V_{O1} measured at f_{HFin} = 700 kHz; $I_{HFin(p\text{-}p)}$ = 7 μA; V_{GCHF} = 2,4 V.
   Voltage output signal V_{O2} measured at f_{HFin} = 100 kHz; $I_{HFin(p\text{-}p)}$ = 7 μA; V_{GCHF} = 2,4 V.
2. Voltage output signal V_{O1} measured at f_{HFin} = 1 MHz; $I_{HFin(p\text{-}p)}$ = 7 μA; V_{GCHF} = 2,4 V.
   Voltage output signal V_{O2} measured at f_{HFin} = 100 kHz; $I_{HFin(p\text{-}p)}$ = 7 μA; V_{GCHF} = 2,4 V.
3. Phase of input/output signal, group delay and flatness measured at $I_{HFin(p\text{-}p)}$ = 1 μA; V_{GCHF} = 4 V.

   Group delay: $\tau = \frac{d\phi}{dw}$; $\Delta f \approx 50$ kHz.

   Flatness: $\Delta\tau = \tau_{max} - \tau_{min}$.
4. HF part output vpltage for closed loop conditions; f_{HFin} = 500 kHz.
5. HF part output voltage for closed loop conditions; f_{HFin} = 0,1 to 1 MHz.
   M_1 is the measured value of V_{O1}.
6. P_1 is the measured value of $\frac{I_{Re1}(1)}{I_{D1}(1) + I_{D2}(1)} \cdot \frac{I_{D1}(2) + I_{D2}(2)}{I_{Re1}(2)}$

   Where:

   (1) are the current levels at f_i = 25 kHz.
   (2) are the current levels at f_i = 1 kHz.

   Measurement taken at V_{GCLF} = 3,5 V.
7. P_2 is the measured value of $\frac{I_{Re2}(1)}{I_{D3}(1) + I_{D4}(1)} \cdot \frac{I_{D3}(2) + I_{D4}(2)}{I_{Re2}(2)}$

   Where:

   (1) are the current levels at f_i = 25 kHz.
   (2) are the current levels at f_i = 1 kHz.

   Measurement taken at V_{GCLF} = 3,5 V.
8. S_6, is the measured value of $S_1 \cdot \frac{I_{DT}}{4} - 1{,}1\ I_{Bgc}$

   Measurement taken at V_{GCLF} = 3,5 V.
9. LF part reference current I_{ret} and low-pass filter output voltage for closed loop conditions.
   Measurement taken at $I_{DT} > I_{DT3}$; $\Delta V_{DET} < V_{DETn2}$ or $\Delta V_{DET} > V_{DETp2}$.
10. FE output current measured at V_{GCLF} = 3,5 V and Si/$\overline{RD}$ = HIGH Z; $I_{ST} = \frac{V_{FOC\ START}}{R_{FOC\ START}}$.
11. Laser supply transconductance for DC

    $G_{LDC} = \frac{\Delta I_{LO}}{\Delta V_{LM}}$ $(0 < -I_{LO} < 2$ mA).
12. Laser supply transconductance for AC

    $G_{LAC} = G_{LO} \cdot \frac{1}{1 + S \cdot \tau LO}$

    Where: S is the laplace operator in the frequency domain.

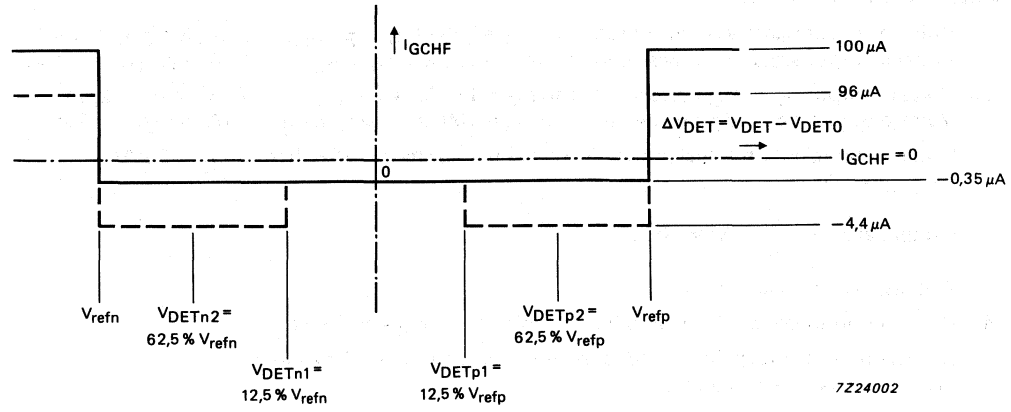
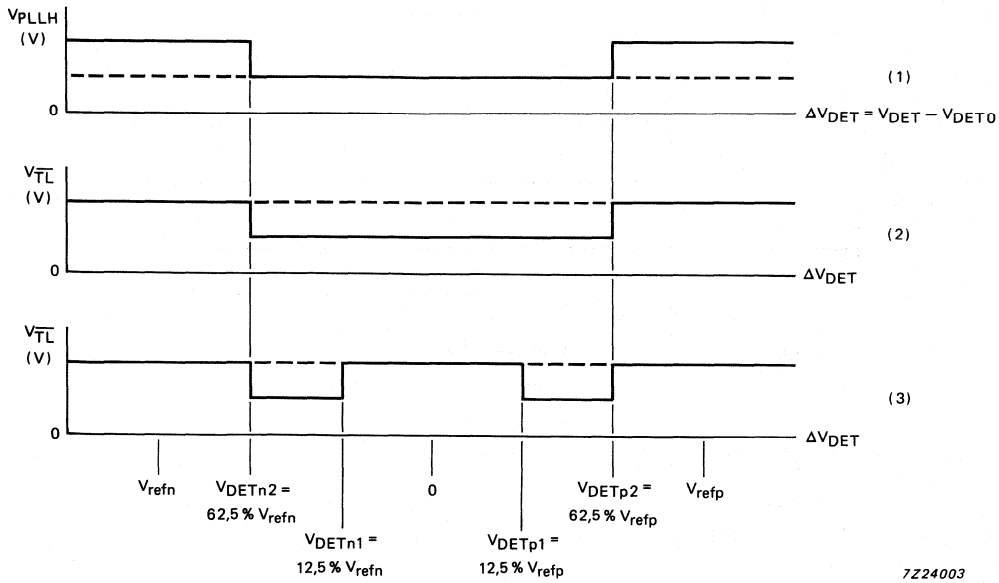


Fig. 5 HF gain control current (I_{GCHF}) as a function of input voltage ΔV_{DET}.



(1)

——— $I_{DT} > I_{DT1}$

--------- $I_{DT} < I_{DT1}$

$I_{DT} = I_{D1} + I_{D2} + I_{D3} + I_{D4}$

$I_{DT1} = 2{,}67\ I_{Bgc}/S_1$

$I_{DT2} = 5\ I_{Bgc}/S_1$

S_1 = average maximum LF gain

(2)

——— $I_{DT} > I_{DT2}$

--------- $I_{DT} < I_{DT2}$

$\overline{DODS}$ = LOW

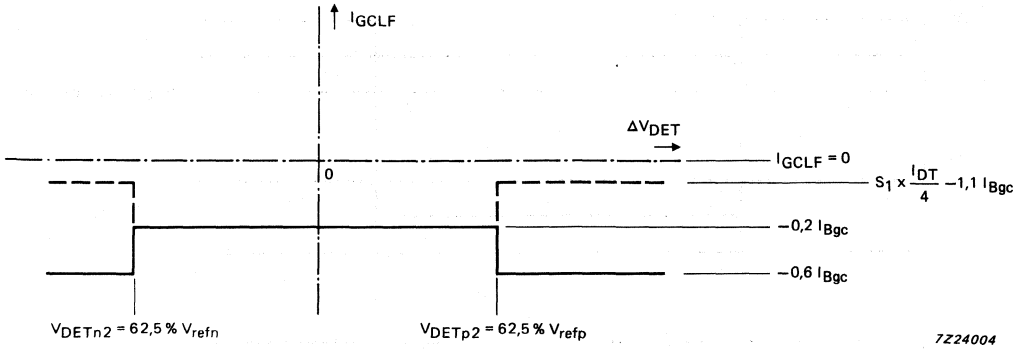
(3)

——— $I_{DT} > I_{DT2}$

--------- $I_{DT} < I_{DT2}$

$\overline{DODS}$ = HIGH

Fig. 6 $\overline{TL}$ voltage as a function of input voltage ΔV_{DET}.



---------- $I_{DT} > I_{DT3}$

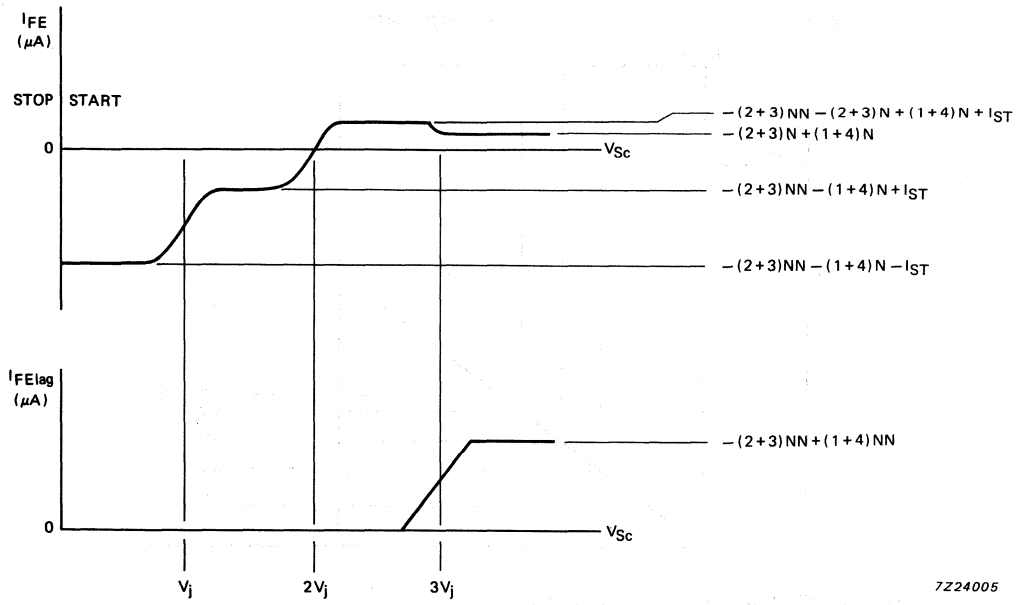
——— $I_{DT} < I_{DT3}$

$I_{DT} = I_{D1} + I_{D2} + I_{D3} + I_{D4}$

$I_{DT3} = 2\ I_{Bgc}/S_1$

S_1 = average maximum LF gain

Fig. 7 LF gain control current (I_{GCLF}) as a function of input voltage ΔV_{DET}.



I_{ST} $= -I_{FOC\ START}$

I_{cont} $= 2\ I_{Bgc}$ if $I_{DT} > I_{DT3}$

I_{cont} $= I_{DT} \times S_1$ if $I_{DT} < I_{DT3}$

I_{DT} $= I_{D1} + I_{D2} + I_{D3} + I_{D4}$

I_{DT3} $= 2\ I_{Bgc}/S_1$

S_1 = average maximum LF gain

(1 + 4)NN = not normalized currents = $(I_{D1} + I_{D4})\ S_1$

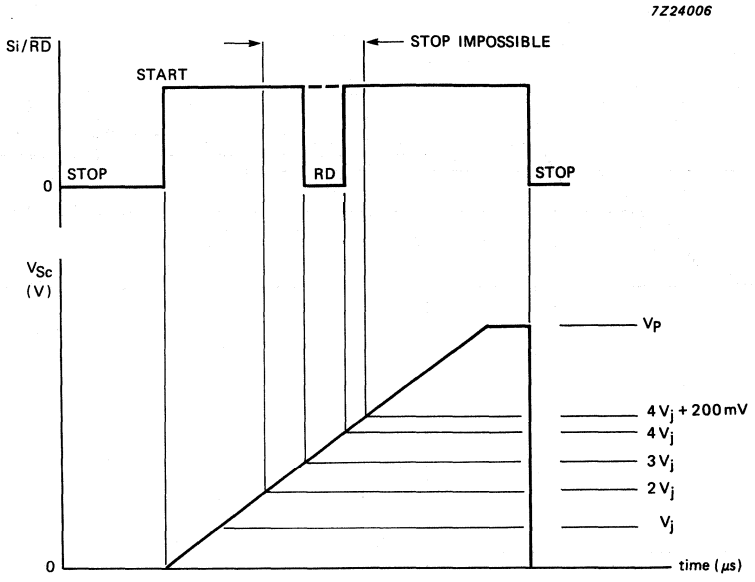
(2 + 3)NN = not normalized currents = $(I_{D2} + I_{D3})\ S_1$

(1 + 4)N = normalized currents = $\left(\frac{I_{D1}}{I_{D1}+I_{D2}} + \frac{I_{D4}}{I_{D3}+I_{D4}}\right) \times I_{cont}$

(2 + 3)N = normalized currents = $\left(\frac{I_{D2}}{I_{D1}+I_{D2}} + \frac{I_{D3}}{I_{D3}+I_{D4}}\right) \times I_{cont}$

V_j is the junction voltage (0,7 V typ.).

Fig. 8 FElag current output as a function of starting voltage input (V_{Sc}).



RD : Si/$\overline{RD}$ forced LOW for ready signal

——— $V_{GCLF} < 2{,}8$ V

--------- $V_{GCLF} > 3{,}5$ V

V_j is the junction voltage (0,7 V typ.)

Fig. 9 Si/$\overline{RD}$ signal as a function of V_{Sc}.

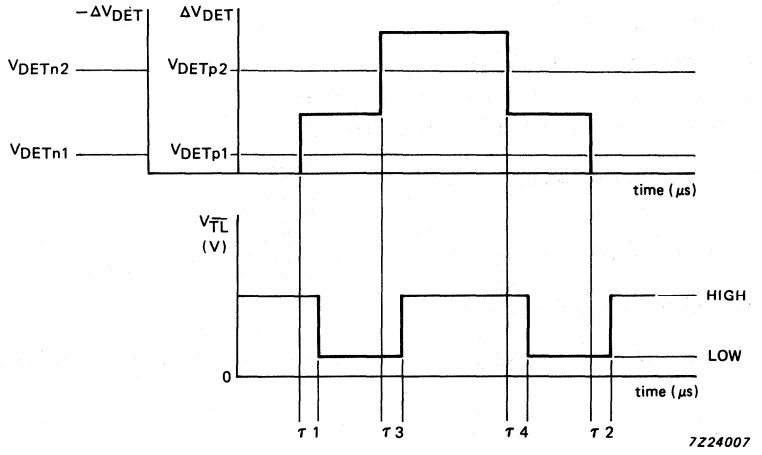


Fig. 10 Delay times between ΔV_{DET} and $V_{\overline{TL}}$.

RADIAL ERROR SIGNAL PROCESSOR FOR COMPACT DISC PLAYERS

GENERAL DESCRIPTION

The TDA8809T is a bipolar integrated circuit which provides control signals for the radial motor. These control signals are generated from radial error signals received from a photo-diode signal processor (TDA8808), and velocity control signals from the control processor.

Features

- Tracking error processor with automatic asymmetry control
- AGC circuitry with automatic start-up and wobble generator
- Tracking control for fast forward/reverse scan, search, repeat and pause functions
- Radial polarity - 4 - tracks counting
- Possibility for car, home and portable applications

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage range		V_P	4,5	5,0	5,5	V
External voltage range						
pin 12		$V_{ext(+)}$	V_P	10	12	V
pin 13		$V_{ext(-)}$	−5,5	−5,0	0	V
pin 12 to pin 13		$V_{ext(+)} - V_{ext(-)}$	4,5	–	12	V
Supply current		I_P	–	5,3	–	mA
Operating ambient temperature range		T_{amb}	−30	–	+85	°C

PACKAGE OUTLINE

28-lead mini-pack; plastic (SO28; SOT136A).

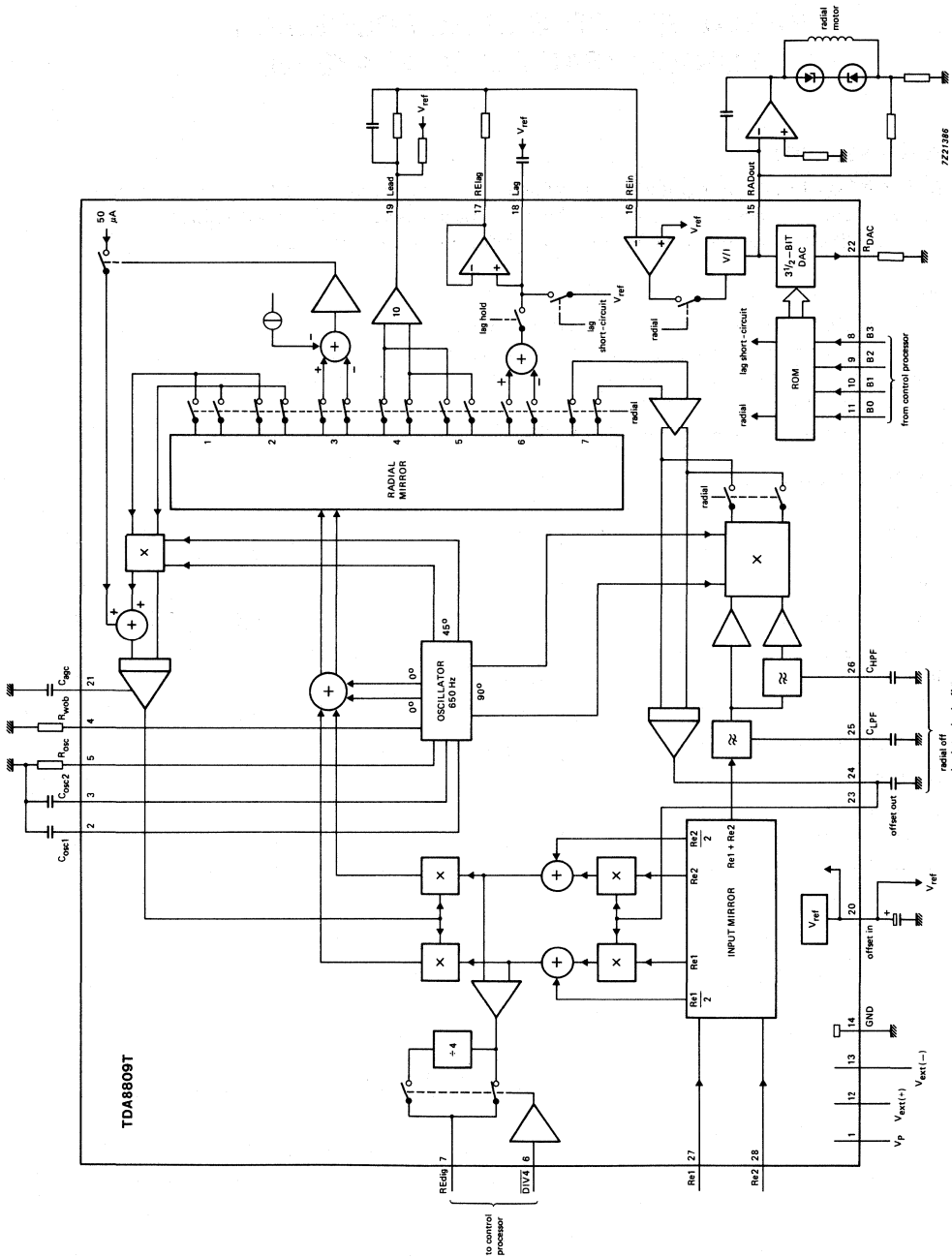


Fig. 1 Block diagram.

PINNING

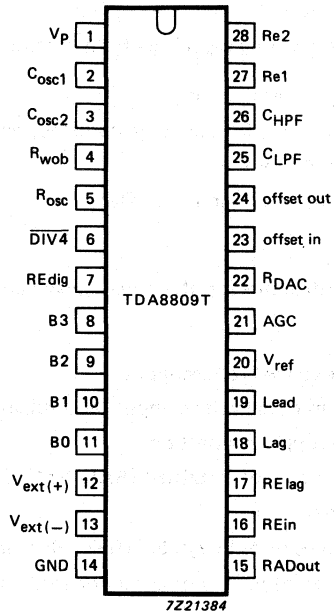


Fig. 2 Pinning diagram.

Pin functions

pin	mnemonic	description
1	V_P	Positive supply voltage
2	C_{osc1}	Frequency setting capacitors for oscillator
3	C_{osc2}	
4	R_{wob}	Wobble generator input
5	R_{osc}	Biassing resistor for oscillator frequency and internal amplitude
6	$\overline{DIV4}$	Divide-by-4 input
7	REdig	Digital output of sign (Re2 - Re1)
8	B3	Input control bits for off-, catch-, play-status and DAC output current
9	B2	
10	B1	
11	B0	
12	$V_{ext(+)}$	Positive external voltage input
13	$V_{ext(-)}$	Negative external voltage input (also substrate connection)
14	GND	Negative supply connection
15	RADout	Current output of amplified (Re2 - Re1) input currents
16	REin	Radial error input
17	RElag	Voltage output of integrated (Re2 - Re1) input currents
18	Lag	Connection of integrator capacitor for (Re1 - Re2) input currents
19	Lead	Lead output
20	V_{ref}	Internal reference voltage output
21	AGC	Gain control input for radial error signal
22	R_{DAC}	Biassing resistor for current output for track jumping (3½ bits)
23	offset in	Offset control input for radial offset
24	offset out	Offset control output for radial offset
25	C_{LPF}	Low-pass filter for Re1 and Re2, used for radial offset control
26	C_{HPF}	High-pass filter for Re1 and Re2, used for radial offset control
27	Re1	Input for amplified currents from photo-diodes D1 and D2
28	Re2	Input for amplified currents from photo diodes D3 and D4

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage ranges (see Fig. 3)				
pin 1 to pin 14	V_P	−0,3	13	V
pin 12 to pin 13	V_{ext}	−0,3	13	V
pin 14 to pin 13	$V_{ext(-)}$	−0,3	13	V
Output voltage ranges				
except RADout	V_O	0	V_P	V
RADout	V_O	$V_{ext(-)}$	$V_{ext(+)}$	V
R_{DAC} current range	I_{RDAC}	50	250	μA
Total power dissipation	P_{tot}	see Fig. 4		
Storage temperature range	T_{stg}	−55	+150	°C
Operating ambient temperature range	T_{amb}	−30	+85	°C
Operating junction temperature	T_j	−	150	°C

THERMAL RESISTANCE

From junction to ambient $R_{th\ j\text{-}a}$ = 140 K/W

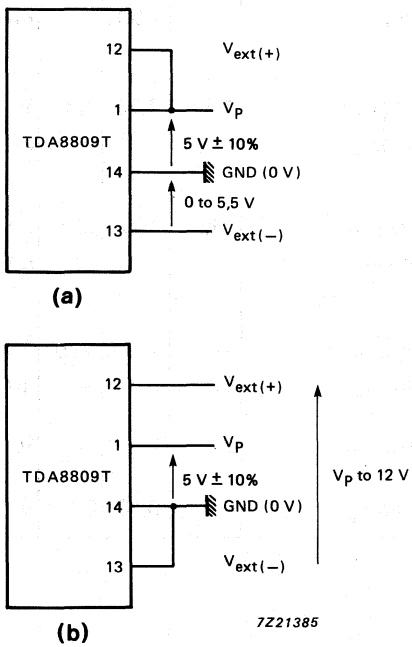


Fig. 3 Supply voltages;
(a) Home application (b) Car application.

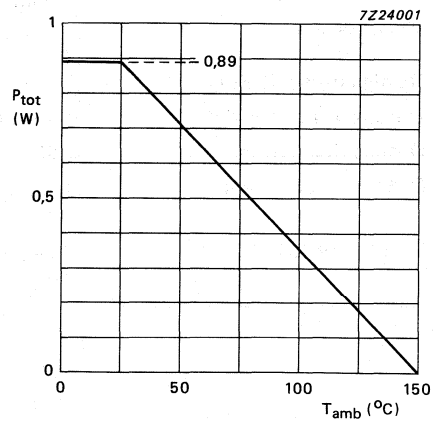


Fig. 4 Power derating curve.

CHARACTERISTICS

V_P = + 5 V; V_{GND} = 0 V; $V_{ext(+)}$ = + 5 V; $V_{ext(-)}$ = −5 V; I_{RDAC} (pin 22) = −75 μA; I_{Rwob} (pin 4) = −8 μA; I_{Rosc} (pin 5) = −50 μA; V_{RADout} = 0 V; $V_{offset\ in}$ = V_{lead} = V_{lag} = V_{Cosc1} = V_{Cosc2} = V_{ref}; $V_{offset\ in}$ is connected to $V_{offset\ out}$; T_{amb} = 25 °C; all voltages measured with respect to V_{GND}; unless otherwise specified.

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage range		V_P	4,5	5,0	5,5	V
External voltage range (see Fig. 3)						
pin 12		$V_{ext(+)}$	V_P	10	12	V
pin 13		$V_{ext(-)}$	−5,5	−5,0	0	V
pin 12 to pin 13		$V_{ext(+)} - V_{ext(-)}$	4,5	–	12	V
Supply current		I_P	4,0	5,3	6,6	mA
Reference output (V_{ref})						
Output voltage	$I_{Vref} \leqslant \pm 1$ mA	V_{ref}	2,25	2,45	2,65	V
Output impedance		$\lvert Z_O \rvert$	–	25	–	Ω
Reference input (R_{osc})						
Input voltage level	I_{Rosc} = −50 μA	V_{Rosc}	1,1	1,24	1,3	V
Input current		I_{Rosc}	–	−50	–	μA
Reference input (R_{DAC})						
Input voltage level	I_{RDAC} = −75 μA	V_{RDAC}	1,1	1,23	1,3	V
Input current		I_{RDAC}	–	−75	–	μA
Reference input (R_{wob})						
Input voltage level	I_{Rwob} = −8 μA	V_{Rwob}	150	165	180	mV
Input current		I_{Rwob}	–	−8	–	μA
REdig output (REdig)						
Output source current	note 1 (A)	I_{REdig}	–	−160	−50	μA
Output sink current	note 1 (B)	I_{REdig}	0,4	3,5	–	mA
Output voltage HIGH	I_{REdig} = −50 μA; note 1 (A)	V_{REdig}	2,4	–	–	V
Output voltage LOW	I_{REdig} = 400 μA; note 1 (B)	V_{REdig}	0	0,13	0,4	V

parameter	conditions	symbol	min.	typ.	max.	unit
Digital inputs						
B0, B1, B2 and B3						
Input voltage HIGH	note 2	V_{IH}	2,0	–	V_P	V
Input voltage LOW	note 2	V_{IL}	0	–	0,8	V
Input sink current HIGH		I_{IH}	0	0,03	1,0	μA
Input source current LOW		I_{IL}	−3,0	−0,1	0	μA
Divide-by-4 input ($\overline{DIV4}$)						
Input voltage HIGH	divide-by-1	V_{IH}	2,0	–	V_P	V
Input voltage LOW	divide-by-4	V_{IL}	0	–	0,8	V
Input sink current HIGH		I_{IH}	0	5,0	*	μA
Input source current LOW		I_{IL}	−10	−3	0	μA
Input frequency at Re1 and Re2		f_i	–	10	50	kHz
Radial error inputs (Re1; Re2)						
Input voltage level	$I_{Re1} = I_{Re2} = -110\,\mu A$	V_{Re1}, V_{Re2}	$V_P-1,81$	$V_P-1,71$	$V_P-1,61$	V
Input current		I_{Re1}, I_{Re2}	–	−110	–	μA
Input impedance		$\lvert Z_{Re1}\rvert, \lvert Z_{Re2}\rvert$	–	2,5	–	kΩ
Gain control input (AGC)	rad on; lag hold off					
Offset current	$V_{AGC} = 3,8$ V; $I_{Re1} = I_{Re2} = 0$	I_{AGC}	−0,2	0	0,2	μA
Lag current for	$I_{Re1} = -85\,\mu A$; $I_{Re2} = -115\,\mu A$					
minimum radial gain	$V_{AGC} = 0,6$ V	I_{lag}	−2,5	−0,45	+ 1,5	μA
maximum radial gain	$V_{AGC} = 3,8$ V	I_{lag}	−42	−30	−18	μA
Input impedance		$\lvert Z_{AGC}\rvert$	–	*	–	MΩ
Gain	$V_{AGC} = 3,8$ V; $V_{Cosc2} = V_{ref} + 1,4$ V; $V_{Cosc1} = V_{ref}$; $I_{Re1} = -100\,\mu A$; $I_{Re2} = -100\,\mu A$	I_{AGC0}	–	−2	–	μA
	$I_{Re1} - I_{Re2} = 4\,\mu A$ − I_{AGC0} then $I_{Re1} - I_{Re2} = -4\,\mu A$ − I_{AGC0}	$\frac{\Delta I_{AGC}}{\Delta(I_{Re1}-I_{Re2})}$	0,7	0,9	1,1	

* Value to be fixed.

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Gain control (continued)						
Radial error trackcrossing	rad off; V_{AGC} = 3,8 V $I_{Re2}-I_{Re1}$ = −12 μA; $I_{Re2}+I_{Re1}$ = −200 μA	I_{AGC}	−3	0	3	μA
	$I_{Re2}-I_{Re1}$ = −48 μA; $I_{Re2}+I_{Re1}$ = −200 μA	I_{AGC}	39	49	59	μA
Offset control (offset out)						
Offset current	rad on; I_{CHPF} = 0; $I_{Re1}=I_{Re2}$ = −110 μA	$I_{offset\ out}$	−0,1	0	0,1	μA
Offset lag current for	rad on; lag hold off; V_{AGC} = 3,8 V; $I_{Re1}=I_{Re2}$ = −100 μA					
minimum amplification Re1 maximum amplification Re2	$V_{offset\ in}$ = V_{ref} − 1,2 V	I_{lag}	−115	−100	−85	μA
minimum amplification Re2 maximum amplification Re1	$V_{offset\ in}$ = V_{ref} + 1,2 V	I_{lag}	+ 85	+100	+115	μA
Offset lag current	note 3	I_{lag}	−7	0	+ 7	μA
Transconductance factor						
	rad off; V_{AGC} = 3,8 V; $I_{Re1}=I_{Re2}$ = −100 μA; $V_{range\ offset\ in}$ = 0,6 V (int.); $I_{tot}=I_{Re1}+I_{Re2}$	$\frac{\Delta I_{offset\ out}}{\Delta V_{offset\ in}.I_{tot}}.V_{range\ offset\ in}$	0,17	0,21	0,25	
	rad off; $V_{AGC}=V_{GND}$ $I_{Re1}=I_{Re2}$ = −100 μA; $V_{range\ offset\ in}$ = 0,6 V (int.); $I_{tot}=I_{Re1}+I_{Re2}$	$\frac{\Delta I_{offset\ out}}{\Delta V_{offset\ in}.I_{tot}}.V_{range\ offset\ in}$	−0,1	0	0,1	
Input impedance		$\lvert Z_{offset\ in}\rvert$	−	*	−	MΩ
High-pass filter (C_{HPF})						
Voltage level at I_{CHPF} = 0	$I_{Re1}=I_{Re2}$ = 0; I_{CLPF} = 0	V_{CHPF}	V_P −0,82	V_P −0,72	V_P −0,62	V
Transresistance from Re1, Re2 to C_{HPF}	$I_{Re1}+I_{Re2}$ = −200 μA	$\frac{\Delta V_{CHPF}}{\Delta(I_{Re1}-I_{Re2})}$	−200	*	200	Ω
		$\frac{\Delta V_{CHPF}}{\Delta(I_{Re1}+I_{Re2})}$	6,2	8,8	11,5	kΩ
Input impedance		$\lvert Z_{CHPF}\rvert$	−	8	−	kΩ

* Value to be fixed.

parameter	conditions	symbol	min.	typ.	max.	unit
Low-pass filter (C_{LPF})						
Voltage level at $I_{CLPF} = 0$	$I_{Re1} = I_{Re2} = 0$	V_{CLPF}	4,7	–	V_P	V
Input impedance		$\lvert Z_{CLPF} \rvert$	–	8	–	kΩ
RElag output						
Output voltage range	$I_{RElag} = -200\ \mu A$; $V_{lag} = 4{,}25$ V	V_{RElag}	$V_P-1{,}1$	–	–	V
	$I_{RElag} = 200\ \mu A$; $V_{lag} = 0{,}9$ V	V_{RElag}	–	–	1,1	V
Maximum source current output	$V_{lag} = 4{,}1$ V	I_{RElag}	–6,0	–3,5	–1,0	mA
Maximum sink current output	$V_{lag} = 0{,}9$ V	I_{RElag}	2,5	4,1	5,5	mA
Output impedance	f = < 10 kHz	$\lvert Z_{RElag} \rvert$	–	–	50	Ω
Offset ($V_{RElag}-V_{ref}$)	lag short-circuit on; lag hold on	$V_{RElag\ offset}$	–10	–	10	mV
Transfer lag ⟶ RElag	f = < 10 kHz; lag short-circuit off; lag hold on	$\frac{V_{RElag}}{V_{lag}}$	–5%	1	5%	
Slew rate						
RElag output amplifier	lag short-circuit off; lag hold on	SR	–	0,4	–	V/μs
Lag push-pull current output, voltage input (pin 18)	note 4					
Output voltage	$I_{lag} = -20\ \mu A$; $V_{offset\ in} = V_{ref}-1{,}2$ V	V_{lag}	$V_P-1{,}5$	–	–	V
	$I_{lag} = 20\ \mu A$; $V_{offset} = V_{ref} + 1{,}2$ V	V_{lag}	–	–	1,5	V
Output impedance		$\lvert Z_{lag} \rvert$	–	*	–	MΩ
Switch lag short-circuit						
Impedance $\frac{\Delta V_{lag}}{\Delta I_{lag}}$	lag short-circuit on; lag hold on; $I_{lag} = \pm 100\ \mu A$	$\lvert Z_{lag\ sc} \rvert$	–	0,4	1	kΩ
Radial error input (REin)						
Input impedance	rad on	$\lvert Z_{REin} \rvert$	–	0	–	kΩ

* Value to be fixed.

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
RADout push-pull current output						
Output voltage	rad on I_{REin} = 180 μA; I_{RADout} = −50 μA	V_{RADout}	$V_{ext(+)}$−1,5	−	−	V
	I_{REin} = −180 μA; I_{RADout} = 50 μA	V_{RADout}	−	−	$V_{ext(-)}$+1,5	V
Current gain	rad on; I_{REin} = ± 100 μA	$\frac{I_{RADout}}{I_{REin}}$	−10%	1	10%	
Slew rate		SR	−	0,4	−	V/μs
Output impedance		$\lvert Z_{RADout} \rvert$	−	*	−	MΩ
Ratio of output current to reference current	I_{REin} = 0; I_{RDAC} = −75 μA; see also Table 1	$\frac{I_{RADout}}{I_{RDAC}}$				
			−5%	−0,5	+ 15%	
			−8%	−2	+ 12%	
			−0,02	0	0,02	
			−0,02	0	0,02	
			−14%	0,5	+ 6%	
			−12%	2	+ 8%	
			−0,1	0	0,1	
			−0,1	0	0,1	
			−5%	−0,5	+ 15%	
			−5%	−0,375	+ 15%	
			−5%	−0,25	+ 15%	
			−4%	−0,125	+ 16%	
			−14%	+ 0,5	+ 6%	
			−13%	+ 0,375	+ 7%	
			−13%	+ 0,25	+ 7%	
			−13%	+ 0,125	+ 7%	
Lead output	V_{AGC} = 3,8 V					
Output voltage	I_{Re1} = −90 μA; I_{Re2} = −100 μA; I_{lead} = −20 μA	V_{lead}	V_P−1,5	−	−	V
	I_{Re1} = −100 μA; I_{Re2} = −90 μA; I_{lead} = 20 μA	V_{lead}	−	−	1,5	V
Offset current	$I_{Re1} = I_{Re2}$ = −100 μA	$I_{lead\ offset}$	−100	0	100	μA

* Value to be fixed.

parameter	conditions	symbol	min.	typ.	max.	unit
Lead output (continued)						
Current gain	$I_{Re1} = -120\ \mu A$; $I_{Re2} = -100\ \mu A$	$\frac{\Delta I_{lead}}{\Delta(I_{Re1}-I_{Re2})}$	−11,2	−9,9	−8,8	
Output impedance		$\lvert Z_{lead}\rvert$	–	*	–	MΩ
Oscillator						
(C_{osc1} and C_{osc2} connected to 12 nF capacitors)						
Amplitude oscillation (peak-to-peak value)						
C_{osc1}		$V_{osc1(p-p)}$	1,05	1,25	1,45	V
C_{osc2}		$V_{osc2(p-p)}$	1,05	1,25	1,45	V
Operating frequency	$I_{Re1} = I_{Re2} = -110\ \mu A$	f_{osc}	690	740	790	Hz
Output voltages (peak-to-peak value)						
0° injection						
lead (pin 19)	$R_{lead} = 10\ k\Omega$	$V_{lead(p-p)}$	0,85	1,05	1,25	V
C_{lag} (pin 18)	$R_{lag} = 10\ k\Omega$; rad on; lag hold off	$V_{lag(p-p)}$	85	105	125	mV
	rad on; lag hold on	$V_{lag(p-p)}$	–	0	20	mV
90° injection						
offset out	$I_{CHPF} = -100\ \mu A$; $R_{offset\ out} = 10\ k\Omega$; rad on	$V_{offset\ out}$ (p-p)	90	110	130	mV
45° injection						
AGC	$R_{agc} = 10\ k\Omega$; $V_{offset\ in} = V_{ref} + 1\ V$; rad on	$V_{AGC(p-p)}$	200	250	300	mV

Notes to the characteristics

1. REdig output conditions:
   (A) $I_{Re1} > I_{Re2} + 5\ \mu A$; (B) $I_{Re2} > I_{Re1} + 5\ \mu A$.
2. Input voltage HIGH indicates logic 1; Input voltage LOW indicates logic 0; see also Table 1.
3. $\overline{DIV4}$ = HIGH; $V_{offset\ in}$ adjusted for $V_{REdig} = 1,4\ V$; rad on; lag hold off; $V_{AGC} = 3,8\ V$; $I_{Re1} = I_{Re2} = -100\ \mu A$.
4. Output voltage conditions are:
   rad on; lag short-circuit off; lag hold off; $V_{AGC} = 3,8\ V$; $I_{Re1} = I_{Re2} = -100\ \mu A$; $V_{offset} = V_{ref} - 1,2\ V$.

Table 1 Truth table for DAC output current

functions	DAC output	logical inputs				internal switches		
	I_{REout}/I_{DAC}	B3	B2	B1	B0	lag s/c	rad	lag hold
PUSH	−1/2	0	0	0	0	off	off	on
(kick)	−2	0	0	0	1	off	off	off
OFF	0	0	0	1	0	off	off	on
OFF	0	0	0	1	1	on	off	off
PULL	1/2	0	1	0	0	off	off	on
(kick)	2	0	1	0	1	off	off	off
CATCH	0	0	1	1	0	off	on	on
PLAY	0	0	1	1	1	off	on	off
PUSH	−1/2	1	0	0	0	on	off	on
PUSH	−3/8	1	0	0	1	on	off	off
PUSH	−1/4	1	0	1	0	on	off	on
PUSH	−1/8	1	0	1	1	on	off	off
PULL	1/2	1	1	0	0	on	off	on
PULL	3/8	1	1	0	1	on	off	off
PULL	1/4	1	1	1	0	on	off	on
PULL	1/8	1	1	1	1	on	off	off

Where:

0 = input voltage LOW; 1 = input voltage HIGH.

Philips Semiconductors

Data sheet	
status	Product specification
date of issue	September 1990

TEA0655

Dual Dolby* B-type noise reduction circuit for playback applications

FEATURES

- Dual noise reduction channels
- Head preamplifiers
- Equalization with electronically switched time constants
- Dolby reference level = 387.5 mV

GENERAL DESCRIPTION

The TEA0655 is an integrated circuit that provides two Dolby B-type noise reduction channels for playback applications in car radios. The TEA0655 includes head and equalization amplifiers with electronically switched time constants. The device will operate with power supplies in the range 9 to 15 volts, the output overload level increasing with an increase in supply voltage. Current drain varies with supply voltage and noise reduction ON/OFF, therefore it is advisable to use a regulated power supply or a supply with a long time constant.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage range	8	–	15	V
I_{CC}	supply current	–	20	25	mA
(S+N)/N	signal plus noise-to-noise ratio	78	84	–	dB

ORDERING AND PACKAGE INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TEA0655	20	DIL	plastic	SOT146

* Available only to licensees of Dolby Laboratories Licensing Corporation, San Francisco, CA94111, USA, from whom licensing and application information must be obtained. Dolby is a registered trade-mark of Dolby Laboratories Licensing Corporation.

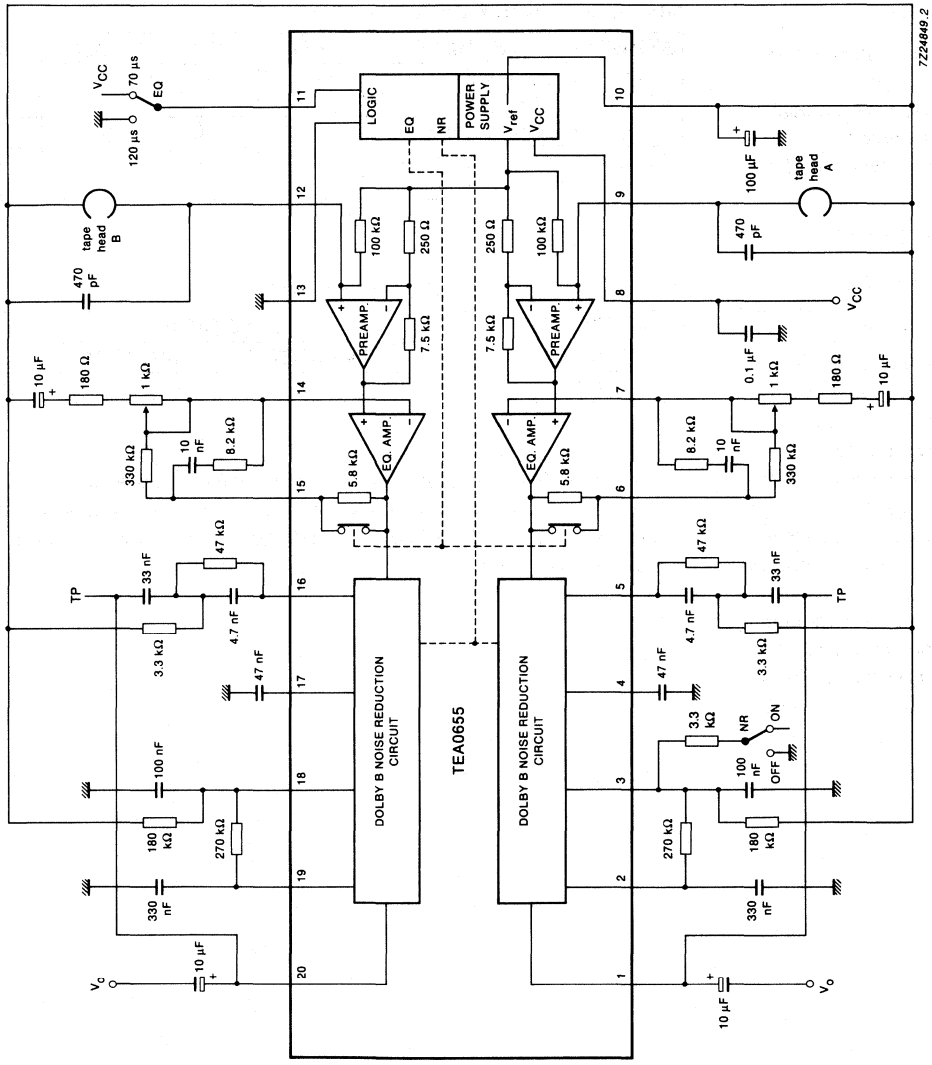


Fig.1 Block and application diagram.

Dual Dolby B-type noise reduction circuit for playback applications

TEA0655

FUNCTIONAL DESCRIPTION

Noise reduction is enabled when pin 3 is open-circuit and disabled when pin 3 is connected to GRD (pin 13) via a 3.3 kΩ resistor (see Fig.1).

Pin 3 performs the functions of a logic input for noise reduction switching for both channels. It also provides smoothing for the control signal in one channel. It is important that no voltage is applied to pin 3 when in the NR ON mode as this will cause irregular noise reduction characteristics in the selected channel. Time constant switching is achieved by applying a DC voltage to pin 11.

PINNING

SYMBOL	PIN	DESCRIPTION
OUTA	1	output channel A
INTA	2	integrating filter channel A
CONTRA	3	control voltage channel A
HPA	4	high-pass filter channel A
SCA	5	side chain channel A
EQA	6	equalizing output channel A
EQFA	7	equalizing input channel A
V_{CC}	8	voltage supply
INA	9	input channel A
V_{ref}	10	reference voltage
SWEQ	11	equalizing switch
INB	12	input channel B
GRD	13	ground
EQFB	14	equalizing input channel B
EQB	15	equalizing output channel B
SCB	16	side chain channel B
HPB	17	high-pass filter channel B
CONTRB	18	control voltage channel B
INTB	19	integrating filter channel B
OUTB	20	output channel B

LIMITING VALUES

Limiting values in accordance with the Absolute Maximum Rating System (IEC 134)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{CC}	supply voltage	–	16	V
V_I	input voltage (pins 1 to 20)	−0.3	V_{CC}	V
T_{amb}	operating ambient temperature range	−40	+85	°C
T_{stg}	storage temperature range	−65	+150	°C
V_{es}	electrostatic handling *	–	–	–

* Classification A: human body model; C = 100 pF, R = 1.5 kΩ, V = ≥ 2 kV; charge device model; C = 200 pF, R = 0 Ω, V ≥ 500 V.

Dual Dolby B-type noise reduction circuit for playback applications

TEA0655

CHARACTERISTICS

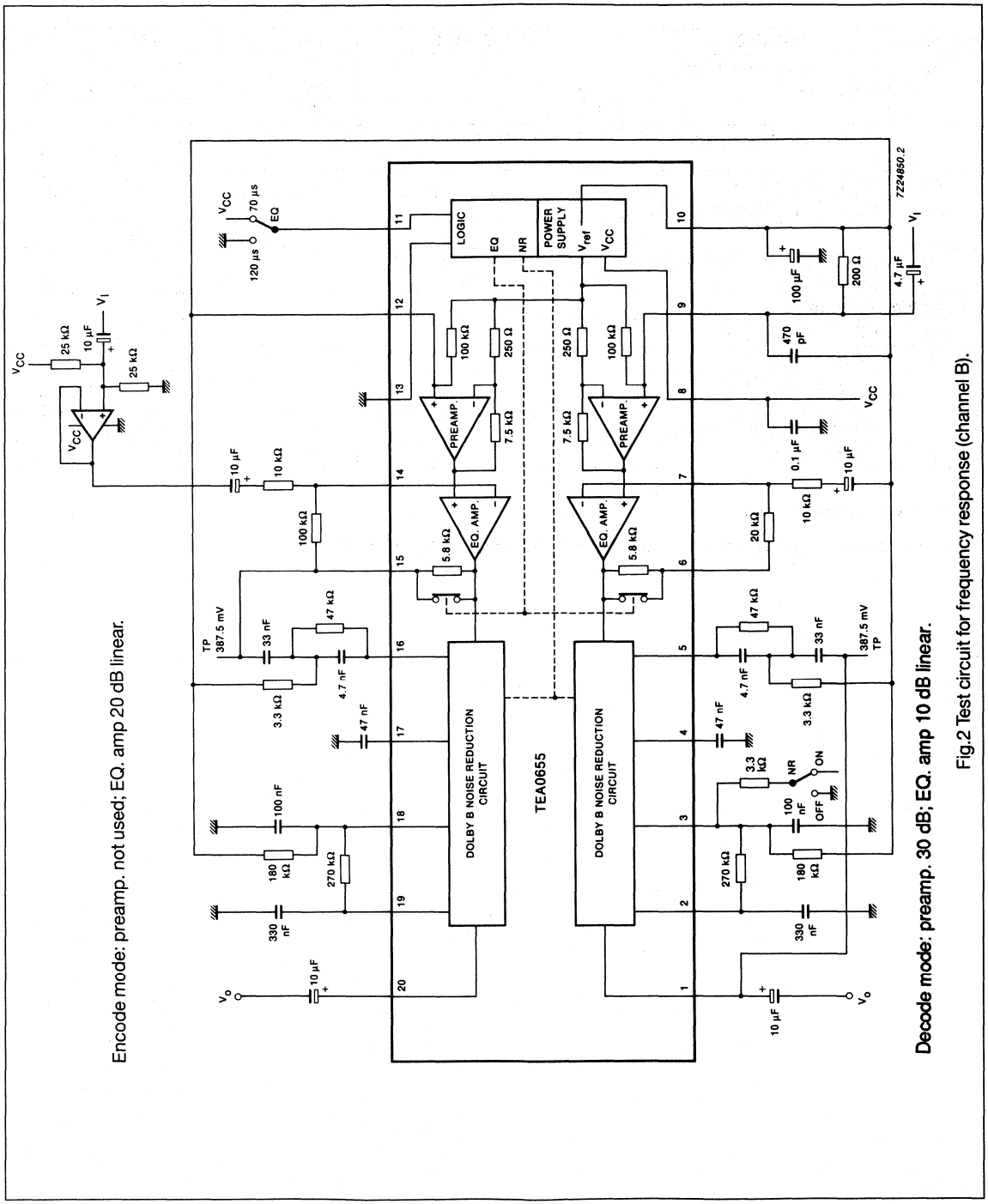
V_{CC} = 10 V; f = 20 Hz to 20 kHz; T_{amb} = +25 °C; all levels referenced to 387.5 mV RMS (0 dB) at test point (TP) (pin 1 or 20); test circuit Fig.1; NR ON; EQ switch in the 70 µs position; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage		8	10	15	V
I_{CC}	supply current		–	20	25	mA
	channel matching	NR OFF	–0.5	–	+0.5	dB
THD	distortion 2nd and 3rd harmonic	f = 1 kHz; 0 dB	–	0.08	0.15	%
		f = 10 kHz; +10 dB	–	0.15	0.3	%
	signal handling	V_{CC} = 8 V; 1% distortion at 1 kHz	12	15	–	dB
(S+N)/N	signal-plus-noise to noise ratio (see Fig.2; decode mode)	internal gain 40 dB linear; CCIR/ARM weighted	78	84	–	dB
PSRR	power supply ripple rejection	f = 1 kHz; 250 mV; see Fig.3	52	57	–	dB
	frequency response measured in encode mode see Fig.2 referenced to test point	note 1				
		f = 1 kHz; 0 dB	–1.5	0	+1.5	dB
		f = 1 kHz; –25 dB	–17.8	–19.3	–20.8	dB
		f = 0.2 kHz; –25 dB	–22.9	–24.4	–25.9	dB
		f = 5 kHz; –25 dB	–18.1	–19.6	–21.1	dB
		f = 10 kHz; –35 dB	–24.4	–25.9	–27.4	dB
α_{CR}	channel separation	f = 1 kHz; see Fig.4	57	63	–	dB
R_{Lmin}	minimum load resistance on output (pins 1 and 20)	12 dB; 1 kHz; 1% THD	10	–	–	kΩ
G_V	voltage gain (pin 9 to 7 or pin 12 to 14)	1 kHz	29	30	31	dB
V_{off}	input offset voltage		–	2	–	mV
I_B	input bias current		–	0.1	0.4	µA
R_{EQ}	equalizing resistor		4.7	5.8	6.9	kΩ
R_I	input resistance pins 9 and 12		60	100	–	kΩ

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
A_V	open loop gain pins 12/15 and pins 9/6	10 kHz	80	86	–	dB
		400 kHz	104	110	–	dB
	DC output voltage pins 1 and 20	NR OFF with reference to $V_{CC}/2$	–	–	±0.15	V
Z_O	output impedance		–	50	70	Ω
I_{OGRD}	DC output current capability	to ground	–	–	–2	mA
I_{OVCC}		to V_{CC}	–	–	300	µA
En	equivalent input noise voltage (RMS value)	NR OFF; unweighted; 20 Hz to 20 kHz; $R_S = 0\ \Omega$	–	0.7	1.4	µV
Switching thresholds						
V_{OFF}	NR switch OFF (pin 3)		0	–	$0.2V_{CC}$	V
I_3	NR switch ON		–	open	–100	nA
	equalizing (EQ) switch (pin 11) at 70 µs		$0.5V_{CC}$	–	V_{CC}	V
	equalizing switch at 120 µs		0	–	$0.2V_{CC}$	V
I_{11}	input current		–	–	–1	µA

Note to the characteristics

1. Equals the corresponding decode mode cut with reference to test point level, see Fig.1.



Encode mode: preamp. not used; EQ. amp 20 dB linear.

Decode mode: preamp. 30 dB; EQ. amp 10 dB linear.

Fig.2 Test circuit for frequency response (channel B).

Dual Dolby B-type noise reduction circuit for playback applications

TEA0655

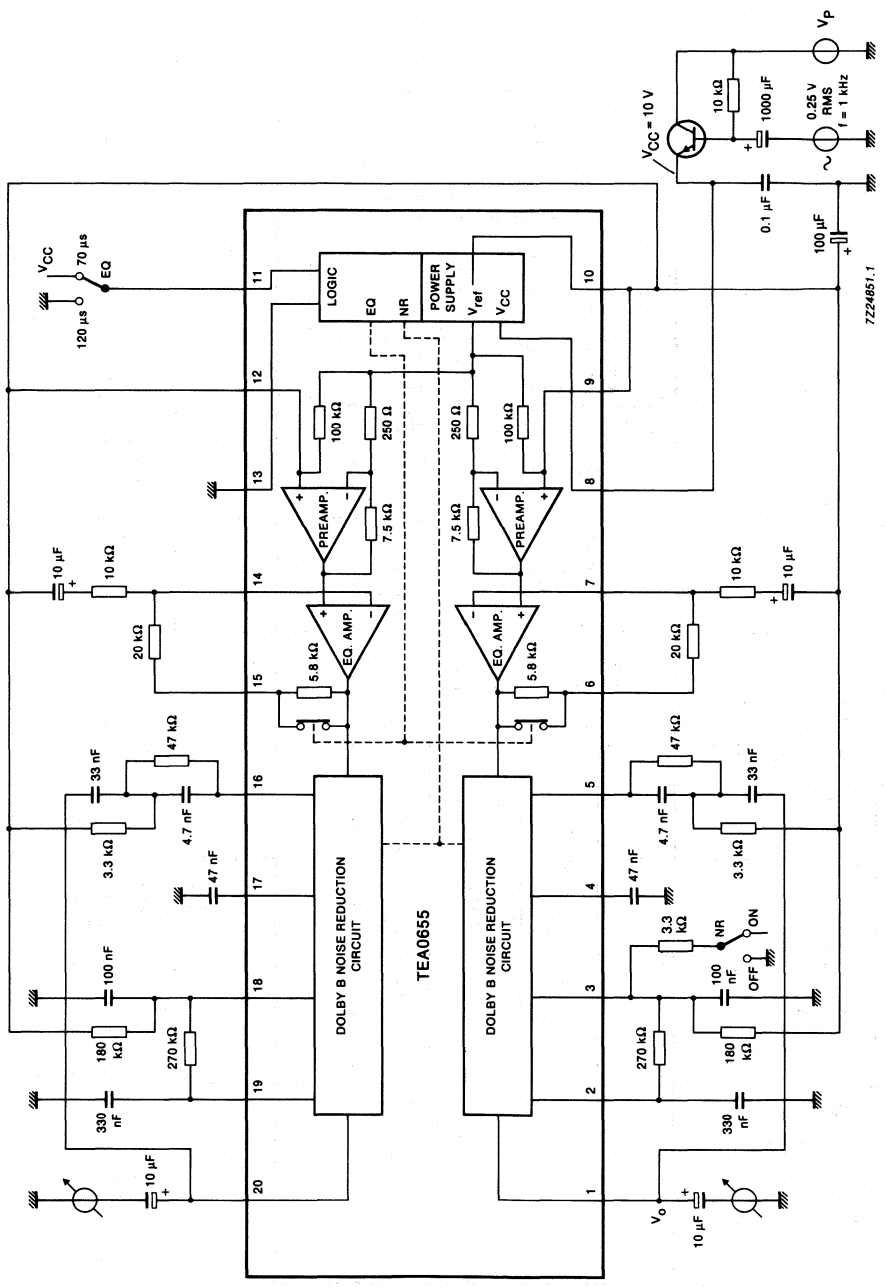


Fig.3 Test circuit for power supply ripple rejection (PSRR).

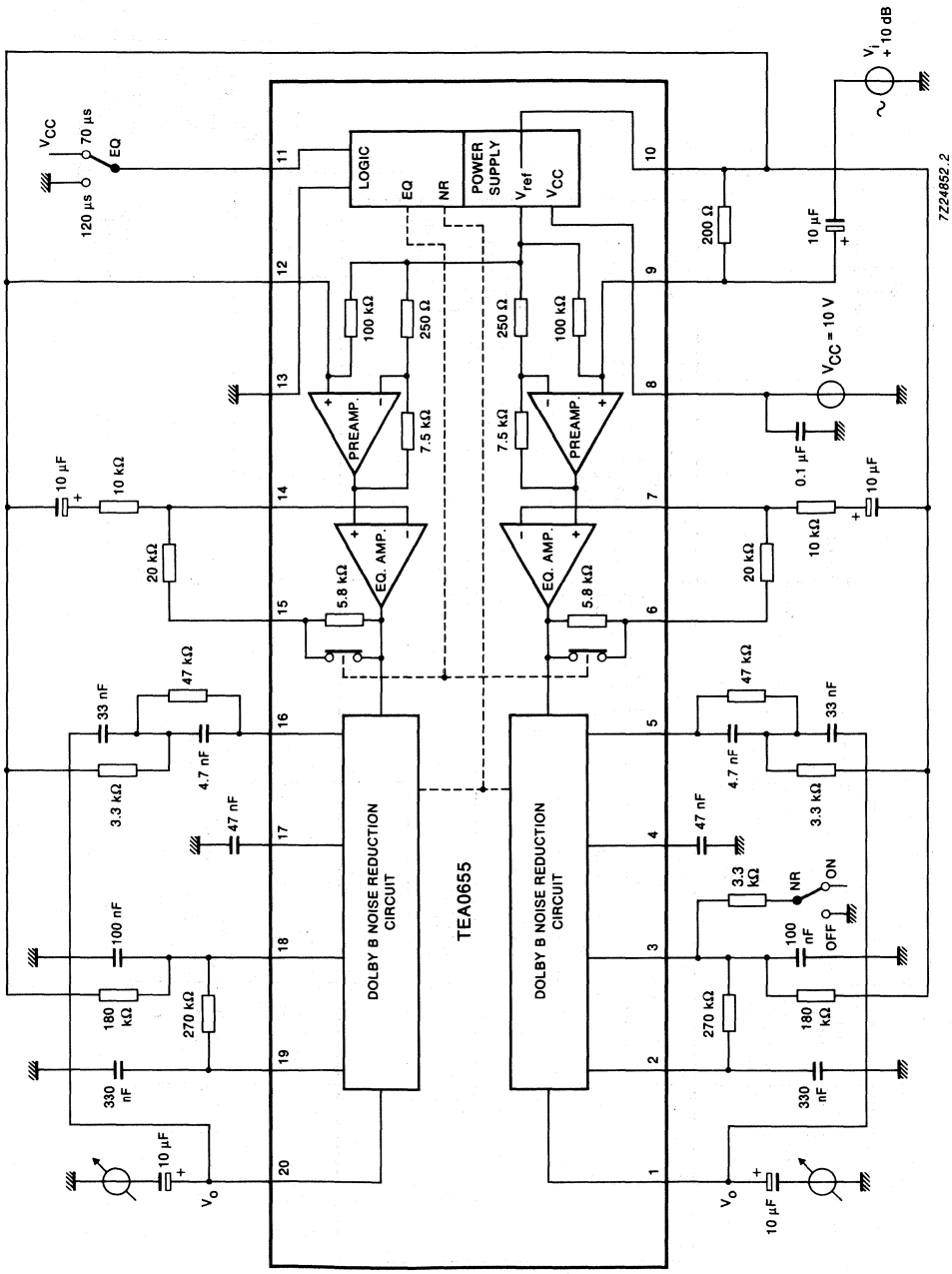


Fig.4 Test circuit for channel separation (α_{CS}).

DUAL DOLBY* B–TYPE NOISE REDUCTION CIRCUIT

GENERAL DESCRIPTION

The TEA0657 is a monolithic bipolar integrated circuit providing two channels of Dolby B-type noise reduction. The circuit contains all internal electronic switching to provide playback or record functions.

In addition the TEA0657 includes preamplifiers for the playback and record modes and multiplex filter buffers for both channels.

The device will operate with power supplies in the range of 9.0 V to 15.0 V, output overload level increasing with increase in supply voltage. Current drain varies with supply voltage and noise reduction ON/OFF so it is advisable to use a regulated power supply or, a supply with a long time constant.

Features

- Dual noise reduction channels
- Full playback/record switching
- Separate playback/record inputs
- Multiplex filter buffers
- Simultaneous switching on both channels
- Dual or single supply operations
- Dolby reference level = 580 mV
- Input sensitivity = 30 mV

QUICK REFERENCE DATA

parameter	symbol	min.	typ.	max.	unit
Supply voltage range	V_{CC}	9.0	–	15.0	V
Supply current	I_{CC}	–	19	–	mA
Signal plus noise to noise ration					
record mode	(S+N)/N	–	72	–	dB
playback mode	(S+N)/N	–	90	–	dB

* Available only to licensees of Dolby Laboratories Licensing Corporation, San Francisco, CA94111, U.S.A., from whom licensing and application information must be obtained.
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PACKAGE OUTLINE

24-lead DIL; plastic (SOT101B).

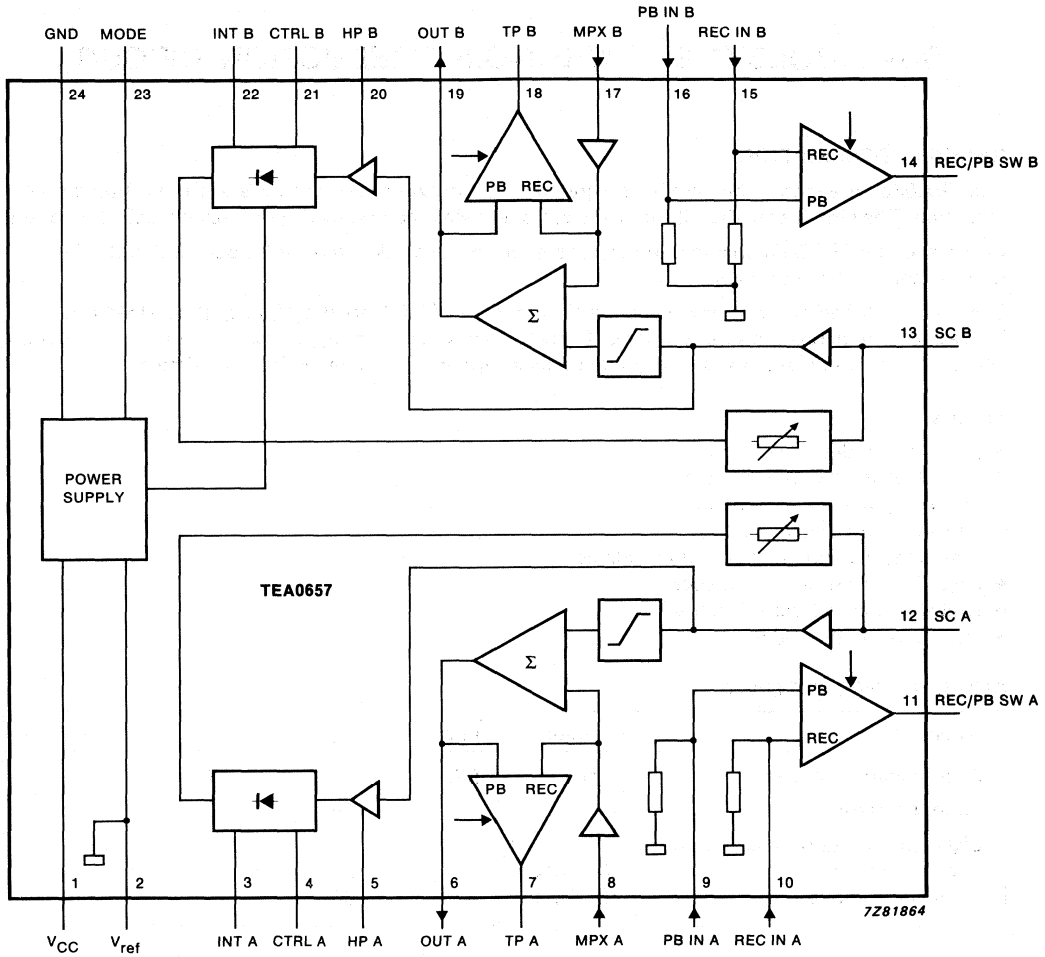


Fig. 1 Block diagram.

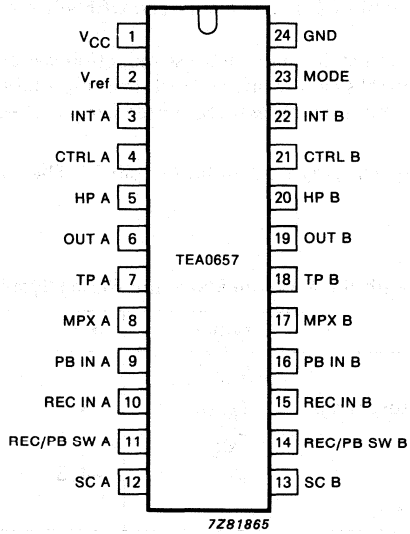


Fig. 2 Pinning diagram.

1	V_{CC}	supply voltage
2	V_{ref}	reference voltage
3	INT A	integrating filter channel A
4	CTRL A	control voltage channel A
5	HP A	high-pass filter channel A
6	OUT A	output channel A
7	TP A	test point channel A, line output channel A
8	MPX A	multiplex buffer channel A
9	PB IN A	playback input channel A
10	REC IN A	record input channel A
11	REC/PB SW A	record/playback switch channel A
12	SC A	side chain channel A
13	SC B	side chain channel B
14	REC/PB SW B	record/playback switch channel B
15	REC IN B	record input channel B
16	PB IN B	playback input channel B
17	MPX B	multiplex buffer input channel B
18	TP B	test point channel B, line output channel B
19	OUT B	output channel B
20	HP B	high-pass filter channel B
21	CTRL B	control voltage channel B
22	INT B	integrating filter channel B
23	MODE	record/playback select switch
24	GND	ground

FUNCTIONAL DESCRIPTION

Noise reduction is enabled when pin 22 is open-circuit and OFF when connected to pin 24 via a 5.1 kΩ resistor (see Fig. 3).
Pin 24 performs the functions of a logic input for noise reduction switching in both channels and provides smoothing for the control signal in one channel. It is important that no voltage is applied to this pin when in the NR ON mode as this will cause irregular noise reduction characteristics in the selected channel.

Record/playback is achieved by applying a DC voltage to pin 23. The circuit will enable the appropriate input for the selected mode.

RATINGS

Limiting values in accordance with the Absolute Maximum Rating System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage	V_{CC}	–	16.0	V
Operating ambient temperature range	T_{amb}	−40	+ 85	°C
Storage temperature range	T_{stg}	–	+ 150	°C
Input voltage (pin 1)	V_I	−0,3	V_{CC}	V
Electrostatic handling (note 1)				

Note to the ratings

Note 1, Classification A:

Human body model; C = 100 pF; R = 1.5 kΩ; V ⩾ 2 kV.
Charge device model; C = 200 pF; R = 0 Ω; V ⩾ 500 V.

CHARACTERISTICS

V_{CC} = 12 V; f = 20 Hz to 20 kHz; T_{amb} = + 25 °C; all levels referenced to 580 mV RMS (0 dB) at TP (pin 7 or 18); test circuit Fig. 4; Record mode; NR ON; unless otherwise specified.

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage		V_{CC}	9	12	15	V
Supply current		I_{CC}	–	19	–	mA
Voltage gain (pins 9 or 10 to 11)	f = 1 kHz	G_v	–	20	–	dB
Voltage gain (pins 8 to 7)	f = 1 kHz	G_v	–	9	–	dB
Channel matching	NR OFF		−0.5	–	+ 0.5	dB
Distortion						
2nd and 3rd harmonic	f = 1 kHz, 0 dB	THD	–	0.08	0.15	%
	f = 10 kHz, + 10 dB	THD	–	0.15	0.3	%
Signal handling; (V_{CC} = 9 V)	1% distortion at 1 kHz		12	–	–	dB
Signal-to-noise plus noise ratio						
record mode	internal CCIR ARM weighted	(S+N)/N	–	72	–	dB
playback mode	R_S = 10 kHz	(S+N)/N	–	90	–	dB
Supply voltage ripple rejection	f = 1 kHz; 250 mV	SVRR	–	40	–	dB
Frequency response; (referenced to TP)	f = 1 kHz;					
	0 dB	Δf	−1.5	–	−1.5	dB
	−20 dB	Δf	−17.3	−15.8	−14.3	dB
	f = 5 kHz					
	−30 dB	Δf	−23.3	−21.8	−20.3	dB
	−40 dB	Δf	−30.2	−29.7	−28.2	dB
	f = 10 kHz					
	0 dB	Δf	−1.1	0.4	1.9	dB
	−30 dB	Δf	−25.0	−23.5	−22.5	dB
Input resistance; (pins 9, 10, 15 and 16)		R_I	–	50	–	kΩ
Channel separation	0 dB at TP; f = 1 kHz	α_{cr}	–	65	–	dB
Back-to-back frequency response shift;						
as a function of T_{amb}	0 to −70 °C		–	± 0.5	–	dB
as a function of V_{CC}	9 V to 15 V		–	± 0.5	–	dB

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
PB/REC separation	30 mV; 1 kHz; at playback input, measure V_{OUT}	$\alpha_{PB/REC}$	–	72	–	dB
Minimum load resistance on output; (pins 6 and 9)	12 dB; 1 kHz; 1% THD	R_{Lmin}	10	–	–	kΩ
Switching thresholds playback; pin 23	V_{PB}	V_{PB}	0.7 V_{CC}	V_{CC}	–	V
record; pin 28		V_{REC}	–	GND	0.4 V_{CC}	V
NR OFF; pin 22		V_{OFF}	–	–	0.2 V_{CC}	V

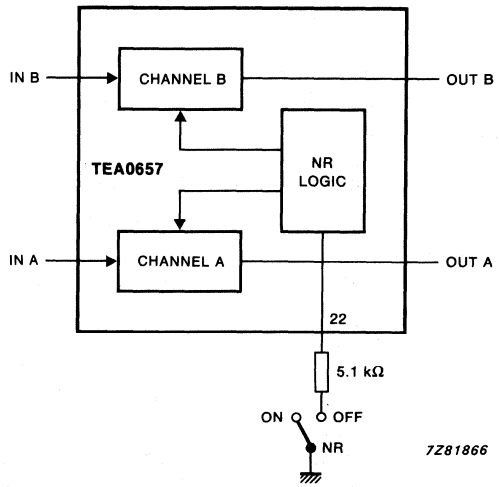
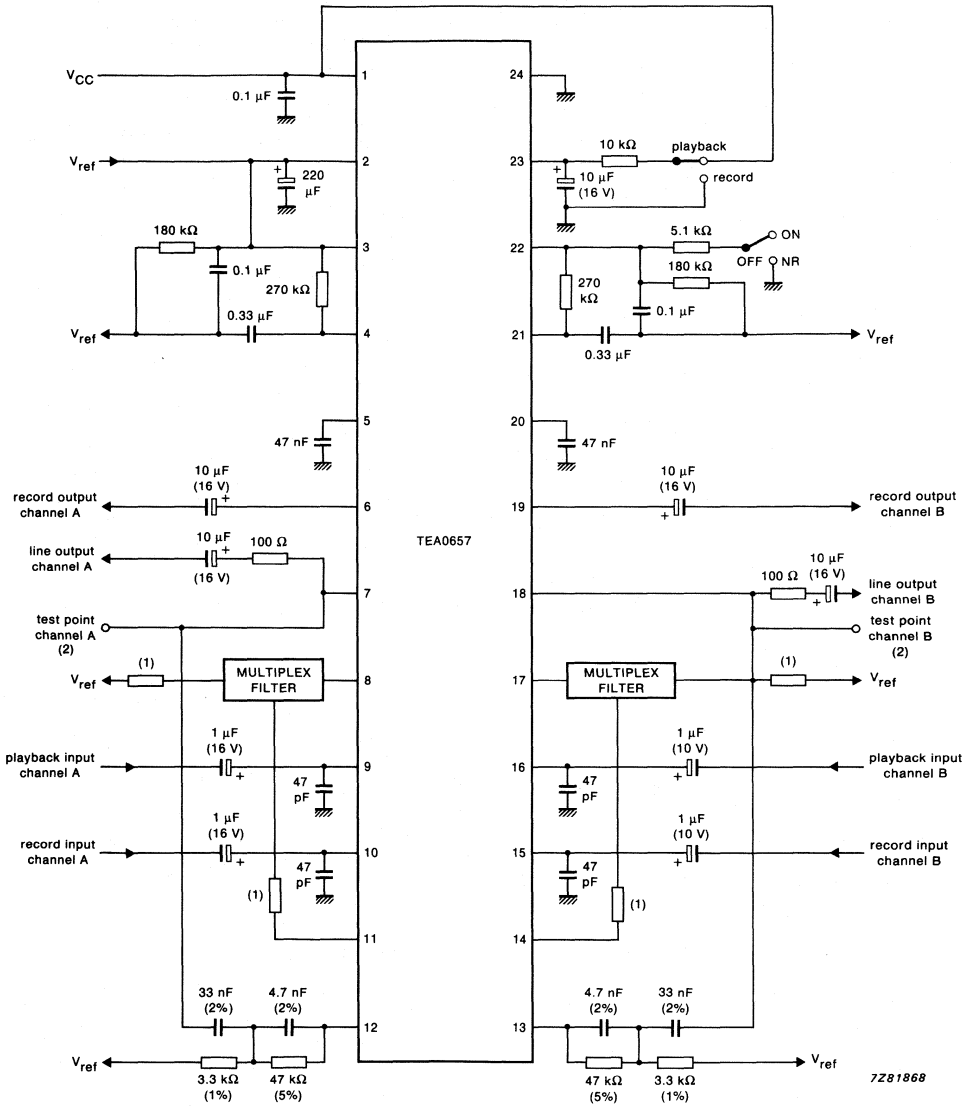


Fig. 3 External NR switch circuit for TEA0657.



All values within ± 10% unless otherwise specified.

Notes:

(1) Value determined by multiplexer in use.
(2) Dolby level = 580 mV at test points.

Fig. 4 Test and application circuit.

DOLBY* B and C TYPE NOISE REDUCTION CIRCUIT

GENERAL DESCRIPTION

The TEA0665 is designed for use in Dolby B and Dolby C type audio Noise Reduction (NR) systems. The device provides the high and low level stages for one channel of a Dolby C-type NR system, including NR ON/OFF switching and all electronic switching necessary for Dolby C-type systems. In addition the TEA0665 includes a preamplifier for the record and playback functions and a multiplex buffer amplifier. The circuit offers two different line-output levels (−6 and 0 dBm) and a low-pass filter, which can be fed into the signal path in playback mode.

Features

- Few external components required
- Included RECORD/PLAY preamplifiers plus multiplex filter buffer amplifier
- Two different line-output levels
- All electronic switching

PACKAGE OUTLINES

TEA0665: 28-lead DIL; plastic (SOT117).
TEA0665T: 28-lead mini-pack; plastic (SO28; SOT136A).

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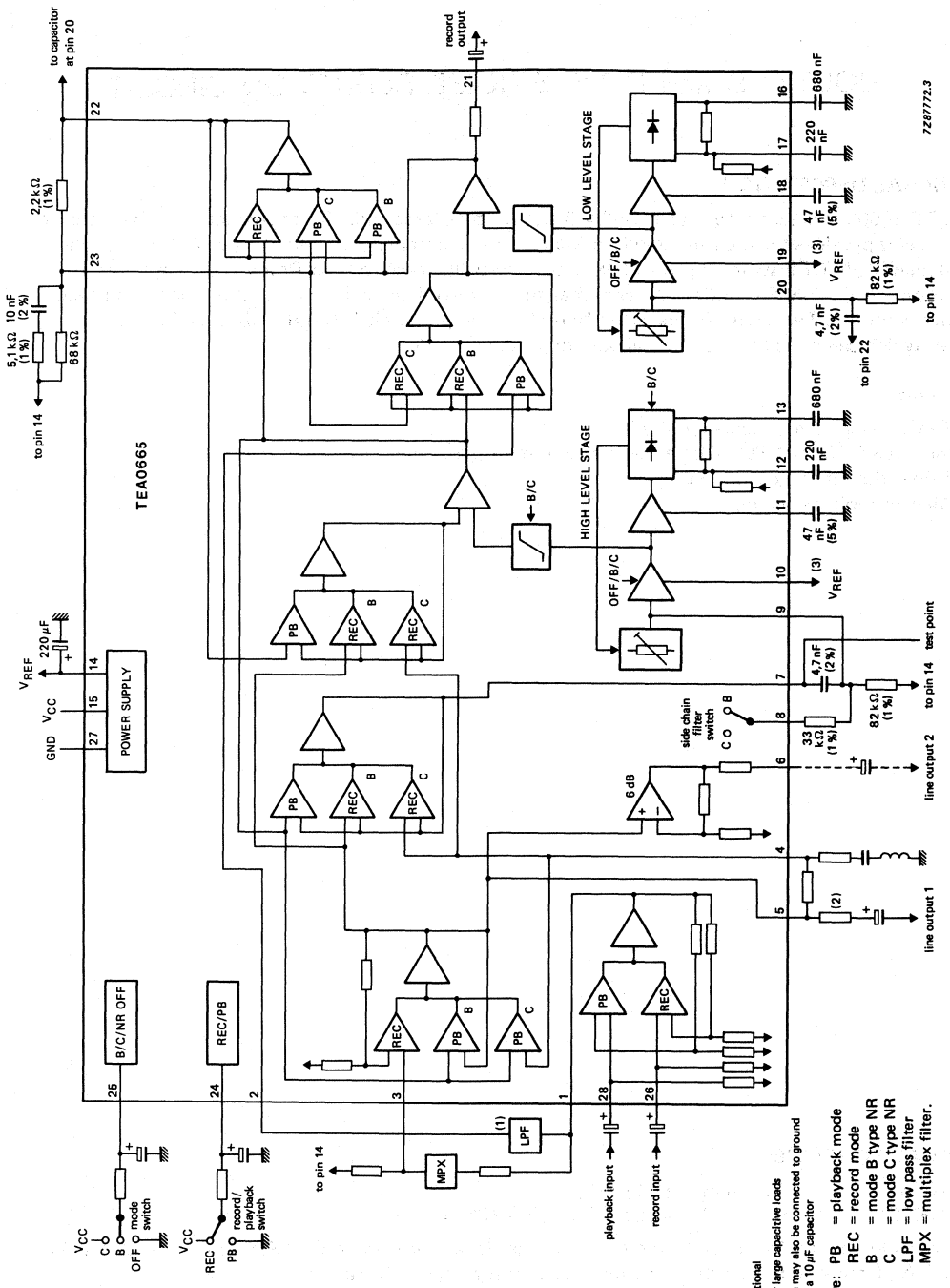


Fig. 1 Block diagram and application circuit.

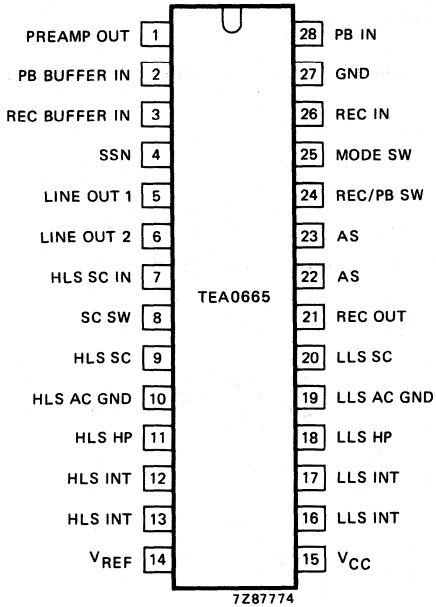


Fig. 2 Pinning diagram.

PINNING

1	PREAMP OUT	record/playback preamplifier output
2	PB BUFFER IN	playback amplifier input buffer
3	REC BUFFER IN	record amplifier input buffer
4	SSN	spectral skewing network
5	LINE OUT 1	line output 1
6	LINE OUT 2	line output 2
7	HLS SC IN	high level stage side chain input
8	SC SW	side chain filter switch
9	HLS SC	high level stage side chain
10	HLS AC GND	high level stage AC ground
11	HLS HP	high level stage high pass filter
12	HLS INT	high level stage integrating filter
13	HLS INT	high level stage integrating filter
14	V_{REF}	reference voltage
15	V_{CC}	positive supply voltage
16	LLS INT	low level stage integrating filter
17	LLS INT	low level stage integrating filter
18	LLS HP	low level stage high pass filter
19	LLS AC GND	low level stage AC ground
20	LLS SC	low level stage side chain
21	REC OUT	record output
22	AS	anti-saturation filter
23	AS	anti-saturation filter
24	REC/PB SW	record/playback switch input
25	MODE SW	mode switch input
26	REC IN	record input
27	GND	ground
28	PB IN	playback input

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 15)	V_{CC}	max. 18	V
Input voltage (pins 26 and 28)	V_I	max. −0,3 to V_{CC}	V
Total power dissipation	P_{tot}	600	mW
Storage temperature range	T_{stg}	−55 to + 150	°C
Operating ambient temperature range	T_{amb}	−40 to + 85	°C

CHARACTERISTICS

V_{CC} = 14 V; f = 20 Hz to 15 kHz; T_{amb} = 25 °C; all levels with reference to 387,5 mV = 0 dB = −6 dBm at test point pin 7; test circuit Fig. 5; record mode; unless otherwise specified.

parameter	conditions			symbol	min.	typ.	max.	unit
	mode	f (kHz)						
Supply								
Supply voltage range	C	–	note 1					
single				V_{CC}	8	14	16	V
(split)				V_{CC}	(±4)	(±7)	(±8)	V
Supply current	OFF	–	no input signal	I_{CC}	–	17	25	mA
Input sensitivity	C		note 2					
of record amplifier			pin 26	V_i	43	50	57	mV
of playback amplifier			pin 28	V_i	25	30	35	mV
Signal handling	C	1	V_{CC} = 8 V					
of record output			THD = 1%		12	15	–	dB
(note 3; see Fig. 8)		1	V_{CC} = 14 V					
			THD = 1%		–	20	–	dB
Line output 1			note 3		−0,5	0	+ 0,5	dB
Line output 2; amplifier gain V_o/V_i (pin 6 to pin 5)				G_v	+ 5,5	+ 6	+ 6,5	dB
Total harmonic distortion	OFF	1	TPL = 0 dB*	THD	–	0,02	0,1	%
			TPL = + 10 dB	THD	–	0,05	0,3	%
Total harmonic distortion	B	1	TPL = 0 dB	THD	–	0,1	0,15	%
			TPL = + 10 dB	THD	–	0,08	0,3	%
		10	TPL = 0 dB	THD	–	0,06	0,1	%
Total harmonic distortion	C	1	TPL = 0 dB	THD	–	0,15	0,3	%
			TPL = + 10 dB	THD	–	0,13	0,5	%
Signal plus noise-to-noise ratio	C		R_S = 10 kΩ CCIR/ARM weighted	(S+N)/N	62	66	–	dB

* TPL is Test Point Level.

parameter	conditions			symbol	min.	typ.	max.	unit
	mode	f (kHz)						
Frequency response	B	2	TPL = −25 dB		−19,0	−18,0	−17,0	dB
		5	TPL = −40 dB		−30,7	−29,7	−28,7	dB
		10	TPL = −30 dB		−24,5	−23,5	−22,5	dB
	C	0,2	TPL = −40 dB		−33,4	−31,9	−30,4	dB
		1	TPL = −30 dB		−20,1	−18,6	−17,1	dB
		1	TPL = −20 dB		−16,1	−14,1	−12,1	dB
		5	TPL = −0 dB		−3,8	−2,3	−0,8	dB
		5	TPL = −20 dB		−19,1	−17,1	−15,1	dB
		5	TPL = −40 dB		−28,5	−26,5	−24,5	dB
Switching thresholds			note 4; pin 24					
for record				V_{24-27}	8,5	–	14	V
for playback				V_{24-27}	0	–	4	V
Switching thresholds			note 5; pin 25					
	OFF			V_{25-27}	0	–	3,5	V
(switch in open position)	B			V_{25-27}	–	7	–	V
(external voltage)	B			V_{25-27}	6,3	7	7,7	V
	C			V_{25-27}	10,8	–	14	V
Switch input current			pin 25					
	OFF		$V_{25-27} = 0$ V	$-I_{25}$	–	–	40	μA
	C		$V_{25-27} = V_{CC}$	I_{25}	–	–	40	μA
Frequency response shift as a function of temperature deviation, range −40 to + 85 °C, measured as deviation from 25 °C	C			Δf	–	± 0,5	–	dB
as a function of voltage deviation, range 8 to 16 V, measured as deviation from 14 V				Δf	–	± 0,1		dB
Input resistance								
			pin 26	R_{26-27}	35	50	65	kΩ
			pin 28	R_{28-27}	35	50	65	kΩ
Output resistance								
			pin 6	R_{6-27}	–	160	220	Ω
			pin 21	R_{21-27}	–	60	100	Ω

Notes to the characteristics

1. Operation with minimum of 12 dB headroom; system remains functional to 7 V.
2. Attenuation between pins 1 and 3 is 3,5 dB (MPX-filter).
   Playback input sensitivity is 45 mV if a switchable MPX-low pass filter is used in playback mode (pins 2 and 3 short-circuited).
3. System headroom is determined by the line output channel in use.
   For low supply voltages line output 2 (pin 6) will saturate at high signal levels. Headroom for line output 1 (pin 5) tracks with record output (pin 21).
4. The equation for REC/PB switch input voltage is:

   REC: $V_{24\text{-}27} > 0{,}55\ V_{CC} - V_{BE} + 1{,}5\ V$,

   PB: $V_{24\text{-}27} < 0{,}45\ V_{CC} - V_{BE} - 1{,}5\ V$.
5. The equation for C/B/OFF mode switch input voltage is:

   OFF: $V_{25\text{-}27} < 0{,}38\ V_{CC} - V_{BE} - 1\ V$,

   B: $0{,}45\ V_{CC} < V_{25\text{-}27} < 0{,}55\ V_{CC}$ (external voltage),

   B: $0{,}5\ V_{CC}$ (switch in open position),

   C: $V_{25\text{-}27} > 0{,}75\ V_{CC} - V_{BE} + 1\ V$.

   The voltage drop across the external time constant resistor must be taken in to account.

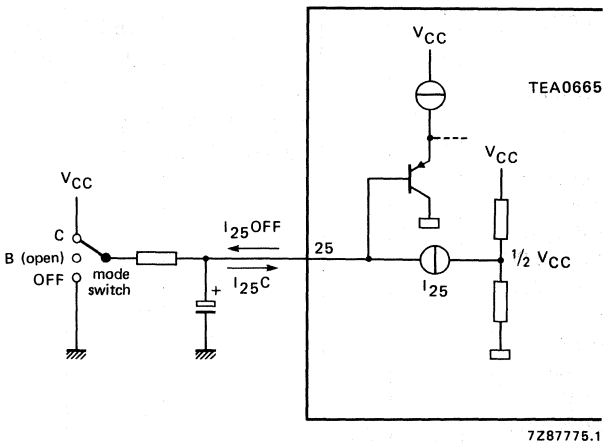


Fig. 3 Mode switch input configuration.

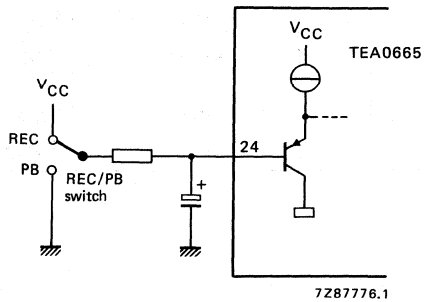


Fig. 4 REC/PB switch input configuration.

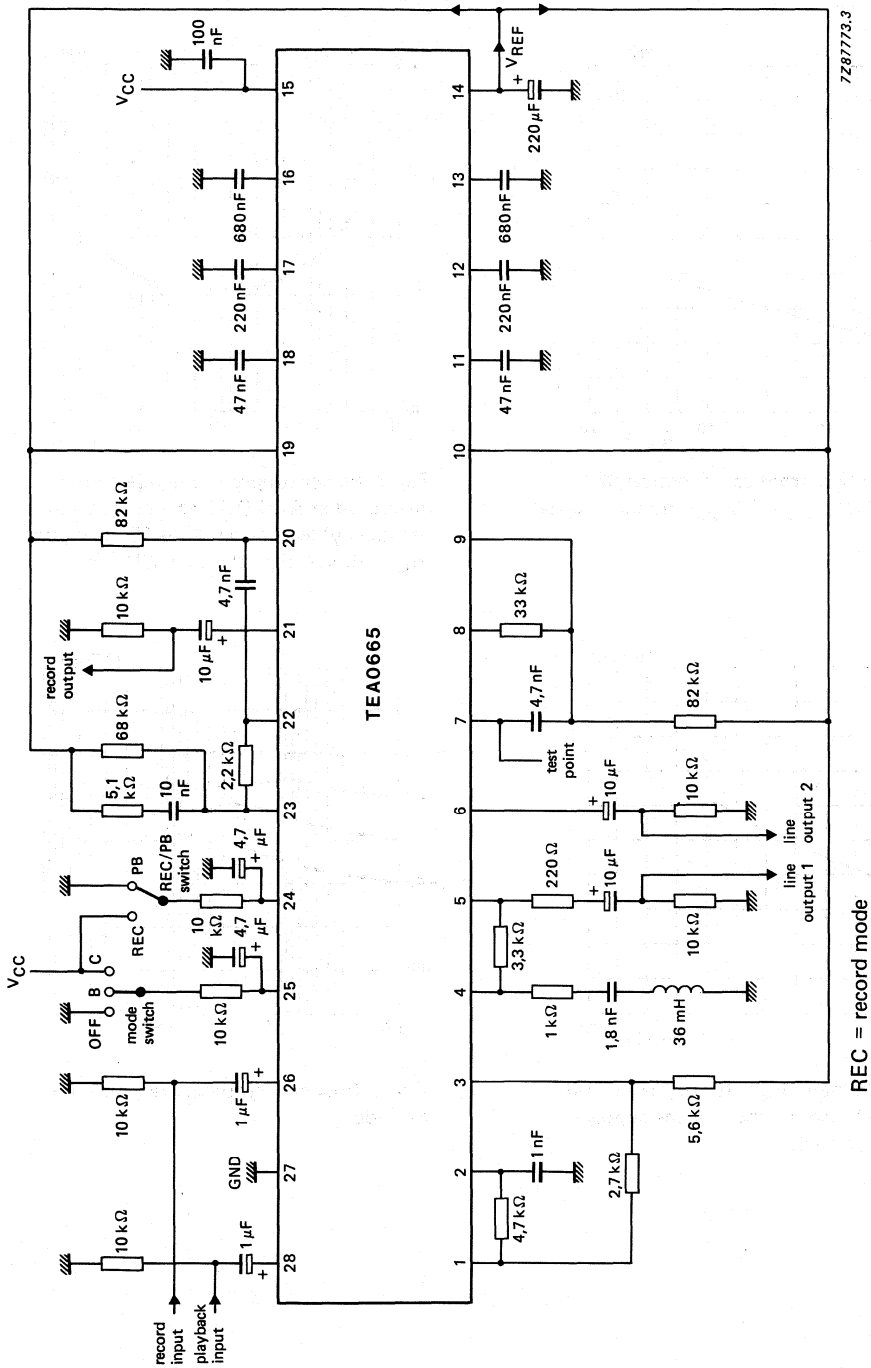


Fig. 5 Test circuit.

SYSTEM GRAPHS

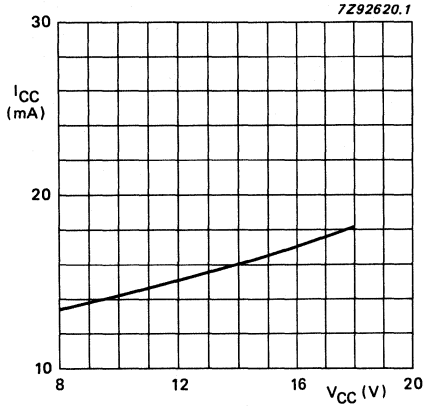


Fig. 6 Supply current as a function of supply voltage; $I_{CC} = f(V_{CC})$; no input signal.

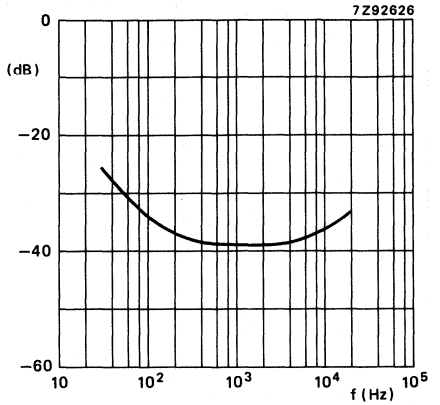


Fig. 7 Power supply ripple rejection measured at REC OUT as a function of frequency; level at pin 15 = 100 mV (rms). R_G = 10 kΩ; record mode; NR OFF.

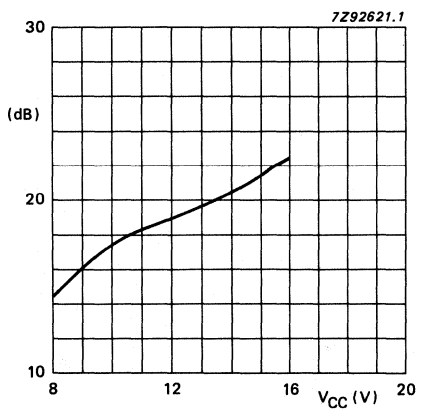


Fig. 8 Signal handling = $f(V_{CC})$ measured at REC OUT as a function of the supply voltage; THD = 1%.

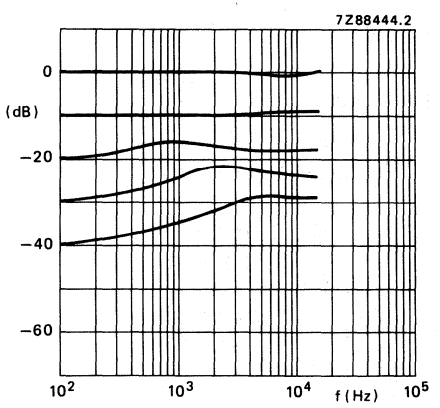


Fig. 9 Encoder frequency response for B-mode.

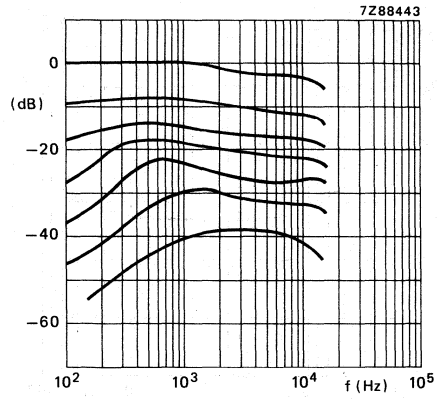


Fig. 10 Encoder frequency response for C-mode.

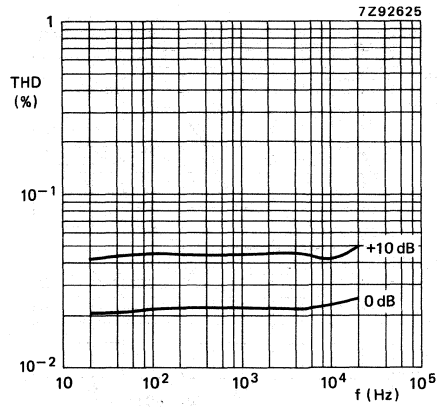


Fig. 11 Total harmonic distortion measured at REC OUT as a function of frequency; for NR OFF mode; V_{CC} = 14 V; LPF 80 kHz.

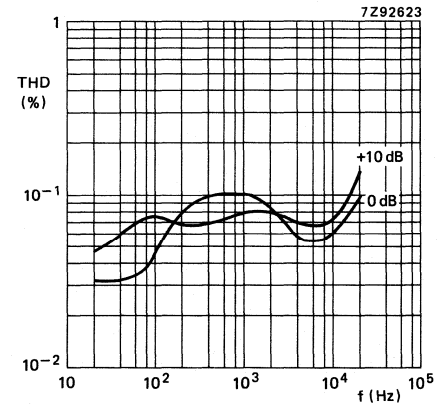


Fig. 12 Total harmonic distortion measured at REC OUT as a function of frequency; for B-mode; V_{CC} = 14 V; LPF 80 kHz.

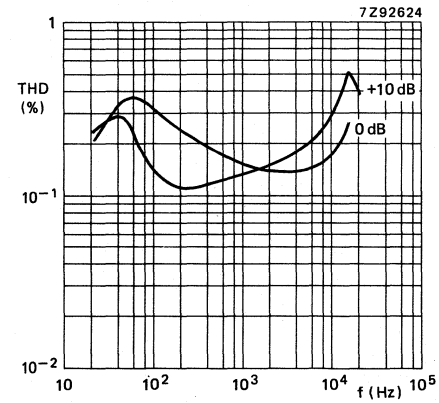


Fig. 13 Total harmonic distortion measured at REC OUT as a function of frequency; for C-mode; V_{CC} = 14 V; LPF 80 kHz.

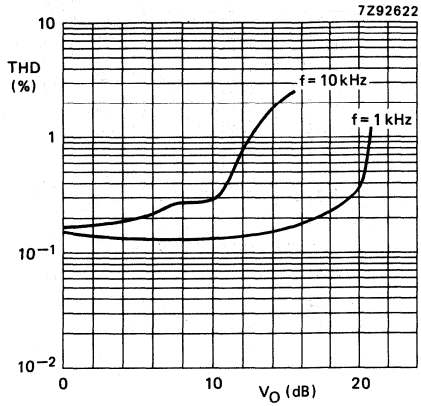


Fig. 14 Total harmonic distortion as a function of the record output level (pin 21); for C-mode; V_{CC} = 14 V; LPF 80 kHz.

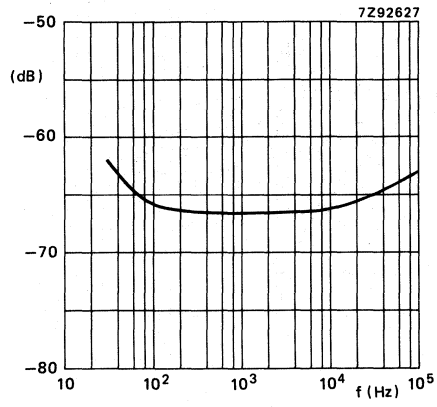


Fig. 15 Crosstalk from record input (pin 26) to line output as a function of frequency in playback mode; record input level is 50 mV; NR OFF; R_G = 10 kΩ.

Dual Dolby* B-type noise reduction circuit for playback applications

TEA0675

FEATURES

- Dual noise reduction (NR) channels
- Head preamplifiers
- Reverse Head switching
- Automatic Music Search (AMS)
- Music Scan
- Equalization with electronically switched time constants
- Dolby reference level = 387.5 mV
- 24 pins.

GENERAL DESCRIPTION

The TEA0675 is a monolithic bipolar integrated circuit providing two channels of Dolby B noise reduction for playback applications in car radios. The TEA0675 includes head and equalization amplifiers with electronically switchable time constants. Furthermore the TEA0675 includes electronically switchable inputs for tape drives with reverse heads. This device also detects pauses of music in AMS (Automatic Music Search) scan mode, for applications with an intelligent controlled tape drive, or AMS latch mode, for applications with a simple controlled tape drive, with a delay time fixed externally by a resistor for both modes.

The device will operate with power supplies in the range of 7.6 V to 12.0 V, output overload level increasing with increase in supply voltage. Current drain varies with supply voltage, noise reduction on/off and AMS on/off so it is advisable to use a regulated power supply or a supply with a long time constant.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage	7.6	–	12	V
I_{CC}	supply current	–	26	31	mA
(S+N)/N	signal-plus-noise to noise ratio	78	84	–	dB

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TEA0675	24	SDIL	plastic	SOT234
TEA0675T	24	SO	plastic	SOT137

*Available only to licensees of Dolby Laboratories Licensing Corporation, San Francisco, CA94111, USA, from whom licensing and application information must be obtained. Dolby is a registered trade-mark of Dolby Laboratories Licensing Corporation.

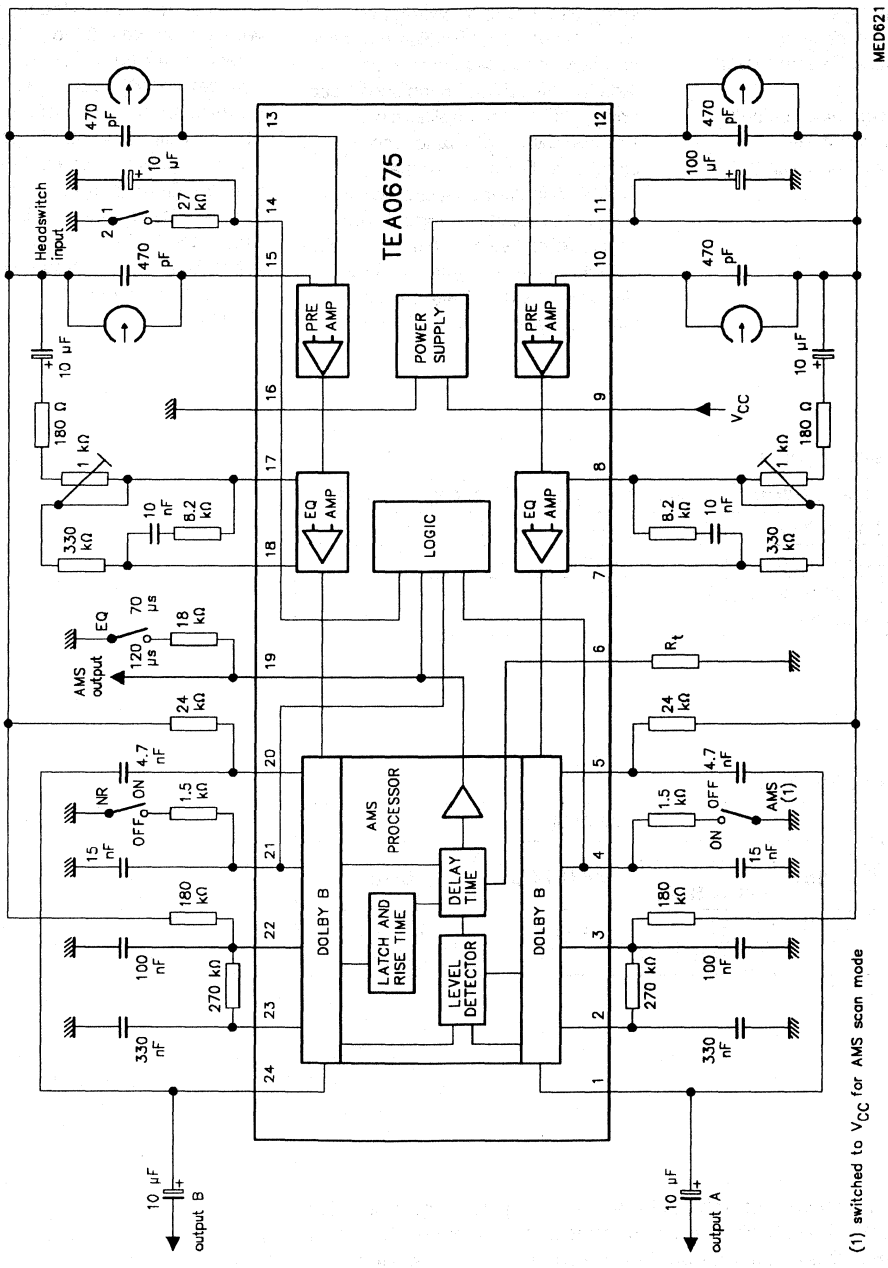


Fig.1 Block and application diagram.

Dual Dolby* B-type noise reduction circuit for playback applications

TEA0675

FUNCTIONAL DESCRIPTION

NR is enabled when pin 21 (HPB) is open-circuit and disabled when connected to GND via an 1.5 kΩ resistor.

AMS-scan mode is enabled when pin 4 (HPA) is connected to V_{CC} via an 1.5 kΩ resistor and disabled when pin 4 is open-circuit. Switching AMS ON, internally NR is switched OFF simultaneously (see Figs 5 and 6 for principle timing in AMS-scan mode).

AMS-latch mode is enabled when pin 4 (HPA) is connected to GND via an 1.5 kΩ resistor and disabled when pin 4 is open-circuit. Switching AMS ON, NR is switched OFF internally. In this mode the device detects a pause level signal, when a music level signal has appeared first (see Figs 7 and 8 for principle timing). Furthermore a longer rise time constant is supplied for suppressing the detection of plops on tape. The output signal at pin 19 (AMSEQ) in this mode may be applied to drive a tape drive logic circuit.

Time constant switching for equalization is achieved when pin 19 (AMSEQ) is connected to GND via an 18 kΩ resistor (120 µs), or open-circuit (70 µs). This does not affect the AMS output signal during AMS mode (see Fig.1).

Head switching is achieved when pin 14 (HS) is connected (IN2) to GND via a 27 kΩ resistor, or left open-circuit (IN1). The 10 µF capacitor at pin 14 (HS) sets the time constants for smooth switching.

In AMS mode the signals of both channels are rectified and then added. This means, even if one channel signal appears inverted to the other channel, the normal AMS function is ensured.

Pin 21 (HPB) and pin 4 (HPA) perform the function of a logic input for AMS, respectively NR mode switching in both channels and provide the frequency dependent feed back of the control chain amplifier in the corresponding channel. Thus it is important that no voltage is applied to pin 21 (HPB) and pin 4 (HPA) during NR ON / AMS OFF mode, otherwise this will cause irregular NR characteristics.

Dolby B noise reduction only operates correctly if 0 dB Dolby level is adjusted at 387.5 mV.

PINNING

SYMBOL	PIN	DESCRIPTION
OUTA	1	output channel A
INTA	2	integrating filter channel A
CONTRA	3	control voltage channel A
HPA	4	high-pass filter channel A
SCA	5	side chain channel A
TD	6	delay time constant
EQA	7	equalizing output channel A
EQFA	8	equalizing input channel A
V_{cc}	9	voltage supply
INA1	10	input channel A1 (forward or reverse)
V_{REF}	11	reference voltage
INA2	12	input channel A2 (reverse or forward)
INB2	13	input channel B2 (reverse or forward)
HS	14	headswitch input
INB1	15	input channel B1 (forward or reverse)
GND	16	ground
EQFB	17	equalizing input channel B
EQB	18	equalizing output channel B
AMSEQ	19	AMS output and EQ-switch input
SCB	20	side chain channel B
HPB	21	high-pass filter channel B
CONTRB	22	control voltage channel B
INTB	23	integrating filter channel B
OUTB	24	output channel B

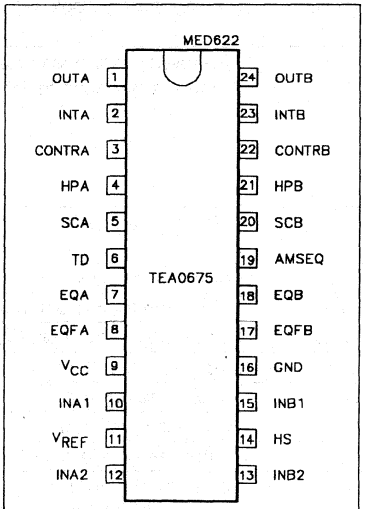


Fig.2 Pin configuration.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{CC}	supply voltage	0	14	V
V_I	input voltage (except pin 11)	−0.3	V_{CC}	V
t_{short}	pin 11 to V_{CC} duration	–	5	s
T_{amb}	operating ambient temperature	−40	+85	°C
T_{stg}	storage temperature	−55	+150	°C
V_{es}	electrostatic handling (see note 1)	–	–	–

Note to the Limiting values

1. Classification A: human body model; C = 100 pF, R = 1.5 kΩ, V ≥ 2 kV; charge device model; C = 200 pF, R = 0 Ω, V ≥ 500 V.

CHARACTERISTICS

V_{CC} = 10 V; f = 20 Hz to 20 kHz; T_{amb} = +25 °C; all levels are referenced to 387.5 mV RMS (0 dB) at test point (TP) pin (OUTA) or (OUTB); test circuit Fig.1; NR ON/AMS OFF; EQ switch in the 70 µs position; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage		7.6	10	12	V
I_{CC}	supply current		–	26	31	mA
	channel matching	NR OFF	−0.5	–	+0.5	dB
THD	total harmonic distortion 2nd and 3rd harmonic	f = 1 kHz; 0 dB	–	0.08	0.15	%
		f = 10 kHz; +10 dB	–	0.15	0.3	%
	signal handling	V_{CC} = 7.6 V; 1% distortion at 1 kHz	12	–	–	dB
(S+N)/N	signal-plus-noise to noise ratio (decode mode)	internal gain 40 dB, linear; see Fig.12; CCIR/ARM weighted	78	84	–	dB
PSRR	power supply ripple rejection	f = 1 kHz; 250 mV; see Fig.9	52	57	–	dB
	frequency response measured in encode mode; referenced to TP	see Fig.12				
		f = 1 kHz; 0 dB	−1.5	0	+1.5	dB
		f = 1 kHz; −25 dB	−17.8	−19.3	−20.8	dB
		f = 0.2 kHz; −25 dB	−22.9	−24.4	−25.9	dB
		f = 5 kHz; −25 dB	−18.1	−19.6	−21.1	dB
		f = 10 kHz; −35 dB	−24.4	−25.9	−27.4	dB
α_{CS}	channel separation	+10 dB at TP; f = 1 kHz; see Fig.10	57	63	–	dB
α_{CC}	crosstalk between active and inactive input	NR OFF; f = 1 kHz; +10 dB	70	77	–	dB
R_{Lmin}	minimum load resistance at output	12 dB; 1 kHz; 1% THD	10	–	–	kΩ
G_v	voltage gain from pin (IN) to pin (EQF)	1 kHz	29	30	31	dB
V_{off}	input offset voltage		–	2	–	mV
I_B	input bias current		–	0.1	0.4	µA
R_{EQ}	equalizing resistor		4.7	5.8	6.9	kΩ
R_I	input resistance pin (IN)		60	100	–	kΩ
A_V	open-loop gain pins 10/12 (INA1)/(INA2) to pin 7 (EQA); pins 15/13 (INB1)/(INB2) to pin 18 (EQB)	10 kHz	80	86	–	dB
		400 Hz	104	110	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	DC output voltage pins 1 (OUTA) and 24 (OUTB)	NR OFF with reference to V_{REF}; tape head DC coupled	–	–	±0.15	V
I_{OGND}	DC output current capability	to ground	–2	–	–	mA
I_{OVCC}		to V_{CC}	300	–	–	µA
Z_o	output impedance		–	80	100	Ω
N	equivalent input noise voltage (RMS value)	NR OFF; unweighted; 20 Hz to 20 kHz; R_{source} = 0 Ω	–	0.7	1.4	µV
V_{TD}	TD (pin 6) AMS timing; DC level	resistor R_t connected	V_{CC} – 3	–	V_{CC}	V
Switching thresholds						
V_{NROFF}	HPB (pin 21) NR OFF		0.19V_{CC}	0.23V_{CC}	0.25V_{CC}	V
I_{NROFF}	output current	NR OFF	–	–0.7	–1	mA
I_{NRON}	NR ON		–	open	200	nA
V_{HPBmax}	maximum voltage		–	–	0.75V_{CC}	V
HPA (pin 4)						
V_{AMSION}	AMS-latch ON		0.19V_{CC}	0.23V_{CC}	0.25V_{CC}	V
I_{AMSION}	output current		–	–0.7	–1	mA
V_{AMSsON}	AMS-scan ON		0.75V_{CC}	0.77V_{CC}	0.81V_{CC}	V
I_{AMSsON}	input current		–	0.8	1	mA
I_{AMSOFF}	AMS OFF		–	open	200	nA
V_{HPAmax}	maximum voltage		–	–	0.75V_{CC}	V
AMSEQ (pin 19) AMSout (AMS mode)						
V_{OH}	HIGH level output voltage		4	4.6	5	V
I_{OH1}	HIGH level output current	note 1	10	–	–150	µA
I_{OH2}	HIGH level output current	note 1	0.01	–	–1	mA
t_d	minimum pulse width; delay time range	note 2	–	23 to 160	–	ms
V_{OL}	LOW level output voltage		–	0.1	0.7	V
I_{OL}	LOW level output current		–0.02	–	1	mA
t_r	minimum pulse width rise time	AMS-scan mode	2	6	10	ms
		AMS-latch mode	130	150	170	ms
$A_{M/P}$	signal level at output for AMS switching music to pause	AMS mode; see Fig.11 f = 10 kHz; note 3	–25	–22	–19	dB
$A_{P/M}$	signal level at output for AMS switching pause to music	AMS mode f = 10 kHz	–24	–21	–18	dB
AMSEQ (pin 19) EQ-switch input (not AMS mode)						
I_{EQ70}	70 µs input current		–	–	–150	µA
I_{EQ120}	120 µs input current		–250	–	–1000	µA
I_{EQth}	threshold current	note 1	–	–200	–	µA
HS (pin 14) headswitch input						
V_{IN1}	dual input IN1 active	note 4	0.65V_{CC}	0.775V_{CC}	1.0V_{CC}	V
I_{HS1}	output current		–150	90	150	µA
V_{IN2}	dual input IN2 active		0.1V_{CC}	–	0.35V_{CC}	V
I_{HS2}	output current		–50	–90	–150	µA

Notes to the characteristics

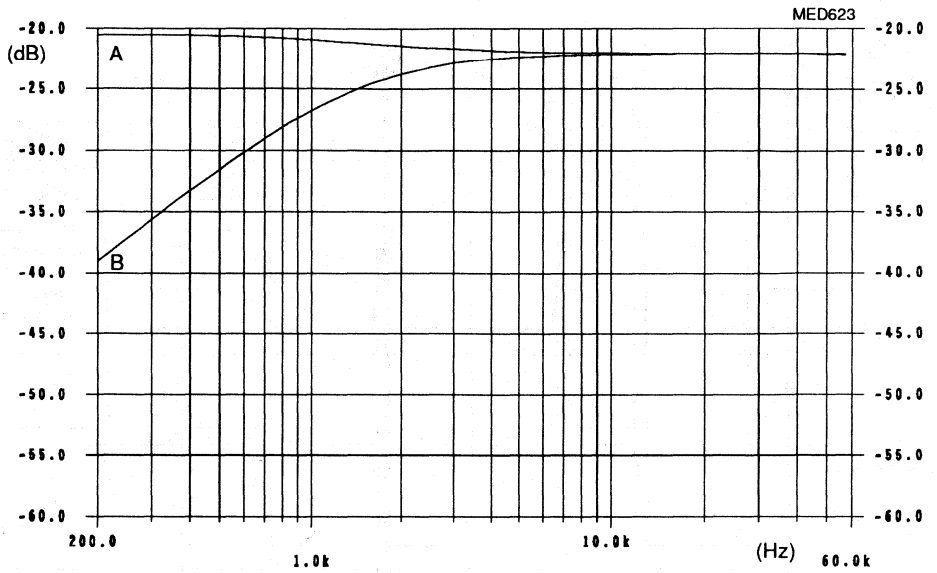
1. In AMS OFF mode, pin 19 (AMSEQ) is HIGH-level, the equalization time constant will be switched by pulling approximately 200 µA out of pin 19 (AMSEQ). This means for the device connected to pin 19 (AMSEQ), a restriction of input current at high level less than 200 µA during AMS OFF; otherwise the switching of the equalization time constant is disabled but fixed at 120 µs. If the following devices, input consumes more than 200 µA, this input has to be disconnected in AMS OFF mode. (To ensure switching the currents for the different switched modes are specified with a headroom of ±50 µA in the list of characteristics.)
   For an application with a fixed EQ time constant of 120 µs the equalizing network may be applied completely external. Change 8.2 kΩ resistor to 14 kΩ the internal resistor R_{EQ} = 5.8 kΩ is shortened by fixing the EQ-switch input at the 70 µs position (I_{EQ70}).
2. The minimum of pulse width depends on the delay time t_d set by R_t:

RESISTOR VALUE R_t (kΩ)	DELAY TIME t_d TYP. (ms)	TOLERANCE (%)
68	23	20
150	42	15
180	48	15
220	56	15
270	65	10
330	76	10
470	98	10
560	112	10
680	126	10
820	142	10
1000	160	10

3. The high speed of the tape (FF, REW) at the tape head during AMS mode causes a transformation of level and frequency of the originally recorded signal. It means a boost of signal level of about 10 dB and more for recorded frequencies from 500 Hz up to 4 kHz. So the threshold level of –22 dB corresponds to signal levels in PB mode of about –32 dB.
   The AMS inputs for each channel are pin 5 (SCA) and pin 20 (SCB). As the frequency spectrum is transformed by a factor of approximately 10 to 30 due to the higher tape speed in FF, REW, the high pass filter (4.7 nF/24 kΩ) removes the effect of offset voltages but does not affect the music search functionality.
   Furthermore for the application circuit (Fig.1) the frequency response of the system between tape heads input, e. g. pins 12/13 (INA2/INB2), to the AMS input pins 5 and 2 (SCA and SCB) is quite constant over the whole frequency range (see Fig.3).
4. To activate the inputs IN1 pin (HS) might be left open-circuit. In this event the DC level at pin (HS) is 0.775V_{CC}.

General note

It is recommended to switch off V_{CC} with a gradient of 400 V/s at maximum to avoid plops on tape in case of contact between tape and tape head while switching off.



A: AMS threshold level for application circuit (Fig.1)
B: AMS threshold level for test circuit (Fig.11)

Fig.3 AMS threshold level.

Short description 'music search'

A system for 'music search' mainly consists of a level- and a time detection (see Fig.4).

For adapting and decoupling the input signal will be amplified (A), then rectified (B) and smoothed with a time constant (C). So the voltage at (C) corresponds to the signal level and will be compared to the predifined pause level at the first comparator (D), the level detector. If the signal level becomes smaller than the pause level, the level comparator (D) changes its output signal. Due to the output level of comparator 1 the capacitor of the second time constant (E) will be charged, respectively discharged. If the pause level of the input signal remains for a certain time, the voltage at the capacitor reaches a certain value, which corresponds to an equivalent time value. The voltage at the capacitor will be compared to a predefined time-equivalent voltage by the second comparator (F), the time detector. If the pause level of the input signal remains for this predefined time, the time detector (F) changes its output level for 'pause found' status.

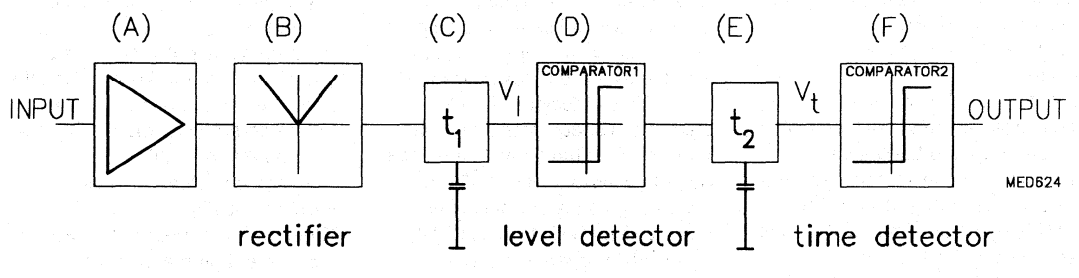


Fig.4 Integrated 'music search' function.

Dual Dolby* B-type noise reduction circuit for playback applications

TEA0675

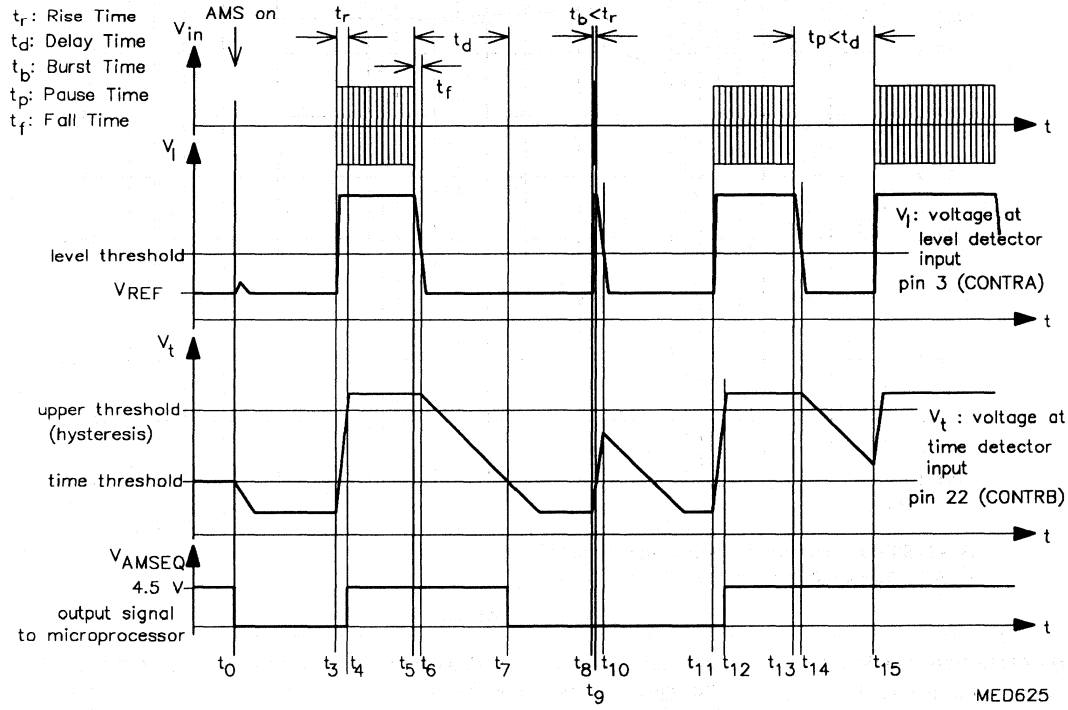


Fig.5 AMS-scan without initial signal.

Description of the principle timing diagram for AMS-scan mode (see Fig.5)

By activating AMS-scan mode, the AMS output level directly indicates whether the input level corresponds to a pause level (V_{AMSEQ} = LOW) or not (V_{AMSEQ} = HIGH).

At t_0 the AMS-scan mode is activated.

Without a signal at V_{in}, the following initial procedure runs until the AMS output changes to LOW level:

Due to no signal at V_{in} the voltage at the level detector input V_l (pin 3 (CONTRA)) remains below the level threshold and the second time constant will be discharged (time detector input V_t). When V_t passes the time threshold level, the time detector output changes to LOW level.

Now the initial procedure is completed.

If a signal burst appears at t_3, the level detector input voltage rises immediately and causes its output to charge the second time constant, which supplies the input voltage V_t for the time detector. When V_t passes the upper threshold level after the rise time t_r (at t_4), the AMS output changes to HIGH. IF the signal burst ends at t_5 the level detector input V_l falls to its LOW level. When passing the level threshold at t_6, the discharging of the second time constant begins.

Now the circuit measures the delay time t_d, which is externally fixed by a resistor and defines the length of a pause to be detected. If no signal appears at V_{in} within the time intervall t_d, the time detector output switches the AMS output to LOW level at t_7.

If a plop noise pulse appears at V_{in} (t_8) with a pulse width less than the rise time $t_r > t_b$, the plop noise will not be detected as music. The AMS output remains LOW.

Similar the system handles 'no music pulses' t_p:

When music appears at t_{11} with a small interuption at t_{13}, this interuption will not affect the AMS output for $t_p < t_d$.

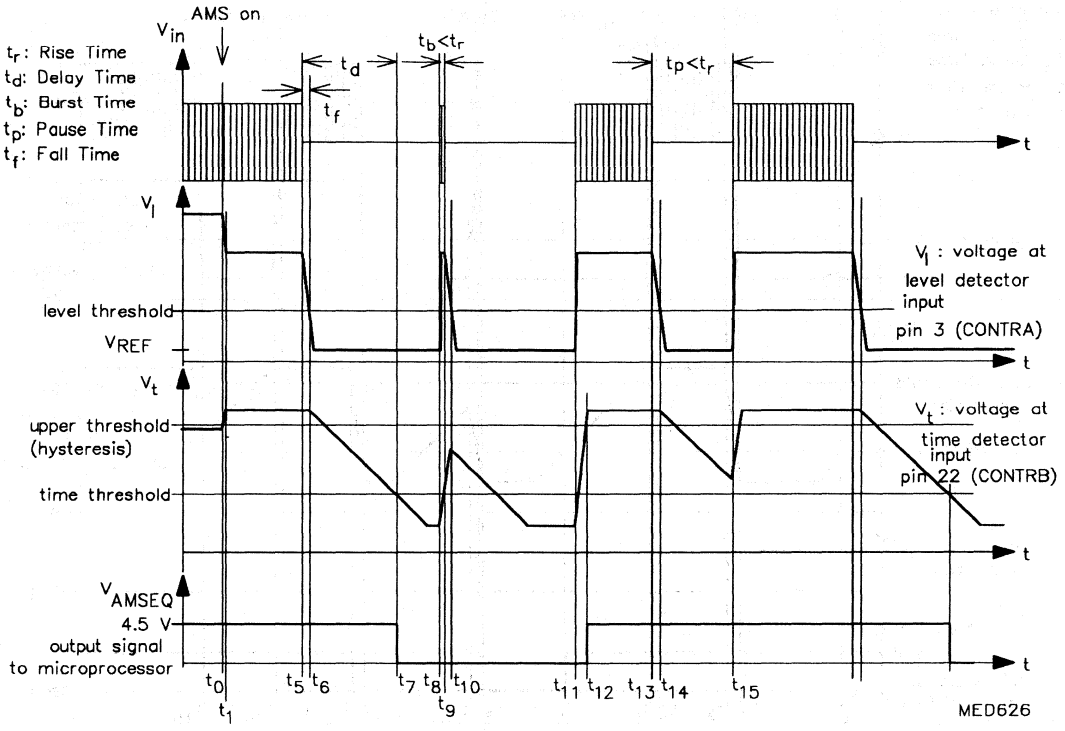


Fig.6 AMS-scan with initial signal.

Description of the principle timing diagram for AMS-scan mode with initial signal (see Fig.6)

At t_0 the AMS-scan mode is activated.

With a signal at V_{in}, the following initial procedure runs until the circuit gets a steady state status. Due to the signal at V_{in} the voltage at the level detector input V_l (pin 3 (CONTRA)) slides to a value which is defined by a limiter. This voltage causes the level detector output charging the second time constant (time detector input V_t) to its maximum voltage level at t_1.

Now the initial procedure is completed.

The following behaviour does not differ from the description of the principle timing diagram for AMS-scan mode (Fig.5).

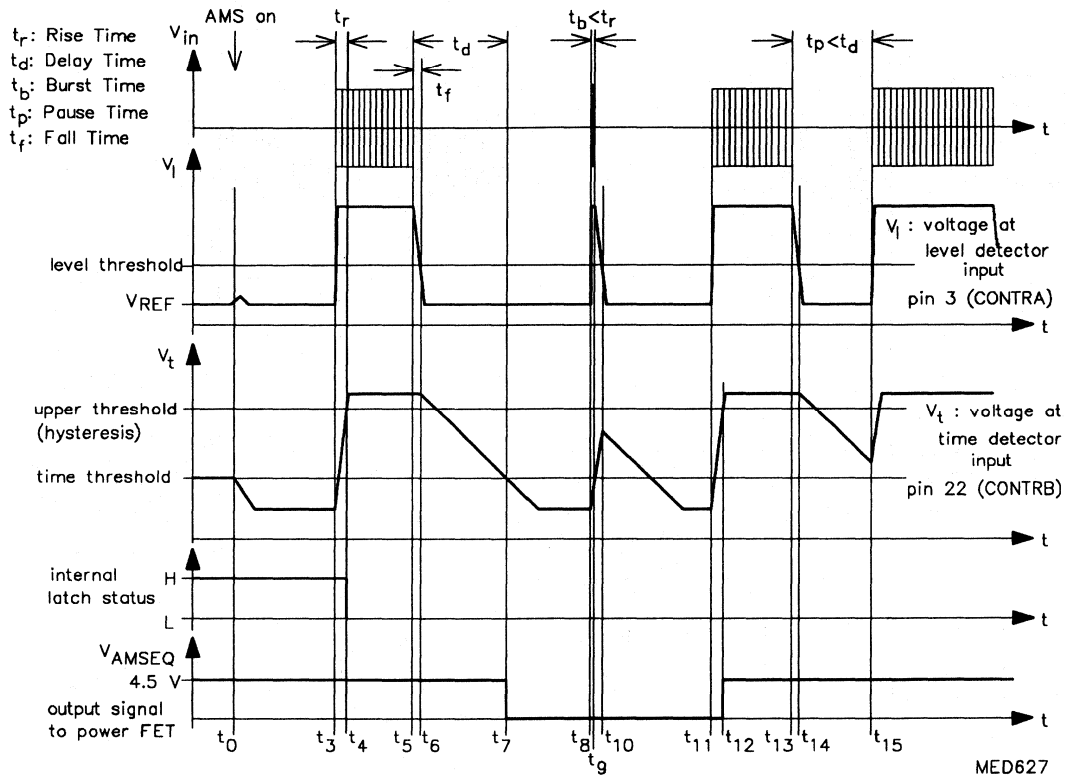


Fig.7 AMS-latch without initial signal.

The description of the principle timing diagram for AMS-latch mode (see Fig.7)

This is similar to the description of the principle timing diagram for AMS-scan mode. It only differs in its initial behaviour and its rise time t_r. (Please notice that the different t_r does not occure in the principle timing diagrams for latch and scan mode).

Running in AMS-latch mode, the circuit may be simply applied to drive a stop solenoid via a power FET. So the AMS output signal has not to be processed by a controller. Because there is no processor to make a decision whether there is a plop noise or not, for this mode the rise time t_r is extended to approximately 150 ms.

By activating AMS-latch mode the AMS output will not change to LOW level at t_2 if there is no initial signal at V_{in}. A latch forces the AMS output to be HIGH until a signal appears at V_{in} (t_4). After t_4 the latch will not affect the output any more until AMS-latch mode is started again.

The existance of the latch appears necessary if the AMS output for example drives a stop solenoid via a power FET. The LOW output level will cause a drive of the stop solenoid. This would happen after a maximum time of t_d occurred without any input signal. If there is no music on tape for a long time (e. g. at tape end), the AMS mode would be activated repeatedly as long as there is no signal at V_{in}. Thus the circuit waits until first music appears before detecting the pauses.

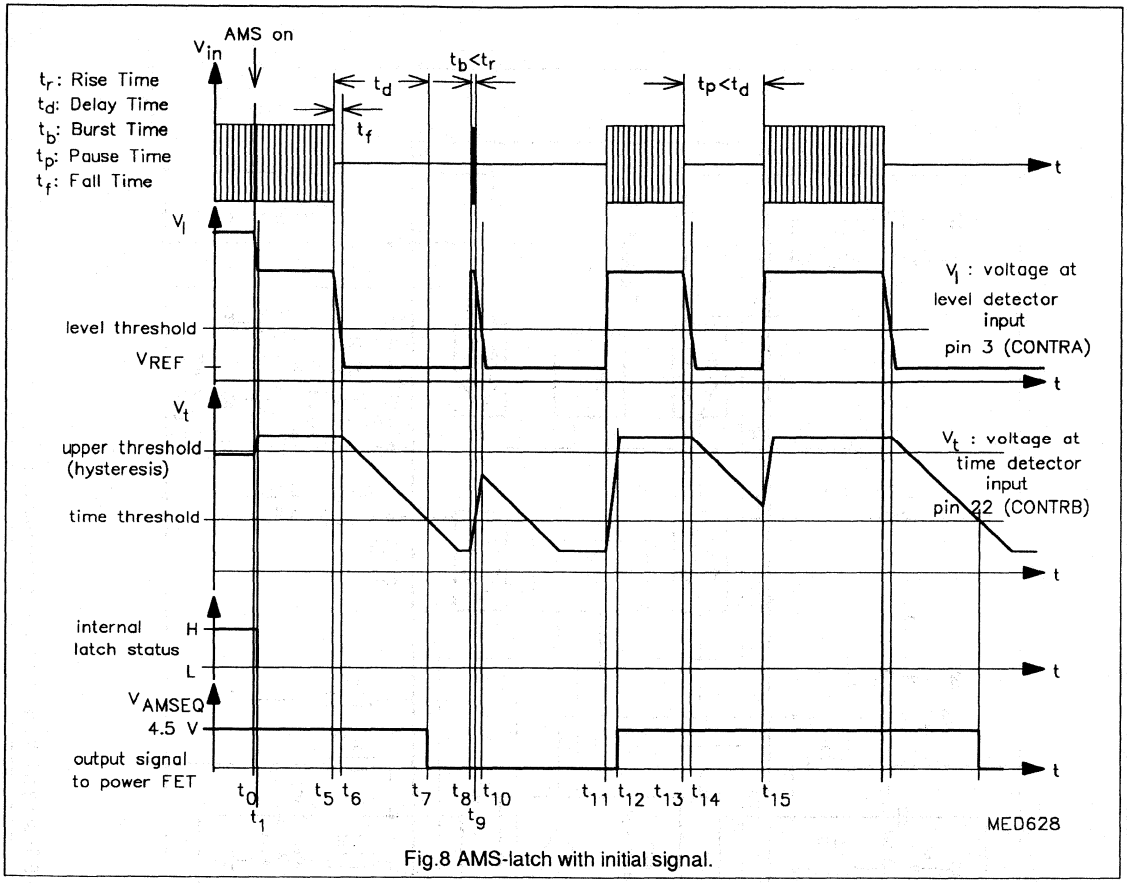


Fig.8 AMS-latch with initial signal.

The description of the principle timing diagram for AMS-latch mode with initial signal (see Fig.8)

This is similar to the description of the principle timing diagram for AMS-scan mode with initial signal (see Fig.6). It only differs in its rise time t_r and a release of its internal latch when voltage V_t passes the upper threshold between t_0 and t_1. Now the initial procedure is completed.

The following behaviour does not differ from the description of the principle timing diagram for AMS-latch mode (Fig.7).

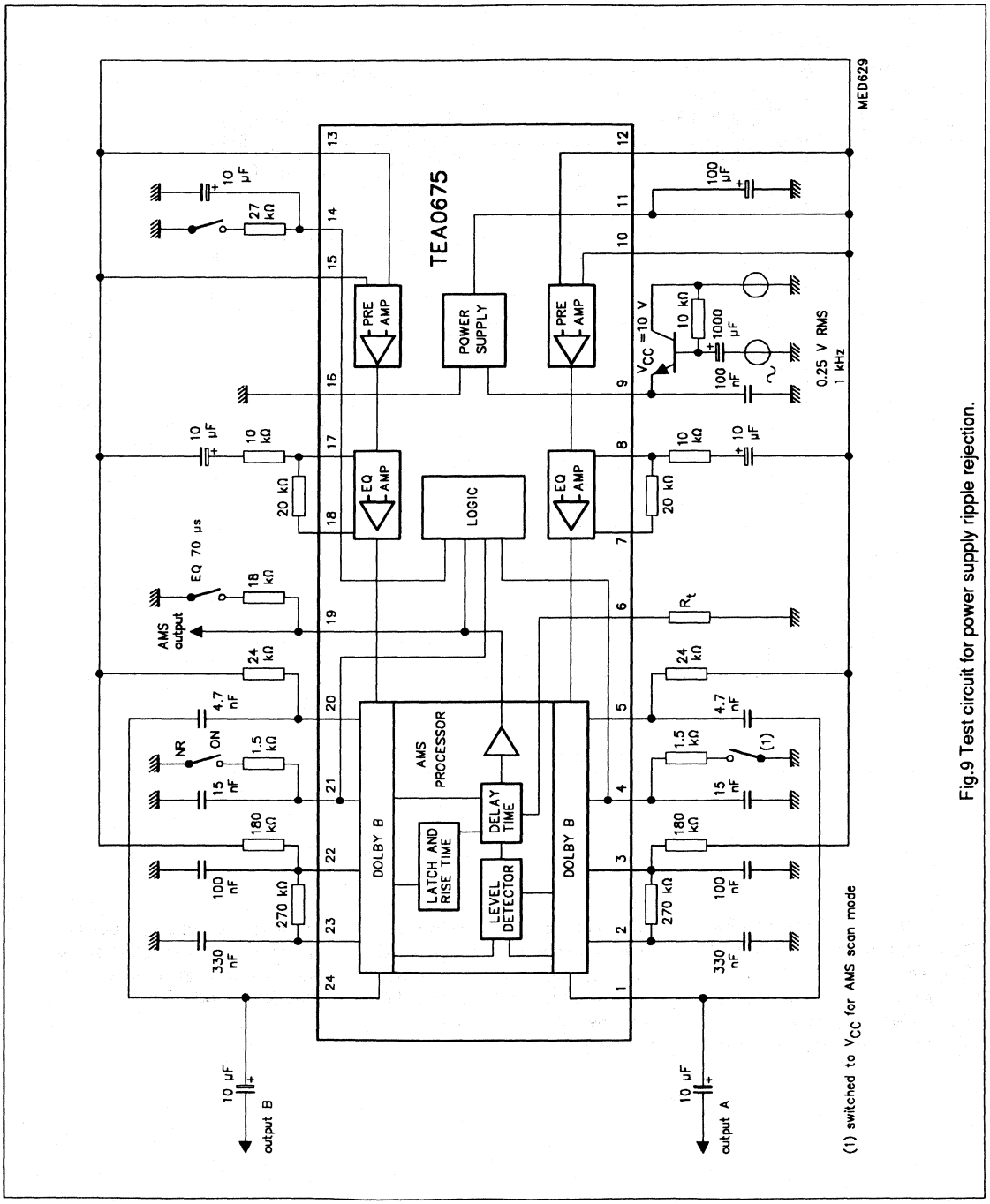


Fig.9 Test circuit for power supply ripple rejection.

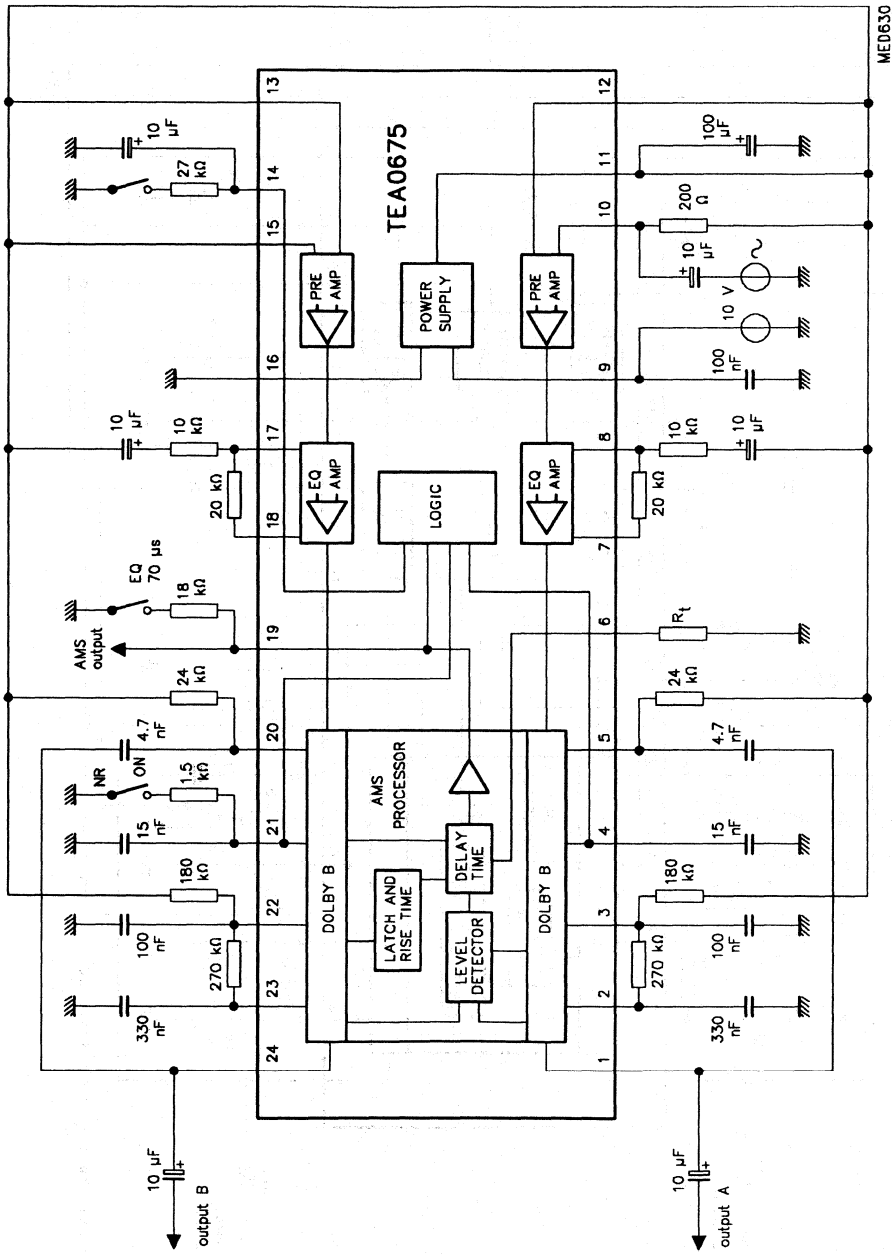


Fig.10 Test circuit for channel separation.

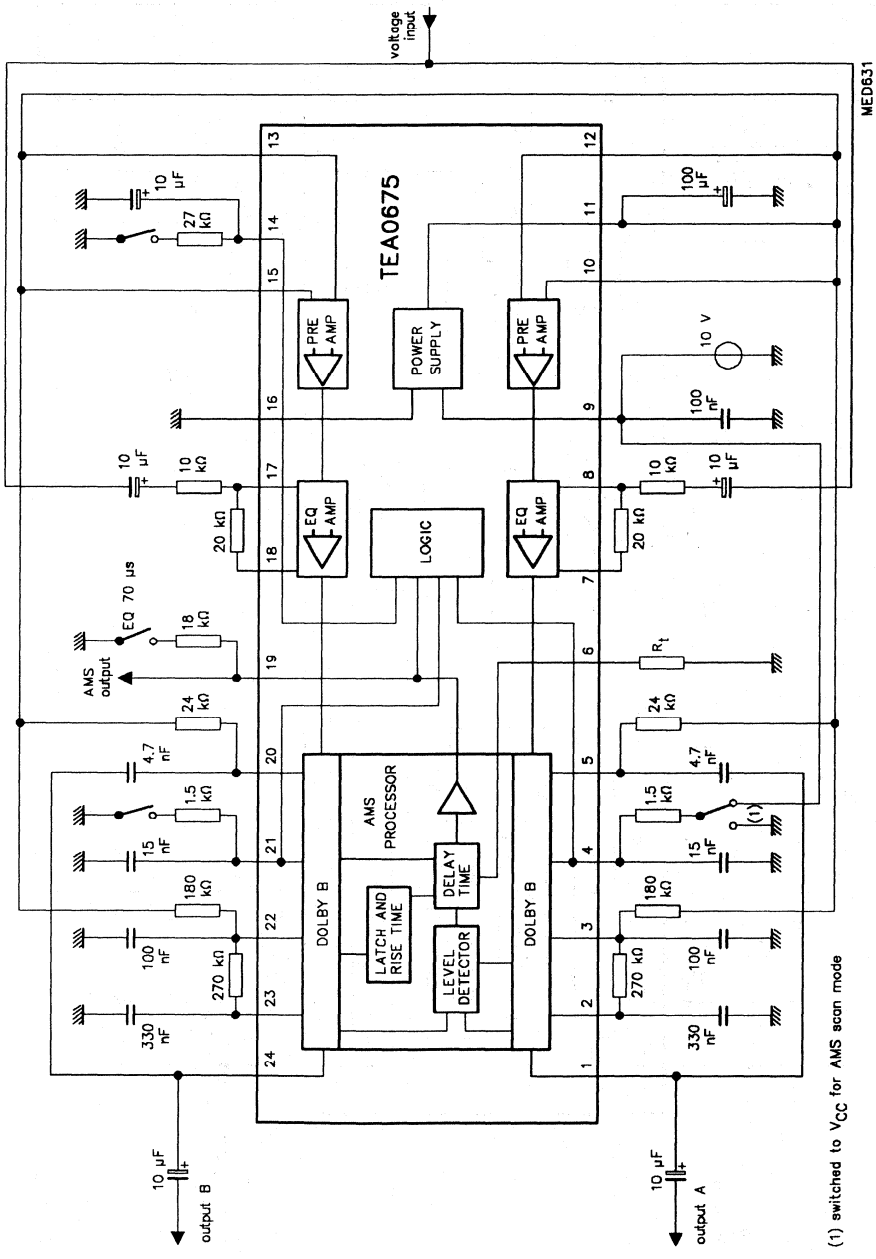


Fig.11 Test circuit for AMS threshold level.

Dual Dolby* B-type noise reduction circuit for playback applications

TEA0675

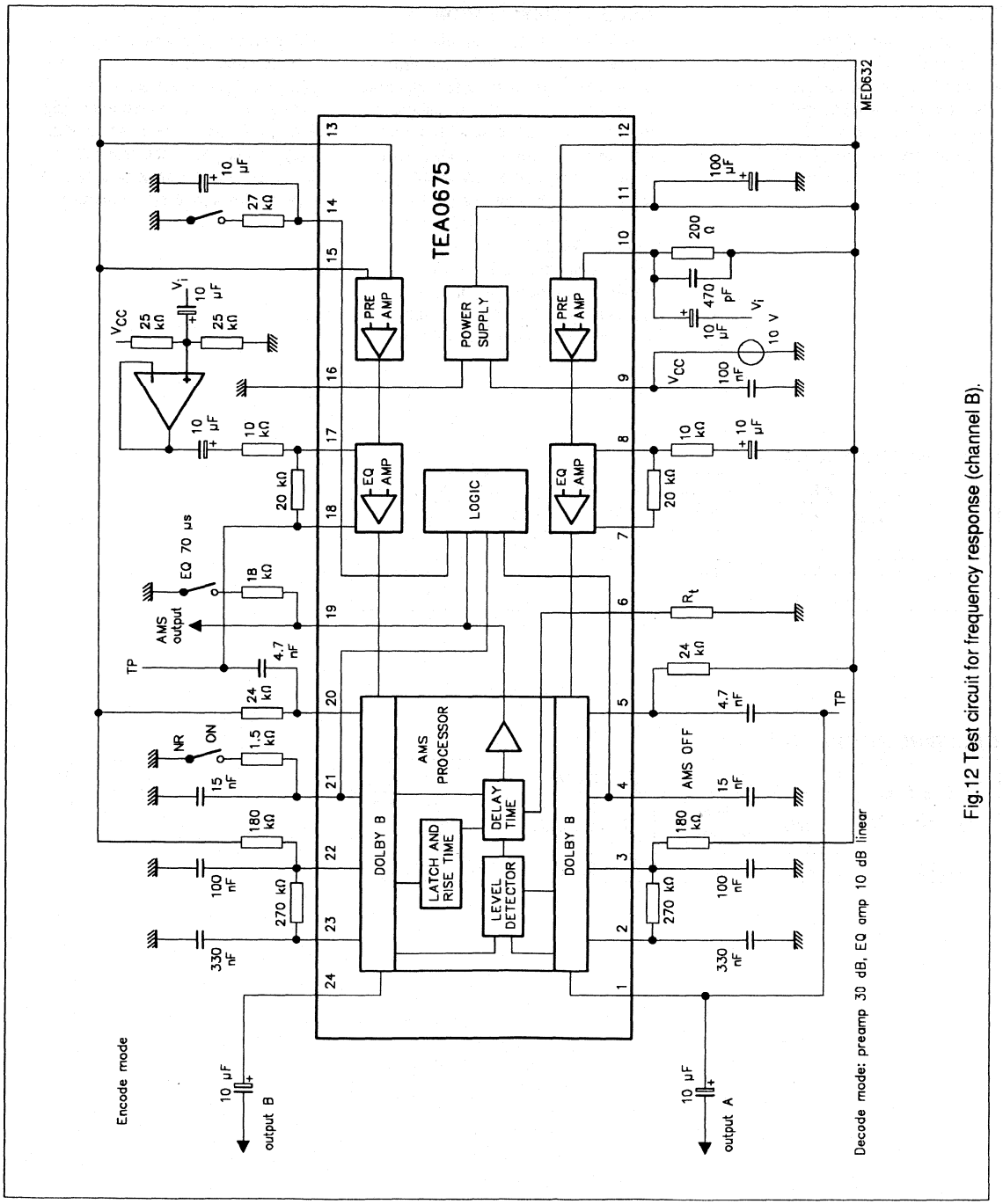


Fig.12 Test circuit for frequency response (channel B).

Dual pre-amplifier and equalizer for reverse tape decks

TEA0677T

FEATURES

- Head pre-amplifiers
- Reverse head switching
- Equalization with electronically switched time constants
- 0 dB = 387.5 mV
- Pin compatible to TEA0675 Dolby B, music search IC.

GENERAL DESCRIPTION

The TEA0677T is a monolithic bipolar integrated circuit intended for applications in car radios. It includes head and equalization amplifiers with electronically switchable time constants. Furthermore it includes electronically switchable inputs for tape drives with reverse heads. The device is intended to replace the regular TEA0675T in low-cost car radios using the same PCB. External components that are necessary for Dolby B and music search features can be omitted.

The device will operate with power supplies in the range of 7.6 V to 12.0 V, output overload level increasing with increase in supply voltage. Current drain varies with supply voltage, so it is advisable to use a regulated power supply or a supply with a long time constant.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage	7.6	10	12	V
I_{CC}	supply current	–	23	26	mA
(S+N)/N	signal-plus-noise to noise ratio	68	74	–	dB

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TEA0677T	24	SO	plastic	SOT137A

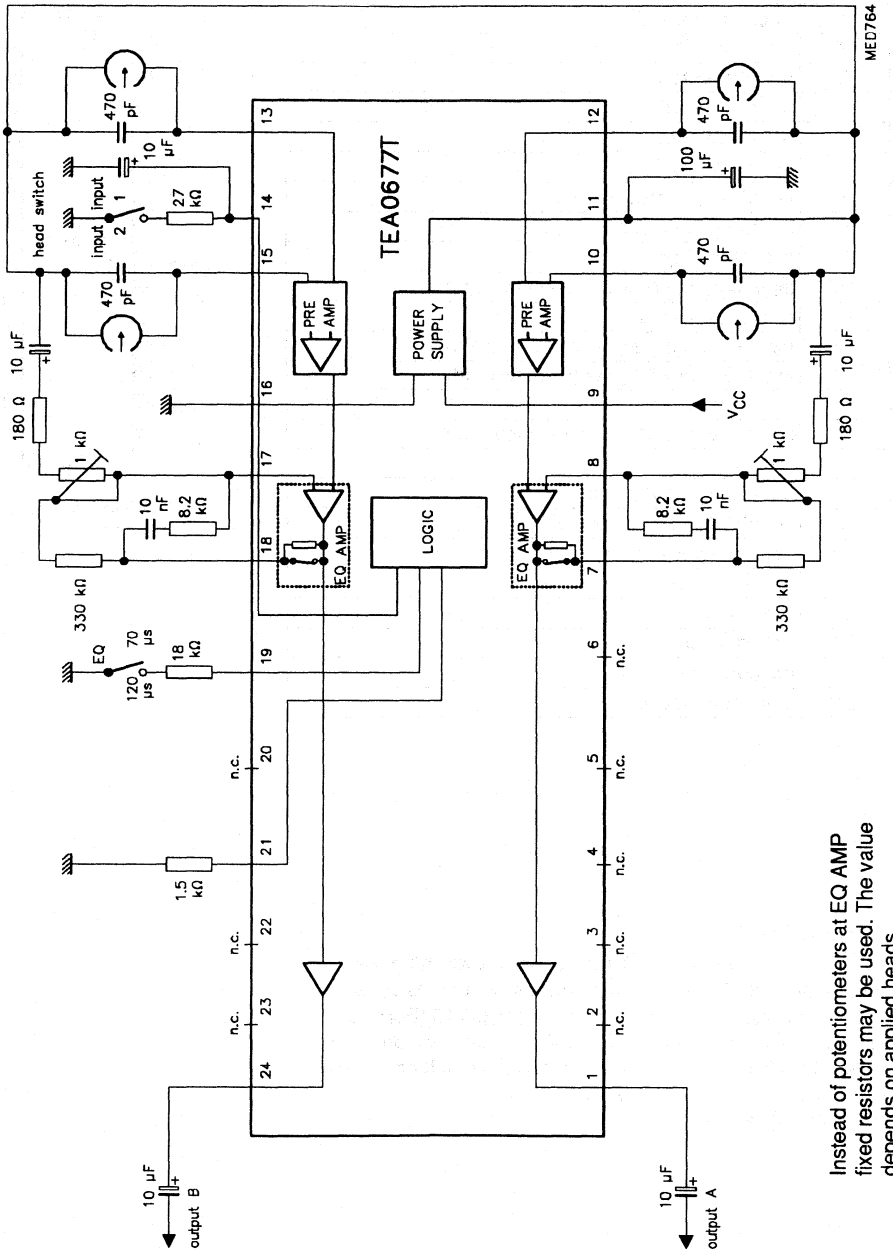


Fig.1 Block and application diagram.

Dual pre-amplifier and equalizer for reverse tape decks

TEA0677T

PINNING

SYMBOL	PIN	DESCRIPTION
OUTA	1	output channel A
n.c.	2	not connected
n.c.	3	not connected
n.c.	4	not connected
n.c.	5	not connected
n.c.	6	not connected
EQA	7	equalizing output channel A
EQFA	8	equalizing input channel A
V_{CC}	9	supply voltage
INA1	10	input channel A1 (forward or reverse)
V_{REF}	11	reference voltage
INA2	12	input channel A2 (reverse or forward)
INB2	13	input channel B2 (reverse or forward)
HS	14	head switch input
INB1	15	input channel B1 (forward or reverse)
GND	16	ground
EQFB	17	equalizing input channel B
EQB	18	equalizing output channel B
EQS	19	equalizing switch input
n.c.	20	not connected
ACUR	21	auxiliary current
n.c.	22	not connected
n.c.	23	not connected
OUTB	24	output channel B

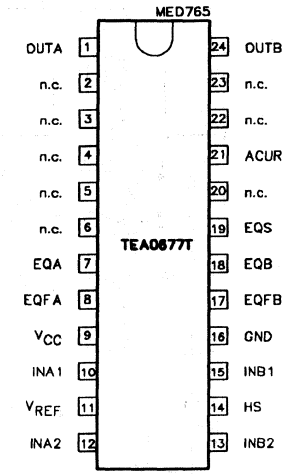


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

Head switching is achieved when pin 14 (HS) is connected to GND via a 27 kΩ resistor (inputs INA2, INB2 active), or left open-circuit (inputs INA1, INB1 active). The 10 μF capacitor at pin 14 sets the time constant for smooth switching.

Time constant switching for equalization (70 μs/120 μs) is achieved when pin 19 (EQS) is connected to ground via an 18 kΩ resistor (120 μs) or left open-circuit (70 μs).

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{CC}	DC supply voltage	0	16	V
V_I	input voltage (pin 1 to 24) except pin 11 (V_{REF}) to V_{CC}	−0.3	V_{CC}	V
t_{short}	pin 11 (V_{REF}) to V_{CC} short-circuiting duration	–	5	s
T_{amb}	operating ambient temperature	−40	+85	°C
T_{stg}	storage temperature	−65	+150	°C
T_s	soldering temperature (wave solder for 10 s at lead)	–	260	°C
V_{es}	electrostatic handling (note 1)	–	–	–

Note to the Limiting values

1. Classification A: human body model; C = 100 pF, R = 1.5 kΩ, V ≥ 2 kV; charge device model; C = 200 pF, R = 0 Ω, V ≥ 500 V.

CHARACTERISTICS

V_{CC} = 10 V; f = 20 Hz to 20 kHz; T_{amb} = +25 °C; all levels are referenced to 387.5 mV (RMS; 0 dB) at output; see Fig.1; EQ switch in the 70 μs position; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage		7.6	10	12	V
I_{CC}	supply current	pins 10, 12, 13 and 15 connected to V_{REF}	–	23	26	mA
	channel matching	f = 1 kHz; V_O = 0 dB	−0.5	–	+0.5	dB
THD	total harmonic distortion 2nd and 3rd harmonic	f = 1 kHz; V_O = 0 dB	–	0.04	0.1	%
		f = 10 kHz; V_O = 6 dB	–	0.08	0.15	%
	head room at output	V_{CC} = 7.6 V; THD = 1%; f = 1 kHz	12	14	–	dB
PSRR	power supply ripple rejection	0.25 V (RMS); f = 1 kHz; see Fig.3	45	50	–	dB
α_{CS}	channel separation	f = 1 kHz; V_O = +10 dB; see Fig.4	64	70	–	dB
α_{CC}	crosstalk between active and inactive input	f = 1 kHz; V_O = +10 dB	70	77	–	dB
R_{Lmin}	minimum load resistance at output	f = 1 kHz; V_O = 12 dB; THD = 1%	10	–	–	kΩ
G_v	voltage gain (pre-amplifier) from input pins 10, 12, 13 and 15 to pin EQF	f = 1 kHz	29	30	31	dB
V_{off}	input offset voltage		–	2	–	mV
I_B	input bias current		–	0.1	0.4	μA
R_{EQ}	equalizing resistor		4.7	5.8	6.9	kΩ
R_I	input resistance head inputs		60	100	–	kΩ
A_V	open-loop gain					
	pins INA1/INA2 to pin OUTA	f = 10 kHz	80	86	–	dB
	pins INB1/INB2 to pin OUTB	f = 400 Hz	104	110	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
N	equivalent noise voltage input (RMS value)	unweighted; 20 Hz to 20 kHz; R_{source} = 0 Ω	–	0.7	1.4	μV
(S+N)/N	signal-plus-noise to noise ratio	internal gain 40 dB linear; CCIR/ARM weighted; see Fig.4	68	74	–	dB
	DC output voltage; pins 1 (OUTA) and 16 (OUTB)	reference to V_{REF}; tape head DC coupled	–	–	±0.15	V
I_{OGND}	DC output current capability	to ground	–2	–	–	mA
I_{OVCC}	DC output current capability	to V_{CC}	300	–	–	μA
Z_O	output impedance		–	80	100	Ω
Switching thresholds						
Equalization (pin 19)						
V_{EQS}	voltage at pin EQS		–	–	5	V
I_{EQ70}	70 μs input current		–	–	–150	μA
I_{EQ120}	120 μs input current		–250	–	–1000	μA
Head switch (pin 14)						
V_{IN1}	inputs INA1 and INB1 active	note 1	0.65V_{CC}	0.775V_{CC}	1.0V_{CC}	V
I_{IN1}	maximum input current		–150	90	150	μA
V_{IN2}	inputs INA2 and INB2 active		0.1V_{CC}	0.225V_{CC}	0.35V_{CC}	V
I_{IN2}	maximum input current		–50	–90	–150	μA

Note to the characteristics

1. For an application with a fixed EQ time constant of 120 μs the equalizing network may be applied completely external. In this application the 8.2 kΩ resistor has to be changed to 14 kΩ and the internal resistor R_{EQ} = 5.8 kΩ must be short-circuited by fixing the EQ-switch input at the 70 μs position (pin 19; EQS left open-circuit). To activate the inputs INA1 and INB1 pin 10 (HS) may be left open-circuit. In this event the DC level at pin 10 (HS) is 0.775V_{CC}.

General note

It is recommended to switch off V_{CC} with a gradient of 400 V/s at maximum to avoid plops on tape in the event of contact between tape and tape head while switching off.

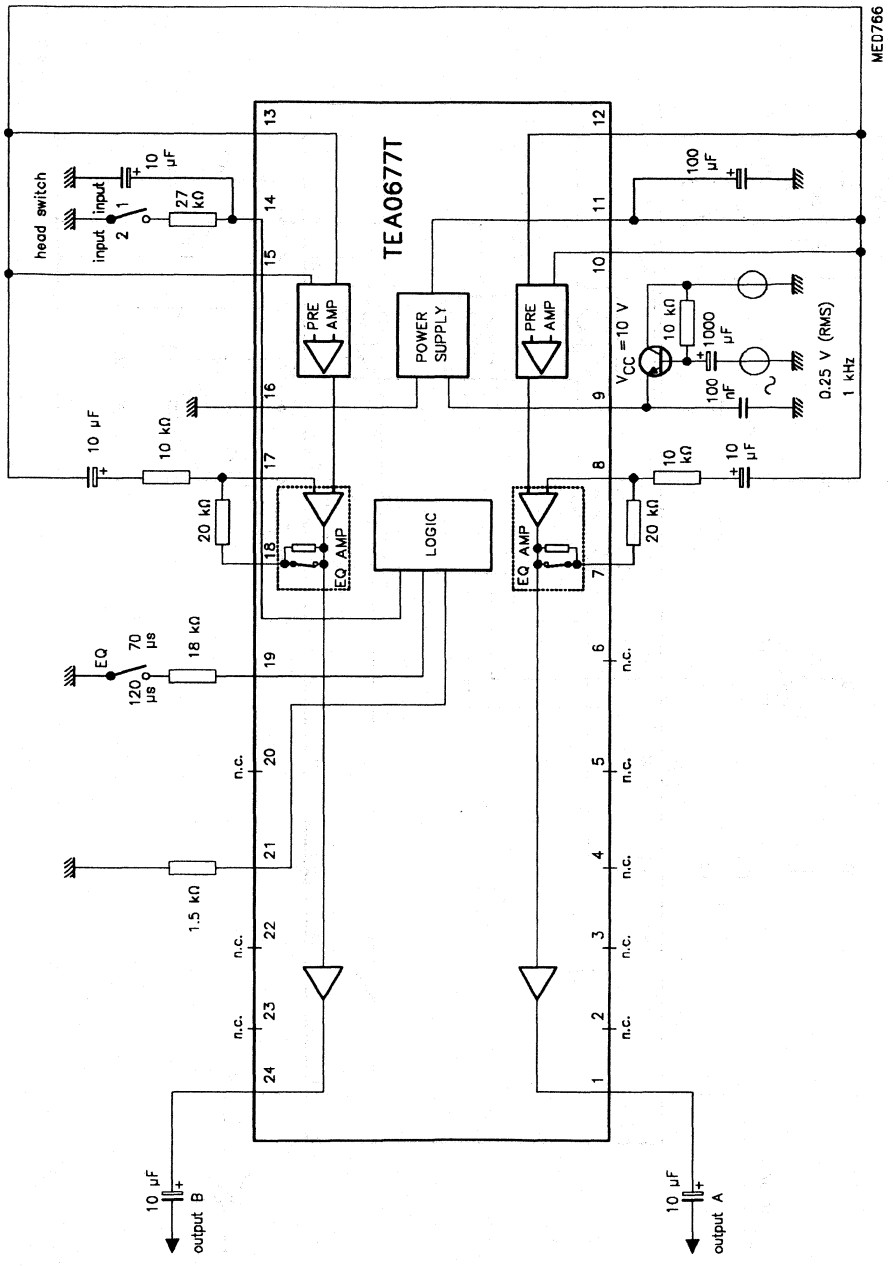


Fig.3 Test circuit for power supply ripple rejection.

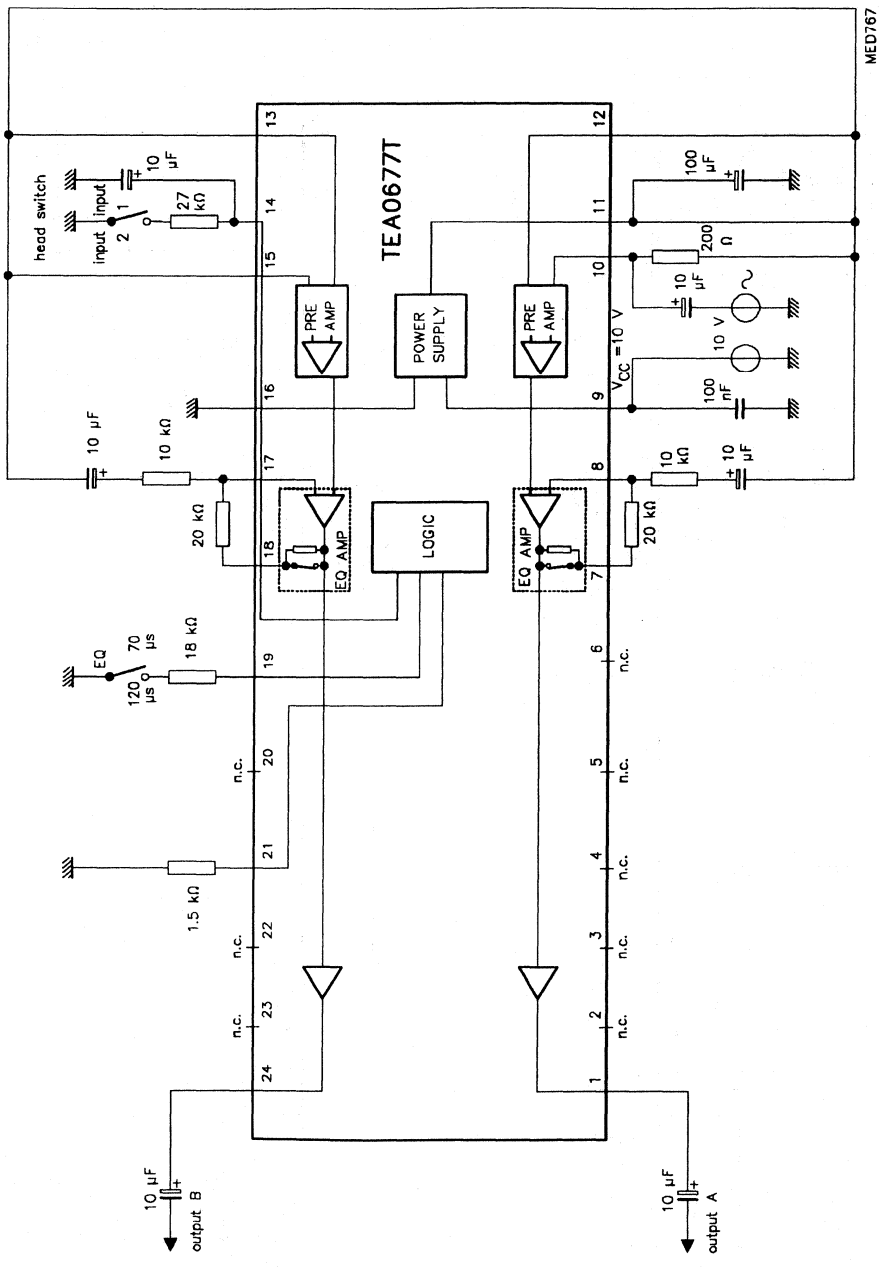
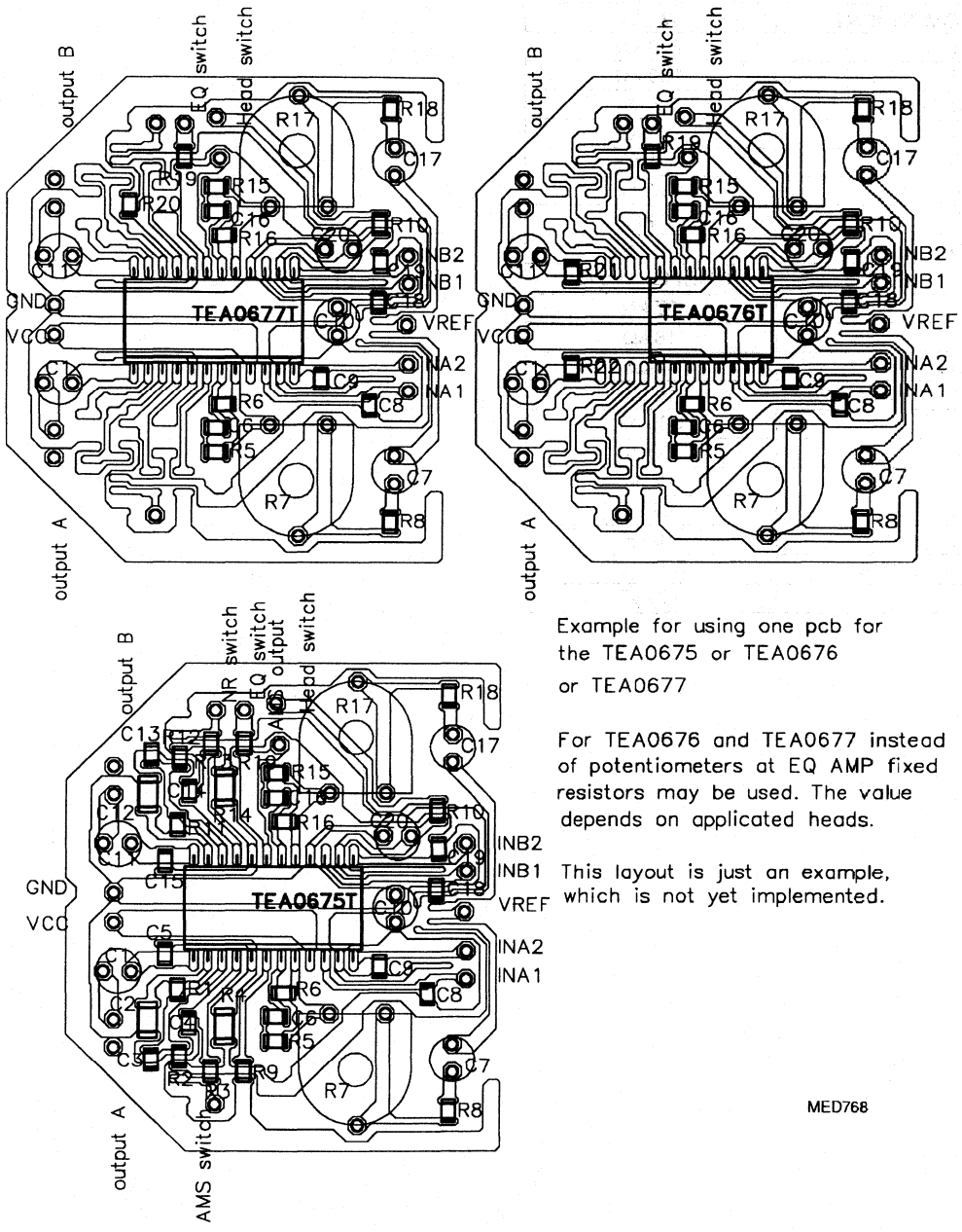


Fig.4 Test circuit for channel separation and signal-to-noise ratio.



Example for using one pcb for the TEA0675 or TEA0676 or TEA0677

For TEA0676 and TEA0677 instead of potentiometers at EQ AMP fixed resistors may be used. The value depends on applicated heads.

This layout is just an example, which is not yet implemented.

MED768

Fig.5 PCB layout example.

Table 1 Component list pcb layout example.

COMPONENT	VALUE
R1, R11	270 kΩ
R2, R12	180 kΩ
R3, R13, R20	1.5 kΩ
R4, R14	24 kΩ
R5, R15	8.2 kΩ
R6, R16	330 kΩ
R7, R17	1 kΩ
R8, R18	0.18 kΩ
R9	68 kΩ to 1000 kΩ
R10	27 kΩ
R19	18 kΩ
R21, R22	0 kΩ
C1, C11, C7, C17, C20	10 µF
C2, C12	330 nF
C3, C13	100 nF
C4, C14	15 nF
C5, C15	4.7 nF
C6, C16	10 nF
C8, C9, C18, C19	0.47 nF
C10	100 µF

Dual Dolby* B-type noise reduction circuit, automatic music search, with differential outputs and mute

TEA0678

FEATURES

- Dual noise reduction (NR) channels
- Head pre-amplifiers
- Reverse head switching
- Automatic Music Search (AMS)
- Mute position
- Equalization with electronically switched time constants
- Dolby reference level = 387.5 mV
- 32 pins
- Switch inputs TTL compatible
- Differential output stage has
  - capability to drive 1.2 nF capacitive load
  - capability to drive 1 kΩ load
  - short-circuit proof
  - short-circuit proof to 16 V via coupling capacitor.

GENERAL DESCRIPTION

The TEA0678 is a monolithic bipolar integrated circuit providing two channels of Dolby B noise reduction for playback applications in car radios. The TEA0678 includes head and equalization amplifiers with electronically switchable time constants. Furthermore the TEA0678 includes electronically switchable inputs for tape drives with reverse heads. This device also detects pauses of music in AMS (Automatic Music Search) mode, with a delay time fixed externally by a resistor. The short-circuit proof output stage of the TEA0678 is differential and provides muting. The device will operate with power supplies in the range of 7.6 V to 12.0 V, output overload level increasing with increase in supply voltage. Current drain varies with supply voltage, noise reduction on/off and AMS on/off so it is advisable to use a regulated power supply or a supply with a long time constant.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage	7.6	10	12	V
I_{CC}	supply current	–	25	28	mA
(S+N)/N	signal-plus-noise to noise ratio	78	84	–	dB

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TEA0678	32	DIL32SHR	plastic	SOT232AG
TEA0678T	32	SO32L	plastic	SOT287AH

*Available only to licensees of Dolby Laboratories Licensing Corporation, San Francisco, CA94111, USA, from whom licensing and application information must be obtained. Dolby is a registered trade-mark of Dolby Laboratories Licensing Corporation.

Dual Dolby* B-type noise reduction circuit, automatic music search, with differential outputs and mute

TEA0678

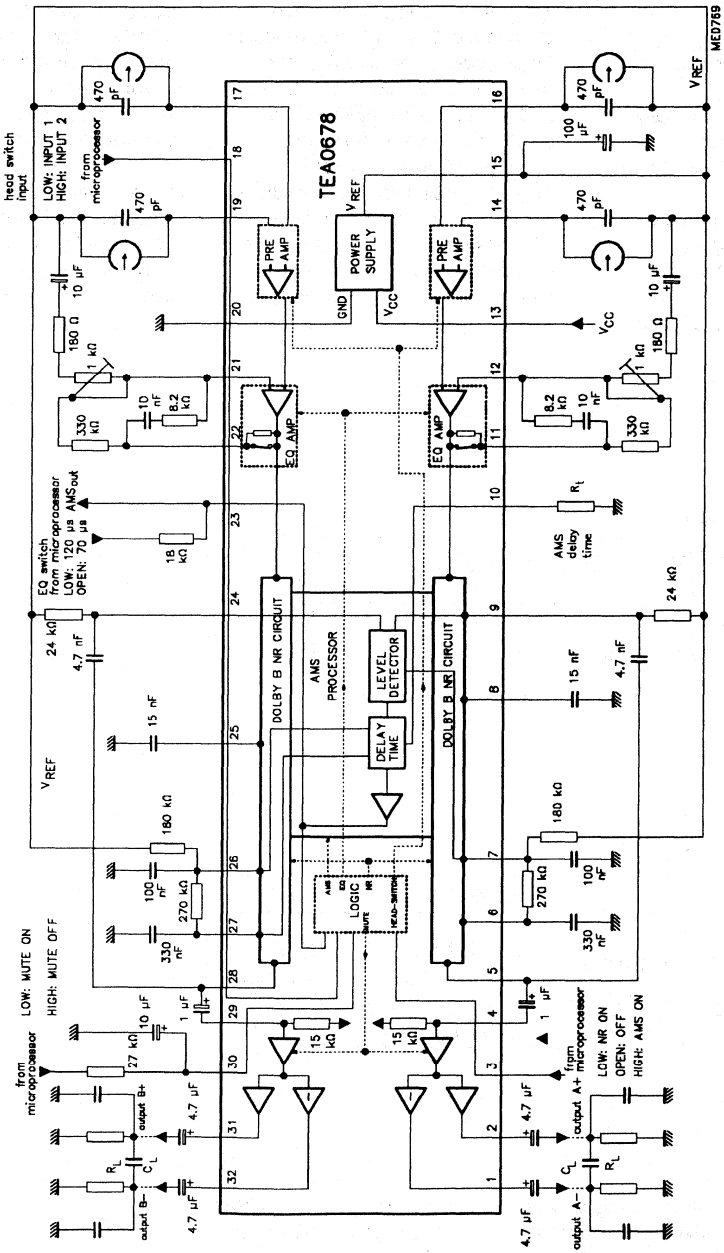


Fig.1 Block and application diagram.

Dual Dolby* B-type noise reduction circuit, automatic music search, with differential outputs and mute

TEA0678

PINNING

SYMBOL	PIN	DESCRIPTION
OUTA–	1	negative output channel A
OUTA+	2	positive output channel A
NR/AMS	3	noise reduction / music search switch
INCA	4	input mute / output stage channel A
OUTCA	5	output Dolby B processor channel A
INTA	6	integrating filter channel A
CONTRA	7	control voltage channel A
HPA	8	high-pass filter channel A
SCA	9	side chain channel A
TD	10	delay time constant
EQA	11	equalizing output channel A
EQFA	12	equalizing feedback channel A
V_{CC}	13	supply voltage
INA1	14	input channel A1 (forward or reverse)
V_{REF}	15	reference voltage
INA2	16	input channel A2 (reverse or forward)
INB2	17	input channel B2 (reverse or forward)
HS	18	head switch input
INB1	19	input channel B1 (forward or reverse)
GND	20	ground
EQFB	21	equalizing feedback channel B
EQB	22	equalizing output channel B
AMSEQ	23	AMS output and EQ-switch input
SCB	24	side chain channel B
HPB	25	high-pass filter channel B
CONTRB	26	control voltage channel B
INTB	27	integrating filter channel B
OUTCB	28	output Dolby B processor channel B
INCB	29	input mute / output stage channel B
MUTE	30	mute switch
OUTB+	31	positive output channel B
OUTB–	32	negative output channel B

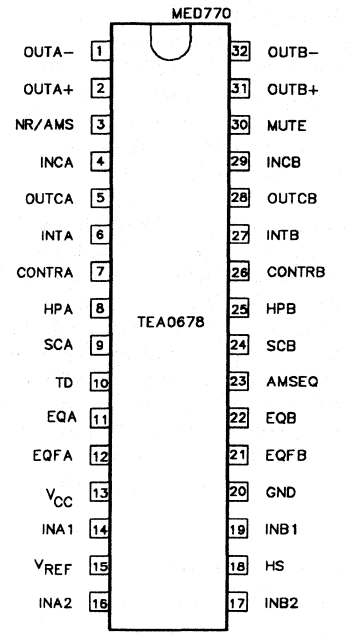


Fig.2 Pin configuration.

Dual Dolby* B-type noise reduction circuit, automatic music search, with differential outputs and mute

TEA0678

FUNCTIONAL DESCRIPTION

Noise Reduction (NR) is enabled when pin 3 (NR/AMS) is connected to ground and OFF when open-circuit (left floating from a 3-state output). Dolby noise reduction only operates correctly if 0 dB Dolby level is adjusted at 387.5 mV at test point TP.

Automatic Music Search (AMS) is enabled when pin 3 (NR/AMS) is connected to HIGH (5 V) and OFF when open-circuit (left floating from a 3-state output). In AMS mode the signal of both channels are rectified and then added. This means, even if one channel signal appears inverted to the other channel, with the TEA0678 the normal AMS function is ensured (see Figs 4, 5 and 6).

Time constant switching for equalization is achieved when pin 23 (AMSEQ) is connected to GND via an 18 kΩ resistor (120 μs), or open-circuit (70 μs). This does not affect the AMS output signal during AMS mode (see Fig.1).

Head switching is achieved when pin 18 (HS) is connected to GND (input IN1 active) or connected to HIGH (5 V) level (input IN2 active). If left open-circuit IN1 is active.

Mute is enabled when pin 30 (MUTE) is connected to ground and OFF when connected to HIGH (5 V) level. For smooth switching a time constant is recommended. If left open-circuit MUTE is active.

The **Differential output stage** of each channel is connected via a provision to the Dolby and pre-amplifier part. This provision may be used for any processing the tape signal or add another signal. Each output drives a resistive load of nominal 10 kΩ and is capable of driving 1 kΩ, also a capacitive load of 1.2 nF to ground and between differential outputs. Each output can be short-circuited to a battery (16 V) via a coupling capacitor (4.7 μF).

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC134).
The device may not operate correctly when subjected to these ratings when the ratings exceed the electrical characteristics of the device as specified in the 'characteristics'. The device will recover automatically when the environment is reduced to the requirements of the 'characteristics'.

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{CC}	DC supply voltage	0	16	V
V_I	input voltage (pin 1 to 32) except pin 15 (V_{REF}), pin 3 (NR/AMS), pin 18 (HS) and pin 30 (MUTE) to V_{CC}	−0.3	V_{CC}	V
	input voltage at pin 3 (NR/AMS), pin 18 (HS) and pin 30 (MUTE); note 1	−0.3	6.5	V
t_{short}	pin 15 (V_{REF}) to V_{CC} short-circuiting duration	−	5	s
T_{amb}	operating ambient temperature	−40	+85	°C
T_{stg}	storage temperature	−65	+150	°C
T_s	soldering temperature (wave solder for 10 s at lead)	0	+260	°C
V_{es}	electrostatic handling (note 2)	−	−	−

Notes to the Limiting values

1. The TEA0678 allows a high level at switching pins without supply voltage (V_{CC} = 0; 'standby' mode). This means a maximum input voltage of 6.5 V for the switching input pins.
2. Classification A: human body model; C = 100 pF, R = 1.5 kΩ, V ≥ 2 kV; charge device model; C = 200 pF, R = 0 Ω, V ≥ 500 V.

CHARACTERISTICS

V_{CC} = 10 V; f = 20 Hz to 20 kHz; T_{amb} = +25 °C; nominal load 10 kΩ; all levels are referenced to 775 mV (RMS; 0 dB) at differential outputs ($V_O = V_{O+} - V_{O-}$), this corresponds to Dolby level 387.5 mV (RMS; 0 dB) at test point (OUTC); see Fig.1; NR ON/AMS OFF; EQ switch in the 70 µs position; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage		7.6	10	12	V
I_{CC}	supply current	pins 14, 16, 17 and 19 connected to V_{REF}	–	25	28	mA
		f = 1 kHz; V_O = 0 dB at each output	–	26	37	mA
	channel matching	f = 1 kHz; V_O = 0 dB; NR OFF; OUTA/OUTB	–0.5	–	+0.5	dB
G_v	voltage gain (output stage)	between OUT and OUTC; f = 1 kHz; NR OFF	5.5	6	6.5	dB
	voltage gain mismatch (output stage)	mismatch between OUT+ and OUT–; f = 1 kHz; NR OFF	–0.5	–	+0.5	dB
THD	total harmonic distortion 2nd and 3rd harmonic	f = 1 kHz; V_O = 0 dB	–	0.08	0.15	%
		f = 10 kHz; V_O = 6 dB	–	0.15	0.3	%
	head room at output	V_{CC} = 9 V; THD = 1%; f = 1 kHz	13	–	–	dB
(S+N)/N	signal-plus-noise to noise ratio (decode mode)	pins 14, 16, 17 and 19 connected to V_{REF}; internal CCIR/ARM weighted; differential output 775 mV; see Fig.10	78	84	–	dB
N	equivalent input noise voltage in decode mode (RMS value)	pins 14, 16, 17 and 19 connected to V_{REF}; NR OFF; unweighted; see Fig.10	–	–	1.4	µV
PSRR	power supply ripple rejection	0.25 V (RMS); f = 1 kHz; see Fig.7 for unsymmetrical signal at OUTC	52	57	–	dB
		at differential OUT; note 1	49	52	–	dB
	frequency response measured in encode mode; referenced to TP	see Fig.10; NR OFF				
		V_O = –25 dB; f = 200 Hz	–22.9	–24.4	–25.9	dB
		V_O = 0 dB; f = 1 kHz	–1.5	0	+1.5	dB
		V_O = –25 dB; f = 1 kHz	–17.8	–19.3	–20.8	dB
		V_O = –25 dB; f = 5 kHz	–18.1	–19.6	–21.1	dB
		V_O = –35 dB; f = 10 kHz	–24.4	–25.9	–27.4	dB
α_{CS}	channel separation	V_O = +10 dB; f = 1 kHz; see Fig.8	61	67	–	dB
α_{CC}	crosstalk between active and inactive input	NR OFF; f = 1 kHz; V_O = +10 dB; see Fig.8	70	77	–	dB
R_L	load resistance at each output OUTA+; OUTA–; OUTB+; OUTB– (corresponds to 2 kΩ at differential output)	AC coupled f = 1 kHz; V_O = 12 dB;				
		THD = 1%	10	–	–	kΩ
		THD = 1%; note 2	1	–	–	kΩ
C_L	capacitive load at each output (between OUT+ and OUT–) and ground	C_{Lmin} at each output to ground (pins 1, 2, 31 and 32)	0.3	–	1.3	nF
G_v	voltage gain (pre-amplifier) from input pins 14, 16, 17 and 19 to pin EQF	f = 1 kHz	29	30	31	dB
V_{off}	input offset voltage		–	2	–	mV
I_B	input bias current		–	–	0.4	µA
R_{EQ}	equalizing resistor		4.7	5.8	6.9	kΩ

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
R_I	input resistance head inputs		60	100	–	kΩ
A_V	open-loop gain					
	pins INA1/INA2 to pin EQA	f = 10 kHz	80	86	–	dB
	pins INB1/INB2 to pin EQB	f = 400 Hz	104	110	–	dB
	DC offset OUT+ to OUT–	pins 14, 16, 17 and 19 connected to V_{REF}	–10	–	10	mV
	MUTE offset OUT+ to OUT–	pins 14, 16, 17 and 19 connected to V_{REF}	–10	–	10	mV
	DC output offset voltage at OUTC	NR OFF; $V_{REF} - V_{OUTC}$; pins 14, 16, 17 and 19 connected to V_{REF}	–0.15	–	+0.15	V
I_O	DC output current	pins 14, 16, 17 and 19 connected to V_{REF}				
		pin OUTC to ground	–2	–	–	mA
		pin OUTC to V_{CC}	0.3	–	–	mA
		pin OUT± to ground	–2.5	–	–	mA
		pin OUT± to V_{CC}	2.5	–	–	mA
R_{IO}	input resistance output stage pins 4 and 29 (INC)		10	16	–	kΩ
R_O	output resistance OUTA+, OUTA–, OUTB+ and OUTB–	each output	–	90	110	Ω
	mute depth at differential output	NR OFF;				
		f = 1 kHz	–80	–	–	dB
		f = 10 kHz	–80	–	–	dB
AMSL	AMS threshold level at music to pause	NR OFF; f = 10 kHz; see Fig.9	–25	–22	–19	dB
AMSH	AMS threshold level at pause to music	note 3	–24	–21	–18	dB
t_d	AMS delay time range	f = 10 kHz; 0 dB burst; note 4	–	23 to 160	–	ms
t_r	AMS rise/delay time	f = 10 kHz; 0 dB burst	2	–	10	ms
Switching thresholds						
NR/AMS switch (pin 3)						
V_{IL}	LOW level input voltage	NR ON	–0.3	–	0.8	V
I_{IL}	LOW level input current		–10	–20	–40	µA
	allowed floating input current	pin left open-circuit; NR/AMS OFF	–10	0	10	µA
	floating voltage		–	2.4	5	V
V_{IH}	HIGH level input voltage	AMS ON	4	–	5.5	V
I_{IH}	HIGH level input current		10	20	40	µA
Equalization (pin 23)						
I_{EQ70}	70 µs floating leakage current		0.002	–	–0.15	mA
V_{EQ70}	70 µs floating voltage		–	4.6	5	V
I_{EQ120}	120 µs input current		–0.25	–	–1	mA
AMS output (pin 23)						
V_{OH}	HIGH level output voltage	music present	4	4.6	5	V
I_{OH}	HIGH level output current	current capability	0.01	–	–1	mA
I_{OH}	HIGH level output current	current capability; note 5	0.01	–	–0.15	mA
V_{OL}	LOW level output voltage	music not present	–	–	0.8	V
I_{OL}	LOW level output current	current capability	–0.01	–	1	mA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
MUTE switch (pin 30)						
V_{IL}	LOW level input voltage	MUTE ON	−0.3	–	0.8	V
I_{IL}	LOW level input current		–	−4	−100	μA
V_{IH}	HIGH level input voltage	MUTE OFF	4	–	5.5	V
I_{IH}	HIGH level input current	MUTE OFF; smooth switching with a time constant is recommended	–	10	100	μA
Head switch (pin 18)						
V_{IL}	LOW level input voltage	INPUT 1 ON	−0.3	–	0.8	V
I_{IL}	LOW level input current		–	–	−100	μA
V_{IH}	HIGH level input voltage	INPUT 2 ON	4	–	5.5	V
I_{IH}	HIGH level input current		–	30	100	μA

Notes to the characteristics

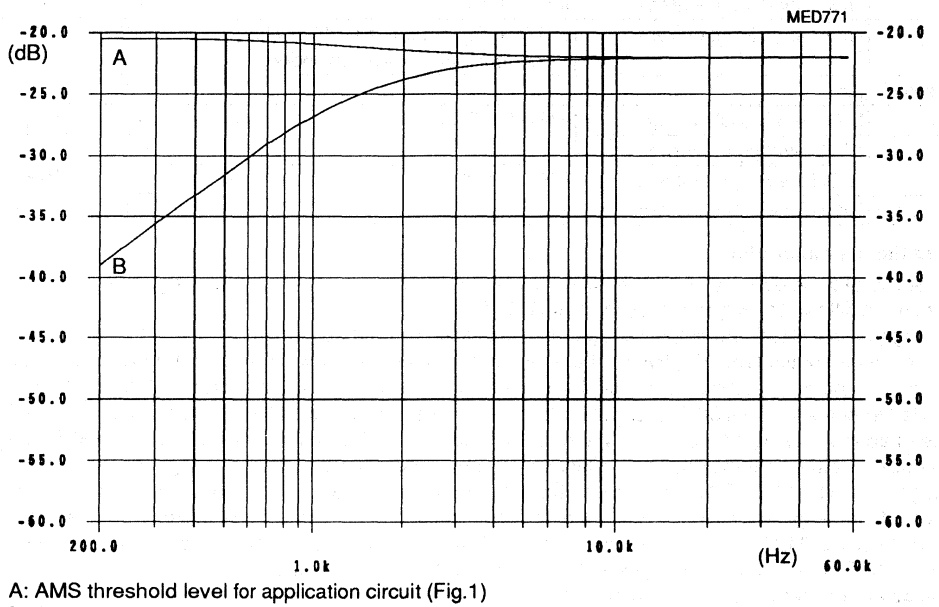
1. For the signal to be doubled (+6 dB) at differential output as a function of OUTC, the signal-to-ripple ratio is improved at differential output for approximately 3 dB.
2. By using the small load, the output voltage may be divided by −0.8 dB.
3. The high speed of the tape (FF, REW) at the tape head during AMS mode causes a transformation of level and frequency of the originally recorded signal. It means a boost of signal level of approximately 10 dB and more for recorded frequencies from 500 Hz up to 4 kHz. So the threshold level of −22 dB corresponds to signal levels in PB mode of approximately −32 dB. The AMS inputs for each channel are pin 9 (SCA) and pin 24 (SCB). As the frequency spectrum is transformed by a factor of approximately 10 to 30 due to the higher tape speed in FF, REW, the high-pass filter (4.7 nF/24 kΩ) removes the effect of offset voltages but does not affect the music search function. In the application circuit (Fig.1) the frequency response of the system between tape heads input, e. g. pins 16/17 (INA2/INB2), to the AMS input pins 9 and 24 (SCA and SCB) is constant over the whole frequency range (see Fig.3). The frequency dependence of threshold level is shown in Fig.3.
4. Blank delay time set by resistor R_t at pin TD:

RESISTOR VALUE R_t (kΩ)	DELAY TIME t_d TYP. (ms)	TOLERANCE (%)
68	23	20
150	42	15
180	48	15
220	56	15
270	65	10
330	76	10
470	98	10
560	112	10
680	126	10
820	142	10
1000	160	10

5. In AMS OFF mode, pin 23 (AMSEQ) is HIGH level, the equalization time constant will be switched by pulling approximately 200 μA out of pin 23 (AMSEQ). This means for the device connected to pin 23 (AMSEQ), a restriction of input current at HIGH level less than 200 μA during AMS OFF; otherwise the switching of the time constants is disabled but fixed at 120 μs. If the following devices input consumes more than 200 μA, this input has to be disconnected in AMS OFF mode. (To ensure switching the currents for the different switched modes are specified with a head room of ±50 μA in the 'characteristics.') For an application with a fixed EQ time constant of 120 μs the equalizing network may be applied completely external. Change 8.2 kΩ resistor to 14 kΩ the internal resistor R_{EQ} = 5.8 kΩ is short-circuited by fixing the EQ-switch input at the 70 μs position (I_{EQ70}).

General note

It is recommended to switch off V_{CC} with a gradient of 400 V/s at maximum to avoid plops on tape in the event of contact between tape and tape head while switching off.



A: AMS threshold level for application circuit (Fig.1)
B: AMS threshold level for test circuit (Fig.9)

Fig.3 AMS threshold level.

General note on AMS

The speed of tape at the tape head during FF, REW depends on the diameter of the tape on the spindle.
In dependence of this speed the recorded signal occurs transformed in frequency and magnitude as a function of the original signal in playback mode speed. For example:
A recorded pause of 3 s passes the tape head at its highest speed in 111 ms, e. g. during FF mode near tape end. This time constant of 111 ms corresponds to a pause of 1.3 s at the beginning of the tape in playback mode. Thus a pause T is uniquely defined outside the interval $1.3\ s < T < 3\ s$. Inside this interval T will be recognized as a pause or not dependent on the local point of tape, respectively the speed of tape. Times of pauses described investigated for this document are valid for tape devices with a speed of its spindle (FF, REW):

$$\omega_r = 51\ \frac{1}{s}$$

respectively 12 to 27 times of the playback speed.

Dual Dolby* B-type noise reduction circuit, automatic music search, with differential outputs and mute

TEA0678

Short description 'music search'

A system for 'music search' mainly consists of a level- and a time detection (see Fig.4).
For adapting and decoupling the input signal will be amplified (A), then rectified (B) and smoothed with a time constant (C). So the voltage at (C) corresponds to the signal level and will be compared to the predefined pause level at the first comparator (D), the level detector. If the signal level becomes smaller than the pause level, the level comparator (D) changes its output signal. Due to the output level of comparator 1 the capacitor of the second time constant (E) will be charged, respectively discharged. If the pause level of the input signal remains for a certain time, the voltage at the capacitor reaches a certain value, which corresponds to an equivalent time value due to the charging. The voltage at the capacitor will be compared to a predefined time-equivalent voltage by the second comparator (F), the time detector. If the pause level of the input signal remains for this predefined time, the time detector (F) changes its output level for 'pause found' status.

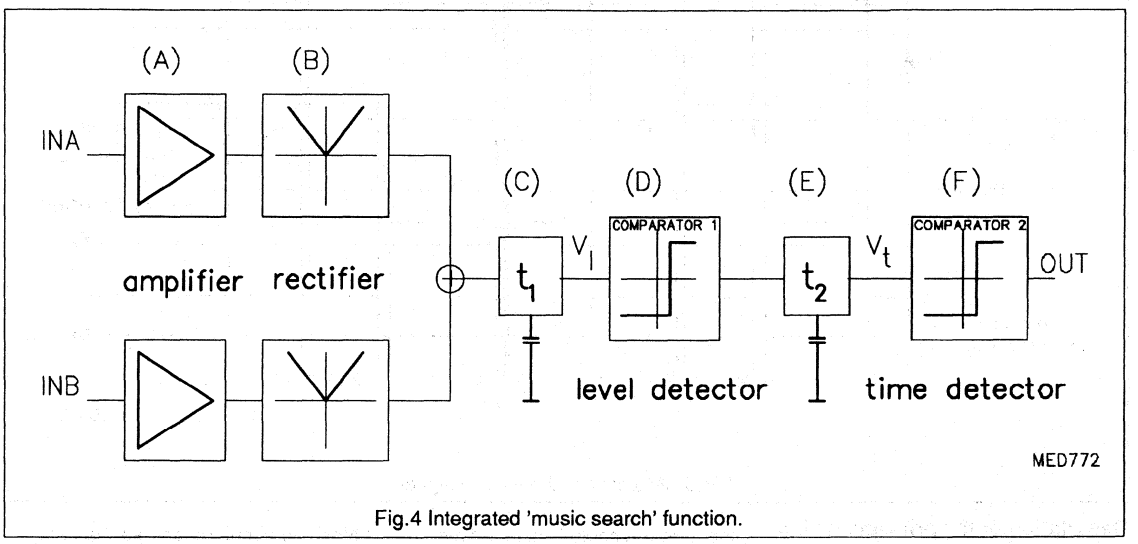


Fig.4 Integrated 'music search' function.

In this IC the signals of both channels are first rectified and then added. The signal behind the adder is described by
$V_{add} = |V_{chanA}| + |V_{chanB}|$
$|V_{chanA}|$: Absolute value channel A
$|V_{chanB}|$: Absolute value channel B
This means, even if one channel signal appears phase shifted to the other channel (at worst cases inverted), the TEA0678 will ensure the normal AMS function.

Dual Dolby* B-type noise reduction circuit, automatic music search, with differential outputs and mute

TEA0678

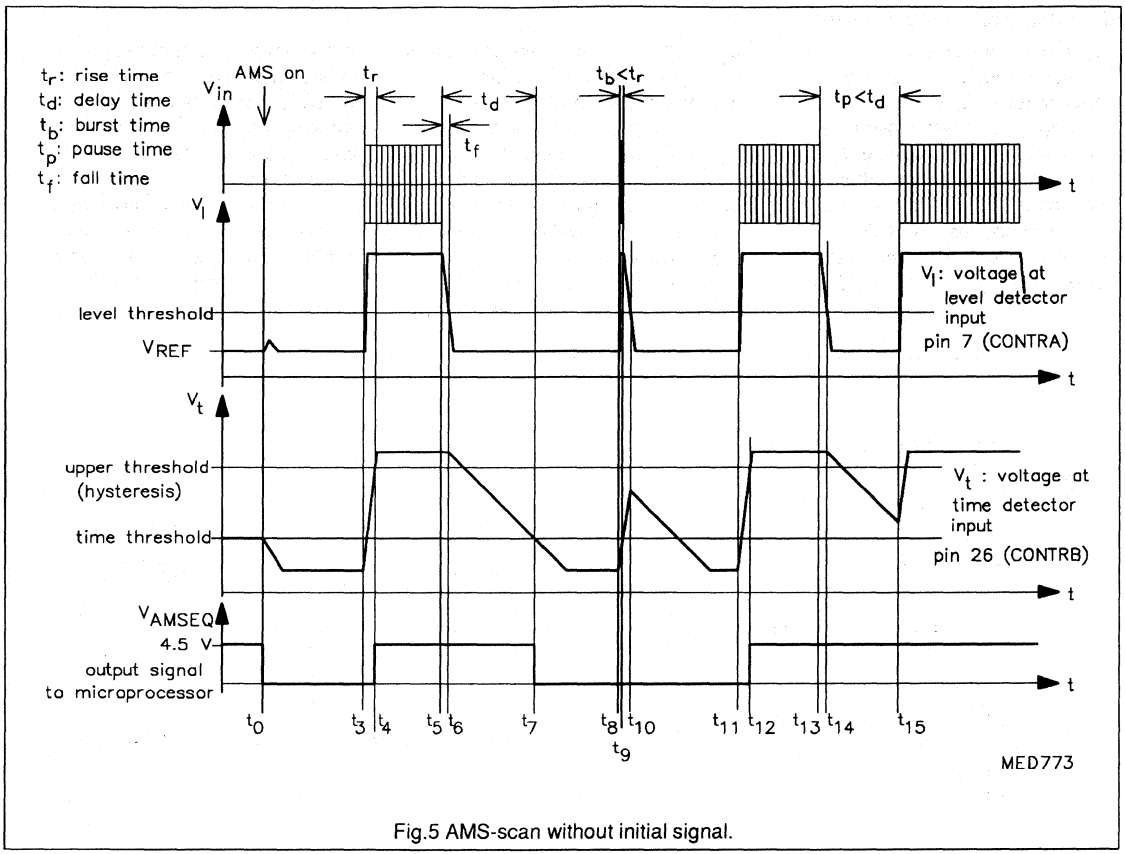


Fig.5 AMS-scan without initial signal.

Description of the principle timing diagram for AMS-scan mode without initial input signal (see Fig.5)

By activating AMS-scan mode, the AMS output level directly indicates whether the input level corresponds to a pause level (V_{AMSOUT} = LOW) or not (V_{AMSOUT} = HIGH). At t_0 the AMS-scan mode is activated.
Without a signal at V_{in}, the following initial procedure runs until the AMS output changes to LOW level:
Due to no signal at V_{in} the voltage at the level detector input V_l (pin 7 (CONTRA)) remains below the level threshold and the second time constant will be discharged (time detector input V_t). When V_t passes the time threshold level, the time detector output changes to LOW level.
Now the initial procedure is completed.
If a signal burst appears at t_3, the level detector input voltage rises immediately and causes its output to charge the second time constant, which supplies the input voltage V_t for the time detector. When V_t passes the upper threshold level after the rise time t_r (at t_4), the AMS output changes to HIGH. If the signal burst ends at t_5 the level detector input V_l falls to its LOW level. When passing the level threshold at t_6, the discharging of the second time constant begins.
Now the circuit measures the delay time t_d, which is externally fixed by a resistor and defines the length of a pause to be detected. If no signal appears at V_{in} within the time intervall t_d, the time detector output switches the AMS output to LOW level at t_7.
If a plop noise pulse appears at V_{in} (t_8) with a pulse width less than the rise time $t_r > t_b$, the plop noise will not be detected as music. The AMS output remains LOW.
Similarly the system handles 'no music pulses' t_p:
When music appears at t_{11} with a small interuption at t_{13}, this interuption will not affect the AMS output for $t_p < t_d$.

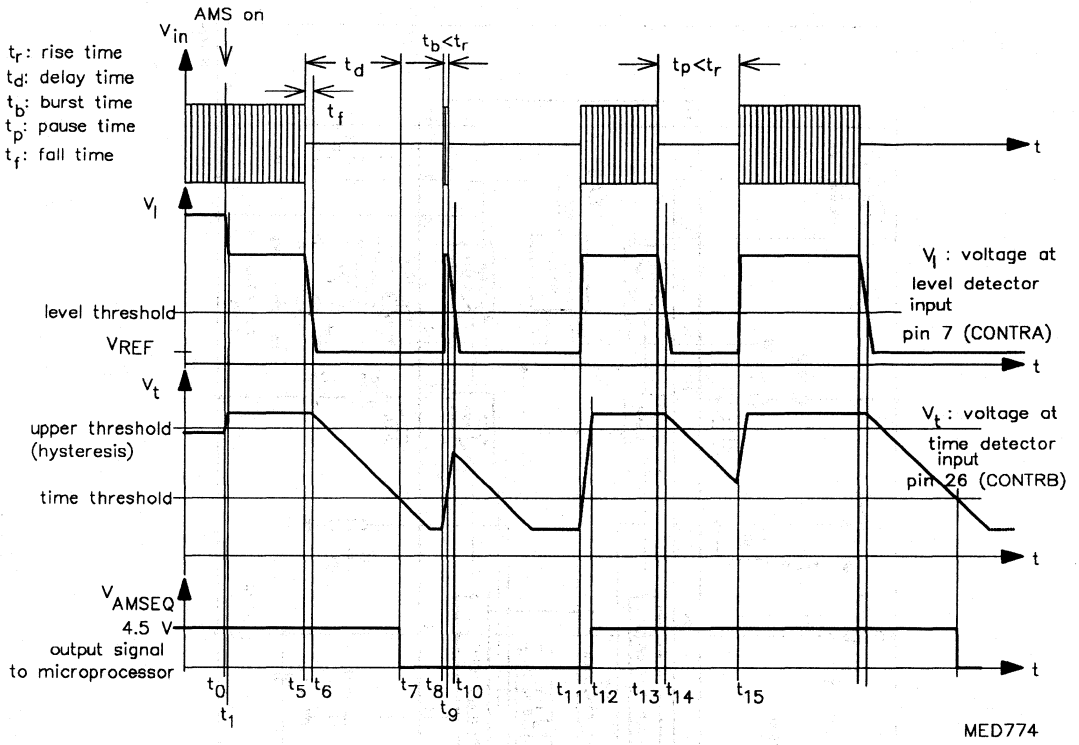


Fig.6 AMS-scan with initial signal.

Description of the principle timing diagram for AMS-scan mode with initial input signal (see Fig.6)

At t_0 the AMS-scan mode is activated.

With an input signal at V_{in}, the following initial procedure runs until the circuit gets a steady state status.

Due to the signal at V_{in} the voltage at the level detector input V_l (pin 7 (CONTRA)) slides to a value which is defined by a limiter. This voltage causes the level detector output charging the second time constant (time detector input V_t) to its maximum voltage level at t_1.

Now the initial procedure is completed.

The following behaviour does not differ from the description of the principle timing diagram for AMS-scan mode (Fig.5).

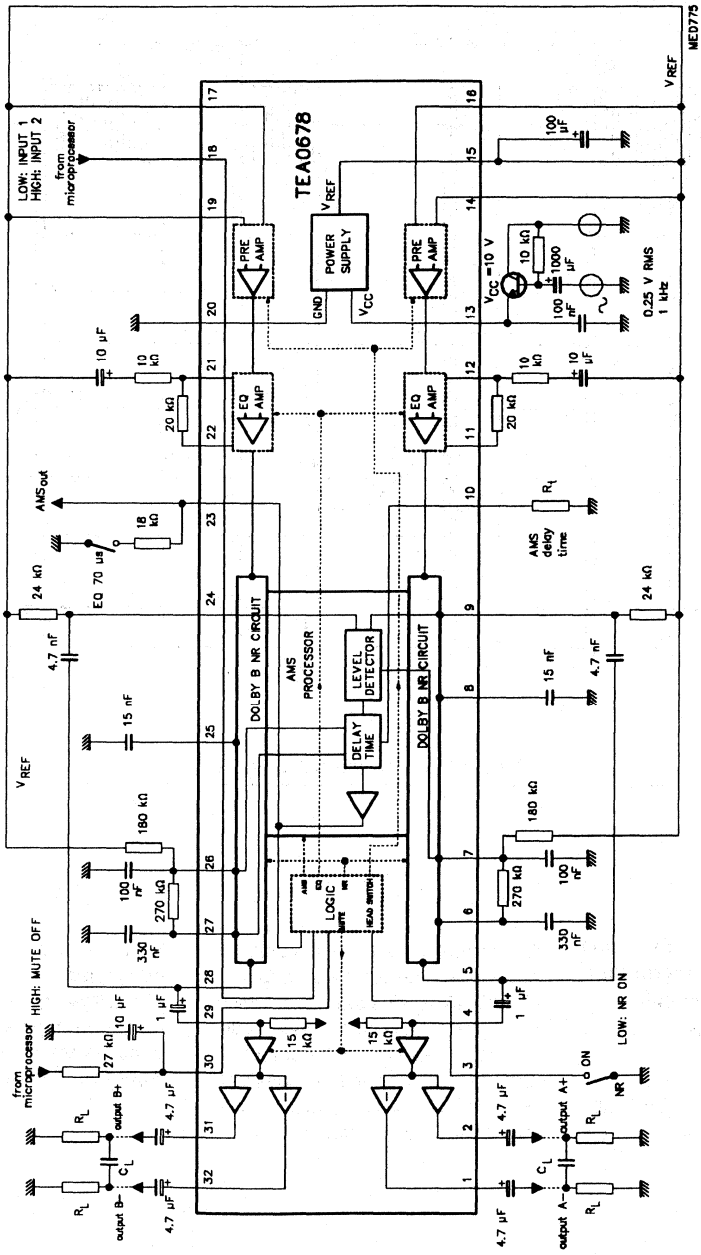


Fig.7 Test circuit for power supply ripple rejection.

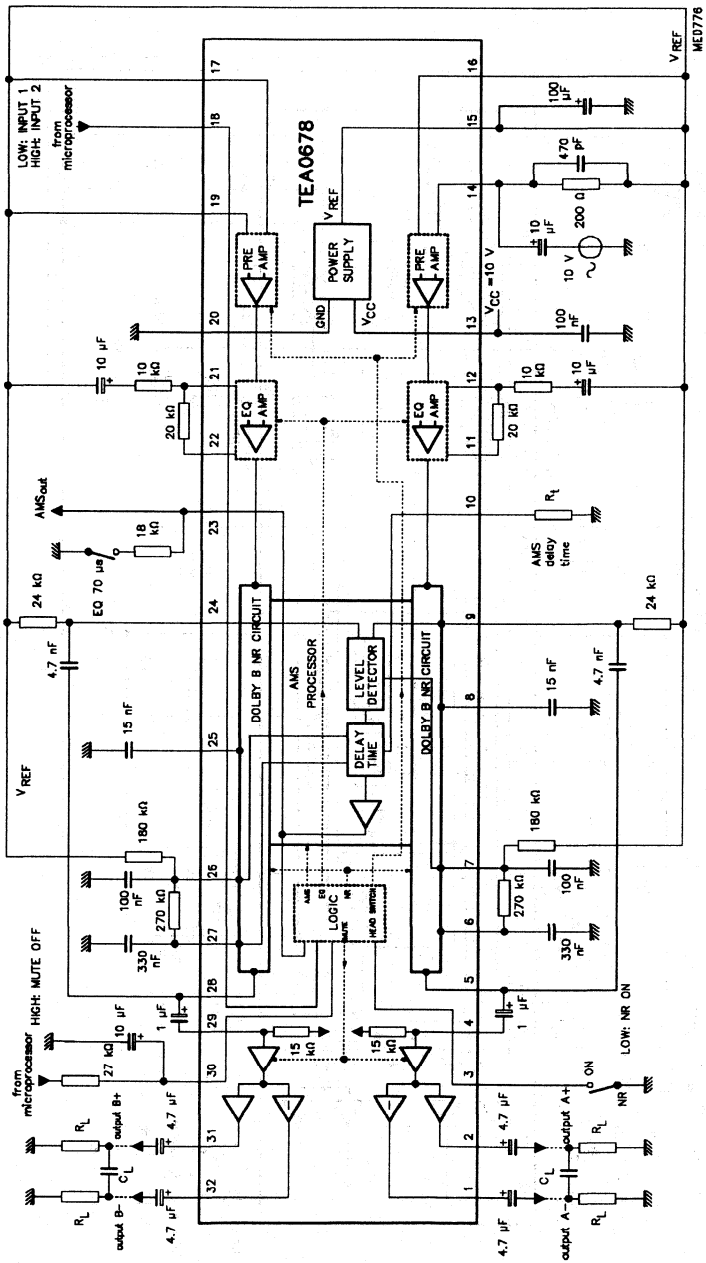


Fig.8 Test circuit for channel separation.

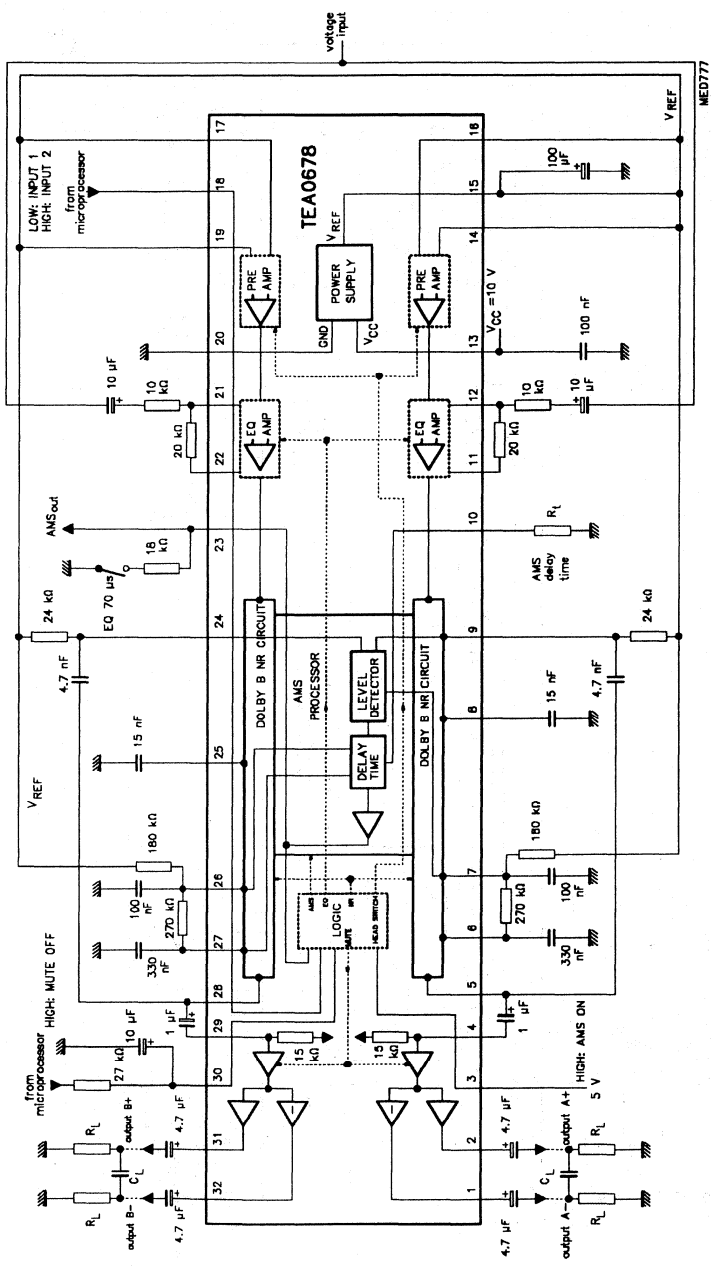


Fig.9 Test circuit for AMS threshold level.

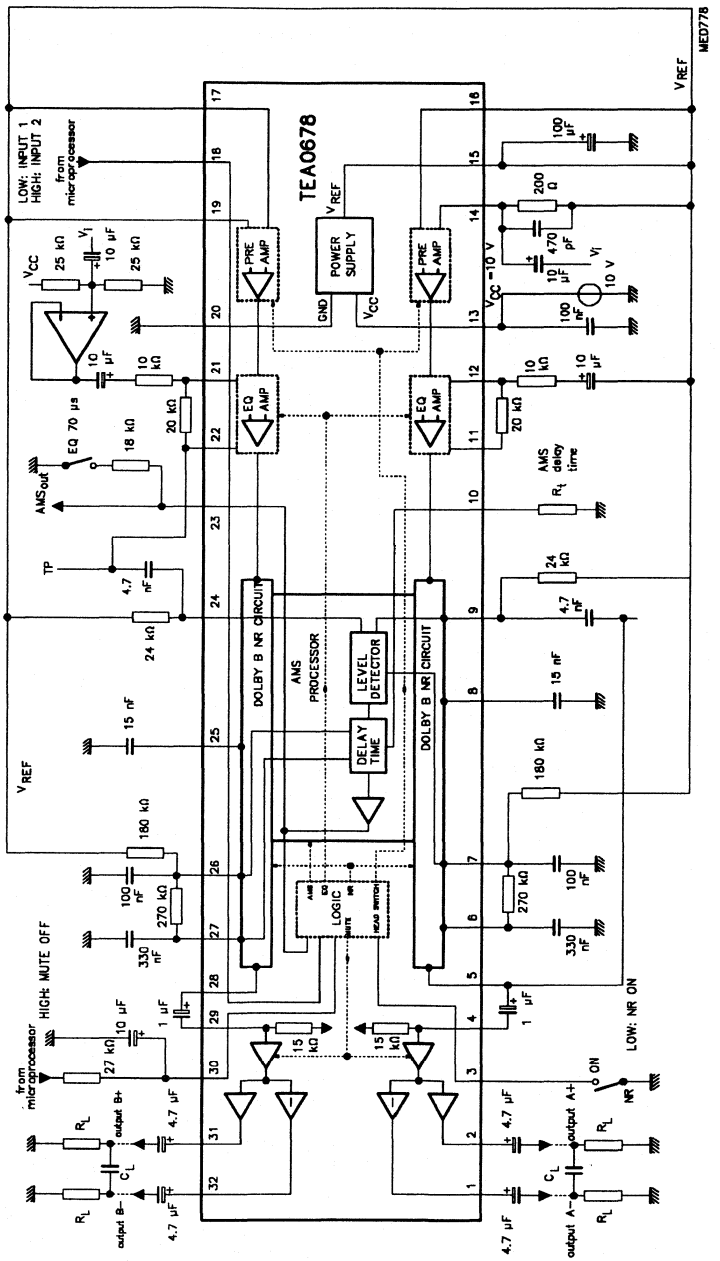


Fig.10 Test circuit for frequency response (channel B, encode mode).

1-CHIP AM RADIO

GENERAL DESCRIPTION

The TEA5551T is a 1-chip monolithic integrated radio circuit which is designed for use as a pocket receiver with headphones in a supply voltage range (V_S) of 1.8 V to 4.5 V.
The circuit consists of a complete AM part and dual AF amplifier with low quiescent current. The AF part has low radiation (HF noise) and good overdrive performance. The dual AF amplifier makes the device suitable for operation in an AM/FM stereo receiver with or without stereo cassette player.
The IC has a 1-pin switch for AM or other applications.

Features

- Low voltage operation (V_S = 1.8 V to 4.5 V)
- Low current consumption (I_{tot} = 5 mA at V_S = 3 V)
- All pins provided with ESD protection

AM part

- High sensitivity (V_i = 1.5 μV for V_o = 10 mV)
- Good IF suppression
- Good signal handling ($V_{i(max)}$ = 80 mV)
- Switch for AM or other applications
- Short waveband (> 40 MHz)

AF part

- A fixed integrated gain of 32 dB
- Few external components required
- Very low quiescent current
- Low HF radiation and good AF overdrive performance
- 0 to 20 kHz limited frequency response
- 25 mW per channel output power in 32 Ω

QUICK REFERENCE DATA (at T_{amb} = 25 °C)

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage		V_S	1.8	3.0	4.5	V
Supply current		$I_5 + I_{10}$	–	6	–	mA
AM part	m = 0.3					
RF sensitivity						
RF input voltage						
	$V_{o(AF)}$ = 10 mV	$V_{i(RF)}$	–	1.5	–	μV
	S/N = 26 dB	$V_{i(RF)}$	–	15	–	μV
	S/N = 50 dB	$V_{i(RF)}$	–	10	–	mV
AF output voltage	$V_{i(RF)}$ = 1 mV	$V_{o(AF)}$	–	80	–	mV
Total harmonic distortion	$V_{i(RF)}$ = 100 μV to 30 mV	THD	–	0.8	–	%
Signal handling capability	m = 0.8; THD = 10%	$V_{i(RF)}$	–	80	–	mV
AF part	both channels driven					
Output power	R_L = 32 Ω; THD = 10%					
at V_S = 3.0 V		P_o	–	25	–	mW
at V_S = 4.5 V		P_o	–	60	–	mW
Voltage gain	P_o = 10 mW	G_v	–	32	–	dB
Channel separation	1 kHz	α	–	50	–	dB

PACKAGE OUTLINE

16-lead mini-pack; plastic (SO16; SOT109A).

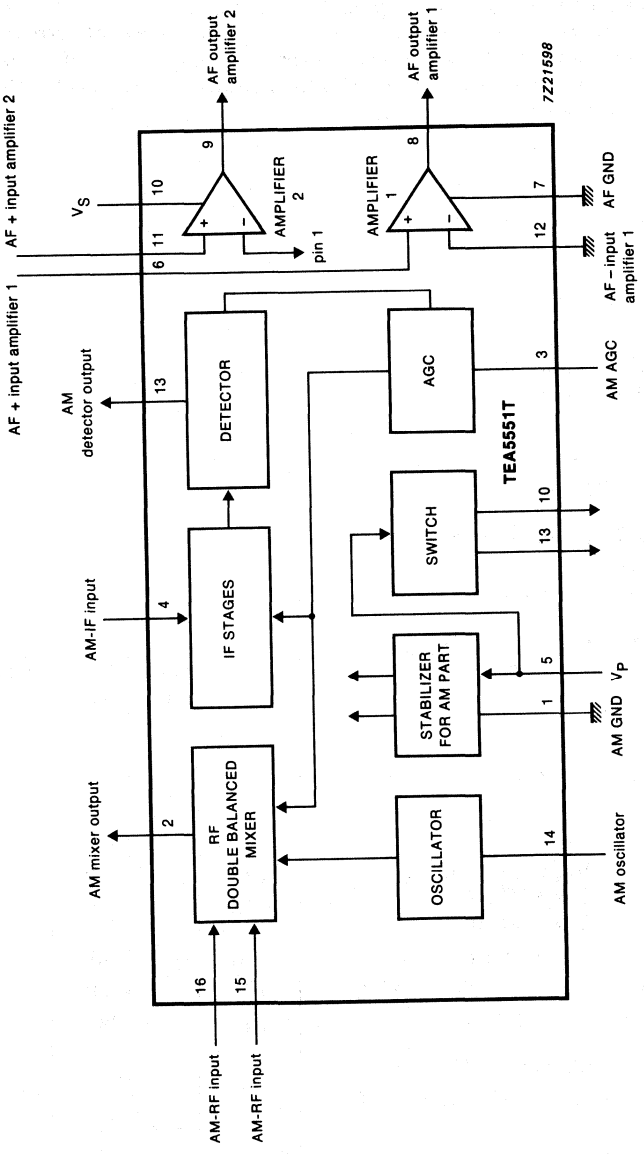


Fig. 1 Block diagram.

PINNING

1	AM GND	9	AF output amplifier 2
2	AM mixer output	10	AF supply voltage (V_S)
3	AM AGC	11	AF + input amplifier 2
4	AM–IF input	12	AF – input amplifier 1
5	AM supply voltage (Vp)	13	AM detector output
6	AF + input amplifier 1	14	AM oscillator
7	AF GND	15	AM–RF input
8	AF output amplifier 1	16	AM–RF input

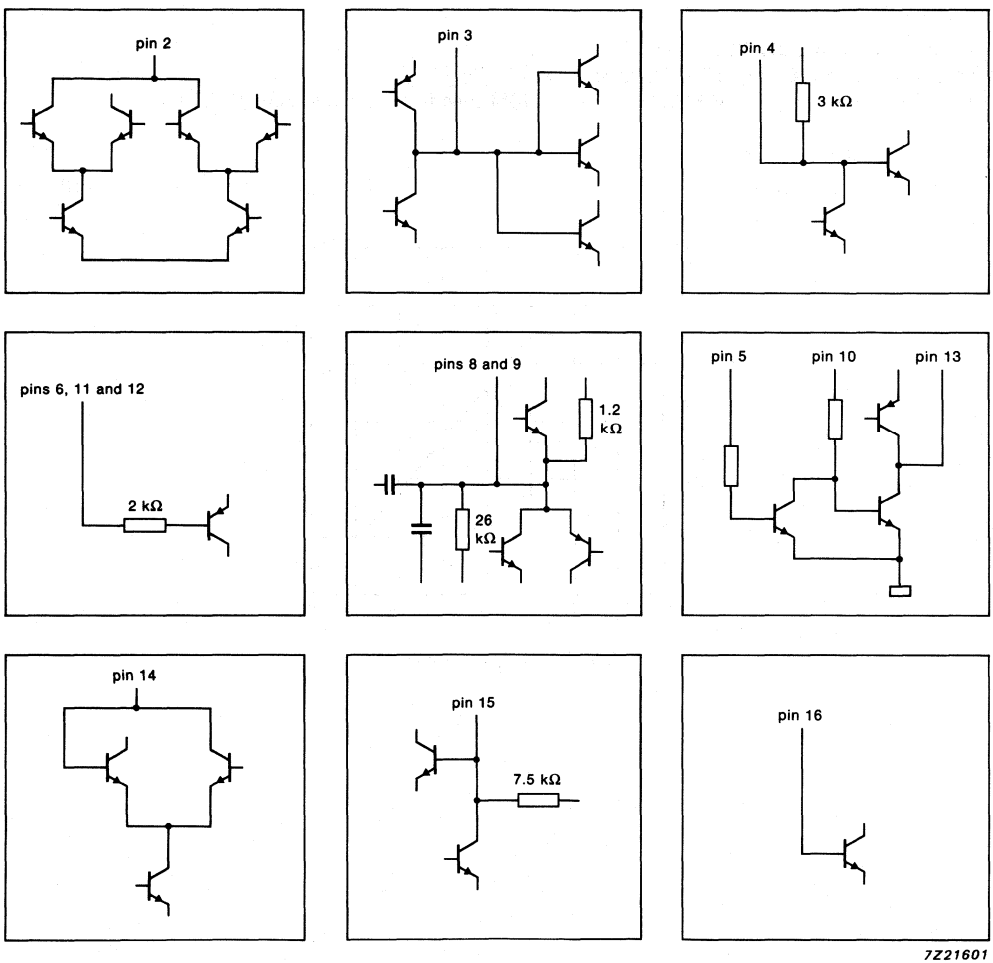


Fig. 2 All pins provided with ESD protection diodes to substrate.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage		V_S	–	6	V
Supply current (peak)		I_M	–	150	mA
Crystal temperature		T_c	–	150	°C
Short-circuit protection	V_S = 4.5 V	t_{sc}	–	5	s
Total power dissipation		P_{tot}	see Fig. 3		
Storage temperature range		T_{stg}	−65	+150	°C
Operating ambient temperature range		T_{amb}	−25	+60	°C

QUALITY

In accordance with UZW-BO/FQ-0601.
Operating life endurance verified 2000 hours at T_j = 85 °C.
The product meets the 600 V ESD on all pins (HBM specification UZW-BO/FQ-A302).

THERMAL RESISTANCE

From junction to ambient $R_{th\ j\text{-}a}$ = 110 K/W

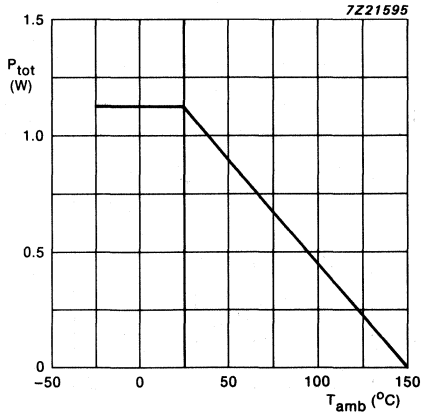


Fig. 3 Power derating curve.

DC CHARACTERISTICS

All voltages are referenced to pin 1 and pin 7; all input currents are positive; all parameters are measured in test circuit of Fig. 6 at V_S = 3 V; T_{amb} = 25 °C unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply voltage	V_S	1.8	3.0	4.5	V
Voltages					
pin 5	V_5	1.6	2.8	4.3	V
pin 10	V_{10}	1.8	3.0	4.5	V
HF part					
Total current consumption (pin 5)	I_5	–	2.2	–	mA
Oscillator current (pin 14)	I_{14}	–	100	–	μA
Mixer current (pin 2)	I_2	–	200	–	μA
Voltages					
pin 3	V_3	–	150	–	mV
pin 13	V_{13}	–	600	–	mV
pin 15	V_{15}	–	1.1	–	V
pin 16	V_{16}	–	1.1	–	V
AF part					
Total current consumption (pin 10)	I_5	–	4.0	–	mA
Input bias current (pin 11 connected to pin 16)	$I_{11} + I_{16}$	–	40	–	nA
DC output voltage					
pin 8	V_8	–	1.5	–	V
pin 9	V_9	–	1.5	–	V

AC CHARACTERISTICS

All parameters are measured in test circuit of Fig. 6 at V_S = 3 V; T_{amb} = 25 °C unless otherwise specified.
RF conditions: Input frequency 1 MHz; 30% modulation where f_{mod} = 1 kHz; unless otherwise specified.

parameter	conditions	symbol	min.	typ.	max.	unit
RF sensitivity						
RF input voltage	$V_{o(AF)}$ = 10 mV	$V_{i(RF)}$	–	1.5	–	μV
Loss in sensitivity	$V_{o(AF)}$ = 10 mV; V_S = 1.8 V	$\Delta V_{i(RF)}$	–	6	–	dB
Noise						
Signal-to-noise ratio for RF input signal voltage of						
$V_{i(RF)}$ = 2 μV		S/N	–	6	–	dB
$V_{i(RF)}$ = 15 μV		S/N	–	26	–	dB
$V_{i(RF)}$ = 1 mV		S/N	–	46	–	dB
AF output voltage						
	$V_{i(RF)}$ = 1 mV	$V_{o(AF)}$	–	80	–	mV
	$V_{i(RF)}$ = 1 mV; V_S = 1.8 V	$V_{o(AF)}$	–	55	–	mV
Total harmonic distortion						
	$V_{i(RF)}$ = 100 μV to 30 mV	THD	–	0.8	–	%
	$V_{i(RF)}$ = 80 mV; m = 0.8	THD	–	10	–	%
AGC range						
Change in RF input voltage for 10 dB change in AF output voltage	$V_{i(RF1)}$ = 50 mV	$V_{i(RF1)}$/ $V_{i(RF2)}$	–	86	–	dB
Optimum source impedance		Z_{source}	–	3	–	kΩ
IF suppression						
at $V_{o(AF)}$ = 10 mV	note 1	α	–	20	–	dB
Oscillator (pin 14)	f_{osc} = 1468 kHz					
Oscillator voltage		V_i	–	100	–	mV
	V_5 = 1.5 V	V_i	–	*	–	mV

Note to the AC characteristics

1. $\alpha = \frac{V_i \text{ at } f_i = 468 \text{ kHz}}{V_i \text{ at } f_i = 1 \text{ MHz}}$

* Value to be fixed.

AC CHARACTERISTICS

All parameters are measured in test circuit of Fig. 6 at V_S = 3 V; T_{amb} = 25 °C unless otherwise specified

AF conditions: f = 1 kHz; R_L = 32 Ω; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Output power						
	THD = 10%	P_o	–	25	–	mW
	THD = 10%; V_S = 1.8 V	P_o	–	8	–	mW
	THD = 10%; V_S = 4.5 V	P_o	–	60	–	mW
Total harmonic distortion	P_o = 10 mW	THD	–	0.5	–	%
Voltage gain	P_o = 10 mW	G_v	–	32	–	dB
Noise						
Noise output voltage	R_S = 5 kΩ; B = 15 kHz	V_{no}	–	240	–	μV
HF noise output voltage	R_S = 5 kΩ; B = 5 kHz; f = 500 kHz	$V_{no(RF)}$	–	20	–	μV
Input circuit						
Input impedance	pin 11 connected to pin 12	Z_i	–	3	–	MΩ
Mute switch						
AC impedance (pin 13 to ground)	V_5 = 0 V; I_{13} = 0.32 mA	R_S	–	200	–	Ω

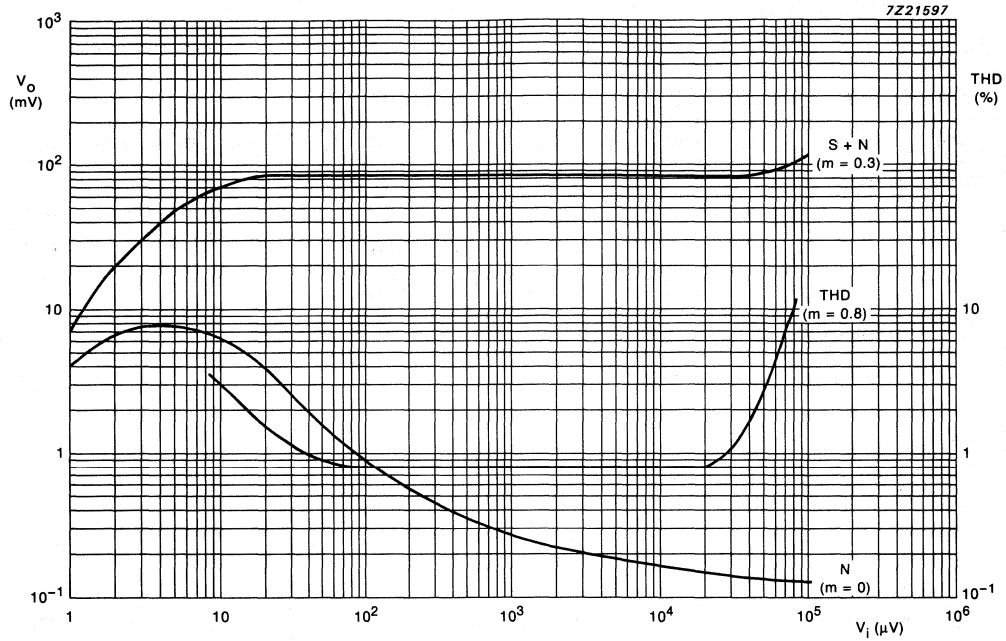


Fig. 4 Typical signal (S) and noise (N) output voltages, where V_o is the AF output voltage at pin 13, as a function of the input voltage V_i. V_i is the input voltage at pin 16. Also shown is the total harmonic distortion (THD).
Conditions: f_o = 1 MHz; f_m = 1 kHz; V_S = 3 V; R_g = 50 Ω; m = 0.3 (unless otherwise specified).

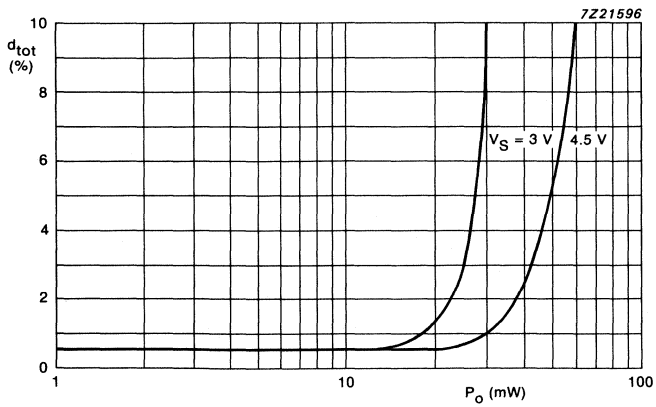


Fig. 5 Total distortion (d_{tot}) as a function of output power (P_o).
Conditions: V_S = 3 V and 4.5 V; R_L = 32 Ω; f = 1 kHz.

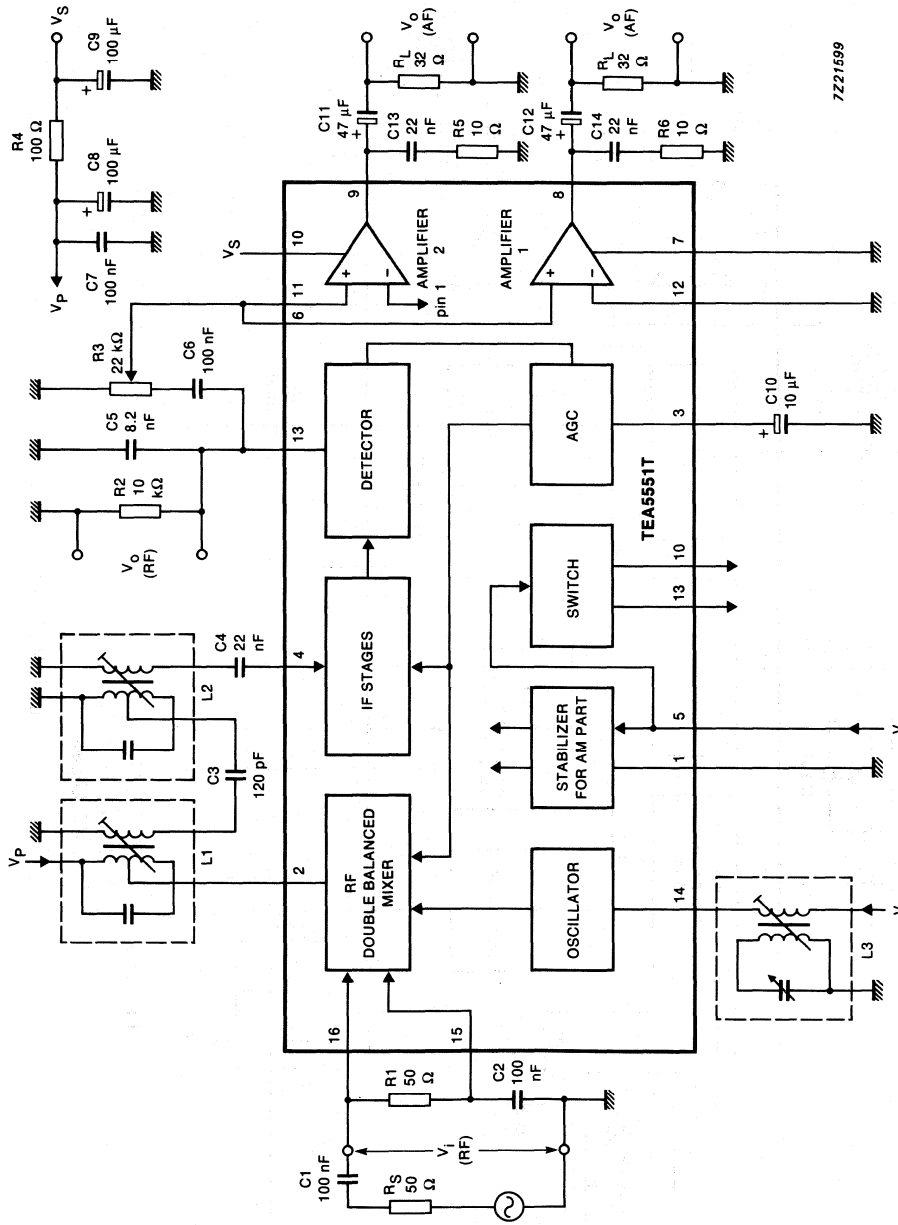


Fig. 6 Test circuit.

APPLICATION INFORMATION

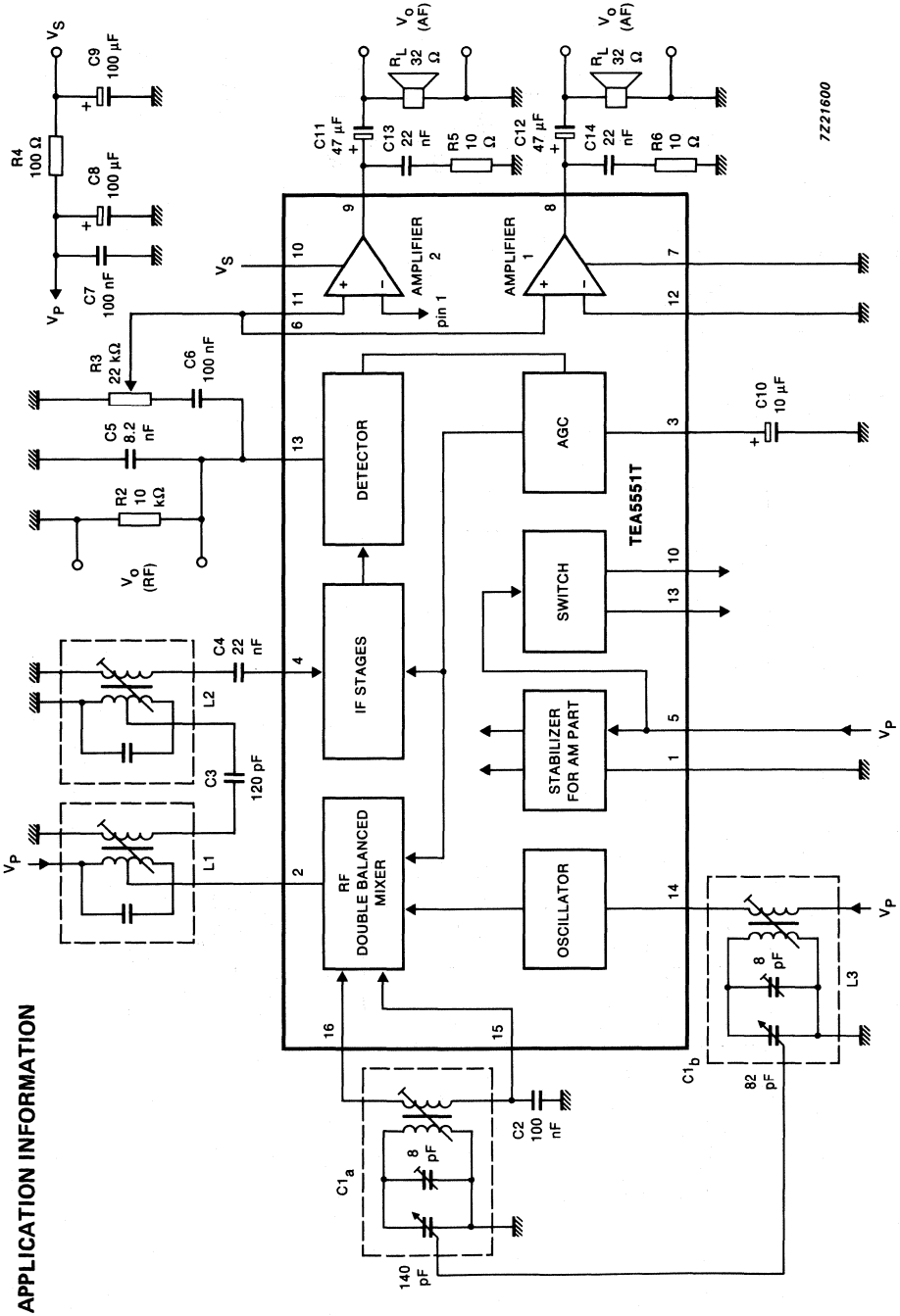
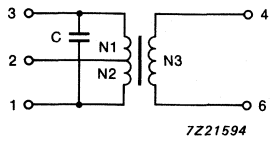


Fig. 7 Application circuit.

Coil data: L1 7MCS2199
L2 7MCS2197
L3 7BRS10869X

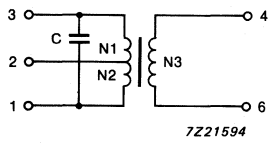
COIL DATA

AM coils (Figs 6 and 7)



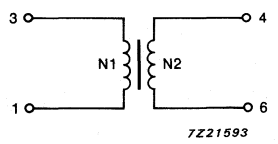
N1 = 60
N2 = 80
N3 = 15
C = 180 pF (internal)
L1–L3 = 643 μH
Qo = 110
Wire = 0.07 mm dia.
Coil type 7P–TOKO
Material 7MC

Fig. 8 IF bandpass filter (L1). TOKO sample no. 7MCS2199.



N1 = 125
N2 = 15
N3 = 6
C = 180 pF (internal)
L1–L3 = 643 μH
Qo = 110
Wire = 0.07 mm dia.
Coil type 7P–TOKO
Material 7MC

Fig. 9 IF bandpass filter (L2). TOKO sample no. 7MCS2197.



N1 = 90
N2 = 6
L1–L3 = 295 μH
Qo = 110
Wire = 0.07 mm dia.
Coil type 7P–TOKO
Material 7BR

Fig. 10 Oscillator coil (L3). TOKO sample no. 7BRS10869X.

RF/IF CIRCUIT FOR AM/FM RADIO

GENERAL DESCRIPTION

The TEA5570 is a monolithic integrated radio circuit for use in portable receivers and clock radios. The IC is also applicable to mains-fed AM and AM/FM receivers and car radio-receivers. Apart from the AM/FM switch function the IC incorporates for AM a double balanced mixer, 'one-pin' oscillator, i.f. amplifier with a.g.c. and detector, and a level detector for tuning indication. The FM circuitry comprises i.f. stages with a symmetrical limiter for a ratio detector. A level detector for mono/stereo switch information and/or indication complete the FM part.

Features

- Simple d.c. switching for AM to FM by only one d.c. contact to ground (no switch contacts in the i.f. channel, a.f. or level detector outputs)
- AM and FM gain control
- Low current consumption (I_{tot} = 6 mA)
- Low voltage operation (V_P = 2,7 to 9 V)
- Ability to handle large AM signals; good i.f. suppression
- Applicable for inductive, capacitive and diode tuning
- Double smoothing of a.g.c. line
- Short-wave range up to 30 MHz
- Lumped or distributed i.f. selectivity with coil and/or ceramic filters
- AM and a.g.c. output voltage control
- Distribution of PCB wiring provides good frequency stability
- Economic design for 'AM only' receivers

QUICK REFERENCE DATA (at T_{amb} = 25 °C)

Supply voltage	$V_P = V_{7-16}$	typ.	5,4 V
Supply current	I_7	typ.	6,2 mA
AM performance (pin 2) for m = 0,3			
Sensitivity			
at V_o = 10 mV	V_i	typ.	1,7 μV
at S/N = 26 dB	V_i	typ.	16 μV
A.F. output voltage at V_i = 1 mV	V_o	typ.	100 mV
Total harmonic distortion at V_i = 1 mV	THD	typ.	0,5 %
FM performance (pin 1) for Δf = ± 22,5 kHz			
limiting sensitivity, −3 dB	V_i	typ.	110 μV
Signal-to-noise ratio for V_i = 1 mV	S/N	typ.	65 dB
A.F. output voltage at V_i = 1 mV	V_o	typ.	100 mV
Total harmonic distortion at V_i = 1 mV	THD	typ.	0,3 %
AM suppression at V_i = 10 mV	AMS	typ.	50 dB

PACKAGE OUTLINE

16-lead DIL; plastic (SOT38).

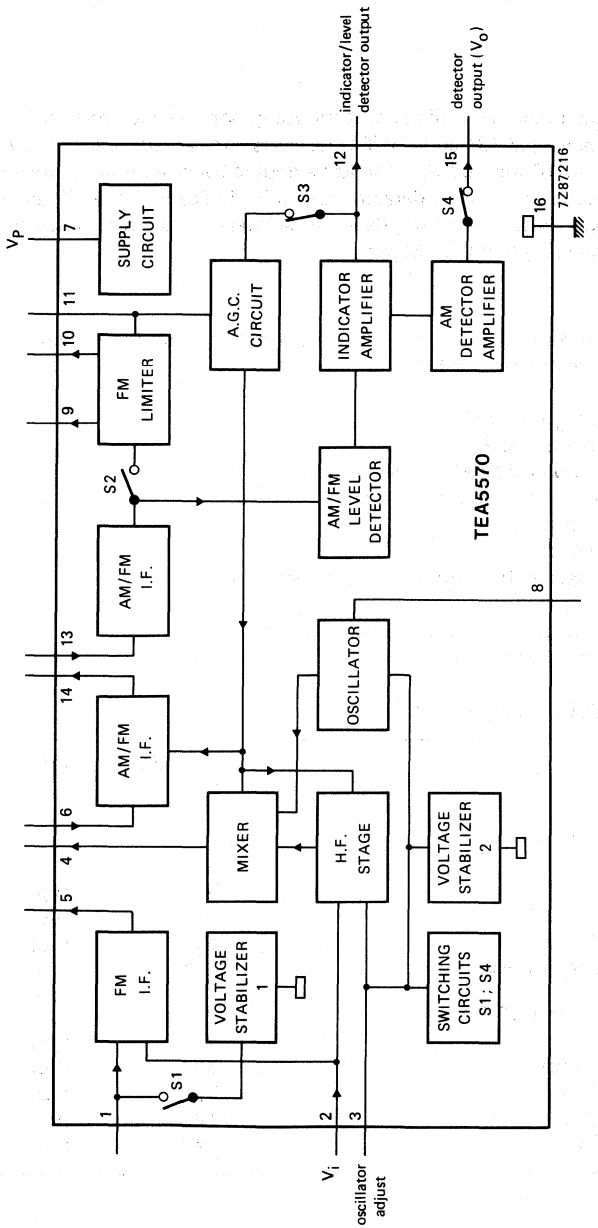


Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 7)	$V_P = V_{7-16}$	max.	12 V
Voltage at pins 4, 5, 9 and 10 to pin 16 (ground)	V_{n-16}	max.	12 V
Voltage range at pin 8	V_{8-16}		$V_P \pm 0{,}5$ V
Current into pin 5	I_5	max.	3 mA
Total power dissipation	P_{tot}	see Fig. 2	W
Storage temperature range	T_{stg}		−55 to +150 °C
Operating ambient temperature range	T_{amb}		−30 to +85 °C

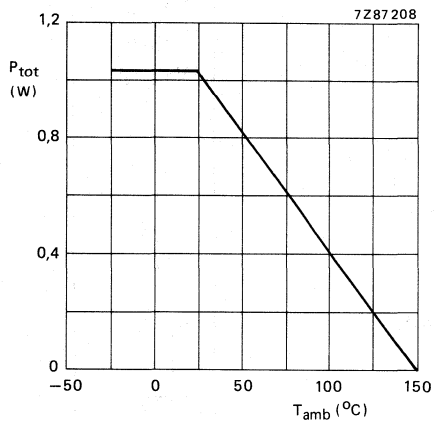


Fig. 2 Power derating curve.

D.C. CHARACTERISTICS

V_P = 6 V; T_{amb} = 25 °C; measured in Fig. 10; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply (pin 7)					
Supply voltage (note 1)	$V_P = V_{7-16}$	2,4	5,4	9,0	V
Voltages					
at pin 1 (FM)	V_{1-16}	–	1,42	–	V
at pin 1; $-I_1$ = 50 μA (FM)	V_{1-16}	–	1,28	–	V
at pins 2 and 3 (AM)	$V_{2,3-16}$	–	1,42	–	V
at pin 6	V_{6-16}	–	0,7	–	V
at pin 11	V_{11-16}	–	1,4	–	V
at pin 13	V_{13-16}	–	0,7	–	V
at pin 14	V_{14-16}	–	4,3	–	V
Currents					
Supply current	I_7	4,2	6,2	8,2	mA
Current supplied from pin 1 (FM)	$-I_1$	–	–	50	μA
Current supplied from pin 12	$-I_{12}$	–	–	20	μA
Current supplied from pin 15	$-I_{15}$	–	30	–	μA
Current into pin 4 (AM)	I_4	–	0,6	–	mA
Current into pin 5 (FM) (note 4)	I_5	–	0,35	–	mA
Current into pin 8 (AM)	I_8	–	0,3	–	mA
Current into pins 9, 10 (FM)	$I_{9,10}$	–	0,65	–	mA
Current into pin 14	I_{14}	–	0,4	–	mA
Power consumption	P	–	40	–	mW

A.C. CHARACTERISTICS

AM performance

V_P = 6 V; T_{amb} = 25 °C; r.f. condition: f_i = 1 MHz, m = 0,3, f_m = 1 kHz; transfer impedance of the i.f. filter $|Z_{tr}| = v_6/I_4$ = 2,7 kΩ; measured in Fig. 10; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
R.F. sensitivity (pin 2)					
at V_o = 30 mV	V_i	3,5	5,0	7,0	μV
at S + N/N = 6 dB	V_i	–	1,3		μV
at S + N/N = 26 dB	V_i	–	16	20	μV
at S + N/N = 50 dB	V_i	–	1	–	mV
Signal handling (THD ⩽ 10% at m = 0,8)	V_i	200	–	–	mV
A.F. output voltage at V_i = 1 mV	V_o	80	100	125	mV
Total harmonic distortion					
at V_i = 100 μV to 100 mV (m = 0,3)	THD	–	0,5	–	%
at V_i = 2 mV (m = 0,8)	THD	–	1,0	2,5	%
at V_i = 200 mV (m = 0,8)	THD	–	4,0	10	%
I.F. suppression at V_o = 30 mV (note 2)	α	26	35	–	dB
Oscillator voltage (pin 8; note 3)					
at f_{osc} = 1455 kHz	$V_{8\text{-}16}$	120	160	200	mV
Indicator current (pin 12) at V_i = 1 mV	I_{12}	–	200	230	μA

FM performance

V_P = 6 V; T_{amb} = 25 °C; i.f. condition: f_i = 10,7 MHz, Δf = ± 22,5 kHz, f_m = 1 kHz; transfer impedance of the i.f. filter $|Z_{tr}| = v_6/i_5$ = 275 Ω; measured in Fig. 10; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
I.F. part					
I.F. sensitivity (adjustable; note 4)					
Input voltage					
at −3 dB before limiting	V_i	90	110	130	μV
at S + N/N = 26 dB	V_i	–	6	–	μV
at S + N/N = 65 dB	V_i	–	1	–	mV
A.F. output voltage at V_i = 1 mV	V_o	80	100	125	mV
Total harmonic distortion at V_i = 1 mV	THD	–	0,3	–	%
AM suppression (note 5)	AMS	–	50	–	dB
Indicator/level detector (pin 12)					
Indicator current	I_{12}	–	250	325	μA
D.C. output voltage					
at V_i = 300 μV	$V_{12\text{-}16}$	–	0,25	–	V
at V_i = 2 mV	$V_{12\text{-}16}$	–	1,0	–	V
AM to FM switch					
Switching current at $V_{3\text{-}16} < 1$ V	$-I_3$	–	–	400	μA

Notes to characteristics

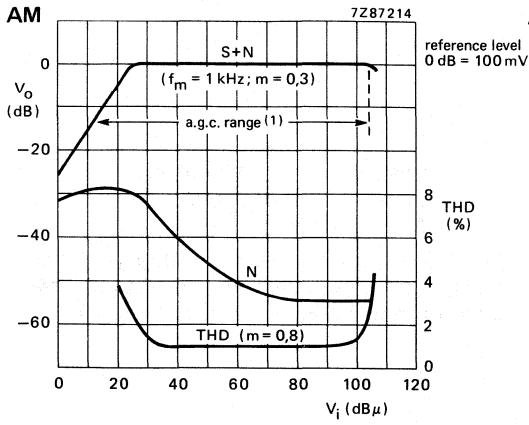
1. Oscillator operates at $V_{7\text{-}16} > 2{,}25$ V.
2. I.F. suppression is defined as the ratio $\alpha = 20 \log \frac{V_{i1}}{V_{i2}}$ where: V_{i1} is the input voltage at f = 455 kHz and V_{i2} is the input voltage at f = 1 MHz.
3. Oscillator voltage at pin 8 can be preset by R_{osc} (see Fig. 10).
4. Maximum current into pin 5 can be adjusted by R1 (see Fig. 10);
   $I_5 = \frac{V_{3\text{-}16}}{R1} - I_3$ when $V_{3\text{-}16} = 800$ mV; $I_3 = 400\ \mu$A.
5. AM suppression is measured with $f_m = 1$ kHz, m = 0,3 for AM; $f_m = 400$ Hz, $\Delta f = \pm 22{,}5$ kHz for FM.

Facility adaptation

Facility adaptation is achieved as follows (see Fig. 10):

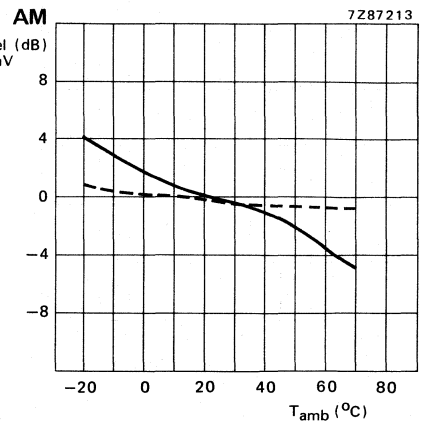
Facility	Component
FM sensitivity	R1 fixes the current at pin 5 ($I_5 = \frac{V_{3\text{-}16}}{R1} - 400\ \mu$A) (gain adjustable ± 10 dB; see note 4)
AM sensitivity	R11 and coil tapping
AM oscillator biasing	R_{osc}
AM output voltage	R7, R11
AM a.g.c. setting	R7

Typical graphs



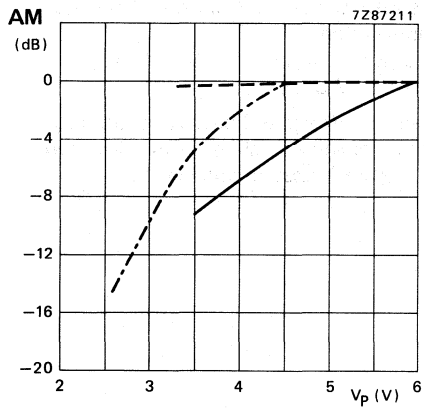
(1) A.G.C. range (figure of merit, FOM).

Fig. 3 Signal, noise and distortion as a function of input voltage (V_i). Measured at f_i = 1 MHz in test circuit Fig. 10.



——— sensitivity (V_i) at V_o = 30 mV; m = 0,3.
– – – – output voltage (V_o) at V_i = 2 mV; m = 0,3.

Fig. 4 Sensitivity (V_i), output voltage (V_o) as a function of temperature behaviour (T_{amb}). Measured at f_i = 1 MHz in test circuit Fig. 10.



——— sensitivity (V_i) at V_o = 30 V; m = 0,3: 6,0 V application.
—·—·— sensitivity (V_i) at V_o = 30 mV; m = 0,3: 4,5 V application.
– – – – output voltage (V_o) at V_i = 0,2 mV; m = 0,3.

Fig. 5 Sensitivity (V_i) and output voltage (V_o) as a function of supply voltage (V_P). Measured at f_i = 1 MHz in test circuit Fig. 10, for application V_P = 6 V. Also shown is the sensitivity for V_P = 4,5 V application (Fig. 16).

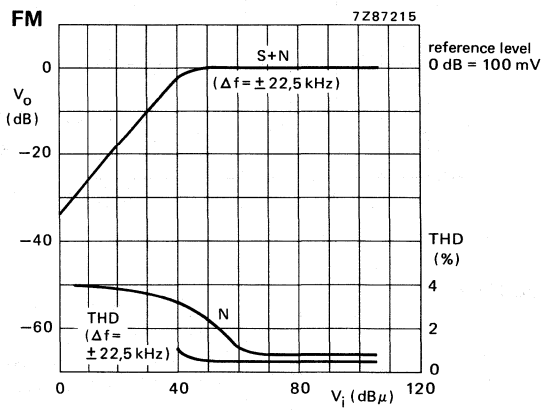
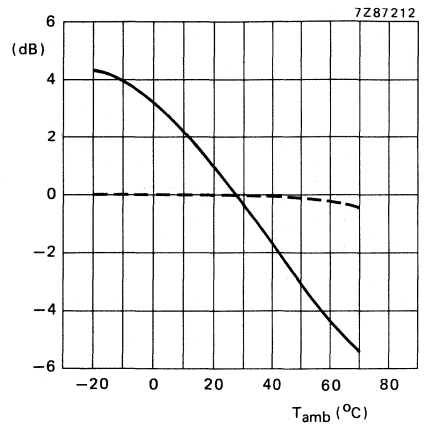


Fig. 6 Signal, noise and distortion as a function of input voltage (V_i). Measured at f_i = 10,7 MHz in test circuit Fig. 10.

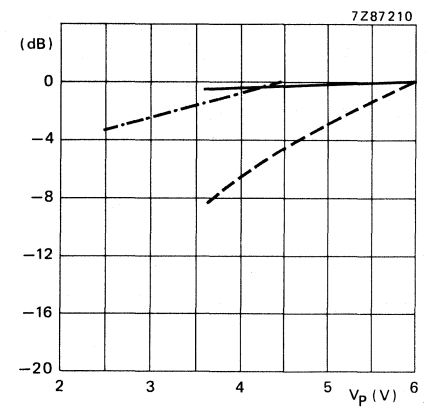
FM



——— sensitivity at −3 dB limiting.
– – – – output voltage (V_o) at V_i = 1 mV; $\Delta f = \pm 22$ kHz.

Fig. 7 Sensitivity (V_i), output voltage (V_o) as a function of temperature behaviour (T_{amb}). Measured at f_i = 10,7 MHz in test circuit Fig. 10.

FM



——— sensitivity at −3 dB limiting: V_P = 6,0 V application.
—·—·— sensitivity at −3 dB limiting: V_P = 4,5 V application.
– – – – output voltage (V_o) at V_i = 1 mV; $\Delta f = \pm 22{,}5$ kHz.

Fig. 8 Sensitivity (V_i) and output voltage (V_o) as a function of supply voltage (V_P). Measured at f_i = 10,7 MHz in test circuit Fig. 10.

AM/FM

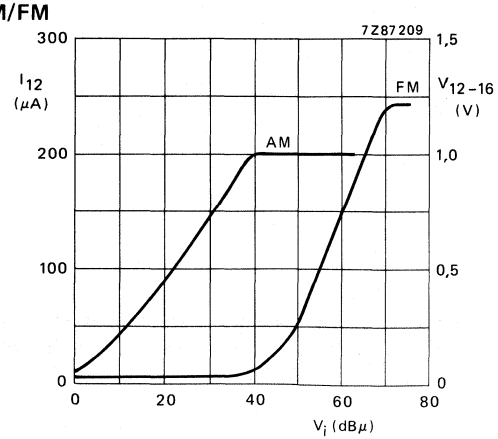


Fig. 9 Indicator output current (I_{12}) and d.c. output voltage ($V_{12\text{-}16}$): AM f_i = 1 MHz; FM f_i = 10,7 MHz as a function of input voltage (V_i). Measured in Fig. 10; V_P = 6 V; $R_{12\text{-}16}$ = 5 kΩ.

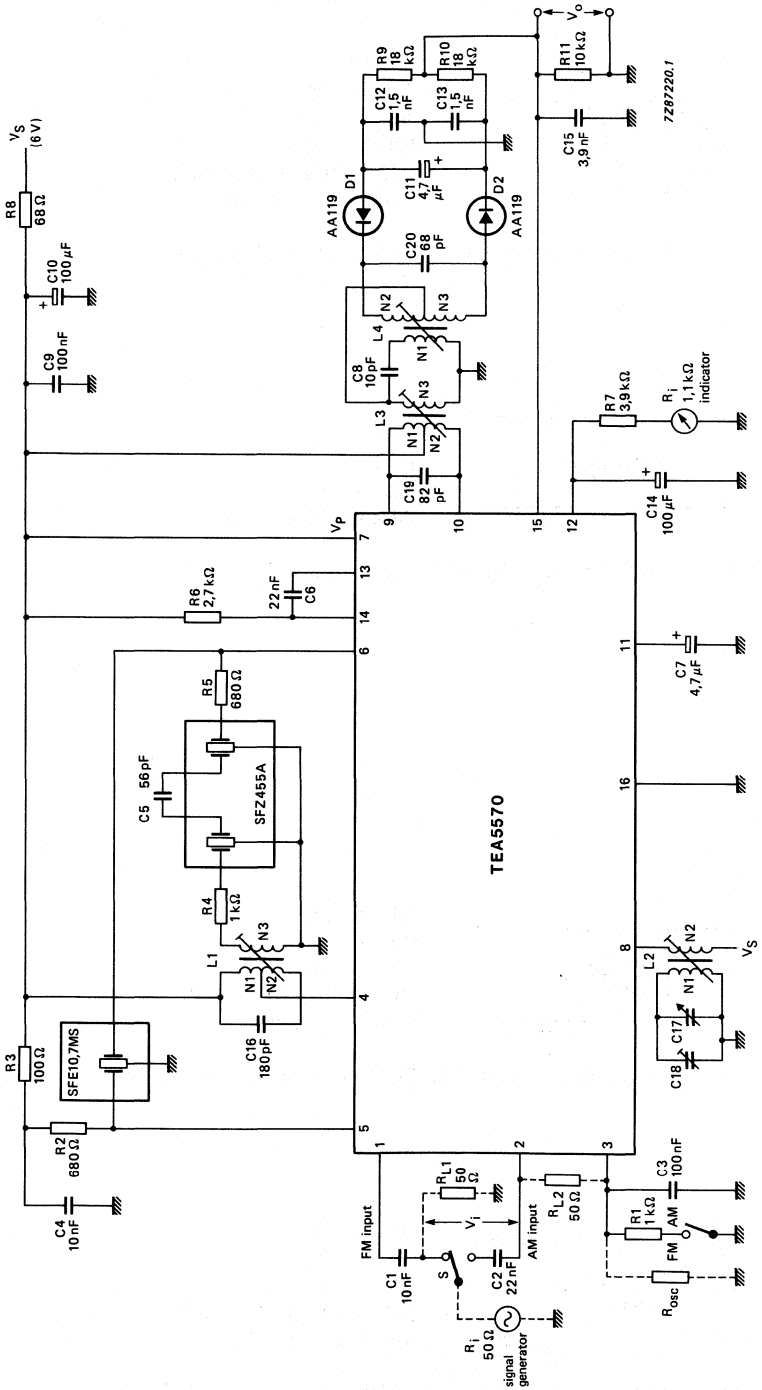


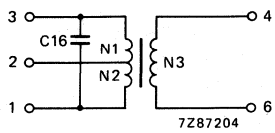
Fig. 10 Test circuit.

Coil data

The transfer impedance of the i.f. filter is:
AM: $|Z_{tr}| = v_6/i_4 = 2{,}7$ kΩ (SFZ 455A).
FM: $|Z_{tr}| = v_6/i_5 = 275$ Ω (SFE 10,7 MS).
See also Figs 11, 12, 13 and 14.

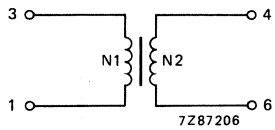
COIL DATA

AM i.f. coils (Fig. 10)



N1 = 73
N2 = 73
N3 = 9
C16 = 180 pF (internal)
Wire = 0,07 mm dia.

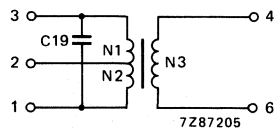
Fig. 11 I.F. bandpass filter (L1). TOKO sample no. 7 MC-7 P.



N1 = 90
N2 = 7
Wire = 0,07 mm dia.

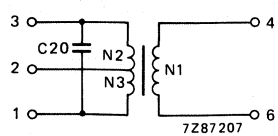
Fig. 12 Oscillator coil (L2). TOKO sample no. 7 BR-7 P.

FM i.f. coils (Fig. 10)



N1 = 5
N2 = 5
N3 = 4
C19 = 82 pF (internal)
Wire = 0,1 mm dia.

Fig. 13 Primary ratio detector coil (L3). TOKO sample no. 119 AN-7 P.

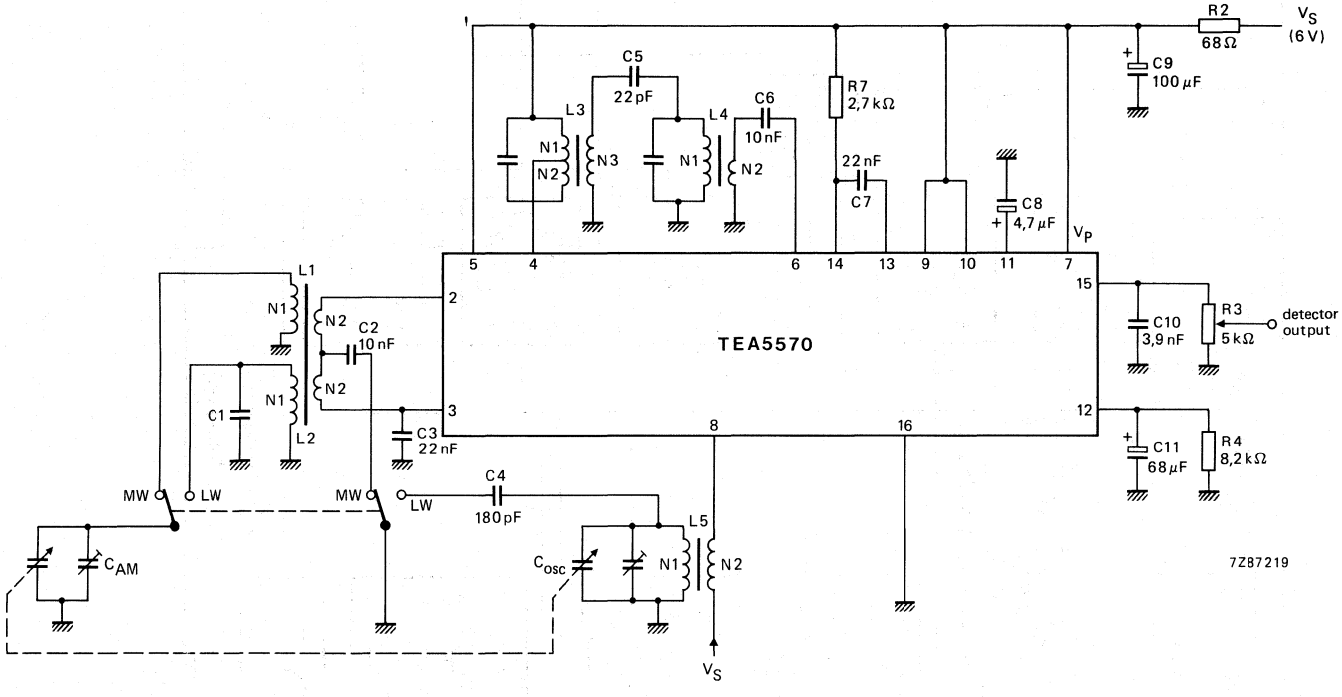


N1 = 2
N2 = 6
N3 = 6
C20 = 68 pF (internal)
Wire = 0,1 mm dia.

Fig. 14 Secondary ratio detector coil (L4). TOKO sample no. 119 AN-7 P.

APPLICATION INFORMATION

Figs 15 and 17 show the circuit diagrams for the application of 6 V AM MW/LW and 4,5 V AM/FM channels respectively, using the TEA5570. Fig. 16 shows the circuitry of the TEA5570.



Coil data

L3	N1 = 73	L4 N1 = 146	L5 N1 = 90
	N2 = 73	N2 = 9	N2 = 6
	N3 = 9	C = 180 pF	
	C = 180 pF		

Fig. 15 Typical application circuit for 6 V AM MW/LW reception using the TEA5570.

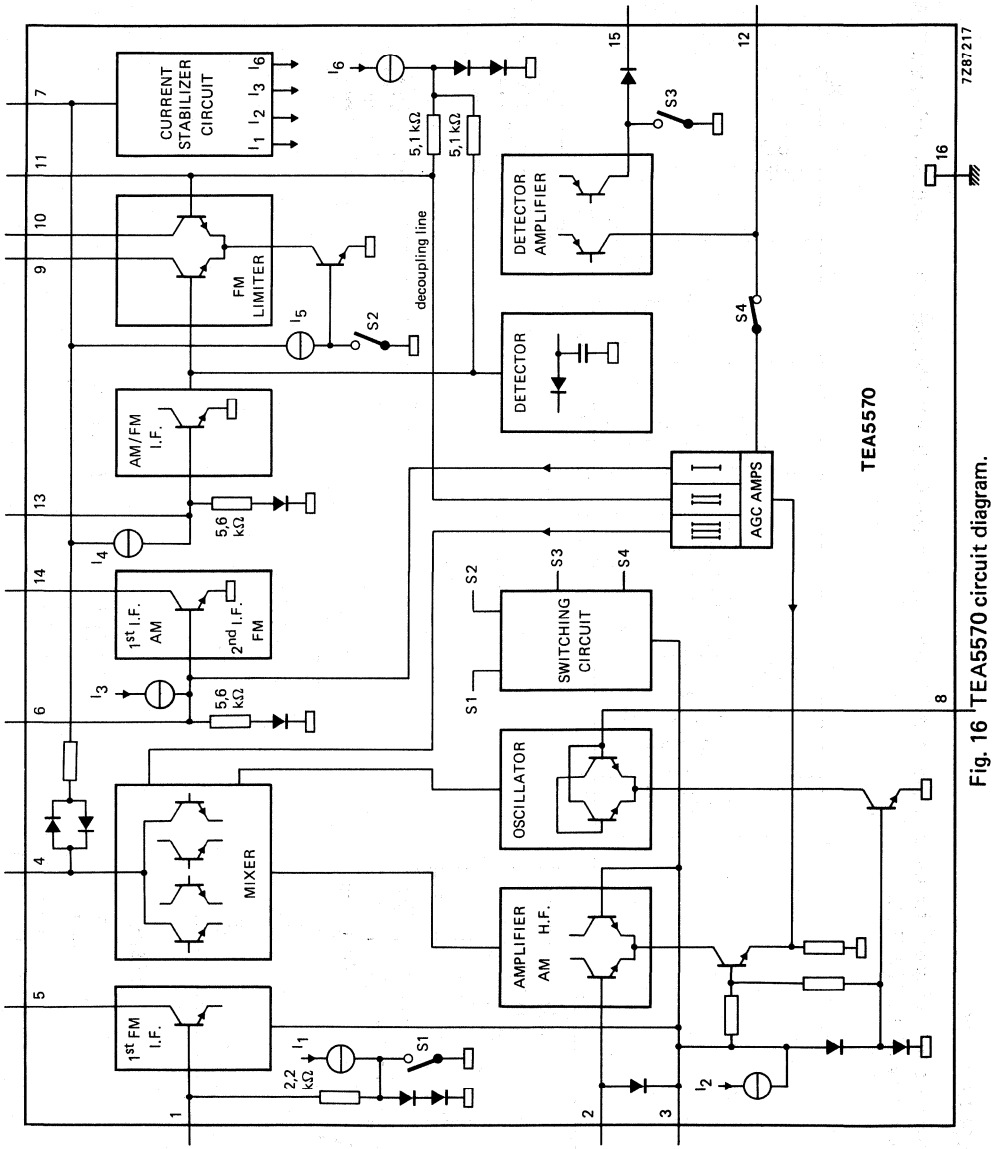


Fig. 16 TEA5570 circuit diagram.

APPLICATION INFORMATION (continued)

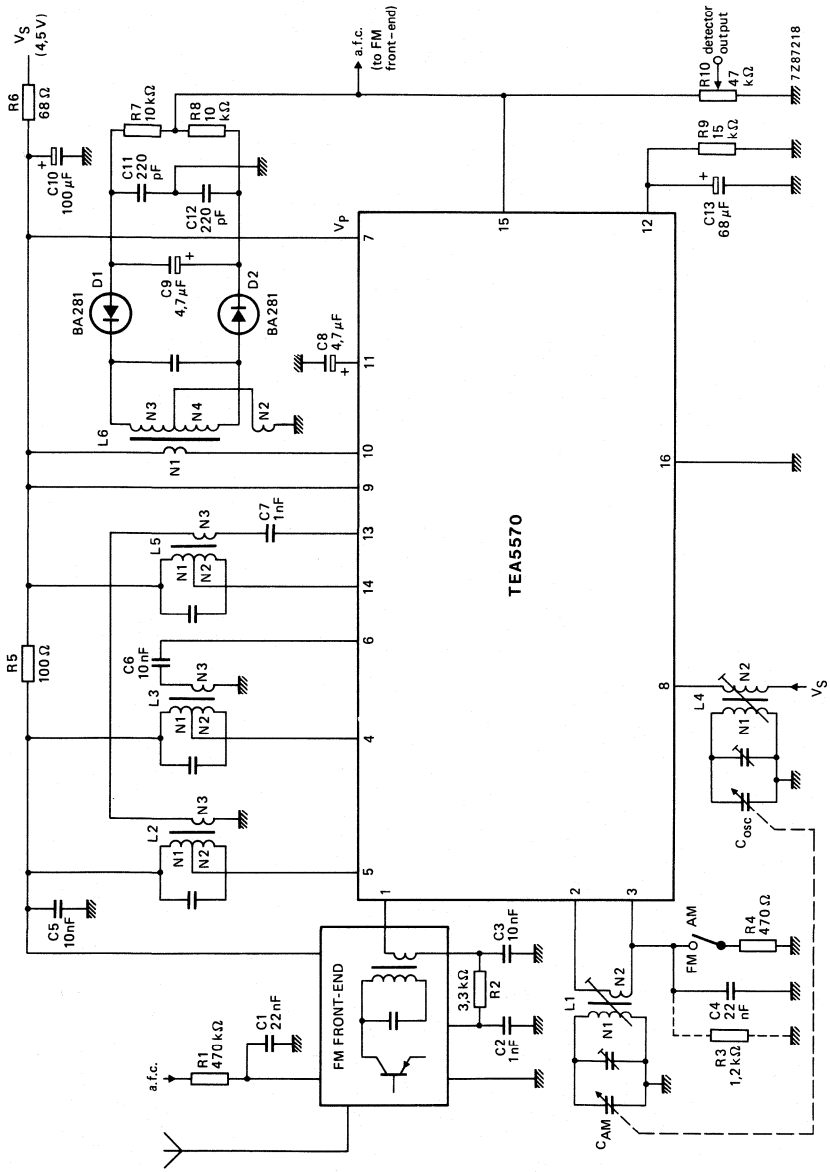


Fig. 17 Typical application circuit for 4,5 V AM/FM reception using the TEA5570 with coils and single-tuned ratio detector (with silicon diodes).

DETAILED APPLICATION INFORMATION WILL BE SUPPLIED ON REQUEST.

Coil data

L2	N1 = 3	L3	N1 = 33	L4	N1 = 90	L5	N1 = 33
	N2 = 8		N2 = 113		N2 = 6		N2 = 113
	N3 = 1		N3 = 9				N3 = 9
	C = 82 pF		C = 180 pF				

L6	N1 = 50
	N2 = 50
	N3 = 4,5
	N4 = 6,5
	C = 82 pF

PLL STEREO DECODER

GENERAL DESCRIPTION

The TEA5580 PLL stereo decoder is for car, portable and mains-fed medium-fi radios and radio recorders. It features a 228 kHz voltage-controlled oscillator (VCO) that is locked to the 19 kHz stereo pilot tone by a phase-locked loop (PLL) system. Subcarrier frequencies of 19, 38, 57 and 114 kHz are regenerated via I^2L logic from the VCO output.

The PLL phase detector suppresses phase distortion due to the 57 kHz pilot tone from the German 'Verkehrs Warnfunk' (VWF) traffic warning system. Typical suppression of the 19 kHz stereo pilot tone is 50 dB, or up to 60 dB with adjustment of the pilot-cancelling resistor (R3, Figs 3 and 4). Adjacent channel interference is prevented by the use of two demodulators, one driven by the 38 kHz decoding signal and the other at 114 kHz to suppress the third harmonic of the multiplexed input signal.

The gain of the input amplifier can be adjusted by an external resistor and the circuit includes compensation for an IF filter typical roll-off frequency of 50 kHz (2 dB down at 38 kHz).

The supply voltage range of the circuit is 3,6 V to 16 V.

Features

- Wide supply voltage range
- Automatic mono/stereo switching (pilot presence detector)
- Smooth stereo-to-mono change-over at weak signals (signal-dependent stereo channel separation)
- LED driver for stereo/mono indicator
- Suppresses:
  - third harmonics (114 kHz) of multiplexed signal to prevent interference from strong adjacent channels;
  - phase distortion due to the 57 kHz signal from VWF transmitters
- Pilot cancelling circuit to give added suppression of 19 kHz pilot tone
- IF filter roll-off compensation

PACKAGE OUTLINE

16-lead DIL; plastic (SOT38).

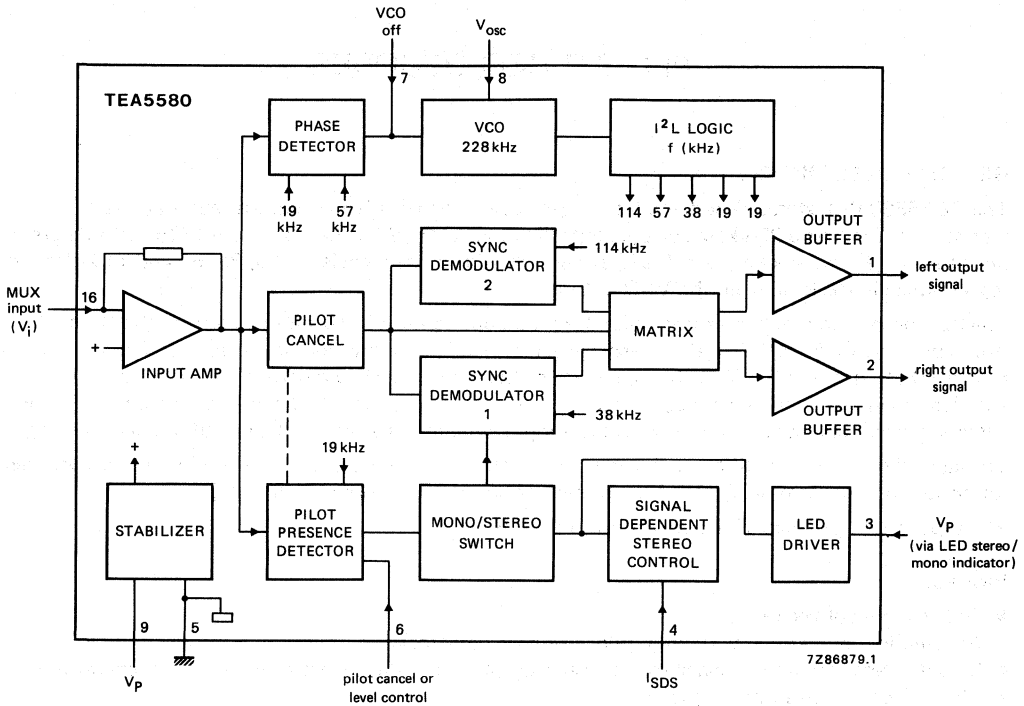


Fig. 1 Block diagram.

Note

Do **not** connect pins 10, 11, 12, 13, 14 or 15.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage (pins 3 and 9)	V_{3-5}, V_{9-5}	–	18	V
LED-driver current (peak value)	$-I_{3M}$	–	75	mA
Total power dissipation	P_{tot}	see derating curve Fig. 2		
Storage temperature range	T_{stg}	−55	+ 150	°C
Operating ambient temperature range	T_{amb}	−30	+ 80	°C

THERMAL RESISTANCE

From junction to ambient $R_{th\ j\text{-}a}$ = 75 K/W

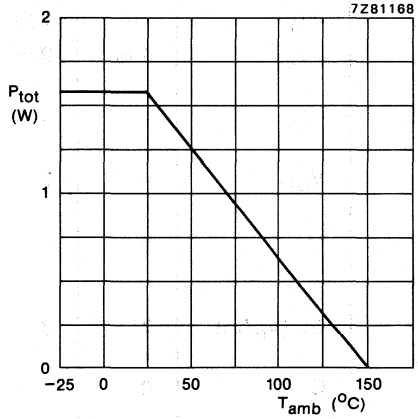


Fig. 2 Power derating curve.

CHARACTERISTICS

Measured in the circuit of Fig. 3; V_P = 7,5 V; T_{amb} = 25 °C; all d.c. voltages are with respect to pin 5; all currents are positive into the IC; a.c. measurements have an input MUX-signal of 1 V (peak-to-peak); V_{pilot} = 32 mV; f_m = 1 kHz; de-emphasizing time = 50 μs; oscillator adjusted to I_{osc} at V_i = 0 V; values are measured with an external roll-off network of 50 kHz (2 dB down at 38 kHz) at the input (dashed components R1 and C1 in Fig. 3); unless otherwise specified.

parameter	symbol	min.	typ.	max.	unit
D.C. Characteristics					
Supply voltage (note 1)	V_P	3,6	7,5	16	V
Total current consumption at V_P = 7,5 V (note 2)	I_P	–	10	13,5	mA
Dissipation at V_P = 7,5 V (note 2)	P_{tot}	–	75	–	mW
Bias voltage (pin 16)	V_{16-5}	–	1,4	–	V
Input current (pin 4)	I_4	–	–	400	μA
D.C. output current (pin 1)	$-I_1$	195	275	390	μA
D.C. output current (pin 2)	$-I_2$	195	275	390	μA
Output current (pin 3) (LED driver transistor)	$-I_3$	–	–	50	mA
Switch "VCO-OFF" voltage at pin 7	V_{off}	–	2,2	–	V
Switch "VCO-OFF" current into pin 7	I_7	–	–	50	μA
A.C. Characteristics					
Overall gain (mono)	Go (V_o/V_i)	7	8	9,5	dB
Gain input amplifier (adjustable) (Fig. 5)	G	0	–	20	dB
AF output voltage (mono) (r.m.s. value)	$V_{1-5} = V_{2-5}$	800	900	–	mV
Output channel unbalance	$\Delta V_o/V_o$	–	± 0,2	± 1,0	dB
Total harmonic distortion at $V_{o(rms)}$ = 0,9 V (note 3)	THD	–	0,2	0,5	%
Total harmonic distortion at $V_{o(rms)}$ = 1,0 V	THD	–	1,0	–	%
Channel separation L = 1; R = 0	α	26	40	–	dB
Signal-to-noise ratio bandwidth 20 Hz to 16 kHz	S/N	–	76	–	dB
Bandwidth IEC 79 (A-curve)	S/N	–	82	–	dB
Input impedance (external)	$\|Z_i\|$	–	47	–	kΩ
Output impedance (external) R = 12 kΩ; C = 3,9 nF	$\|Z_o\|$	–	9,3	–	kΩ

parameter	symbol	min.	typ.	max.	unit
SDS control (Fig. 6)					
10 dB channel separation	I_4	–	50	–	μA
Full stereo channel separation > 26 dB	I_4	100	–	–	μA
Full mono channel separation < 1 dB	I_4	–	–	10	μA
Stereo/mono switch					
R3 = 180 kΩ; note 4; Fig. 7					
Switching to stereo	V_i	–	18	24	mV
Switching to mono	V_i	8	–	–	mV
Hysteresis	ΔV_i	–	4	–	mV
Carrier and harmonic suppression at the output (note 5)					
Pilot signal suppression f = 19 kHz; R3 = 180 kΩ; note 4; Fig. 4	α_{19}	40	50	–	dB
Subcarrier suppression f = 38 kHz	α_{38}	–	50	–	dB
f = 57 kHz	α_{57}	–	50	–	dB
f = 228 kHz	α_{228}	–	80	–	dB
Intermodulation suppression (note 6) f_m = 10 kHz; spurious signal f_s = 1 kHz	α_2	–	60	–	dB
f_m = 13 kHz; spurious signal f_s = 1 kHz	α_3	–	60	–	dB
VWF tone suppression f = 57 kHz (note 7)	α_{57}	–	80	–	dB
SCA tone rejection f = 67 kHz (note 8)	α_{67}	–	80	–	dB
ACI rejection (note 9) f = 114 kHz	α_{114}	–	90	–	dB
f = 190 kHz	α_{190}	–	60	–	dB

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Ripple rejection					
f = 100 Hz; V_{ripple} = 200 mV; measured including RC network in supply line					
V_P = 7,5 V	RR_{100}	–	42	–	dB
V_P = 6,0 V	RR_{100}	–	46	–	dB
V_P = 3,6 V	RR_{100}	–	35	–	dB
VCO					
Oscillator frequency adjustable with R8	f_{osc}	–	228	–	kHz
Capture range (deviation from 228 kHz centre frequency) V_{pilot} = 9% (note 10)	$\Delta f/f$	–	8	–	%
Temperature coefficient	TC	–	+ 400 x 10^{-6}	–	K^{-1}

Notes to the characteristics

1. Minimum supply voltage only applicable in 6 V portable.
2. Without LED-driver current.
3. Guaranteed for mono, mono + pilot, stereo.
4. Also adjustable.
5. Reference output voltage at 1 kHz (measured channel R, pin 2).
6. Intermodulation suppression (BFC: Beat-Frequency Components):

$$\alpha_2 = \frac{V_{o(signal)}\ (\text{at 1 kHz})}{V_{o(spurious)}\ (\text{at 1 kHz})};\ f_s = (2 \times 10\ \text{kHz}) - 19\ \text{kHz}$$

$$\alpha_3 = \frac{V_{o(signal)}\ (\text{at 1 kHz})}{V_{o(spurious)}\ (\text{at 1 kHz})};\ f_s = (3 \times 13\ \text{kHz}) - 38\ \text{kHz}$$

measured with 91% mono signal; f_m = 10 or 13 kHz; 9% pilot signal.

7. Traffic radio (VWF) tone suppression:

$$\alpha_{57} = \frac{V_{o(signal)}\ (\text{at 1 kHz})}{V_{o(spurious)}\ (\text{at 1 kHz} \pm 23\ \text{Hz})}$$

measured with 91% stereo signal; f_m = 1 kHz; 9% pilot signal; 5% traffic subcarrier (f = 57 kHz; 60% AM modulated with f_{mod} = 23 Hz).

8. SCA (Subsidary Communication Authorization) tone rejection:

$$\alpha_{67} = \frac{V_{o(signal)}\ (\text{at 1 kHz})}{V_{o(spurious)}\ (\text{at 9 kHz})};\ f_s = (2 \times 38\ \text{kHz}) - 67\ \text{kHz}$$

measured with 81% mono signal; f_m = 1 kHz; 9% pilot signal; 10% SCA-subcarrier (f_s = 67 kHz, unmodulated).

9. ACI (Adjacent Channel Interference) rejection at:

$$\alpha_{114} = \frac{V_{o(signal)}\ (\text{at } 1\ \text{kHz})}{V_{o(spurious)}\ (\text{at } 4\ \text{kHz})}\ ;\ f_s = (3 \times 38\ \text{kHz}) - 110\ \text{kHz}$$

$$\alpha_{190} = \frac{V_{o(signal)}\ (\text{at } 1\ \text{kHz})}{V_{o(spurious)}\ (\text{at } 4\ \text{kHz})}\ ;\ f_s = (5 \times 38\ \text{kHz}) - 186\ \text{kHz}$$

measured with 90% mono signal; f_s = 1 kHz; 9% pilot signal; 1% spurious signal (f_s = 110 or 186 kHz, unmodulated).

10. The capture range of the PLL may be decreased to 4% by changing the value of C2 to 470 nF (see Fig. 4), if a small ambient temperature range is provided.

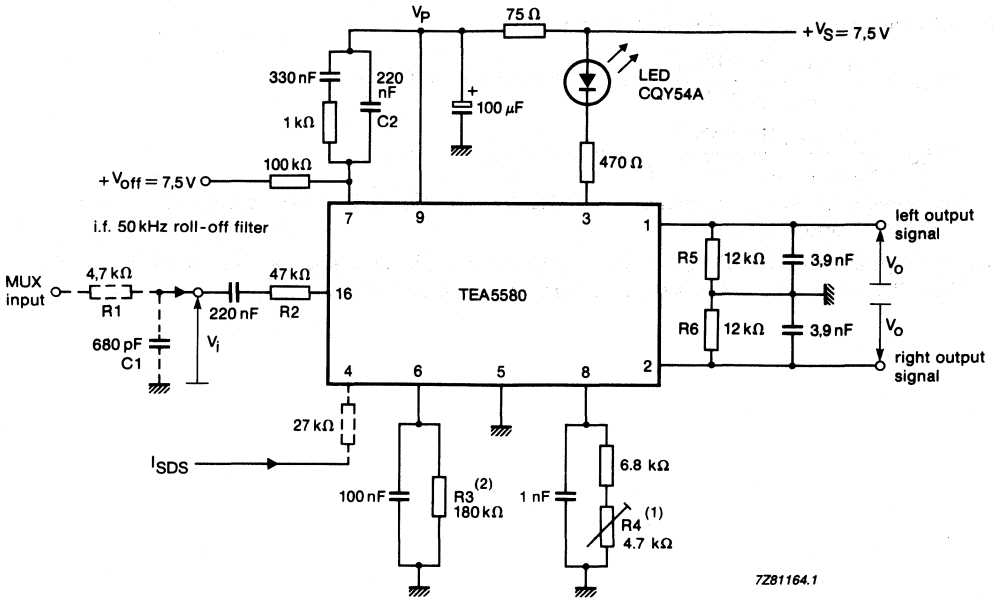


Fig. 3 Car radio application and test circuit.

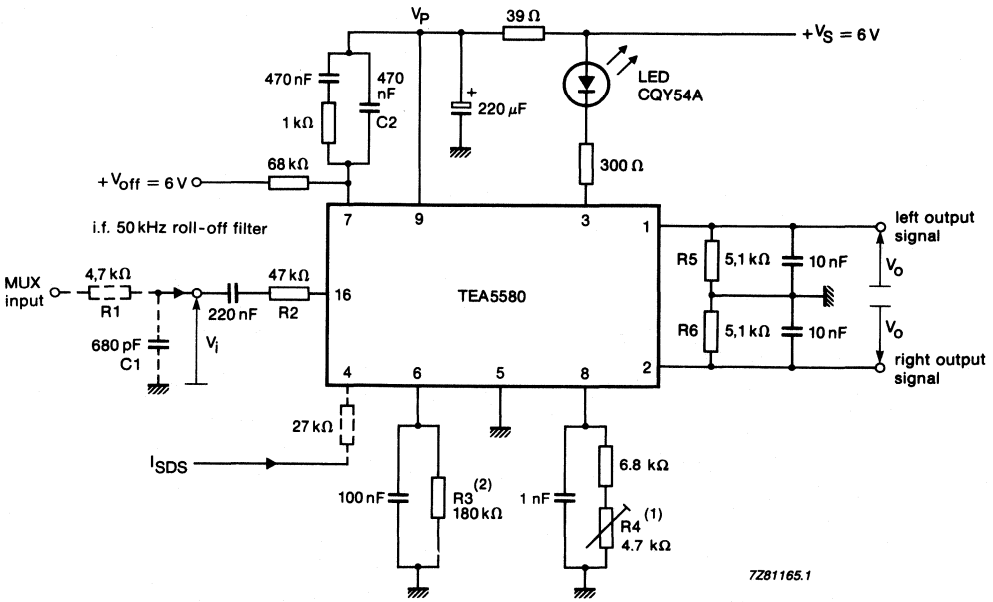
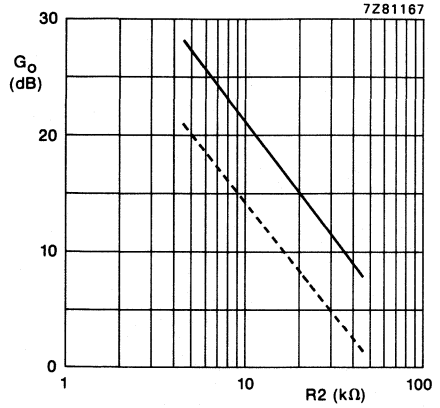


Fig. 4 Portable application circuit.

Notes to Figs 3 and 4

(1) R4: VCO frequency adjustment (228 kHz).

(2) R3: pilot cancelling or pilot level adjustment; best adjustment obtained with 470 kΩ potentiometer (see Figs 7 and 8); adjust for pilot cancellation of approx. 58 dB ± 10 dB and pilot sensitivity (mono to stereo) of approx. 23 mV ± 3 mV.



——— R5 = R6 = 12 kΩ

– – – R5 = R6 = 5,1 kΩ

Fig. 5 Overall gain as a function of input resistance (R2).

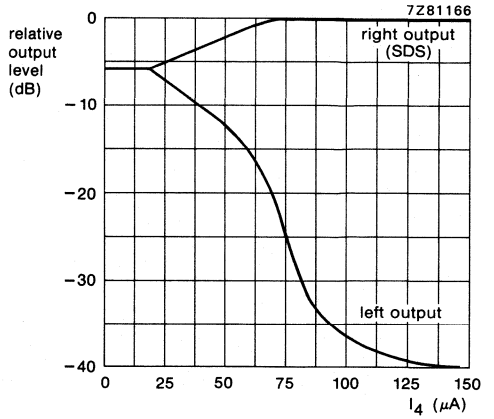
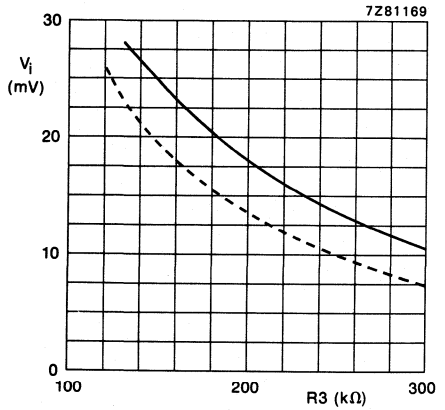


Fig. 6 Relative output level as a function of the signal dependent stereo (SDS) current (I_4); typical curves.



——— stereo "ON"

– – – stereo "OFF"

Fig. 7 Pilot sensitivity: pilot input voltage (V_i) as a function of pilot adjustment resistor R3; typical curves.

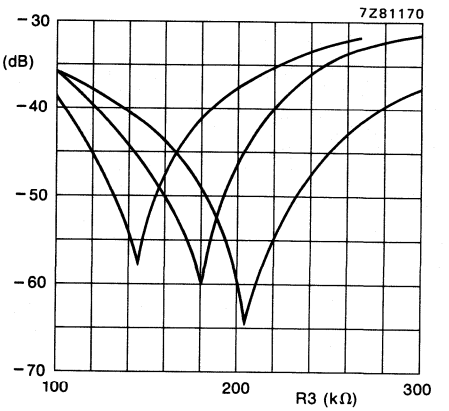


Fig. 8 Random samples of pilot cancelling: $\frac{V_o \text{ (at 19 kHz)}}{V_o \text{ (at 1 kHz)}}$ in dB as a function of R3; $V_{i(p\text{-}p)}$ = 1 V; V_{pilot} = 32 mV (9%).

PLL STEREO DECODER

GENERAL DESCRIPTION

The TEA5581 PLL stereo decoder is for car and medium-fi radios. It incorporates all the features provided by the TEA5580 together with a source selector, muting circuit and output amplifiers with adjustable gain. It also features a switch for radio or cassette function and a 228 kHz voltage-controlled oscillator (VCO) that is locked to the 19 kHz stereo pilot tone by a phase-locked loop (PLL) system. Subcarrier frequencies of 19, 38, 57 and 114 kHz are regenerated via I^2L logic from the VCO output.

The PLL phase detector suppresses phase distortion due to the 57 kHz pilot tone from the German 'Verkehrs Warnfunk' (VWF) traffic warning system. Typical suppression of the 19 kHz stereo pilot tone is 40 dB. Adjacent channel interference is prevented by the use of two demodulators, one driven by the 38 kHz decoding signal and the other at 114 kHz to suppress the third harmonic of the multiplexed input signal.

The gain of the input amplifier can be adjusted by an external resistor and the circuit includes compensation for an IF filter typical roll-off frequency of 50 kHz (2 dB down at 38 kHz).

The supply voltage range of the circuit is 7 V to 16 V.

Features

- Wide supply voltage range
- Automatic mono/stereo switching (pilot presence detector)
- Smooth stereo-to-mono change-over at weak signals (signal-dependent stereo channel separation)
- LED driver for stereo/mono indicator
- Suppresses:

  third harmonics (114 kHz) of multiplexed signal to prevent interference from strong adjacent channels;

  phase distortion due to the 57 kHz signal from VWF transmitters
- Pilot cancelling circuit to give added suppression of 19 kHz stereo pilot tone (up to 25 dB)
- IF filter roll-off compensation
- Source selector for radio or cassette input (typ. 90 dB)
- Mute circuit for 90 dB (typ.) muting of the output level
- Matrix and two output buffers with adjustable gain (max. 20 dB)

PACKAGE OUTLINES

TEA5581 : 16-lead DIL; plastic (SOT38).
TEA5581T: 16-lead mini-pack; plastic (SO16L; SOT162A).

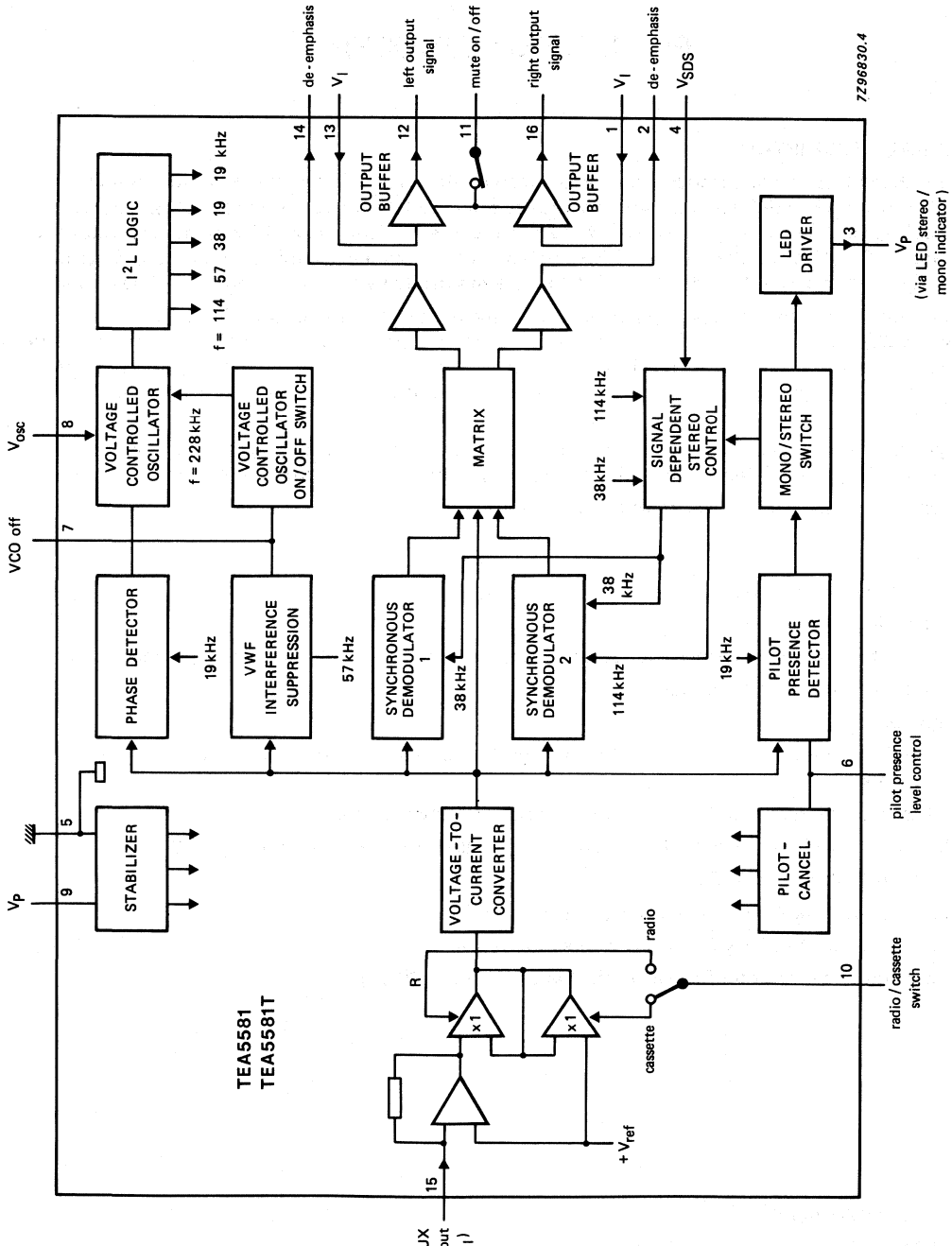


Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage range		V_{3-5}, V_{9-5}	–	18	V
LED-driver current (peak value)		$-I_{3M}$	–	75	mA
Total power dissipation		P_{tot}	see derating curve Fig. 2		
Storage temperature range		T_{stg}	−65	+150	°C
Operating ambient temperature range		T_{amb}	−30	+80	°C
Electrostatic handling *		V_{es}	−600	+600	V

From junction to ambient in free air

SOT38	$R_{th\ j-a}$	75 K/W
SOT162	$R_{th\ j-a}$	95 K/W

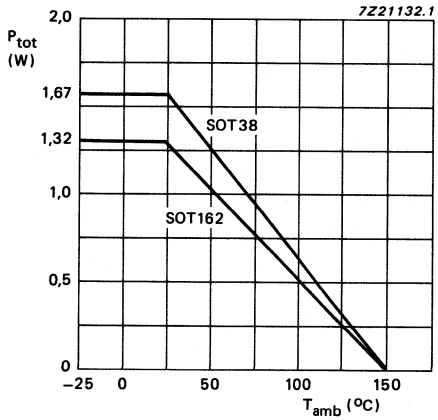


Fig. 2 Power derating curve.

* Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ resistor.

DC CHARACTERISTICS

Measured in the circuit of Fig. 7; V_S = 8.5 V; T_{amb} = 25 °C; all DC voltages are with respect to pin 5; all currents are positive into the IC.

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage	R1 = 75 Ω	V_S	7.0	8.5	16	V
Total current consumption	without LED driver	I_{tot}	–	15	20	mA
Power dissipation		P_{tot}	–	125	–	mW
Voltage						
pin 15		V_{15}	–	2.1	–	V
pins 12 and 16		V_{12}, V_{16}	3.2	3.6	4.0	V
DC output current						
pins 2 and 14		$-I_{14}$, $-I_2$	225	320	450	μA
Output current						
pin 3		$-I_3$	–	–	20	mA
Switch "VCO-OFF"						
voltage		V_7	–	2.2	–	V
Switch "VCO-OFF"						
current		I_7	–	50	75	μA

AC CHARACTERISTICS

Measured in the circuit of Fig. 7; V_S = 8.5 V; T_{amb} = 25 °C; AC measurements have an input MUX-signal of 1 V (peak-to-peak); V_{pilot} = 32 mV (9%); f_m = 1 kHz; oscillator adjusted to 228 kHz at V_i = 0 V; values are measured with an external roll-off network of 50 kHz (2 dB down at 38 kHz) at the input (dashed components R_S and C_S in Fig. 7); unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Transimpedance		V_O/I_I	0.13	0.15	0.17	V/μA
Input current (RMS value)		$I_{I(rms)}$	–	–	12	μA
Overall gain	mono; R3 = 47 kΩ	G_o (V_o/V_i)	9.0	10.0	11.0	dB
AF output voltage (RMS value)		$V_{12} = V_{16}$	0.95	1.14	1.33	V
AF output voltage (RMS value)		$V_2 = V_{14}$	–	–	500	mV
Total harmonic distortion	note 1; $V_{O(rms)}$ = 1 V	THD	–	0.1	0.5	%
Output voltage	THD = 1%	$V_{12} = V_{16}$	–	1.5	–	V
Output channel unbalanced		V_{12}/V_{16}	–	0.2	1.0	dB
Channel separation	IF roll-off frequency = 50 kHz L = 1; R = 0	α	26	40	–	dB
S/N ratio	bandwidth 20 Hz to 16 kHz	S/N	–	76	–	dB
	bandwidth IEC 79 (curve Din A)	S/N	–	82	–	dB
SDS control	see Fig. 6					
Channel separation	V_4 = 1.0 V	α	5	10	15	dB
Full stereo	channel separation ⩾ 26 dB	V_4	–	1.2	1.25	V
Full mono	channel separation ⩽ 1 dB	V_4	0.75	0.8	–	V
Stereo/mono switch	note 2; see Fig. 5; R4 = 180 kΩ					
Switching to:						
stereo		V_{pilot}	–	14	20	mV
mono		V_{pilot}	4	–	–	mV
Hysteresis		ΔV_I	–	4.5	–	mV

AC CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Carrier and harmonic suppression at the output	note 3					
Pilot signal suppression	f = 19 kHz; R4 = 180 kΩ; note 2; see Figs 3 and 4	α_{19}	32	40	–	dB
Subcarrier suppression						
f = 38 kHz		α_{38}	–	50	–	dB
f = 57 kHz		α_{57}	–	50	–	dB
f = 228 kHz		α_{228}	–	75	–	dB
Intermodulation suppression	note 4					
f_m = 10 kHz	spurious signal f_s = 1 kHz	α_2	–	50	–	dB
f_m = 13 kHz	spurious signal f_s = 1 kHz	α_3	–	50	–	dB
VWF tone suppression f = 57 kHz	note 5	α_{57}	–	80	–	dB
SCA tone rejection f = 67 kHz	note 6	α_{67}	–	70	–	dB
ACI rejection	note 7					
f = 114 kHz		α_{114}	–	90	–	dB
f = 190 kHz		α_{190}	–	60	–	dB
Ripple rejection						
Ripple rejection	f = 100 Hz; V_{ripple} = 100 mV; mono	RR_{100}	–	50	–	dB
VCO						
Oscillator frequency adjustable with R5		f_{osc}	–	228	–	kHz
Capture range	deviation from 228 kHz centre frequency; V_{pilot} = 32 mV	$\Delta f/f$	–	6	–	%
Temperature coefficient	uncompensated	TC	–	-200×10^{-6}	–	K^{-1}

parameter	conditions	symbol	min.	typ.	max.	unit
Source selector						
Suppression of MPX signal	$V_{10} \geq 2$ V	α	80	90	–	dB
Switching level	cassette to radio					
voltage		V_{IL}	–	–	0.8	V
current		I_{IL}	–	10	25	μA
Switching level	radio to cassette					
voltage		V_{IH}	2.0	–	V_S	V
current		I_{IH}	–	–	1	μA
Output amplifiers						
Gain	note 8; R_6/R_7	G_v	–	–	20	dB
Output impedance		Z_o	–	200	500	Ω
External load impedance		$\|Z_l\|$	5	–	–	kΩ
Suppression (mute)	$V_{11} = \leq 0{,}8$ V	α	84	90	–	dB
DC offset voltage at outputs during mute switching	mute OFF-to-ON	ΔV_{12}, ΔV_{16}	–	1.0	–	mV
	mute ON-to-OFF	ΔV_{12}, ΔV_{16}	–	2.0	–	mV
Muting circuit						
Input voltage	mute ON	V_{IL}	–	–	0.8	V
	mute OFF	V_{IH}	2.0	–	V_S	V
Input current	mute ON	I_{IL}	–	10	25	μA
	mute OFF	I_{IH}	–	–	1	μA

Notes to the characteristics

1. Guaranteed for mono, mono + pilot and stereo.
2. Also adjustable.
3. Reference output voltage at 1 kHz (measured channel R, pin 16).
4. Intermodulation suppression (Beat-Frequency Components):

$$\alpha_2 = \frac{V_{o(signal)}\ (\text{at } 1\text{ kHz})}{V_{o(spurious)}\ (\text{at } 1\text{ kHz})};\ f_s = (2 \times 10\text{ kHz}) - 19\text{ kHz}$$

$$\alpha_3 = \frac{V_{o(signal)}\ (\text{at } 1\text{ kHz})}{V_{o(spurious)}\ (\text{at } 1\text{ kHz})};\ f_s = (3 \times 13\text{ kHz}) - 38\text{ kHz}$$

measured with 91% mono signal; f_m = 10 or 13 kHz; 9% pilot signal.

5. Traffic radio (VWF) tone suppression:

$$\alpha_{57} = \frac{V_{o(signal)}\ (\text{at } 1\text{ kHz})}{V_{o(spurious)}\ (\text{at } 1\text{ kHz} \pm 23\text{ Hz})}$$

measured with 91% stereo signal; f_m = 1 kHz; 9% pilot signal; 5% traffic subcarrier (f = 57 kHz; 60% AM modulated with f_{mod} = 23 Hz).

6. SCA (Subsidiary Communication Authorization) tone rejection:

$$\alpha_{67} = \frac{V_{o(signal)}\ (\text{at } 1\text{ kHz})}{V_{o(spurious)}\ (\text{at } 9\text{ kHz})};\ f_s = (2 \times 38\text{ kHz}) - 67\text{ kHz}$$

measured with 81% mono signal; f_m = 1 kHz; 9% pilot signal; 10% SCA-subcarrier (f_s = 67 kHz, unmodulated).

7. ACI (Adjacent Channel Interference) rejection at:

$$\alpha 114 = \frac{V_{o(signal)}\ (\text{at } 1\text{ kHz})}{V_{o(spurious)}\ (\text{at } 4\text{ kHz})};\ f_s = (3 \times 38\text{ kHz}) - 110\text{ kHz}$$

$$\alpha 190 = \frac{V_{o(signal)}\ (\text{at } 1\text{ kHz})}{V_{o(spurious)}\ (\text{at } 4\text{ kHz})};\ f_s = (5 \times 38\text{ kHz}) - 186\text{ kHz}$$

measured with 90% mono signal; f_s = 1 kHz; 9% pilot signal; 1% spurious signal (f_s = 110 or 186 kHz, unmodulated).

8. Maximum permitted value of feedback resistor = 220 kΩ.

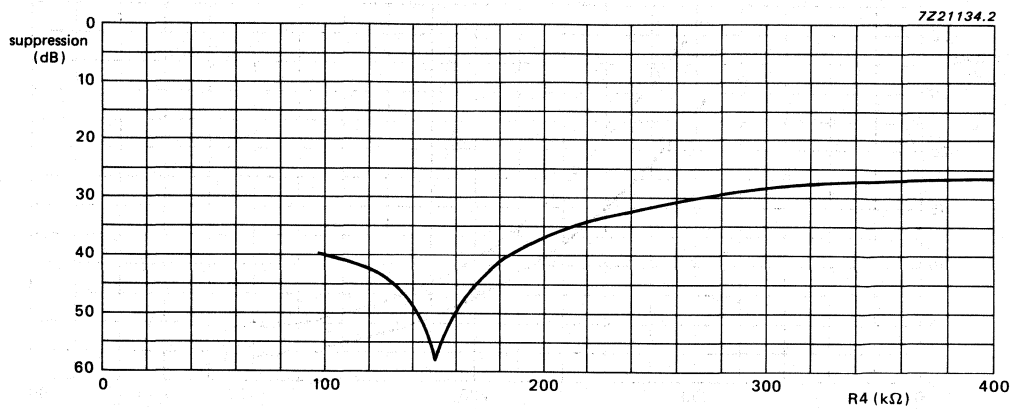
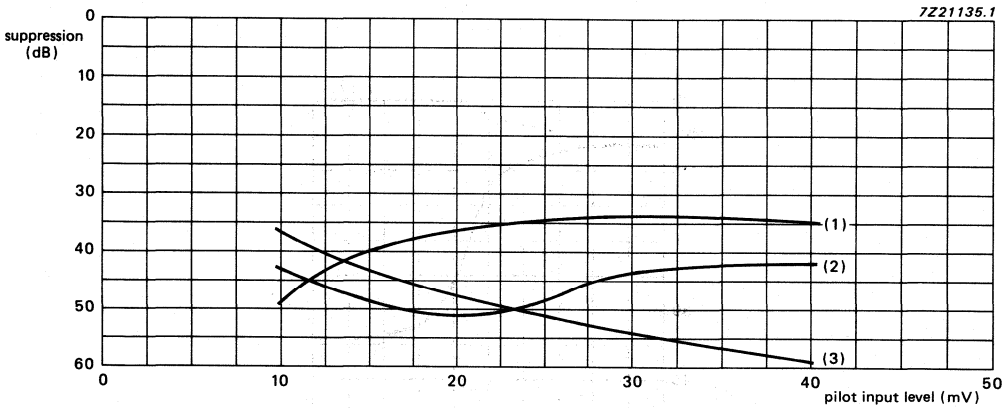
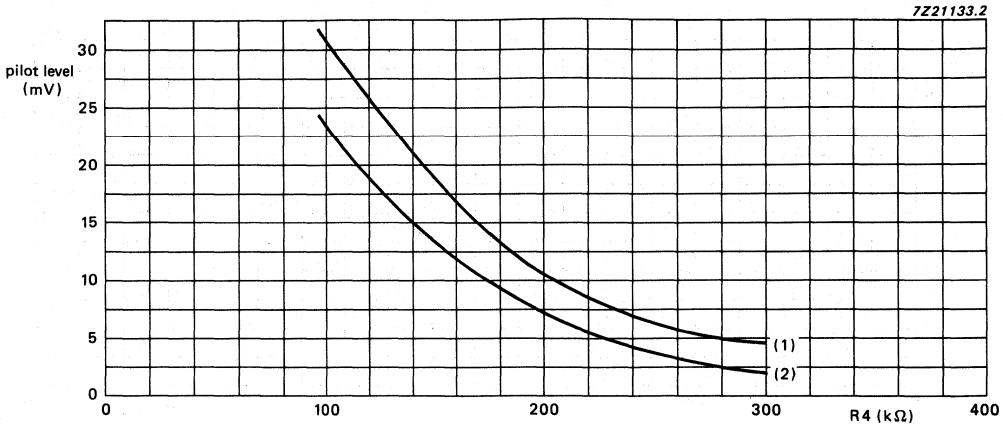


Fig. 3 Pilot suppression plotted against resistance (R4).



(1) 220 kΩ
(2) 180 kΩ
(3) 150 kΩ

Fig. 4 Pilot suppression plotted against pilot input voltage level.



(1) Switching from mono to stereo.
(2) Switching from stereo to mono.

Fig. 5 Pilot sensitivity against resistance (R4).

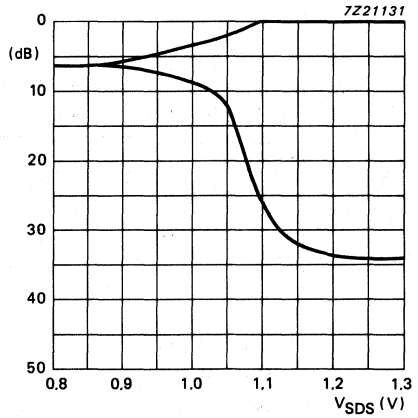
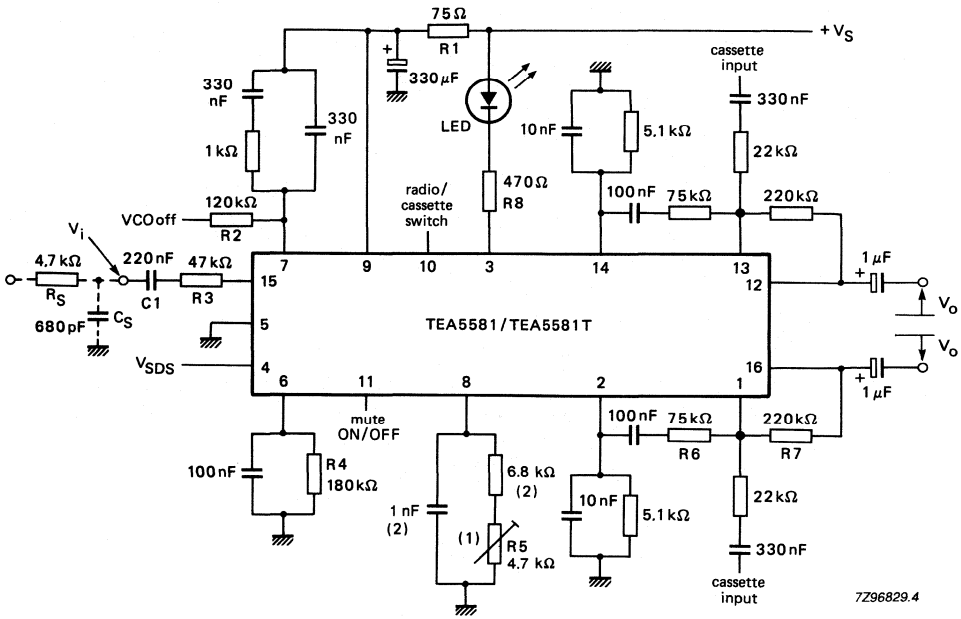


Fig. 6 Channel separation against V_{SDS}.

APPLICATION INFORMATION



(1) 25% tolerance (all other resistors have a 5% tolerance).
(2) 1% tolerance (NP0).

Fig. 7 Application diagram.

AM/FM RADIO RECEIVER CIRCUIT

GENERAL DESCRIPTION

The TEA5591 is an integrated radio circuit which is designed for use in portable receivers and clock radios. The IC is also applicable to mains-fed AM and AM/FM receivers and car radio-receivers. The main advantage of this IC is its ability to operate over a wide range of supply voltages without loss of performance. The AM circuit incorporates a balanced mixer and a 'one-pin' oscillator, which operates in the 0.6 MHz to 30 MHz frequency range, with amplitude control. The circuit also includes an IF amplifier, a detector and an AGC circuit which controls the IF amplifier and the mixer. The FM circuit incorporates an RF amplifier, a balanced mixer and a 'one-pin' oscillator together with two AC coupled IF amplifiers (with distributed selectivity), a quadrature demodulator for the ceramic filter and internal AFC.

Features

- DC AM/FM switch facility
- Three internal separate stabilizers to enable operation over a wide range of supply voltages (1.8 to 15 V)
- All pins (except pin 9) are ESD protected

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage (pin 8)		V_P	1.8	3.0	15	V
Supply current						
AM part		$I_{P(AM)}$	–	14	19	mA
FM part		$I_{P(FM)}$	–	17	23	mA
Operating ambient temperature range		T_{amb}	−15	–	+60	°C
AM performance (pin 13)	m = 0.3					
RF sensitivity						
RF input voltage	V_o = 10 mV	V_i	–	3.5	–	μV
RF input voltage	(S+N)/N = 26 dB	V_i	–	17	–	μV
Signal plus noise-to-noise ratio	V_i = 1 mV	(S+N)/N	–	48	–	dB
AF output voltage		V_o	–	50	–	mV
Total harmonic distortion		THD	–	0.7	–	%
FM performance (pin 1)	Δf = 22.5 kHz					
RF sensitivity						
RF input voltage						
−3 dB before limiting		V_i	–	2.3	4.0	μV
Signal plus noise-to-noise ratio for:						
RF input signal voltage (V_i)	V_i = 3.0 μV	(S+N)/N	23	26	–	dB
	V_i = 1 mV	(S+N)/N	–	60	–	dB
AF output voltage	V_i = 100 μV	V_o	75	90	–	mV
Total harmonic distortion		THD	–	0.8	–	%

PACKAGE OUTLINE

20-lead DIL; plastic (SOT146).

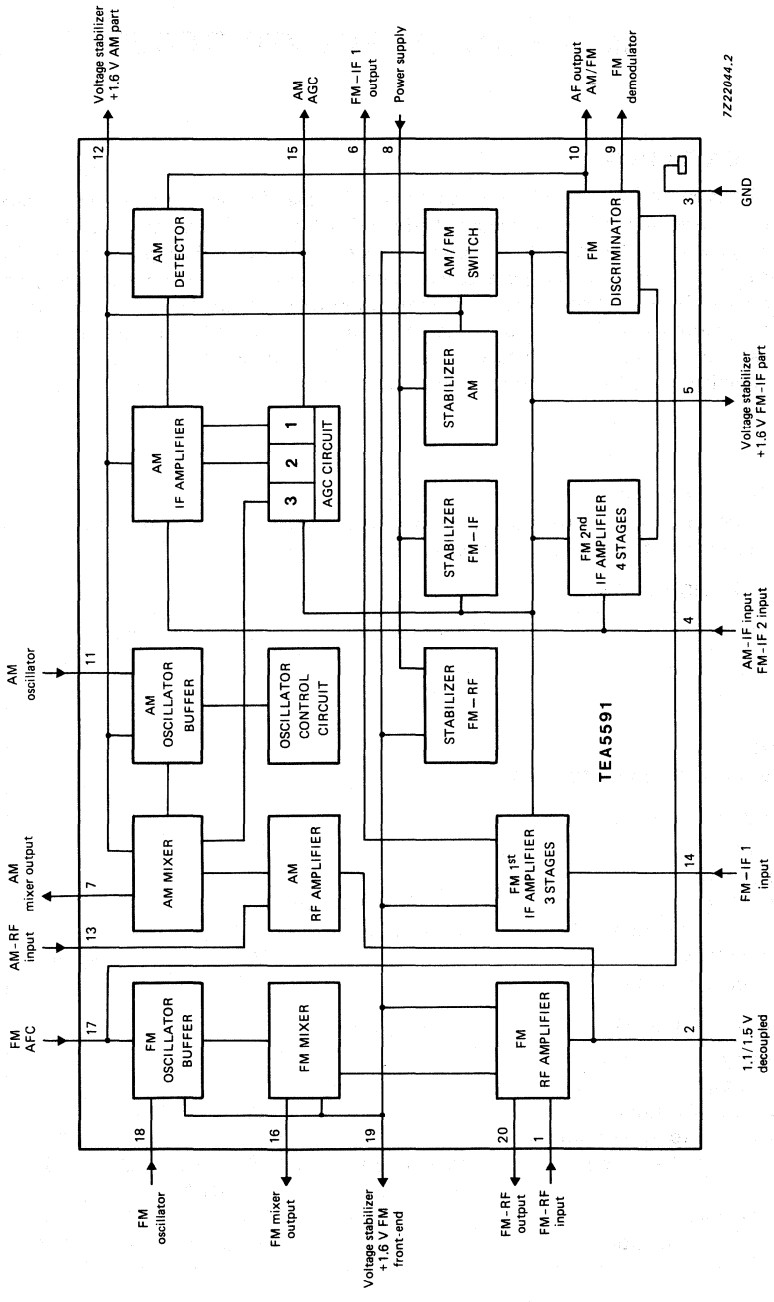


Fig.1 Block diagram.

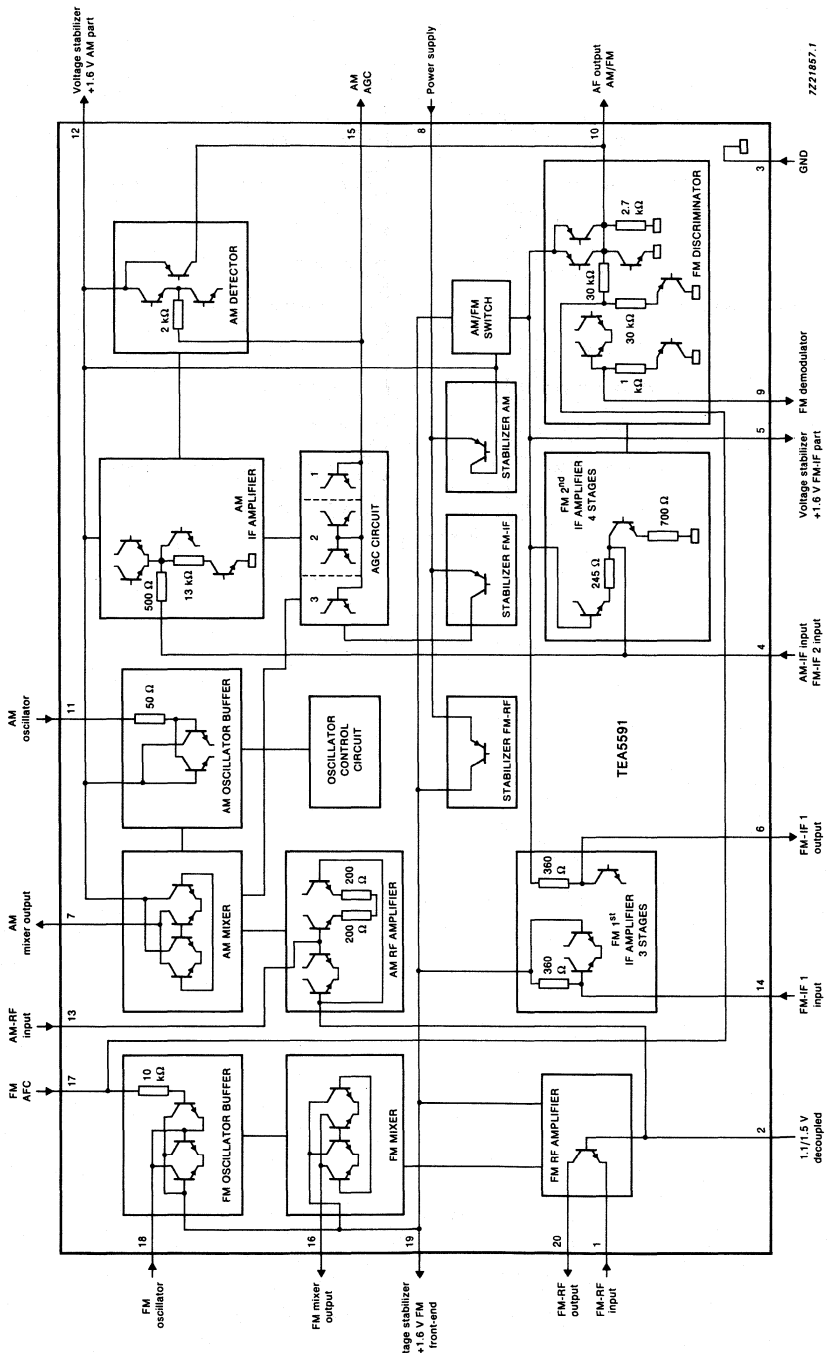


Fig.2 Equivalent circuit diagram.

PINNING

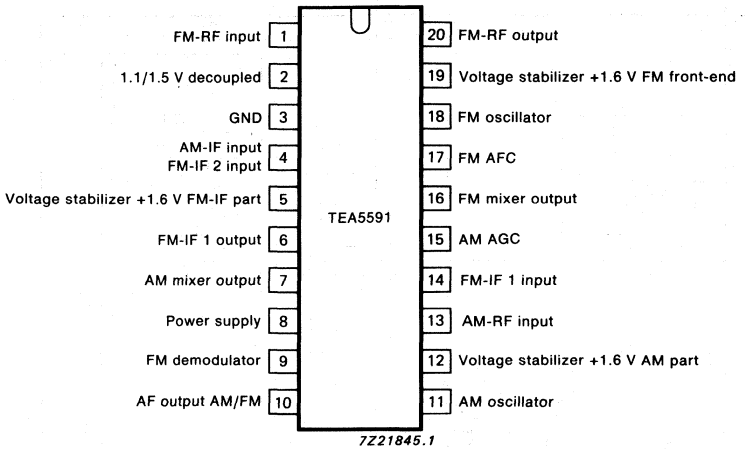


Fig.3 Pinning diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage (pin 8)		V_P	–	18	V
Storage temperature range		T_{stg}	−65	+ 150	°C
Operating ambient temperature range		T_{amb}	−15	+ 60	°C
Total power dissipation		P_{tot}	see Fig.4		

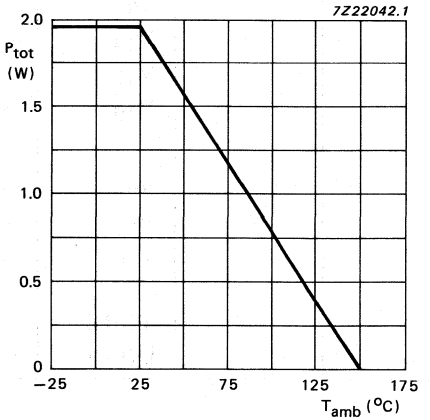


Fig.4 Power derating curve.

DC CHARACTERISTICS

All voltages are referenced to pin 3; all input currents are positive; all parameters are measured in Fig.5 at nominal supply voltage V_P = 3 V; T_{amb} = 25 °C unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage		V_P	1.8	3.0	15	V
Voltages (FM)						
pin 1		V_1	–	0.90	–	V
pin 2		V_2	–	1.60	–	V
pin 4		V_4	–	0.85	–	V
pin 5		V_5	1.5	1.60	1.75	V
pin 6		V_6	–	1.48	–	V
pin 9		V_9	–	1.05	–	V
pin 14		V_{14}	–	1.63	–	V
pin 17		V_{17}	–	0.60	–	V
pin 19		V_{19}	–	1.60	–	V
Voltages (AM)						
pin 2		V_2	–	1.10	–	V
pin 12		V_{12}	–	1.60	–	V
pin 15		V_{15}	–	1.54	–	V
Supply current						
AM part		$I_{P(AM)}$	–	14	19	mA
FM part		$I_{P(FM)}$	–	17	23	mA

AC CHARACTERISTICS

V_P = 3 V; T_{amb} = 25 °C unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
AM PART						
Input conductance pin 4	f = 0.5 MHz	g_{ie}	–	1.7	–	ms
Input capacitance pin 4	f = 0.5 MHz	C_{ie}	–	5	–	pF
Input conductance pin 13	f = 1.0 MHz	g_{ie}	–	230	–	μs
Input capacitance pin 13	f = 1.0 MHz	C_{ie}	–	13	–	pF
Output conductance pin 7	f = 0.5 MHz	g_{oe}	–	4	–	μs
Output capacitance pin 7	f = 0.5 MHz	C_{oe}	–	4.7	–	pF
Conductance pin 11	f = 1.5 MHz	g_e	–	−6.8	–	ms
Capacitance pin 11	f = 1.5 MHz	C_e	–	25	–	pF
FM PART						
Input conductance pin 4	f = 10.7 MHz	g_{ie}	–	2.7	–	ms
Input capacitance pin 4	f = 10.7 MHz	C_{ie}	–	6	–	pF
Input conductance pin 14	f = 10.7 MHz	g_{ie}	–	2.8	–	ms
Input capacitance pin 14	f = 10.7 MHz	C_{ie}	–	2.5	–	pF
Output conductance pin 6	f = 10.7 MHz	g_{oe}	–	2.8	–	ms
Output capacitance pin 6	f = 10.7 MHz	C_{oe}	–	3.0	–	pF
Output conductance pin 16	f = 10.7 MHz	g_{oe}	–	1.6	–	μs
Output capacitance pin 16	f = 10.7 MHz	C_{oe}	–	4.5	–	pF
Conductance pin 9	f = 10.7 MHz	g_e	–	880	–	μs
Capacitance pin 9	f = 10.7 MHz	C_e	–	3.6	–	pF
Conductance pin 18	f = 100 MHz	g_e	–	−4	–	ms
Capacitance pin 18	f = 100 MHz	C_e	–	10	–	pF

AC CHARACTERISTICS

All parameters are measured in Fig.5 at nominal supply voltage V_P = 3 V; T_{amb} = 25 °C unless otherwise specified.
RF conditions: Input frequency 1 MHz; 30% modulation where f_{mod} = 1 kHz; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
AM PERFORMANCE						
RF sensitivity						
AF output voltage for: V_i = 7.5 μV	no AGC	V_o	16	30	40	mV
Noise						
Signal plus noise-to-noise ratio for:						
RF input signal voltage of V_i = 17 μV		(S + N)/N	23	26	–	dB
V_i = 1 mV		(S + N)/N	–	48	–	dB
Optimum source impedance		Z_S	–	1.8	–	kΩ
Noise factor	optimum noise impedance	NF	–	4	–	dB
AGC						
Change in RF input voltage for 10 dB change in output voltage	V_{i1} = 100 mV	V_{i1}/V_{i2}	80	86	–	dB
AF output voltage	V_i = 100 μV	V_o	40	50	60	mV
Total harmonic distortion	V_i = 100 μV to 10 mV	THD	–	0.7	1.5	%
	V_i = 100 μV to 10 mV; m = 0.8	THD	–	3	5	%
	V_i = 80 mV; m = 0.8	THD	–	–	8	%

Transimpedance (Z_{tr}) = v_4/i_7 = 900Ω.

parameter	conditions	symbol	min.	typ.	max.	unit
IF suppression (note 1)	V_o = 30 mV	α	–	20	–	dB
Oscillator (pin 11)						
Input voltage	f_{osc} = 1.5 MHz	V_{osc}	–	150	190	mV
	f_{osc} = 30.5 MHz	V_{osc}	–	150	–	mV
	Vp = 1.5 V	V_{osc}	100	–	–	mV
Temperature behaviour	–15 to +60 °C (only the IC)					
Sensitivity		ΔV_i	–	–2	–	dB
Output voltage	V_i = 1 mV	ΔV_o	–	1	–	dB
Oscillator frequency						
LW		Δf_{osc}	–	500	–	Hz
MW		Δf_{osc}	–	300	–	Hz
SW		Δf_{osc}	–	100	–	kHz
Supply voltage behaviour	Vp = 1.8 to 15 V					
Sensitivity		ΔV_i	–	0	–	dB
Output voltage	V_i = 1 mV	ΔV_o	–	0.5	–	dB
Oscillator frequency						
LW		Δf_{osc}	–	6	–	kHz
MW		Δf_{osc}	–	0.1	–	kHz
SW		Δf_{osc}	–	30	–	kHz

AC CHARACTERISTICS

All parameters are measured in Fig.5 at nominal supply voltage V_P = 3 V; T_{amb} = 25 °C unless otherwise specified

RF conditions: Input frequency 100 MHz; frequency deviation f = ± 22,5 kHz and f_{mod} = 1 kHz

parameter	conditions	symbol	min.	typ.	max.	unit
FM PERFORMANCE						
RF sensitivity						
RF input voltage	−3 dB before limiting	V_{iFM}	–	2.3	4.0	μV
Noise						
Signal plus noise-to-noise ratio for:						
RF input signal voltage (V_i)						
V_i = 3.0 μV		(S + N)/N	23	26	–	dB
V_i = 1 mV		(S + N)/N	–	60	–	dB
Optimum source impedance		Z_{source}	–	50	–	Ω
Noise factor	optimum source impedance	NF	–	6	–	dB
AF output voltage	V_i = 100 μV	V_o	75	90	–	mV
Total harmonic distortion	V_i = 30 μV to 50 mV	THD	–	0.8	–	%
	V_i = 1 mV; Δf = 75 kHz	THD	–	3	–	%
	V_i = 100 mV; Δf = 75 kHz	THD	–	3	–	%
AM suppression	note 2					
RF input signal	V_i = 100 μV to 10 mV	AMS	–	50	–	dB
Oscillator voltage (pin 18)	f_{osc} = 100 MHz	V_{osc}	–	220	–	mV
	V_P = 1.5 V	V_{osc}	100	–	–	mV
IF rejection ratio		IF_{rr}	–	60	–	dB
AFC	f_{osc} = 111.2 MHz					
	V_{17} = 1.4 V	Δf	–	−620	–	kHz
	V_{17} = 0.2 V	Δf	–	+420	–	kHz

parameter	conditions	symbol	min.	typ.	max.	unit
Temperature behaviour	−15 to +60 °C (only the IC)					
RF sensitivity	−3 dB limiting	ΔV_i	–	−6	–	dB
Output voltage	V_i = 100 μV	ΔV_o	–	−2	–	dB
Oscillator frequency		Δf_{osc}	–	−0.3	–	%
Supply voltage behaviour	V_P = 1.8 to 15 V					
RF sensitivity	−3 dB limiting	ΔV_i	–	6	–	dB
Output voltage	V_i = 100 μV	ΔV_o	–	0.5	–	dB
Oscillator frequency		Δf_{osc}	–	100	–	kHz
Oscillator voltage		ΔV_{osc}	–	1.0	–	dB

Notes to the AC characteristics

1. $\alpha = \frac{V_i \text{ at } f_i = 455 \text{ kHz}}{V_i \text{ at } f_i = 1 \text{ MHz}}$.
2. AM suppression is measured at f_{mod} = 400 Hz, m = 0.3 for AM; f_{mod} = 1 kHz, Δf = 75 kHz for FM.

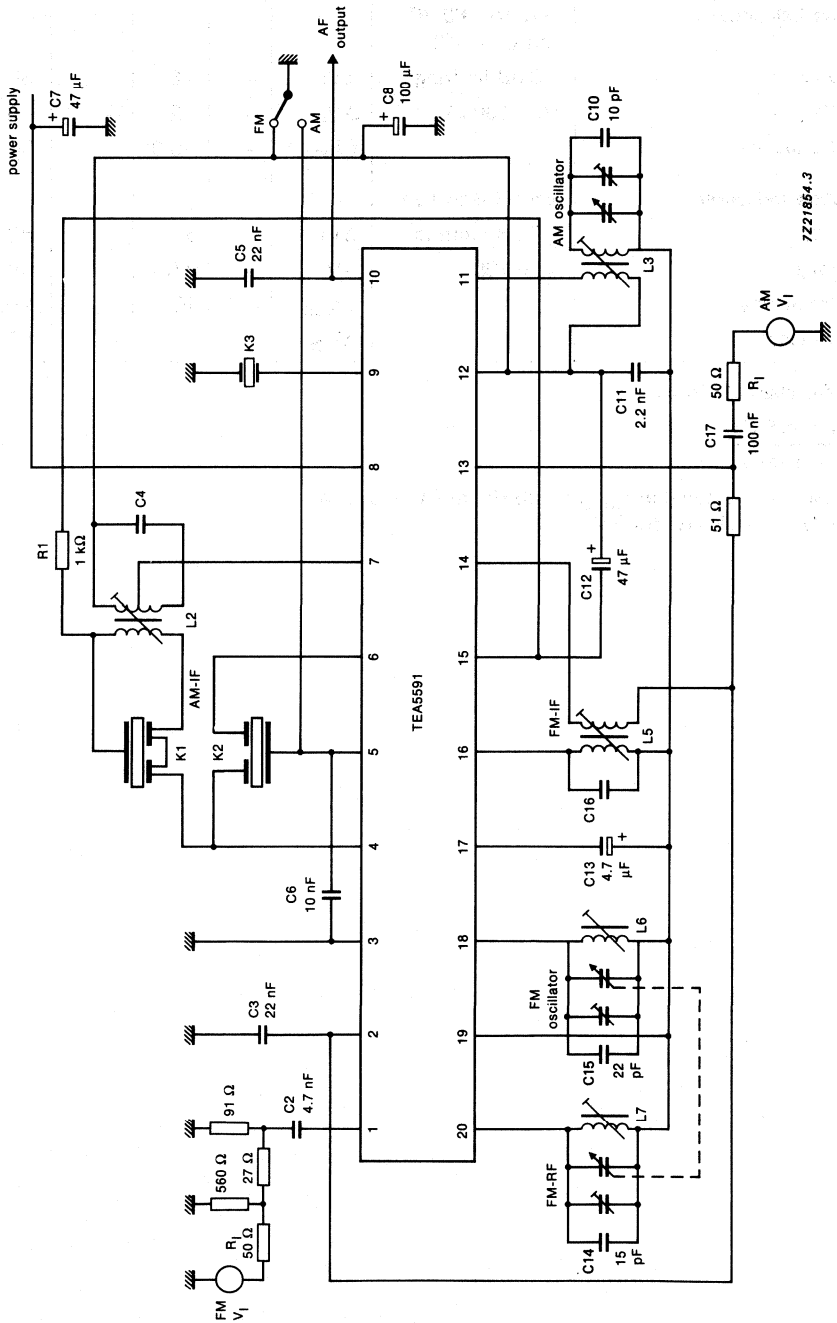


Fig.5 Test circuit.

APPLICATION INFORMATION

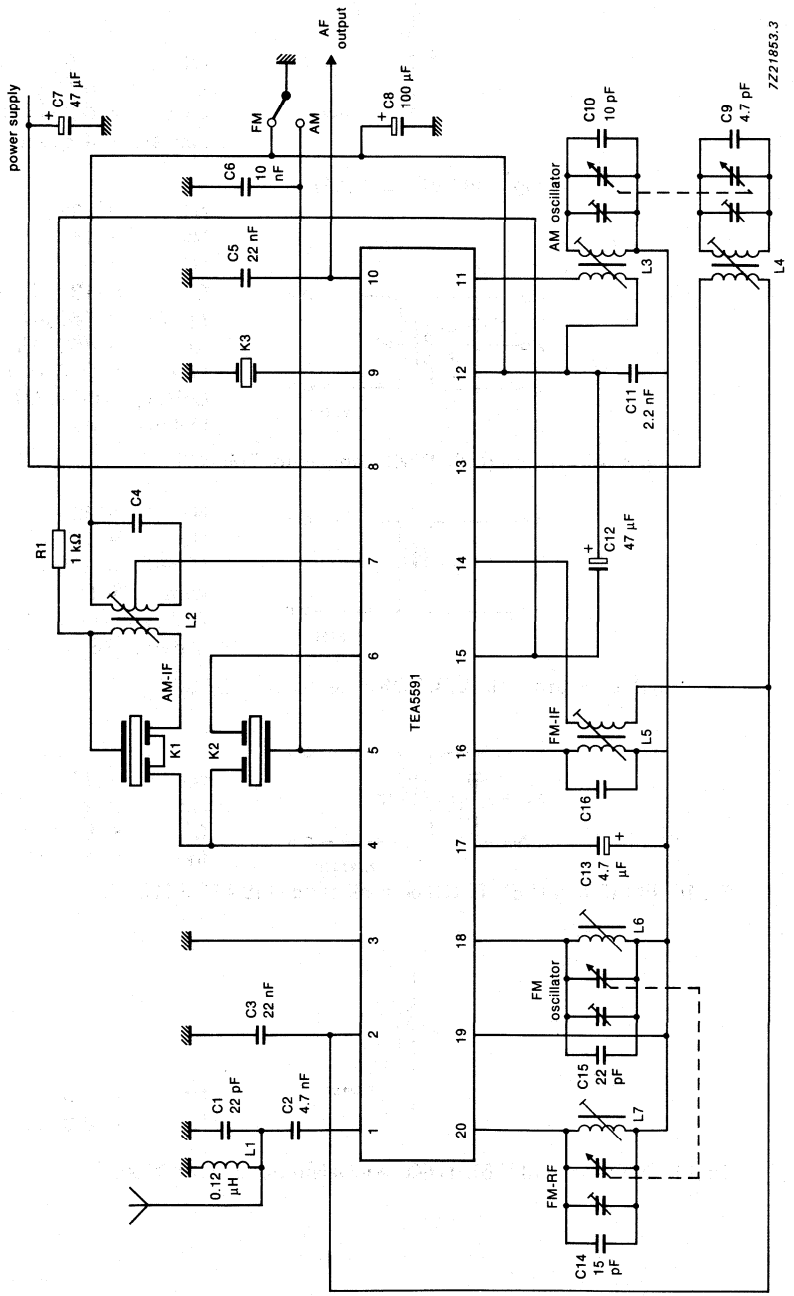
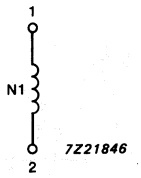


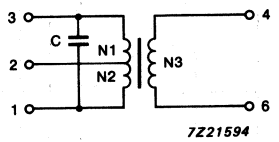
Fig.6 Application diagram.

Component data



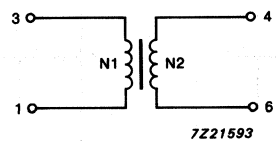
N1 = 4.5
L = 0.12 μH
Wire = 0.8 mm diameter
diameter = 4.5 mm

Fig.7 FM BFP coil (L1).



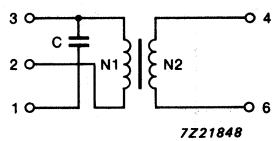
N1 = 132
N2 = 14
N3 = 9
C = 180 pF (internal)
Lprim = 660 μH
fo = 468 kHz
Wire = 0.07 mm diameter
Coil type 7P-TOKO
Material 7MCS

Fig.8 AM IF coil (L2). TOKO sample no. 7MCS-7P.



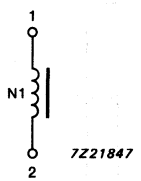
N1 = 86
N2 = 11
Lprim = 270 μH
Wire = 0.07 mm diameter
Coil type 7P-TOKO
Material 7BRS

Fig.9 Oscillator coil (L3). TOKO sample no. 7BRS-7P.



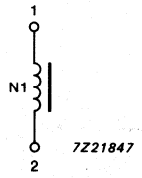
N1 = 11
N2 = 2
C = 85 pF (internal)
fo = 10.7 MHz

Fig.10 FM IF coil (L5). TOKO equivalent no. 119ACS-30120M.



N1 = 1.5
L = 0.03 μH

Fig.11 Oscillator coil (L6). TOKO equivalent no. 301SN-0100.



N1 = 2.5
L = 0.05 μH

Fig. 12 FM RF coil (L7). TOKO equivalent no. 301SN-0200.

Ferroceptor coil

L4: N1 = 105; N2 = 10; L = 625 μH

Ceramic Filters

AM IF (K1). SFZ468 HL.
FM IF (K2). SFE10 . 7 MS2.
FM detector (K3). CDA10 . 7 MC1.

Tuning capacitors

AM 140/82 pF
FM 2 x 20 pF

APPLICATION INFORMATION (continued)

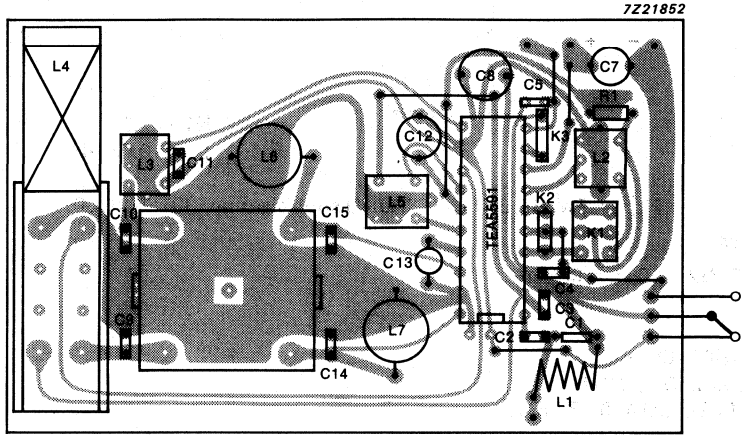


Fig.13 Printed-circuit board component side, showing component layout. For circuit diagram see Fig.6.

Physical dimensions of the printed circuit board = 5.0 x 8.1 cm.

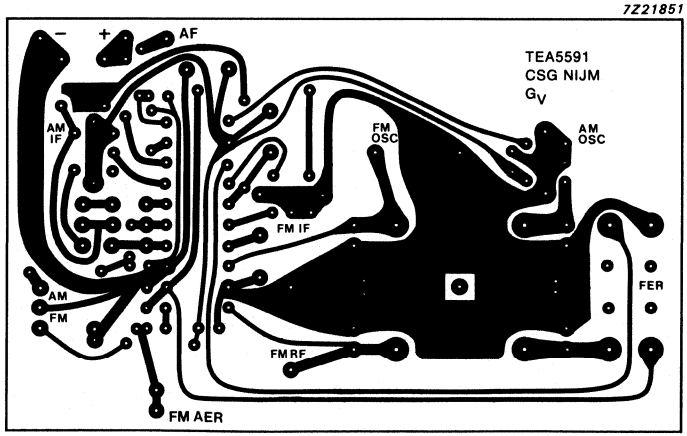


Fig.14 Printed-circuit board showing track side.

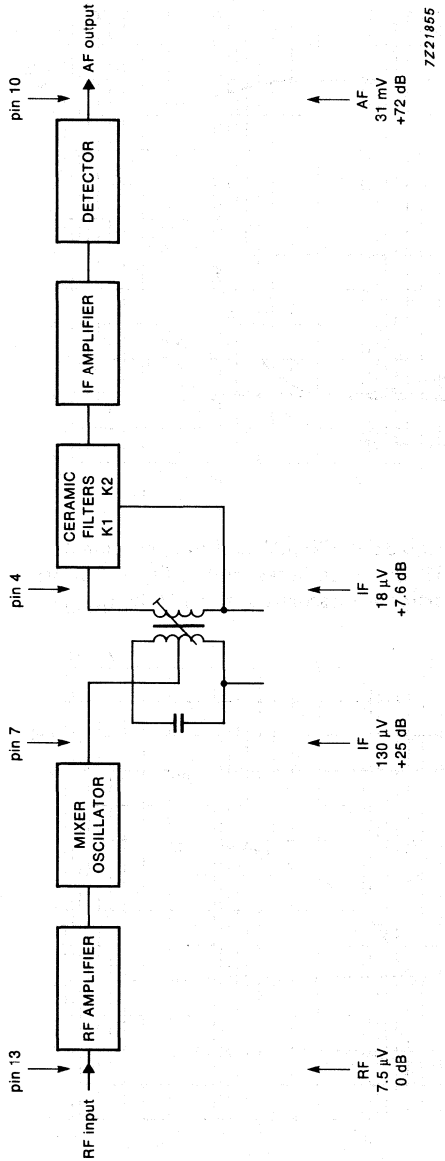


Fig.15 AM signal levels.

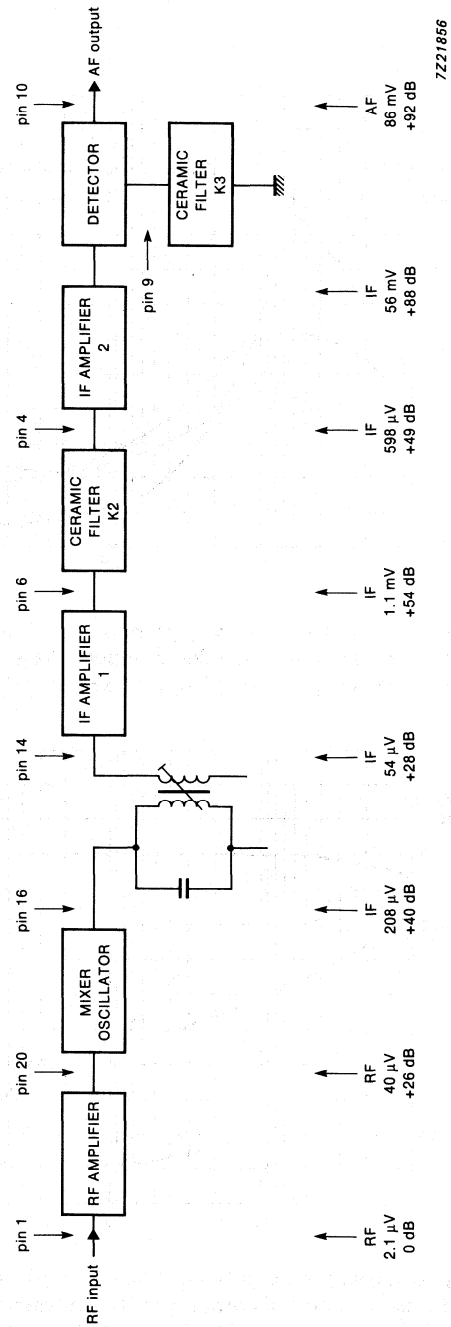


Fig.16 FM signal levels.

APPLICATION INFORMATION (continued)

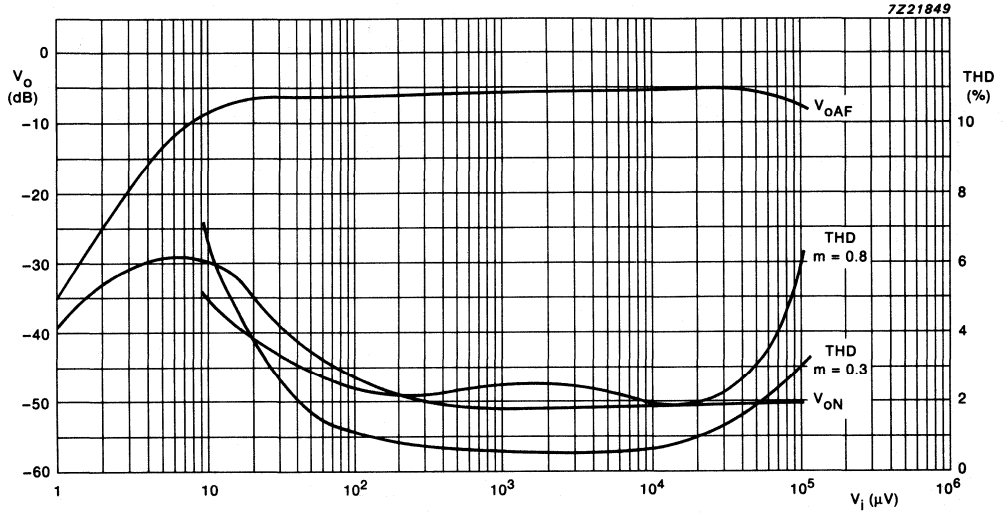


Fig.17 Signal and noise (V_{oAF}), noise (V_{oN}); reference level 0 dB = 100 mV, and total harmonic distortion (THD) as a function of input voltage (V_i) at pin 13. Measured in test circuit Fig.5. AM AGC is measured at f_i = 1 MHz; f_{mod} = 1 kHz; m = 0.3. AM distortion is measured at f_i = 1 MHz; f_{mod} = 1 kHz.

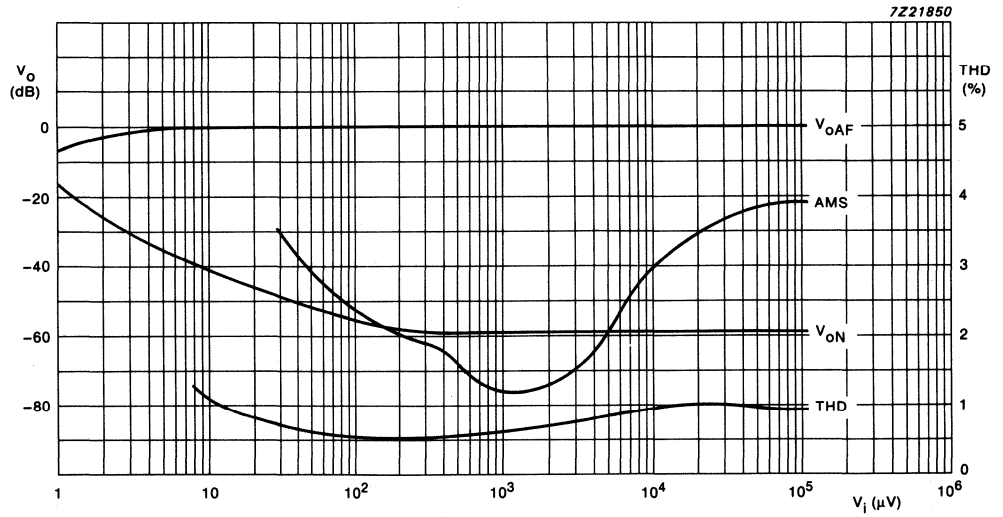


Fig.18 Signal and noise (V_{oAF}), noise (V_{oN}); reference level 0 dB = 100 mV; AM suppression (AMS) and total harmonic distortion (THD) as a function of input voltage (V) at pin 1. Measured in test circuit Fig.5 at f_i = 98 MHz; f_{mod} = 1 kHz; Δf 22.5 kHz. AM suppression is measured at f_{mod} = 400 Hz, m = 0.3 for AM; f_{mod} = 1 kHz, Δf = 75 kHz for FM.

AM/FM RADIO RECEIVER CIRCUIT

GENERAL DESCRIPTION

The TEA5591A is a 24-pin integrated radio circuit, derived from the TEA5591 and is designed for use in AM/FM portable radios and clock radios. The TEA5591A differs from the TEA5591 in that it has:

- Separate IF input pins for AM and FM
- A split-up AM-IF stage (for distributed selectivity)
- An LED driver indicator

The main advantage of the TEA5591A is its ability to operate over a wide range of supply voltages (1.8 to 15 V) without any loss of performance.

The AM circuit incorporates:

- A double balanced mixer
- A 'one-pin' oscillator with amplitude control operating in the 0.6 to 30 MHz frequency range
- A split-up IF amplifier
- A detector
- An AGC circuit which controls the IF amplifier and mixer.

The FM circuit incorporates:

- An RF input amplifier
- A double balanced mixer
- A 'one pin' oscillator
- Two IF amplifiers (for distributed selectivity)
- A quadrature demodulator for a ceramic filter
- Internal AFC

Features

- LED AM/FM indicator
- A DC AM/FM switch facility
- Three separate stabilizers to enable operation over a wide range of supply voltages (1.8 to 15 V)
- All pins (except pin 10) are ESD protected

PACKAGE OUTLINE

24-lead shrink DIL; plastic (SOT234).

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage (pin 8)		V_P	1.8	–	15	V
Total current consumption						
AM part		I_P	–	14	–	mA
FM part		I_P	–	17	–	mA
Operating ambient temperature range		T_{amb}	−15	–	+60	°C
AM performance (pin 1)	note 1					
Sensitivity	V_o = 10 mV	V_i	–	3.5	–	μV
	(S + N)/N = 26 dB	V_i	–	17	–	μV
Signal-to-noise ratio	V_i = 1 mV	(S + N)/N	–	48	–	dB
AF output voltage		V_o	–	45	–	mV
Total harmonic distortion		THD	–	0.7	–	%
Signal handling	m = 80%; THD = 8%	V_i	–	100	–	mV
FM performance (pin 2)	note 2					
Limiting sensitivity	−3 dB	V_i	–	2.3	–	μV
Signal-to-noise ratio	V_i = 2.5 μV	(S + N)/N	–	26	–	dB
	V_i = 1 mV	(S + N)/N	–	60	–	dB
AF output voltage		V_o	–	90	–	mV
Total harmonic distortion		THD	–	0.8	–	%
Signal handling		V_i	–	100	–	mV
AM suppression	100 μV < V_i < 100 mV	AMS	–	40	–	dB

Notes to the quick reference data

1. All parameters are measured in the application circuit (see Fig.4) at nominal supply voltage V_P = 3 V; T_{amb} = 25 °C; unless otherwise specified. RF conditions: Input frequency 1 MHz; 30% modulated with f_{mod} = 1 kHz; unless otherwise specified.
2. All parameters are measured in the application circuit (see Fig.4) at nominal supply voltage V_P = 3 V; T_{amb} = 25 °C; unless otherwise specified. RF conditions: Input frequency 100 MHz; frequency deviation Δf = 22.5 kHz and f_{mod} = 1 kHz; unless otherwise specified.

DEVELOPMENT DATA

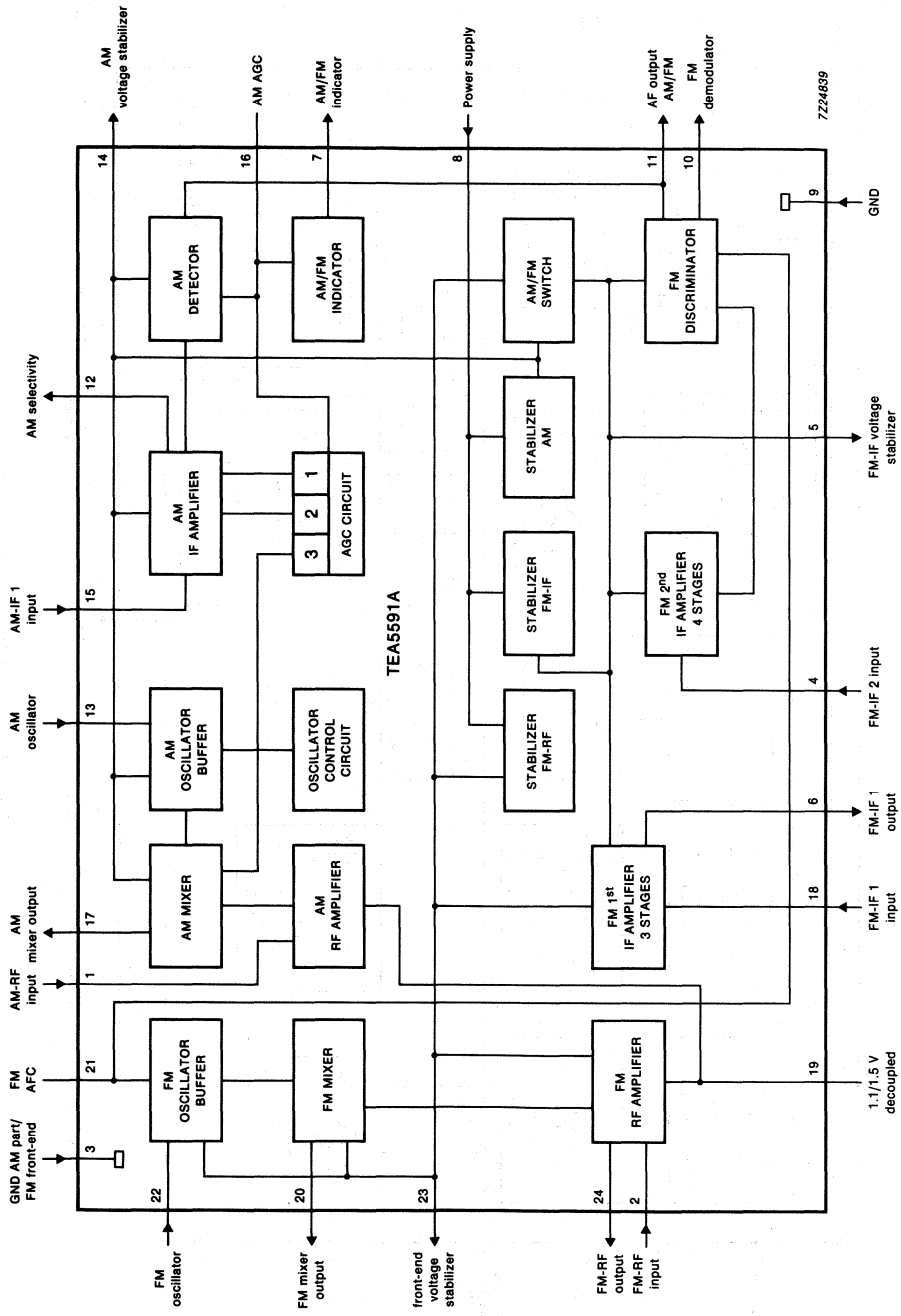


Fig.1 Block diagram.

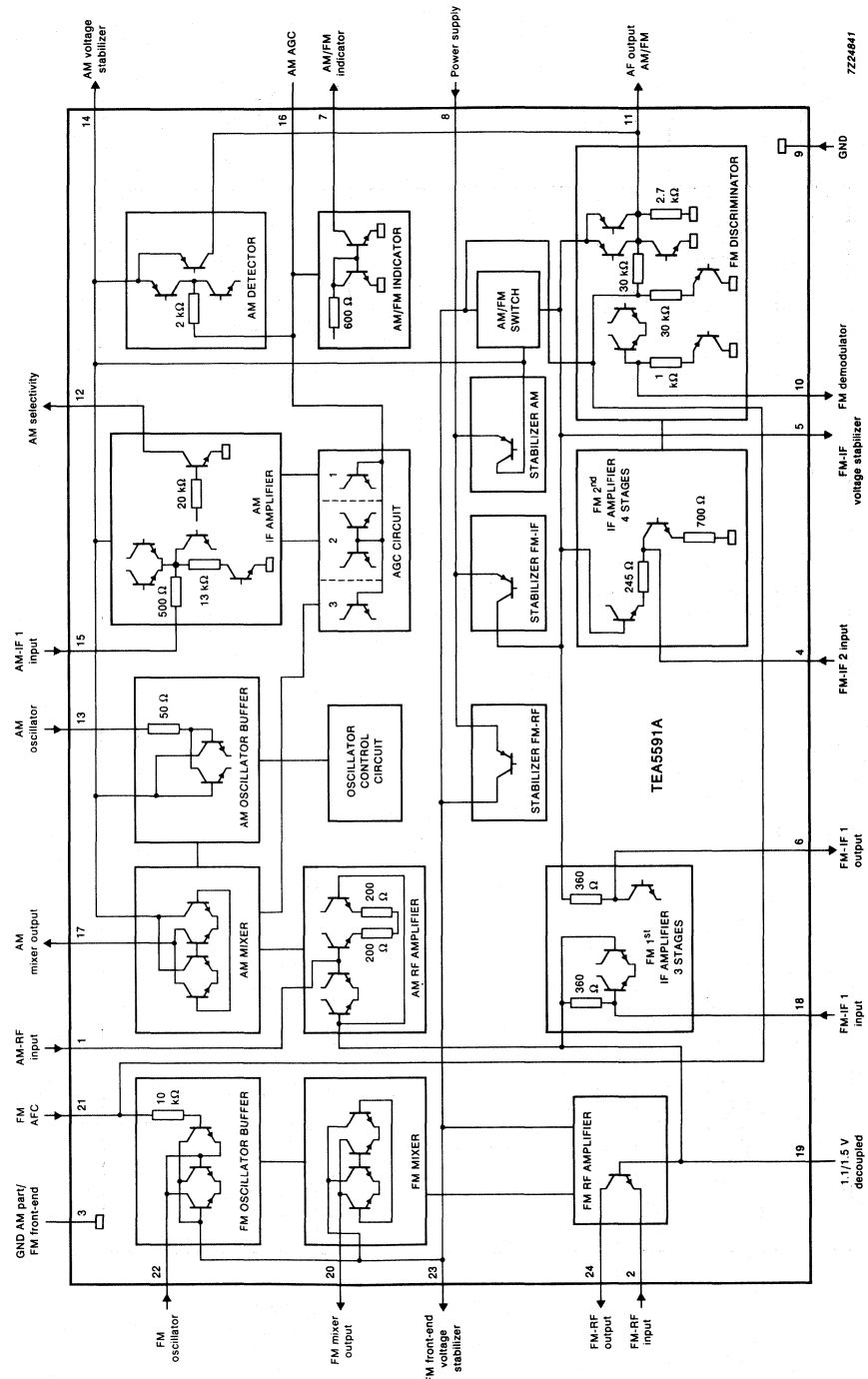


Fig.2 Equivalent circuit diagram.

PINNING

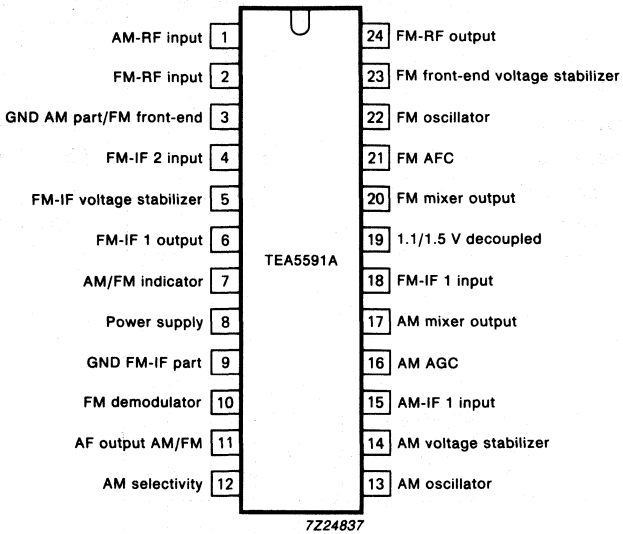


Fig.3 Pinning diagram.

DEVELOPMENT DATA

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage (pin 8)		V_P	–	18	V
LED current (pin 7)		I_7	–	*	mA
Total power dissipation		P_{tot}	see Fig.4		
Storage temperature range		T_{stg}	−65	+150	°C
Operating ambient temperature range		T_{amb}	−15	+60	°C
Electrostatic handling**		V_{es}	−1000	+1000	V

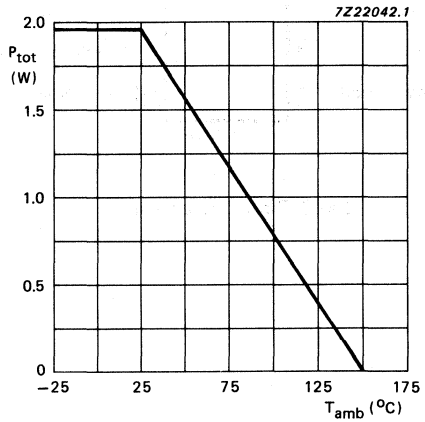


Fig.4 Power derating curve.

* Value to be fixed.

** Equivalent to discharging a 100 pF capacitor through a 1500 Ω series resistor.

DC CHARACTERISTICS

All voltages are referenced to pin 3 and pin 9; all input currents are positive; all parameters are measured in test set-up (see Fig.6) at nominal supply voltage V_P = 3 V; T_{amb} = 25 °C unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage		V_P	1.8	3.0	15	V
Voltages (FM)						
pin 2		V_2	–	0.90	–	V
pin 4		V_4	–	0.85	–	V
pin 5		V_5	–	1.60	–	V
pin 6		V_6	–	1.48	–	V
pin 10		V_{10}	–	1.05	–	V
pin 18		V_{18}	–	1.60	–	V
pin 19		V_{19}	–	1.58	–	V
pin 21		V_{21}	–	0.69	–	V
pin 23		V_{23}	–	1.60	–	V
Voltages (AM)						
pin 14		V_{14}	–	1.60	–	V
pin 16		V_{16}	–	1.54	–	V
pin 19		V_{19}	–	1.10	–	V
Total current consumption	note 1					
AM part		I_P	–	14	19	mA
FM part		I_P	–	17	23	mA

Note to the DC characteristics

1. Without LED current.

DEVELOPMENT DATA

AC CHARACTERISTICS

All parameters are measured in test set-up (see Fig.6) at nominal supply voltage V_P = 3 V; T_{amb} = 25 °C unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
AM part						
AM front end (pin 1 to 17)	note 1					
Conversion transconductance	V_i = 10 mV V_{AGC} (pin 16) = V_{14} − 0.1 V	S_C	9.3	12	13.5	mA/V
	V_i = 10 mV V_{AGC} (pin 16) = V_{14} − 0.45 V	S_C	0.75	1.1	1.3	mA/V
IF suppression	note 2 V_i = 10 mV	α	20	26	–	dB
Oscillator (pin 13)						
Voltage	f = 1.5 MHz	V_{osc}	110	175	200	mV
	f = 1.5 MHz V_P = 1.5 V	V_{osc}	60	160	–	mV
IF and detector part (pin 15 to 11)	note 3					
IF sensitivity; AF output voltage	no AGC; V_i = 45 μV	V_o	12	20	55	mV
Signal + noise to noise ratio for an IF input	no AGC; V_i = 45 μV	S+N/N	23	25	–	dB
AF output voltage	V_i = 1 mV	V_o	35	45	60	mV
Total harmonic distortion	V_i = 10 mV m = 80%	THD	–	1	2.2	%
LED-indicator circuit (pin 7)						
Output current	V_i = 0 V	I_{ind}	–	*	*	μA
	V_i = 1 mV	I_{ind}	*	*	–	mA
Overall performance (pin 1 to 11)	note 4					
Total harmonic distortion	V_i = * mV	THD	–	4.5	8	%

* Value to be fixed.

parameter	conditions	symbol	min.	typ.	max.	unit
FM part						
FM front end (pin 2 to 20)	note 5					
Conversion transconductance	V_i = 1 mV	S_C	7.5	11	13.5	mA/V
Oscillator (pin 22)						
Voltage	V_{AFC} (pin 21) = 0.8 V	V_{osc}	155	200	245	mV
	V_{AFC} = 0.8 V; V_P = 1.5 V	V_{osc}	60	120	–	mV
AFC control; change in oscillator frequency	V_{AFC} = 0.8 V	f	–	111.2	–	MHz
	ΔV_{AFC} = –0.6 V	Δf	–	+420	–	kHz
	ΔV_{AFC} = +0.6 V	Δf	–	–620	–	kHz
IF and demodulator part (pin 18 to 11)	note 6					
IF sensitivity; AF output voltage	note 7; V_i = 100 μV	V_o	–3	–1	0	dB
Signal + noise to noise ratio for an IF input	V_i = 100 μV; out of limiting	S+N/N	26	30	–	dB
AF output voltage	V_i = 1 mV	V_o	75	90	120	mV
Total harmonic distortion	Δf = 75 kHz; V_i = 50 mV	THD	–	3	–	%
LED-indicator circuit (pin 7)						
Output current	V_i = 0 V	I_{ind}	–	–	20	μA
	V_i = 1 mV	I_{ind}	0.6	1	1.9	mA

DEVELOPMENT DATA

Notes to the AC characteristics

1. Input frequency = 1 MHz; output frequency = 468 kHz.
2. $\alpha = \frac{(V_o \text{ at } f_i = 1 \text{ MHz})}{(V_o \text{ at } f_i = 468 \text{ kHz})}$
3. Input frequency = 468 kHz; m = 30% modulated with f_{mod} = 1 kHz; unless otherwise specified.
4. Front-end connected to IF plus detector part. Input frequency = 1 MHz; m = 80% modulated with f_{mod} = 1 kHz.
5. Input frequency = 100 MHz; output frequency = 10.7 MHz.
6. Input frequency = 10.7 MHz; frequency deviation, Δf = 22.5 kHz and f_{mod} = 1 kHz; unless otherwise specified.
7. Reference: AF output voltage = 0 dB at V_i = 1 mV.

APPLICATION AND TEST INFORMATION

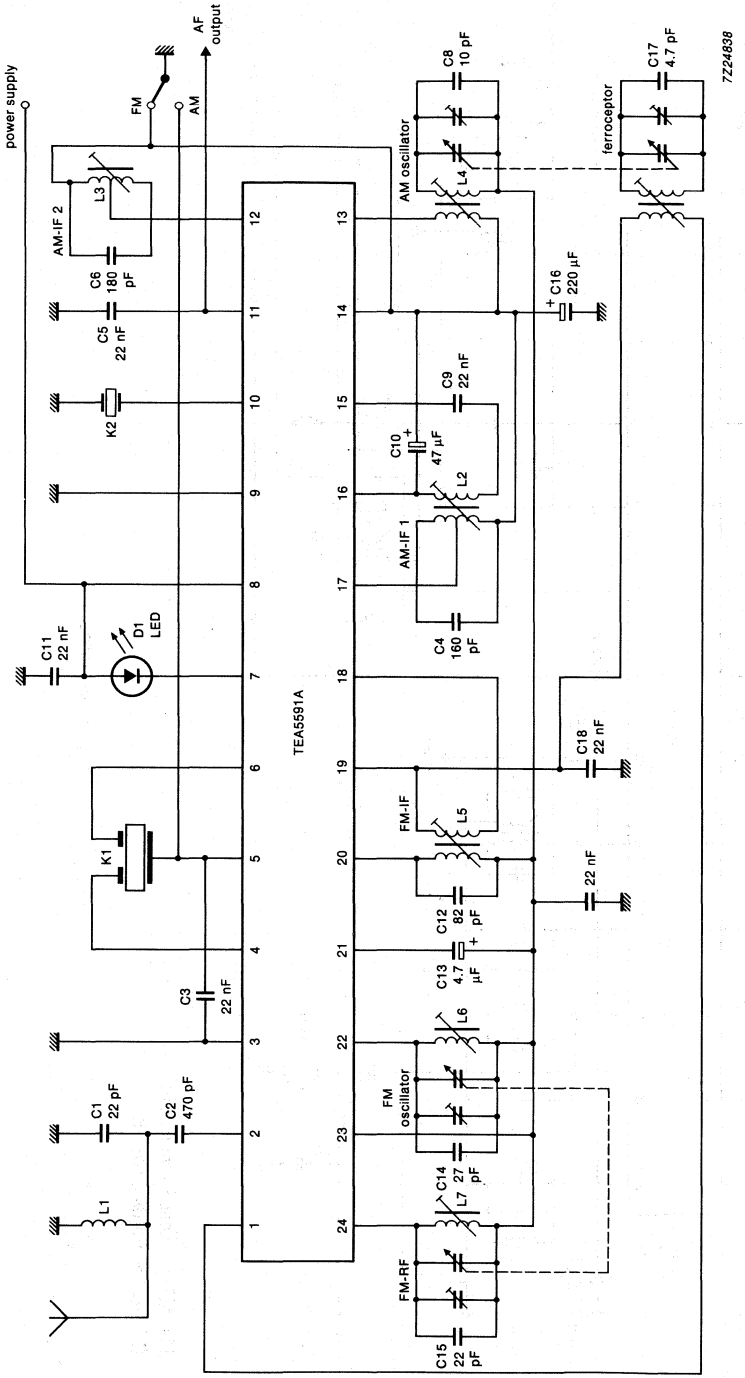


Fig.5 Application circuit.

DEVELOPMENT DATA

APPLICATION AND TEST INFORMATION (continued)

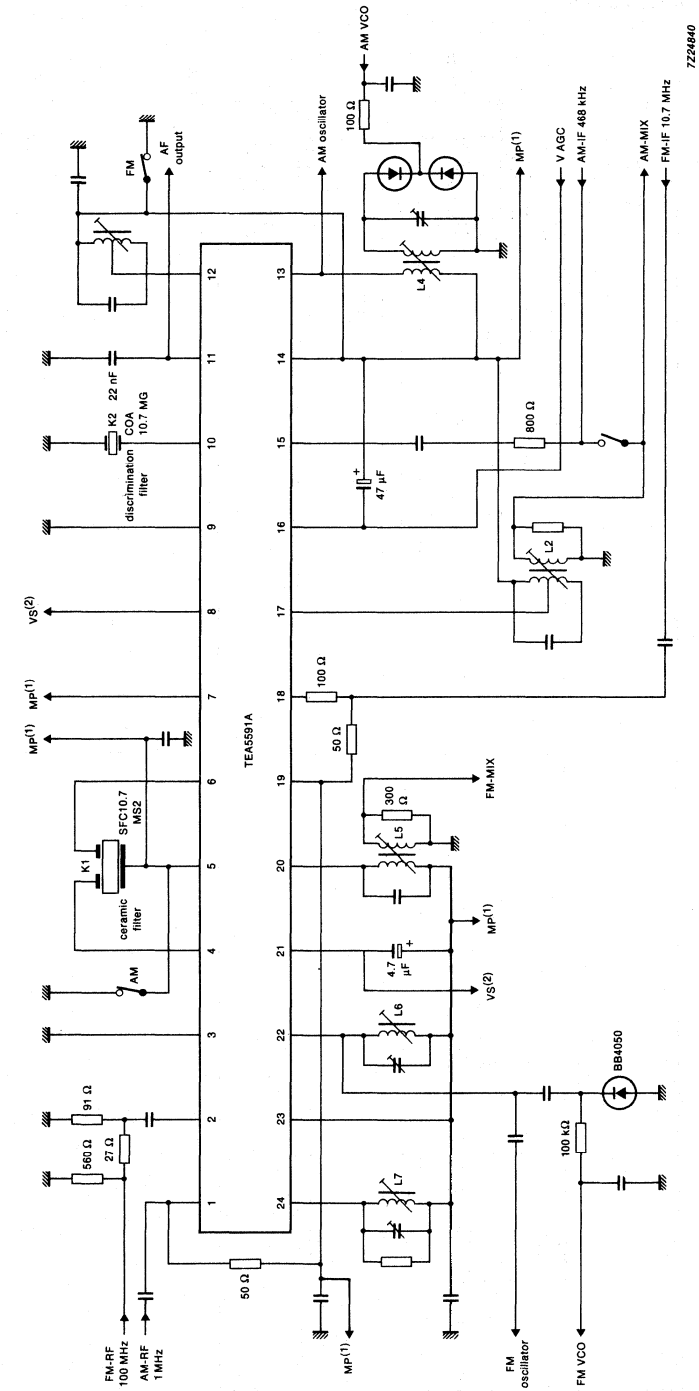


Fig.6 Test circuit.

(1) MP = measurement pin.
(2) VS = voltage source.

AM/FM RADIO RECEIVER CIRCUIT

GENERAL DESCRIPTION

The TEA5592 is a 24-pin integrated radio circuit designed for use in all personal audio and car radio sets especially those sets with in- and out-door aerials that have to fulfill the FTZ (Amtsblatt) requirements.

The AM-IF and FM-IF stages are designed for the application of lumped selectivity. The main advantage of the TEA5592 is its ability to operate over a wide range of supply voltages (2.7 to 15 V) without any loss in performance.

The AM circuit incorporates:

- A double balanced mixer
- A 'one-pin' oscillator with amplitude control operating in the 0.6 to 30 MHz frequency range
- An IF amplifier and AM detector
- An AGC circuit which controls the IF amplifier and mixer

The FM circuit incorporates:

- A front-end (designed for FTZ (Amtsblatt) radio sets)
- A 5-stage IF amplifier
- A quadrature demodulator for a ceramic filter
- Internal AFC

Features

- Low distortion on FM
- AM/FM level/indicator circuit
- A DC AM/FM switch facility
- Three separate stabilizers to enable operation over a wide range of supply voltages (2.7 to 15 V)
- All pins are ESD protected

PACKAGE OUTLINE

24-lead shrink DIL; plastic (SOT234).

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage (pin 5)		V_P	2.7	–	15	V
Total current consumption						
AM part		I_P	–	13	–	mA
FM part		I_P	–	17	–	mA
Operating ambient temperature range		T_{amb}	−40	–	+85	°C
AM performance (pin 13)	note 1					
Sensitivity	V_o = 10 mV	V_i	–	1.5	–	μV
	(S+N)/N = 26 dB	V_i	–	15	–	μV
Signal-to-noise ratio	V_i = 1 mV	(S+N)/N	–	48	–	dB
AF output voltage		V_o	–	55	–	mV
Total harmonic distortion		THD	–	0.8	–	%
Signal handling	m = 80%; THD = 8%	V_i	–	100	–	mV
FM performance (pin 22)	note 2					
Limiting sensitivity	−3 dB	V_i	–	1.8	–	μV
Signal-to-noise ratio	V_i = 2.5 μV	(S+N)/N	–	26	–	dB
	V_i = 1 mV	(S+N)/N	–	60	–	dB
AF output voltage		V_o	–	110	–	mV
Total harmonic distortion		THD	–	0.1	–	%
Maximum signal handling		V_i	–	200	–	mV
AM suppression	100 μV < V_i < 100 mV	AMS	–	40	–	dB

Notes to the quick reference data

1. All parameters are measured in the application circuit (see Fig. 5) at nominal supply voltage Vp = 6 V; T_{amb} = 25 °C; unless otherwise specified. RF conditions: Input frequency 1 MHz; 30% modulated with f_{mod} = 1 kHz; unless otherwise specified.
2. All parameters are measured in the application circuit (see Fig. 5) at nominal supply voltage Vp = 6 V; T_{amb} = 25 °C; unless otherwise specified. RF conditions: Input frequency 100 MHz; frequency deviation Δf = 22.5 kHz and f_{mod} = 1 kHz; unless otherwise specified.

DEVELOPMENT DATA

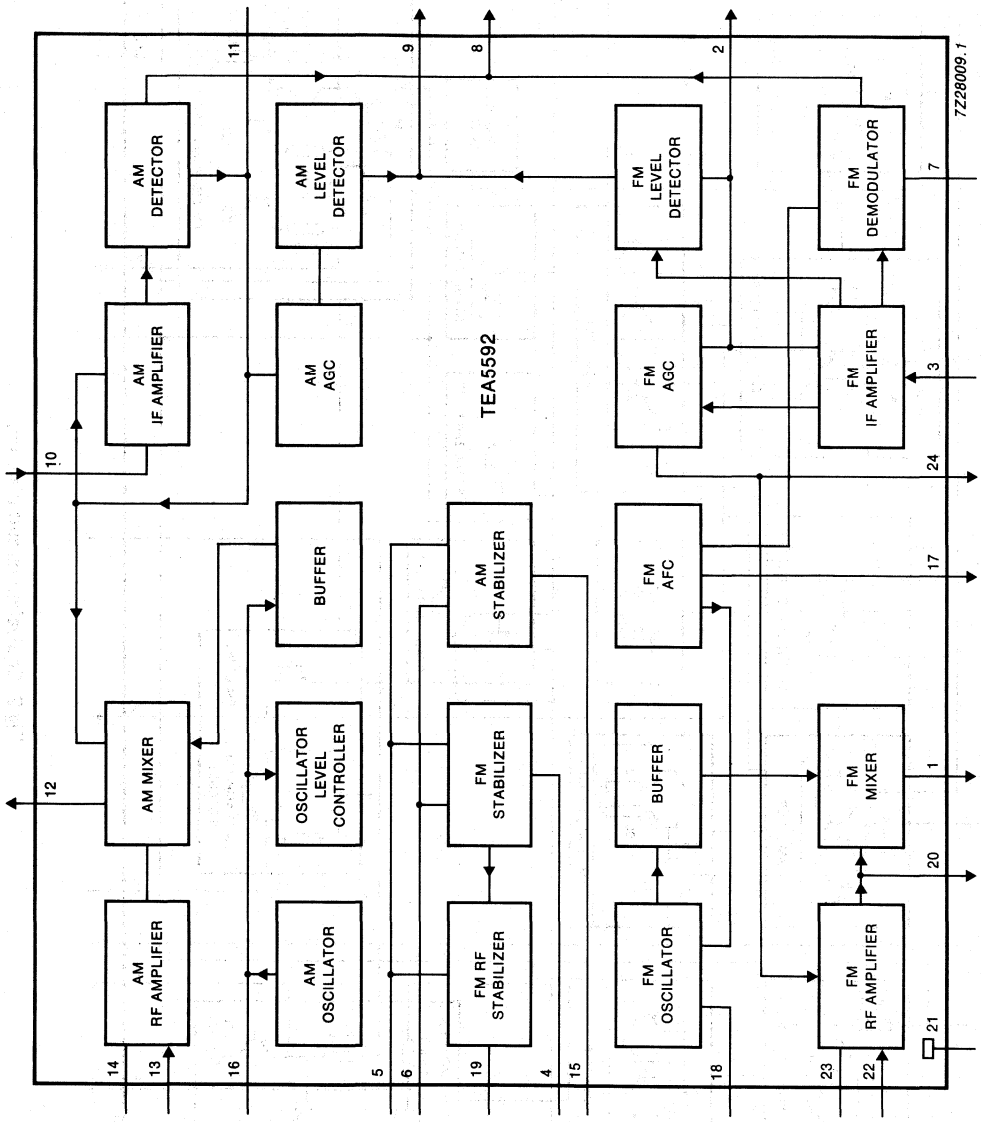


Fig.1 Block diagram.

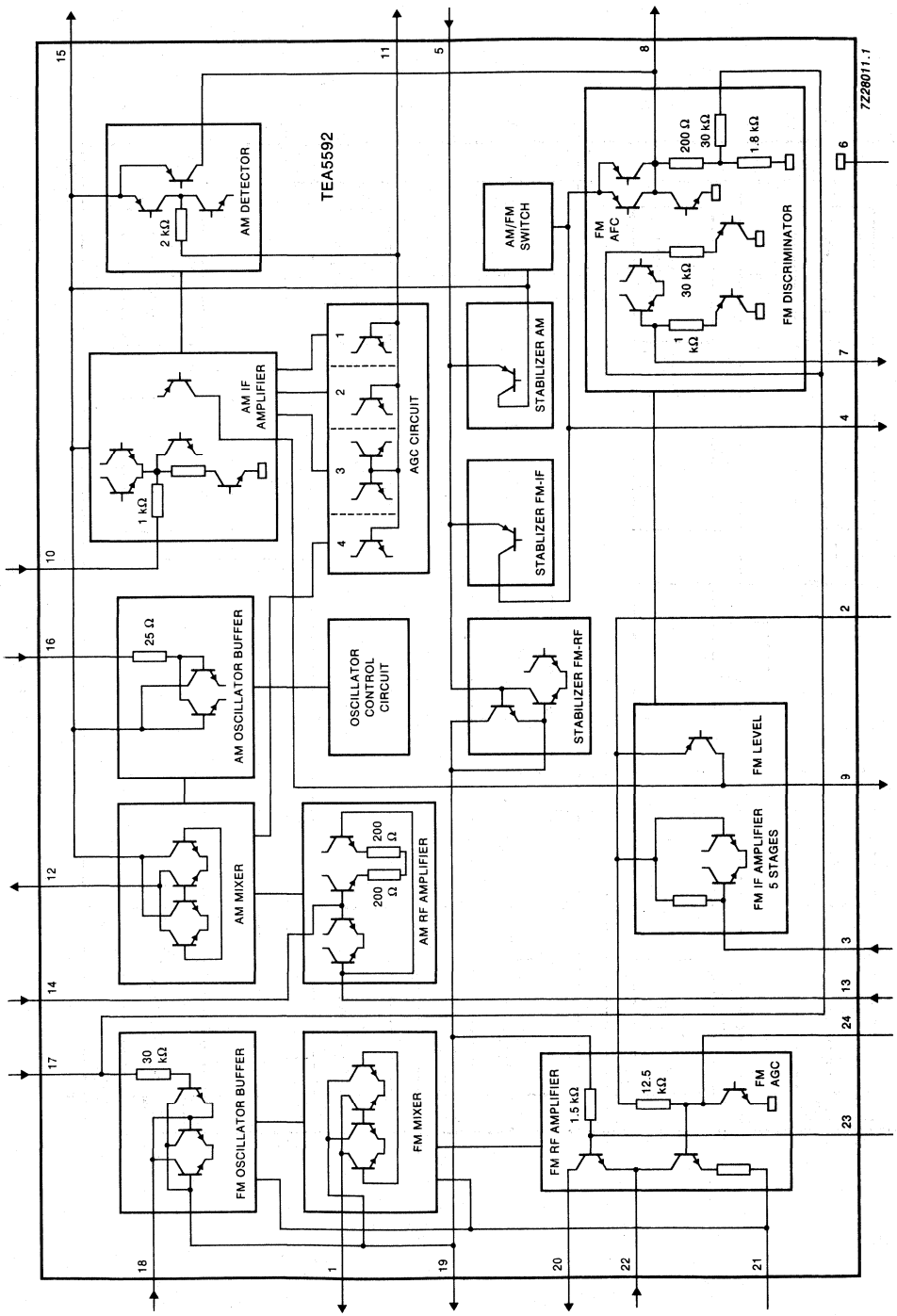


Fig.2 Equivalent circuit diagram.

PINNING

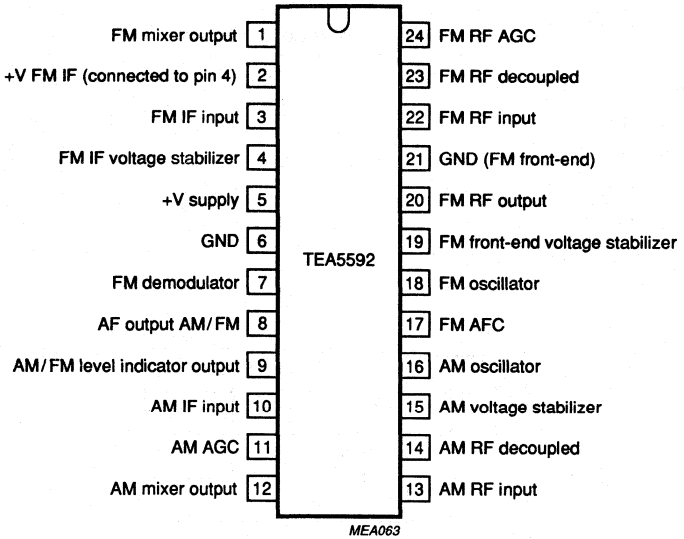


Fig.3 Pinning diagram.

DEVELOPMENT DATA

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage (pin 5)		V_P	–	15	V
Total power dissipation		P_{tot}	see Fig.3		
Storage temperature range		T_{stg}	−65	+150	°C
Operating ambient temperature range		T_{amb}	−40	+85	°C
Electrostatic handling *		V_{es}	−2000	+2000	V

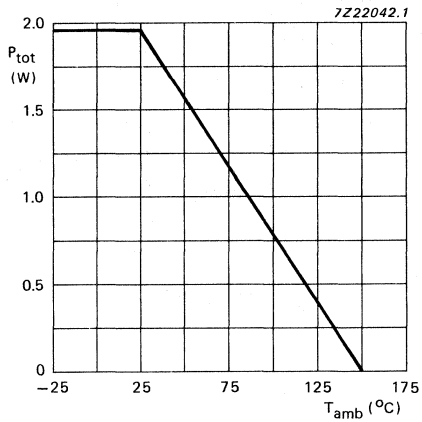


Fig.4 Power derating curve.

* Equivalent to discharging a 200 pF capacitor through a 1.5 kΩ series resistor.

DC CHARACTERISTICS

All voltages are referenced to pin 6 and pin 21; all input currents are positive; all parameters are measured in application circuit (see Fig.5) at nominal supply voltage Vp = 6 V; T_{amb} = 25 °C unless otherwise specified.

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage		V_P	2.7	8.5	15	V
Voltages (FM)						
Pin 2		V_2	–	2.4	–	V
Pin 4		V_4	–	2.4	–	V
Pin 7		V_7	–	1.15	–	V
Pin 8		V_8	–	1.15	–	V
Pin 17		V_{17}	–	0.8	–	V
Pin 19		V_{19}	–	1.6	–	V
Pin 22		V_{22}	–	0.9	–	V
Pin 23		V_{23}	–	1.6	–	V
Pin 24		V_{24}	–	1.0	–	V
Voltages (AM)						
Pin 8		V_8	–	0.2	–	V
Pin 10		V_{10}	–	0.8	–	V
Pins 13 and 14		V_{13}, V_{14}	–	1.1	–	V
Pin 15		V_{15}	–	1.6	–	V
Total current consumption						
AM part		I_P	–	13	19	mA
FM part		I_P	–	17	23	mA

DEVELOPMENT DATA

AC CHARACTERISTICS

All parameters are measured in test circuit (see Fig.11) at nominal supply voltage Vp = 6 V; T_{amb} = 25 °C unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
AM section						
AM front end (pin 13 to 12)	note 1					
Conversion transconductance	V_i = 10 mV V_{AGC} (pin 11) = V_{15} - 0.1 V	S_C	9.1	11.5	14	mA/V
	$V_{AGC} = V_{15}$ - 0.45 V	S_C	0.78	1.1	1.39	mA/V
IF suppression	note 2; V_o = 10 mV	α	20	30	–	dB
Oscillator (pin 16)						
Voltage	f = 1.5 MHz	V_{osc}	110	160	200	mV
	f = 1.5 MHz; V_P = 2.25 V	V_{osc}	60	–	–	mV
IF and detector section (pin 10 to 8)	note 3					
IF sensitivity;						
AF output voltage	no AGC; $V_{i(IF)}$ = 70 μV	V_o	27	40	55	mV
Signal + noise to noise ratio for an IF input	no AGC; $V_{i(IF)}$ = 70 μV	S+N/N	20	26	–	dB
AF output voltage	$V_{i(IF)}$ = 1 mV	V_o	40	55	70	mV
Total harmonic distortion	$V_{i(IF)}$ = 10 mV; m = 80%	THD	–	1	3	%
Indicator/level detector (pin 9)						
Output voltage	$V_{i(IF)}$ = 0 V	V_9	–	–	95	mV
	$V_{i(IF)}$ = 200 μV	V_9	–	200	–	mV
	$V_{i(IF)}$ = 10 mV	V_9	–	450	600	mV
Overall performance (pin 13 to 8)	note 4					
Total harmonic distortion	V_i = 50 mV	THD	–	1.5	4	%

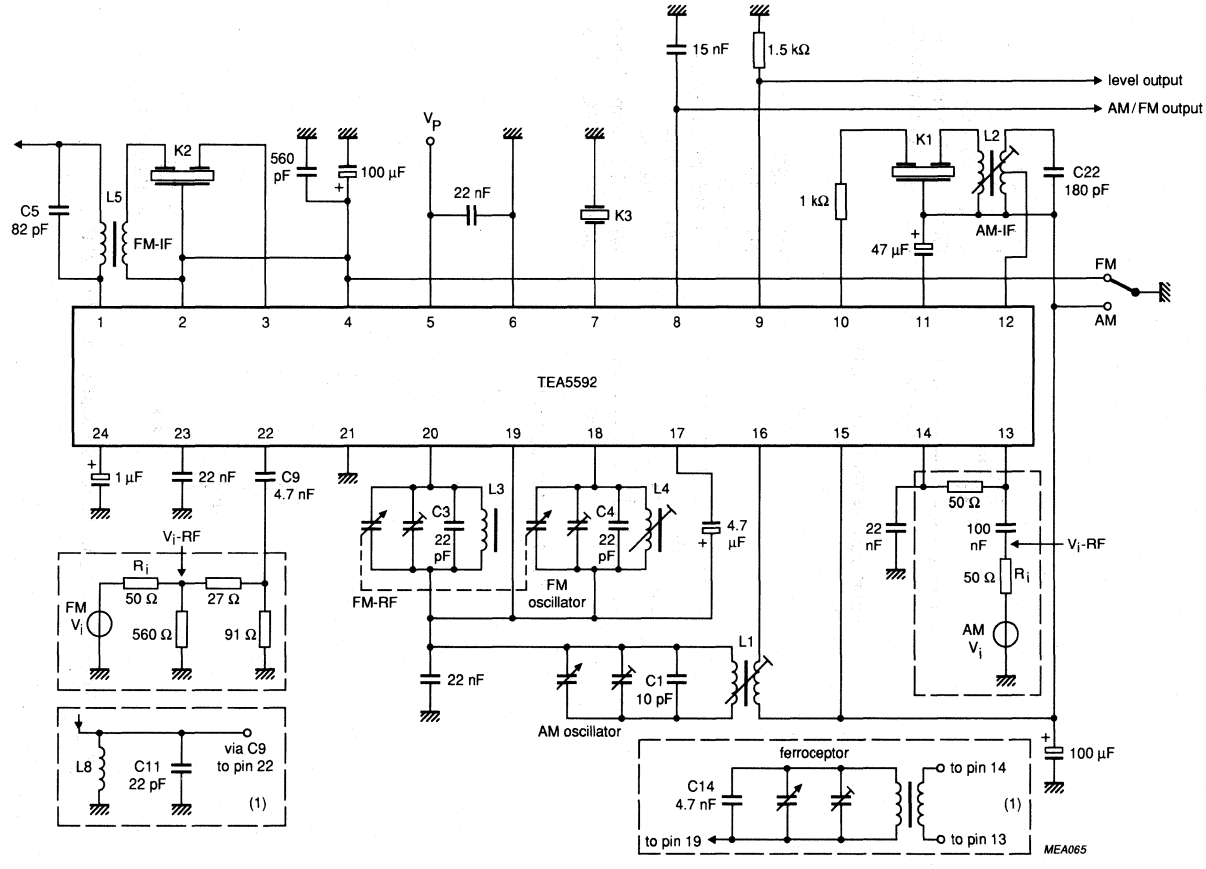
parameter	conditions	symbol	min.	typ.	max.	unit
FM section						
FM front end (pin 22 to 1)	note 5					
Conversion transconductance	V_i = 1 mV; V_{AGC} (pin 24) = 1.1 V	S_c	9	14	19	mA/V
	V_i = 1 mV; V_{AGC} (pin 24) = 0.8 V	S_c	4	8	10	mA/V
Oscillator (pin 18)						
Voltage	V_{AFC} = 0.8 V	V_{osc}	–	–	310	mV
	V_{AFC} = 0.8 V; V_P = 2.25 V	V_{osc}	95	200	–	mV
AFC control; change in oscillator frequency	V_{AFC} (pin 17) = 0.8 V	f	–	111.2	–	MHz
	ΔV_{AFC} = –0.6 V	Δf	–	+420	–	kHz
	ΔV_{AFC} = +0.6 V	Δf	–	–620	–	kHz
IF and demodulator section (pin 3 to 8)	note 6					
IF sensitivity;	note 7					
AF output voltage	$V_{i(IF)}$ = 70 μV	V_o	–3	–1	0	dB
Signal + noise-to-noise ratio for an IF input	$V_{i(IF)}$ = 70 μV no limiting	S+N/N	20	30	–	dB
AF output voltage	$V_{i(IF)}$ = 1 mV	V_o	80	110	130	mV
Total harmonic distortion	Δf = 75 kHz; $V_{i(IF)}$ = 50 mV	THD	–	1	–	%
Indicator/level detector (pin 9)						
Output voltage	$V_{i(IF)}$ = 0 V	V_9	–	–	20	mV
	$V_{i(IF)}$ = 500 μV	V_9	–	260	–	mV
	$V_{i(IF)}$ = 10 mV	V_9	–	550	670	mV

DEVELOPMENT DATA

Notes to the AC characteristics

1. Input frequency = 1 MHz, output frequency = 468 kHz.
2. α = 20 log (V_i at f_i = 468 kHz) / (V_i at f_i = 1 MHz).
3. Input frequency = 468 kHz; m = 30% modulated with f_{mod} = 1 kHz; unless otherwise specified.
4. Front-end connected to IF plus detector part. Input frequency = 1 MHz; m = 80% modulated with f_{mod} = 1 kHz.
5. Input frequency = 100 MHz; output frequency = 10.7 MHz.
6. Input frequency = 10.7 MHz; frequency deviation, Δf = 22.5 kHz and f_{mod} = 1 kHz; unless otherwise specified.
7. Reference: AF output voltage = 0 dB at V_i = 1 mV.

APPLICATION AND TEST INFORMATION



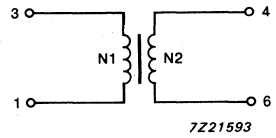
(1) In application the input circuits can be replaced by ferroceptor and aerial input circuit.

Fig. 5 Application circuit.

APPLICATION AND TEST INFORMATION (continued)

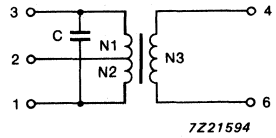
Component data

COILS



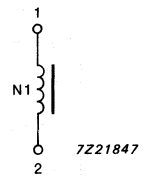
N1 = 86
N2 = 11
Lprim = 270 μH
Wire = 0.07 mm diameter
Coil type TOKO 7BRS

Fig.6 AM oscillator coil (L1).



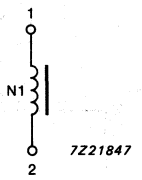
N1 = 135
N2 = 13
N3 = 5
C = 180 pF (internal)
Lprim = 660 μH
f_o = 468 kHz
Wire = 0.07 mm diameter
Coil type TOKO 7MCS

Fig.7 AM-IF coil (L2).



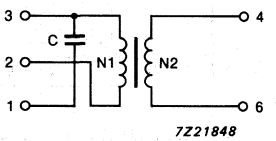
N1 = 2.5
L = 0.066 μH

Fig.8 FM-RF coil (L3). TOKO equivalent no. 301SN-0200.



N1 = 1.5
L = 0.04 μH

Fig.9 FM oscillator coil (L4). TOKO equivalent no 301SN-0100.



N1 = 11
N2 = 2
C = 82 pF (internal)
f_o = 10.7 MHz

Fig.10 FM-IF coil (L5). TOKO equivalent no. 301-20N

CERAMIC FILTERS

AM-IF (K1). SFU468B.
FM-IF (K2). SFE10.7MS3.
FM detector (K3). CDA10.7MC1.

TUNING CAPACITORS

AM section – 140/82 pF
FM section – 2 x 20 pF

APPLICATION AND TEST INFORMATION (continued)

For coil information see Component data.

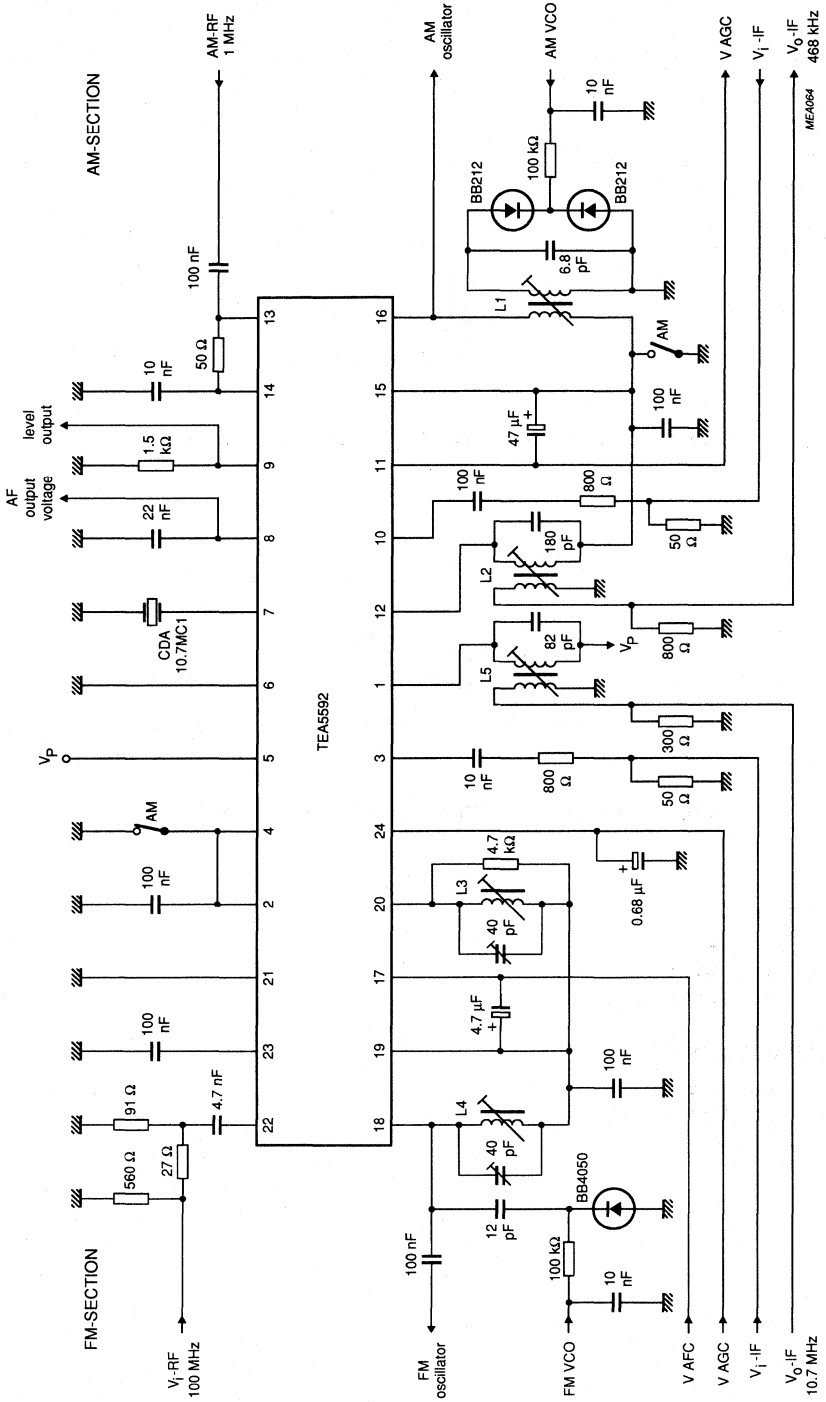


Fig.11 Factory test circuit.

AM/FM RADIO RECEIVER CIRCUIT

GENERAL DESCRIPTION

The TEA5594 is a 32-pin integrated radio circuit designed for use in all Electronic Tuned Radio (ETR) sets especially those sets which have to fulfil the immunity requirements of CENELEC.

The AM circuit incorporates:

- A double balanced mixer
- A 'one-pin' oscillator with amplitude control operating in the LW/MW frequency range
- An IF amplifier and AM detector
- An AGC circuit which controls the IF amplifier and mixer

The FM circuit incorporates:

- A front-end (fulfilling the "out of band" CENELEC requirements)
- Two IF amplifiers (for distributed selectivity)
- A quadrature demodulator with a ceramic filter

The TEA5594 also contains:

- Oscillator output buffers for AM and FM
- A combined AM/FM IF counter output buffer with counter "enable" function
- A field strength level detector for AM and FM
- A soft mute circuit at FM, adjustable
- An extra IF amplifier to split up IF filtering

Features

- Low distortion on FM
- AM/FM level/indicator circuit
- A DC AM/FM switch facility
- Supply voltages 2.7 to 15 V
- A local distance switch facility (LOCAL-DX) at FM
- All pins are ESD protected

PACKAGE OUTLINE

32-lead shrink DIL; plastic (SOT232).

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage (pin 9)		V_P	2.7	–	15	V
Total current consumption						
AM part		I_P	–	13	–	mA
FM part		I_P	–	24	–	mA
Operating ambient temperature range		T_{amb}	−40	–	+85	°C
AM performance (pin 22)	note 1					
Sensitivity	V_o = 10 mV	V_i	–	3.5	–	μV
	(S+N)/N = 26 dB	V_i	–	16	–	μV
Signal-to-noise ratio	V_i = 1 mV	(S+N)/N	–	48	–	dB
AF output voltage		V_o	–	50	–	mV
Total harmonic distortion		THD	–	0.8	–	%
Signal handling	m = 80%; THD = 8%	V_i	–	100	–	mV
FM performance (pin 30)	note 2					
Limiting sensitivity	−3 dB; note 3	V_i	–	2.5	–	μV
Signal-to-noise ratio	V_i = 3 μV	(S+N)/N	–	26	–	dB
	V_i = 1 mV	(S+N)/N	–	60	–	dB
AF output voltage		V_o	–	90	–	mV
Total harmonic distortion		THD	–	0.1	–	%
Maximum signal handling		V_i	–	200	–	mV
AM suppression	100 μV < V_i < 100 mV	AMS	–	50	–	dB

Notes to the quick reference data

1. All parameters are measured in the application circuit (see Fig.5) at nominal supply voltage V_p = 8.5 V; T_{amb} = 25 °C; unless otherwise specified. RF conditions: Input frequency 1 MHz; 30% modulated with f_{mod} = 1 kHz; unless otherwise specified.
2. All parameters are measured in the application circuit (see Fig.5) at nominal supply voltage V_p = 8.5 V; T_{amb} = 25 °C; unless otherwise specified. RF conditions: Input frequency 100 MHz; frequency deviation Δf = 22.5 kHz and f_{mod} = 1 kHz; unless otherwise specified.
3. Soft mute switched off.

DEVELOPMENT DATA

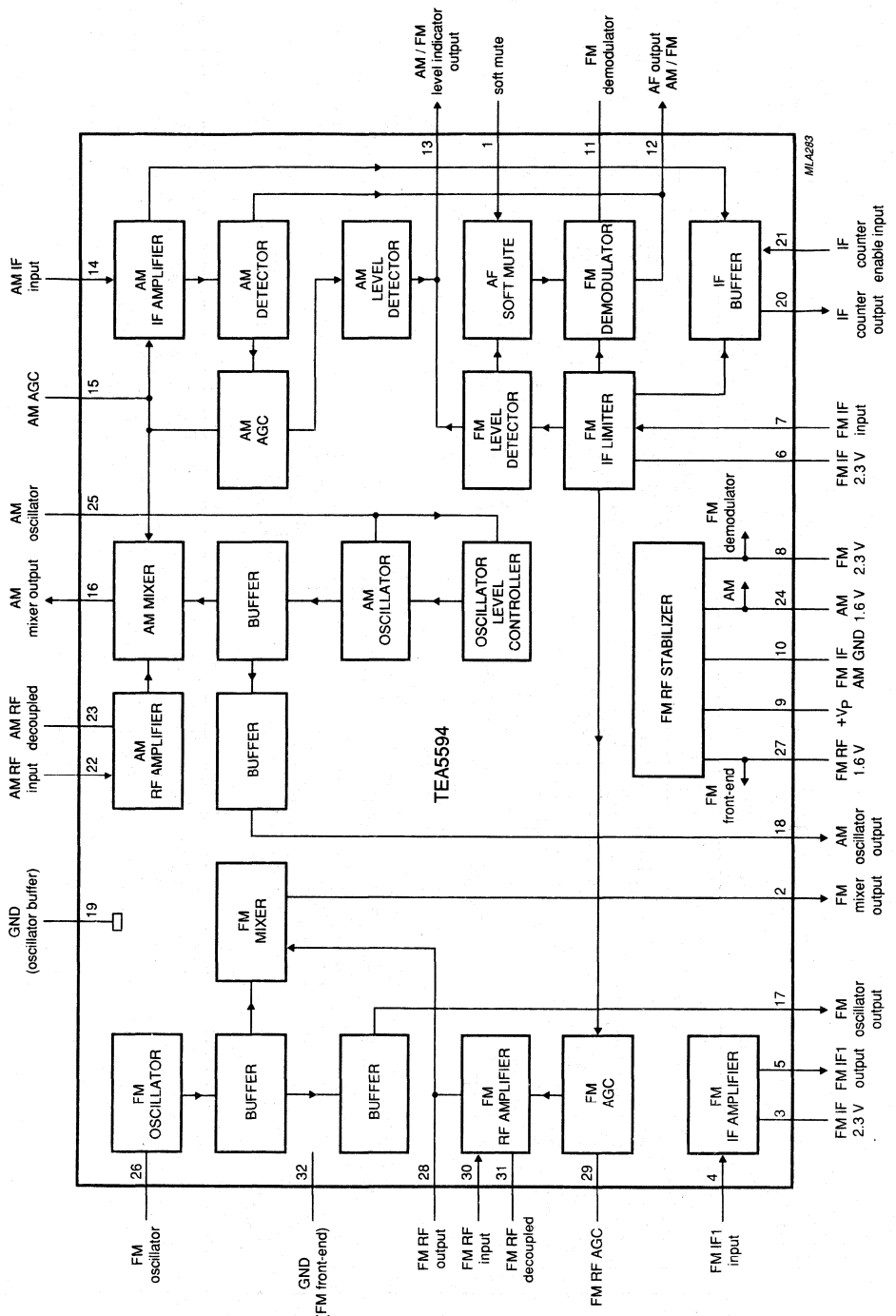


Fig.1 Block diagram.

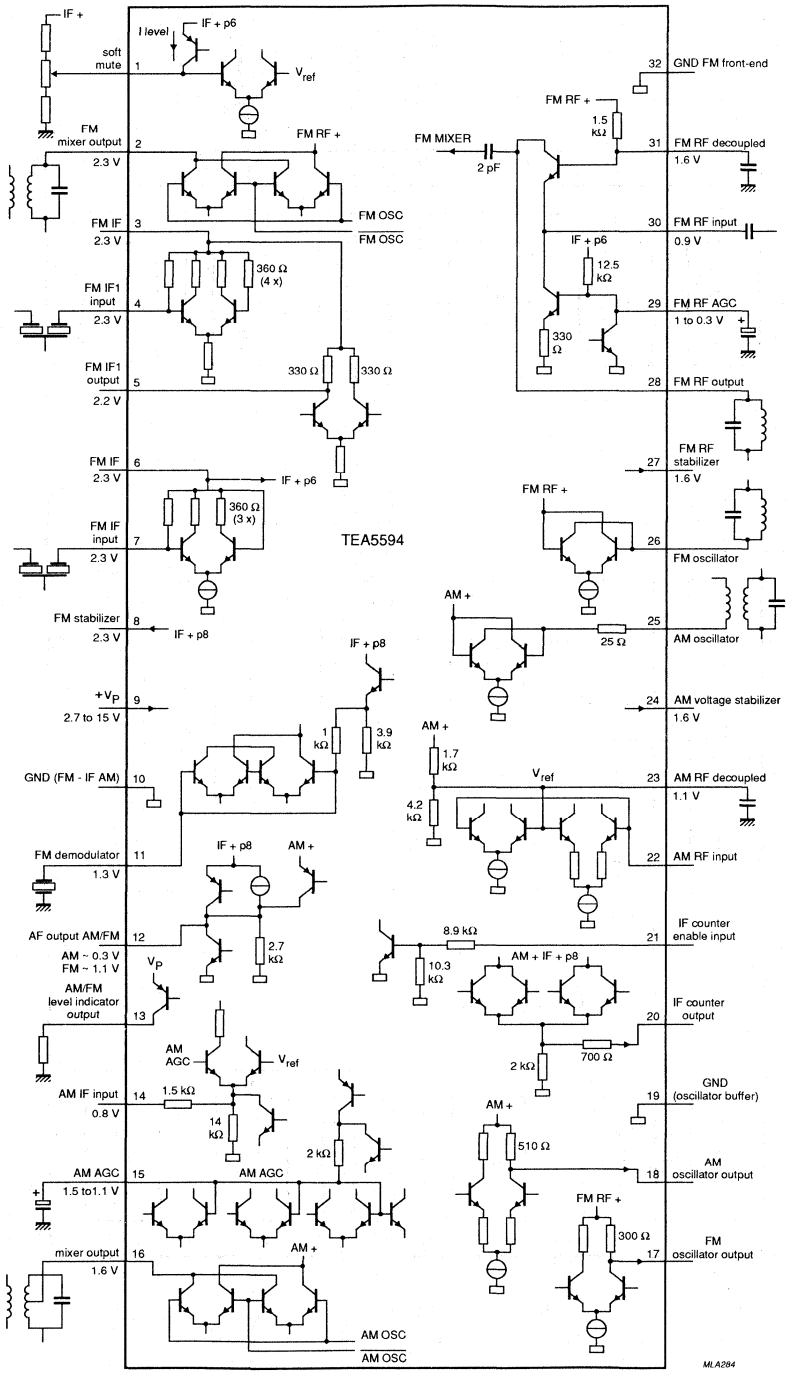


Fig.2 Equivalent circuit diagram.

PINNING

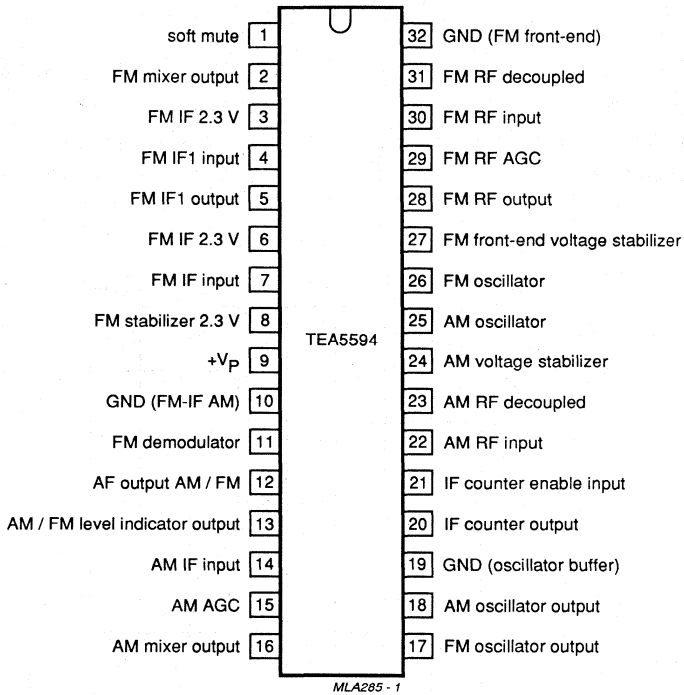


Fig.3 Pinning diagram.

DEVELOPMENT DATA

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage (pin 9)		V_P	–	18	V
Total power dissipation		P_{tot}	see Fig.4		
Storage temperature range		T_{stg}	−65	+ 150	°C
Operating ambient temperature range		T_{amb}	−40	+ 85	°C
Electrostatic handling*		V_{es}	−2000	+ 2000	V

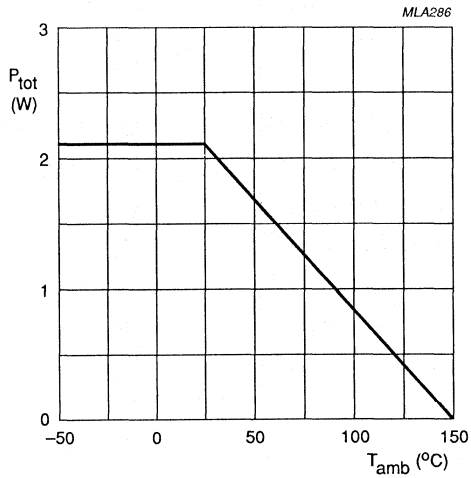


Fig.4 Power derating curve.

* Equivalent to discharging a 200 pF capacitor through a 1.5 kΩ series resistor.

DC CHARACTERISTICS

All voltages are referenced to pin 10, pin 19 and pin 32; all input currents are positive; all parameters are measured in application circuit (see Fig.5) at nominal supply voltage V_P = 8.5 V; T_{amb} = 25 °C unless otherwise specified.

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage		V_P	2.7	8.5	15	V
Voltages (FM)						
Pin 4		V_4	–	2.3	–	V
Pin 5		V_5	–	2.2	–	V
Pin 7		V_7	–	2.3	–	V
Pin 8		V_8	–	2.3	–	V
Pin 12		V_{12}	–	1.15	–	V
Pin 27		V_{27}	–	1.6	–	V
Pin 29		V_{29}	–	1.0	–	V
Pin 30		V_{30}	–	0.9	–	V
Pin 31		V_{31}	–	1.6	–	V
Voltages (AM)						
Pin 12		V_{12}	–	0.2	–	V
Pin 14		V_{14}	–	0.8	–	V
Pin 15		V_{15}	–	1.54	–	V
Pins 22 and 23		V_{22}, V_{23}	–	1.1	–	V
Pin 24		V_{24}	–	1.6	–	V
Total current consumption						
AM part		I_P	–	13	*	mA
FM part		I_P	–	24	*	mA

DEVELOPMENT DATA

* Value to be fixed.

AC CHARACTERISTICS

All parameters are measured in test circuit (see Fig.6) at nominal supply voltage V_P = 6 V; T_{amb} = 25 °C unless otherwise specified.

parameter	conditions	symbol	min.	typ.	max.	unit
AM SECTION						
AM front end	note 1					
Conversion transconductance	V_i = 10 mV V_{AGC} (pin 15) = V_{24} - 0.1 V	S_C	*	13.5	*	mA/V
	$V_{AGC} = V_{24}$ - 0.45 V	S_C	*	1.2	*	mA/V
IF suppression	note 2	α	20	30	–	dB
Oscillator (pin 25)						
Voltage	f = 1.5 MHz	V_{osc}	–	160	*	mV
Oscillator buffer						
Output voltage (peak-to-peak value)		V_{18}	*	140	–	mV
IF and detector part	note 3					
IF sensitivity; AF output voltage	no AGC; $V_{i(IF)}$ = 90 μV	V_o	30	40	60	mV
Signal + noise to noise ratio for an IF input	no AGC; $V_{i(IF)}$ = 90 μV	S+N/N	22	24	30	dB
AF output voltage	$V_{i(IF)}$ = 1 mV	V_o	35	50	70	mV
Total harmonic distortion	$V_{i(IF)}$ = 10 mV; m = 80%	THD	0.75	2	5	%
	$V_{i(IF)}$ = * to * mV; m = 30%	THD	–	*	–	%
Indicator/level detector						
Output voltage	$V_{i(IF)}$ = 0 V	V_{13}	*	560	*	mV
	$V_{i(IF)}$ = 200 μV	V_{13}	*	3200	*	mV
	$V_{i(IF)}$ = 10 mV	V_{13}	*	6600	*	mV

* Value to be fixed.

DEVELOPMENT DATA

parameter	conditions	symbol	min.	typ.	max.	unit
AM IF counter output buffer						
Counter "enable"						
Output voltage (peak-to-peak value)		V_{20}	100	125	–	mV
Counter "disable"						
Suppression of 468 kHz		V_{20}	–40	–	–	dB
Overall performance	note 4					
Total harmonic distortion	$V_{i(RF)}$ = 50 mV	THD	–	–	8	%
Signal handling	THD = * %; m = 0.8%		–	*	–	
Counter enable circuit						
IF counter output OFF		V_{21}	–	–	0.8	V
IF counter output ON		V_{21}	2	–	V_P	V
FM SECTION						
FM front end	note 5					
Conversion transconductance	$V_{i(RF)}$ = 1 mV; V_{AGC} = 1.1 V	S_c	16	24	32	mA/V
	$V_{i(RF)}$ = 1 mV; V_{AGC} = 0.8 V	S_c	5	10	15	mA/V
Oscillator (pin 26)						
Voltage		V_{osc}	–	250	–	mV
Oscillator buffer						
Output voltage (peak-to-peak value)		V_{17}	*	270	–	mV
IF and demodulator part	note 6					
IF sensitivity	note 7					
AF output voltage	$V_{i(IF)}$ = 40 μV no mute	V_o	–3	–1	0	dB
	with mute	V_o	–20	–30	–40	dB
AM suppression	note 8	α	–	*	–	dB
Signal + noise-to-noise ratio for an IF input	no mute; $V_{i(IF)}$ = 40 μV	S+N/N	28	46	50	dB
	$V_{i(IF)}$ = 1 mV	S+N/N	–	*	–	dB
AF output voltage	$V_{i(IF)}$ = 1 mV	V_o	*	85	*	mV
Total harmonic distortion	$V_{i(IF)}$ = 50 mV; Δf = 75 kHz	THD	–	1	–	%
	Δf = 22.5 kHz	THD	–	*	–	%

* Value to be fixed.

AC CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Indicator/level detector						
Output voltage	$V_{i(IF)}$ = 0 V	V_{13}	*	2600	*	mV
	$V_{i(IF)}$ = 50 μV	V_{13}	*	5750	*	mV
	$V_{i(IF)}$ = 1 mV	V_{13}	*	6250	*	mV
AM/FM IF counter output buffer						
Counter "enable"	note 5					
Output voltage (peak-to-peak value)		V_{20}	–	130	–	mV
Counter "disable"						
Suppression of 10.7 MHz		V_{20}	–40	–	–	dB
Counter enable circuit						
IF counter output OFF		V_{21}	–	–	0.8	V
IF counter output ON		V_{21}	2	–	V_P	V
AM/FM switch						
FM OFF/AM ON		$V_{8\text{-}10}$	–	0	0	V
FM ON/AM OFF		$V_{24\text{-}10}$	–	0	0	V

Notes to the AC characteristics

1. Input frequency = 1 MHz, output frequency = 468 kHz;
   $S_c = \frac{V_{o(IF)}}{V_{i(RF)}} \times \frac{N2/N3}{R}$ (see TR2 Component data)
   Where R = 1.2 kΩ (total impedance at pin 16).
2. α = 20 log (V_i at f_i = 468 kHz)/(V_i at f_i = 1 MHz); V_o = 10 mV; no AGC.
3. Input frequency = 468 kHz; m = 30% modulated with f_{mod} = 1 kHz; R_{source} = 800 Ω unless otherwise specified.
4. Front-end connected to IF plus detector part (see Fig.5). Input frequency = 1 MHz; m = 80% modulated with f_{mod} = 1 kHz.
5. Input frequency = 100 MHz; output frequency = 10.7 MHz;
   $S_c = \frac{V_{o(IF)}}{V_{i(RF)}} \times \frac{N1/N2}{R}$ (see TR3 Component data)
   Where R = 6.6 kΩ (total impedance at pin 2).
6. Input frequency = 10.7 MHz; frequency deviation, Δf = 22.5 kHz and f_{mod} = 1 kHz; unless otherwise specified.
7. Reference: AF output voltage = 0 dB at $V_{i(IF)}$ = 1 mV;
   No mute : $V_1 = V_8$;
   With mute : V_1 = 0 V.
8. AM suppression is measured with AM only: m = 0.8% and f_{mod} = 1 kHz referred to AF output at FM only: Δf = 75 kHz and f_{mod} = 1 kHz.

* Value to be fixed.

DEVELOPMENT DATA

APPLICATION AND TEST INFORMATION

For coil information see Component data.

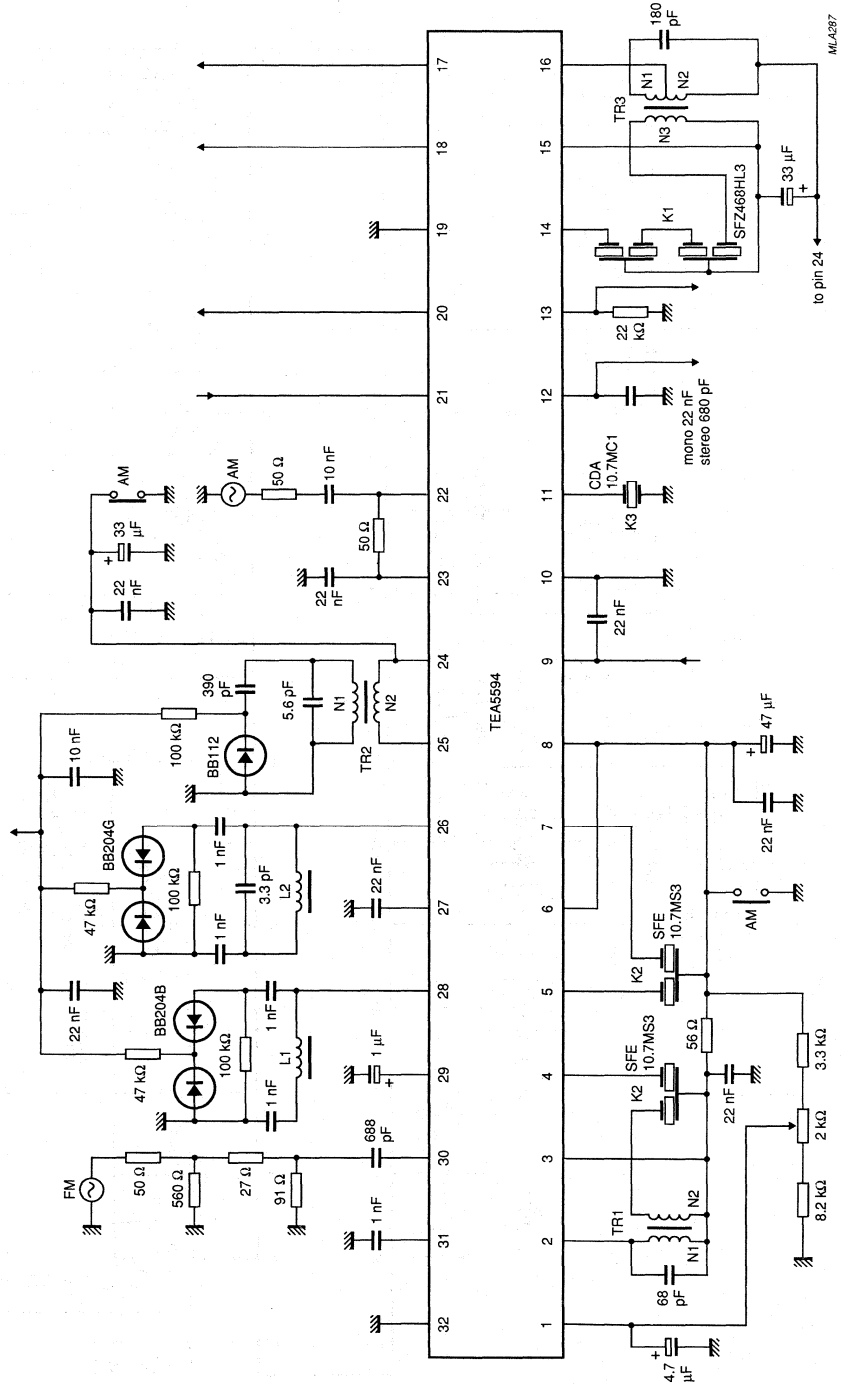


Fig.5 Application circuit for evaluation.

APPLICATION AND TEST INFORMATION (continued)

For coil information see Component data.

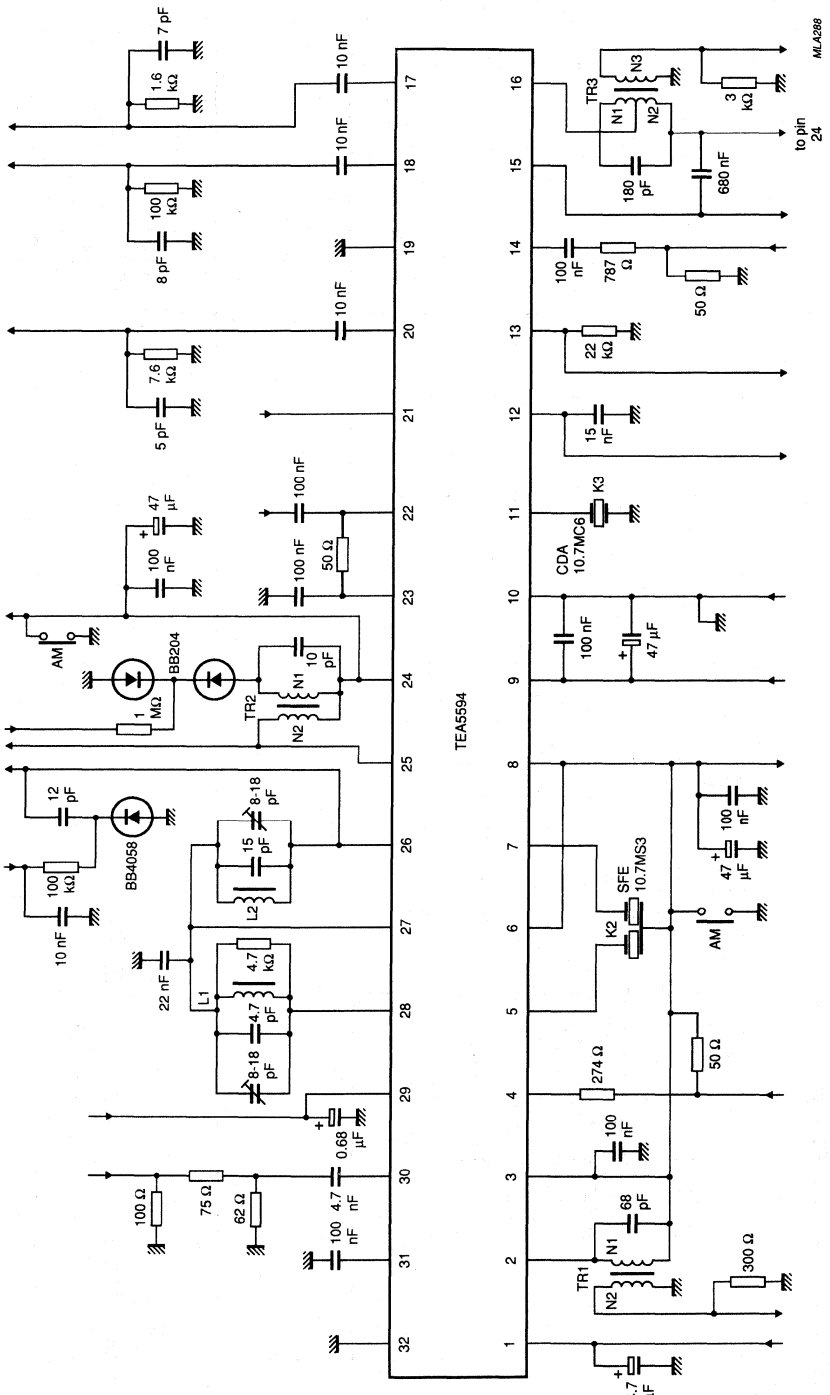
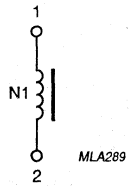


Fig.6 Factory test circuit.

DEVELOPMENT DATA

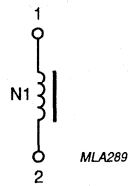
Component data

COILS



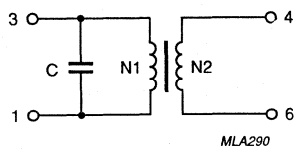
N1 = 4.5
L = 100 μH

Fig.7 FM-RF coil (L1). TOKO equivalent no. MC115.



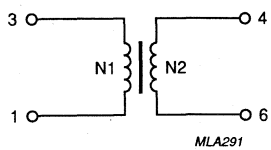
N1 = 4.5
L = 94 μH

Fig.8 FM oscillator coil (L2). TOKO equivalent no. A294SNS-1004NK.



N1 = 12
N2 = 2
C = 68 pF (internal)
f_o = 10.7 MHz
Wire = 0.07 mm diameter
Coil type TOKO 119BCS-A6515BQG

Fig.9 FM-IF coil (TR1).

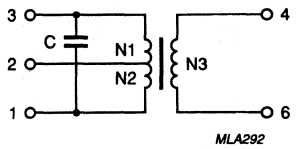


N1 = 55
N2 = 55
Lprim = 106 μH
Wire = 0.05 mm diameter
Coil type TOKO 7MCS

Fig.10 AM oscillator coil (TR2).

Component data (continued)

COILS



N1 = 139
N2 = 15
N3 = 9
C = 180 pF (internal)
Lprim = 660 μH
f_o = 468 kHz
Wire = 0.07 mm diameter
Coil type TOKO 7MC

Fig.11 AM-IF coil (TR3).

CERAMIC FILTERS

AM-IF (K1). SFZ468HL3.
FM-IF (K2). SFE10.7MS3.
FM detector (K3). CDA10.7MC1 (MC6).

AM/FM radio receiver circuit TEA5710; TEA5710T

FEATURES

- Wide supply voltage range: 2.0 to 12 V
- Low current consumption: 7.5 mA at AM, 9.0 mA at FM
- High selectivity with distributed IF gain
- LED driver for tuning indication
- High input sensitivity: 1.6 mV/m (AM), 2.0 µV (FM) for 26 dB S/N
- Good strong signal behaviour: 10 V/m at AM, 500 mV at FM
- Low output distortion: 0.8% at AM, 0.3% at FM
- Designed for simple and reliable PC-board layout
- High impedance MOSFET input on AM

APPLICATIONS

- Portable AM/FM radio
- Clock radio
- Personal headphone radio

DESCRIPTION

The TEA5710 is a high performance Bimos IC for use in AM/FM radios. All necessary functions are integrated: from AM and FM front-end to detector output stages.

QUICK REFERENCE DATA

Conditions AM: f_i = 1 MHz; m = 0.3; f_m = 1 kHz; V_P = 3.0 V; measured in Fig.4 with S1 in position B and S2 in position A, unless otherwise specified. Conditions FM: f_i = 100 MHz; Δf = 22.5 kHz; f_m = 1 kHz; V_P = 3.0 V; measured in Fig.4 with S1 in position B and S2 in position A, unless otherwise specified.

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_P	positive supply voltage	2.0	–	12	V
I_P	supply current in AM mode in FM mode	 5.6 7.3	 7.5 9.0	 9.9 11.2	 mA mA
T_{amb}	operating ambient temperature range	−15	–	+60	°C
AM performance					
V_{in1}	RF sensitivity	40	55	70	µV
V_{13}	AF output voltage	36	45	70	mV
THD	total harmonic distortion	–	0.8	2.0	%
FM performance					
V_{in3}	RF sensitivity	1.0	2.0	3.8	µV
V_{13}	AF output voltage	47	58	69	mV
THD	total harmonic distortion	–	0.3	0.8	%

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TEA5710	24	SDIL	plastic	SOT234AG
TEA5710T	24	SO24L	plastic	SOT137A

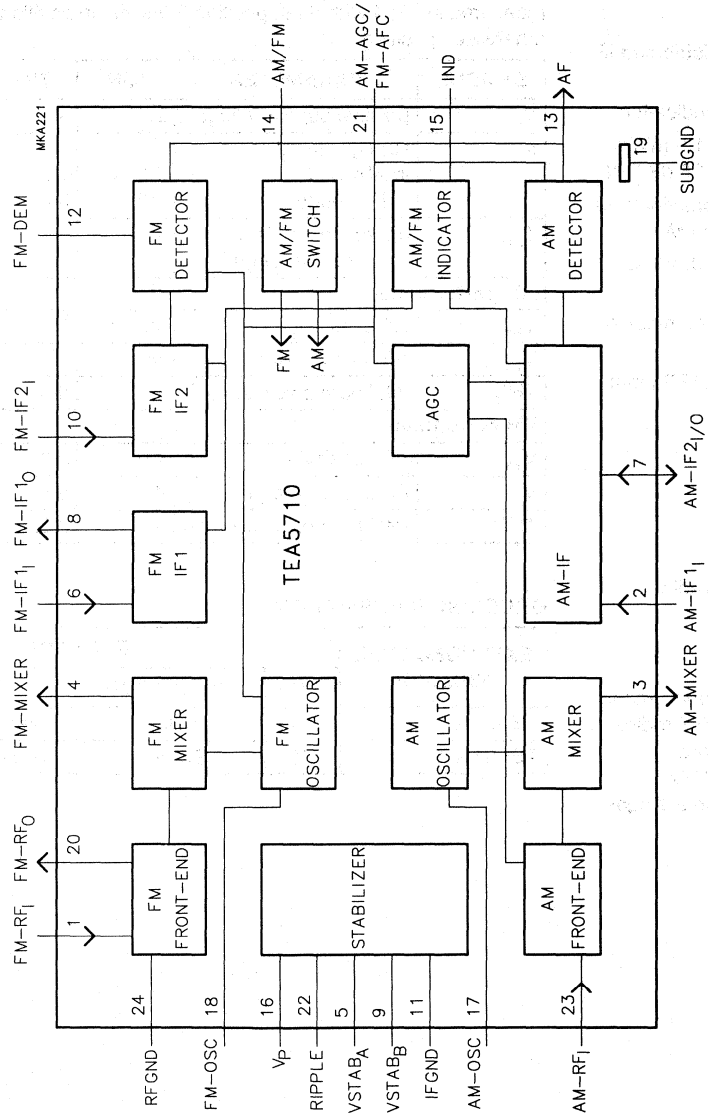


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
$FM\text{-}RF_I$	1	FM-RF aerial input (input impedance typ. 50 Ω)
$AM\text{-}IF1_I$	2	input from IFT or ceramic filter (input impedance typ. 3 kΩ)
AM-MIXER	3	open-collector output to IFT
FM-MIXER	4	output to ceramic IF filter (output impedance typ. 330 Ω)
$VSTAB_A$	5	stabilized internal supply voltage (A)
$FM\text{-}IF1_I$	6	first FM-IF input (input impedance typ. 330 Ω)
$AM\text{-}IF2_{I/O}$	7	input/output to IFT; output: current source
$FM\text{-}IF1_O$	8	first FM-IF output (output impedance typ. 330 Ω)
$VSTAB_B$	9	stabilized internal supply voltage (B)
$FM\text{-}IF2_I$	10	second FM-IF input (input impedance typ. 330 Ω)
IFGND	11	ground of IF and detector stages
FM-DEM	12	ceramic discriminator pin
AF	13	audio output (output impedance typ. 5 kΩ)
AM/FM	14	switch terminal: open for AM; ground for FM
IND	15	field-strength dependent indicator
V_P	16	positive supply voltage
AM-OSC	17	parallel tuned AM-OSC circuit to ground
FM-OSC	18	parallel tuned FM-OSC circuit to ground
SUBGND	19	substrate and RF ground
$FM\text{-}RF_O$	20	parallel tuned FM-RF circuit to ground
AM-AGC/FM-AFC	21	AGC/AFC capacitor pin
RIPPLE	22	ripple capacitor pin
$AM\text{-}RF_I$	23	parallel tuned AM aerial circuit to ground (total input capacitance typ. 3 pF)
RFGND	24	FM-RF ground

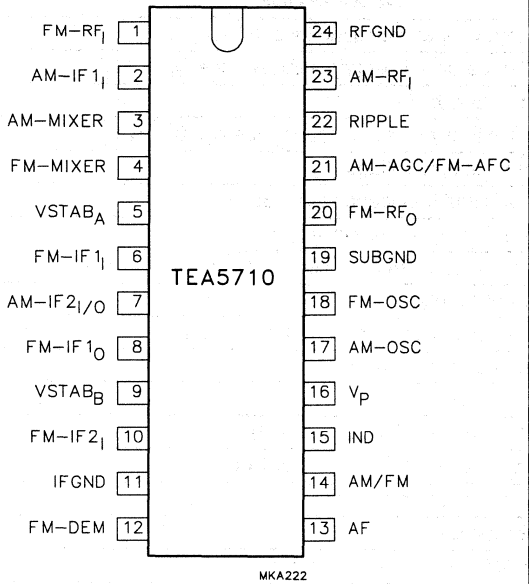


Fig.2 Pin configuration TEA5710.

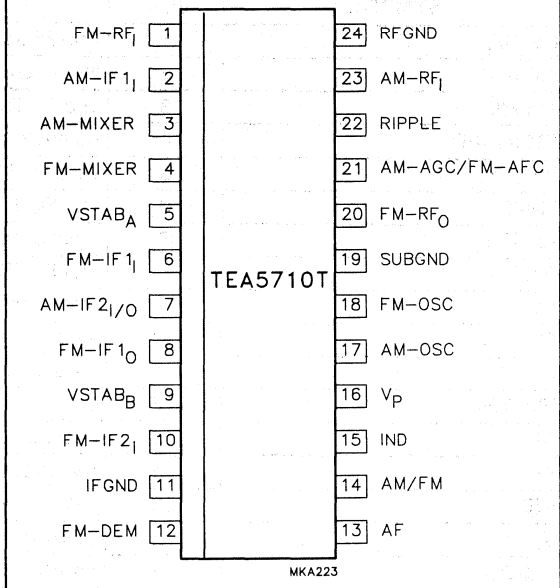


Fig.3 Pin configuration TEA5710T.

FUNCTIONAL DESCRIPTION

The TEA5710 incorporates internal stabilized power supplies. The maximum supply voltage is 12 V, the minimum voltage can go down temporarily to 1.8 V without any loss in performance.

The AM circuit incorporates a double balanced mixer, a one pin low-voltage oscillator (up to 30 MHz), a field-strength dependent indicator output and is designed for distributed selectivity.
The AM input is designed to be connected to the top of a tuned circuit. AGC controls the IF amplification and for large signals it lowers the input impedance.
The first AM selectivity can be an IFT as well as an IFT combined with a ceramic filter; the second one is an IFT.

The FM circuit incorporates a tuned RF stage, a double balanced mixer, a one-pin oscillator, a field-strength indicator output and is designed for distributed IF ceramic filters. The FM quadrature detector uses a ceramic resonator.

LIMITING VALUES

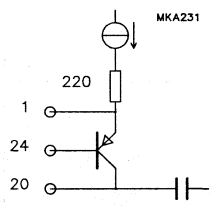
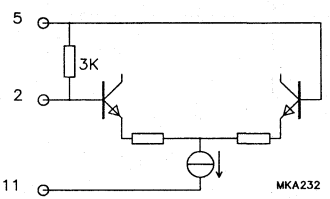
In accordance with the Absolute Maximum Rating System (IEC 134)

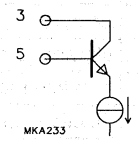
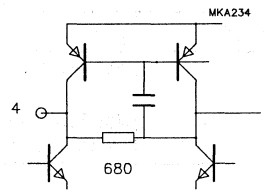
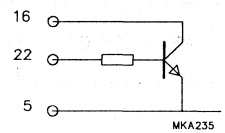
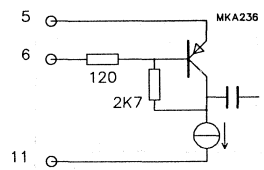
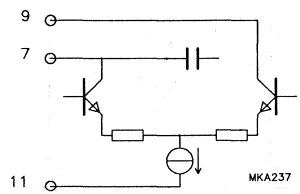
SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_P	positive supply voltage	0	12	V
T_{stg}	storage temperature range	−55	+150	°C
T_{amb}	operating ambient temperature range	−15	+60	°C
T_j	junction temperature range	−15	+150	°C

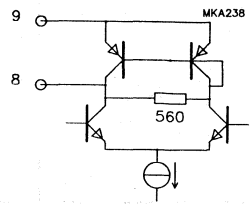
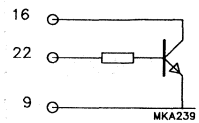
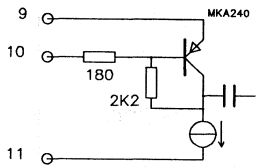
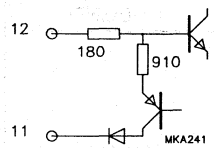
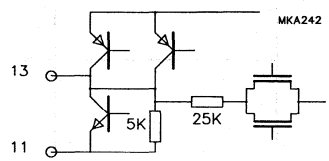
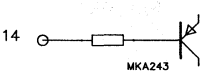
THERMAL RESISTANCE

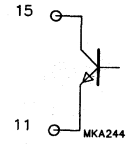
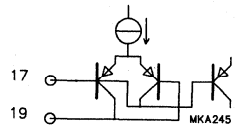
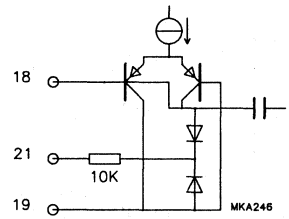
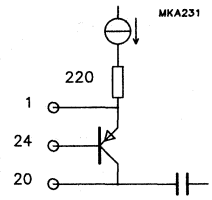
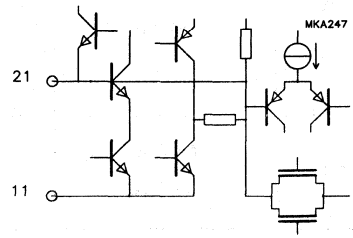
SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	from junction to ambient		
	for SDIL version TEA5710	69	K/W
	for SO24L version TEA5710T	76	K/W

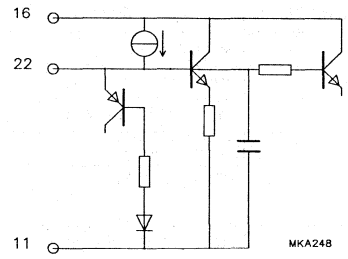
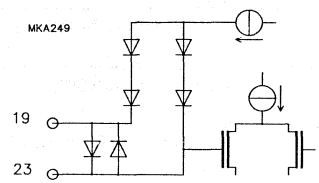
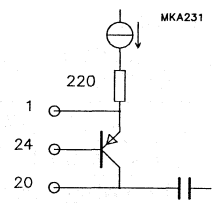
CIRCUIT DESIGN DATA

PIN NO.	PIN SYMBOL	DC PIN VOLTAGE (V)		EQUIVALENT CIRCUIT
		AM	FM	
1	FM-RF_I	–	0.73	
2	AM-$IF1_I$ input	1.4	1.4	

PIN NO.	PIN SYMBOL	DC PIN VOLTAGE (V)		EQUIVALENT CIRCUIT
		AM	FM	
3	AM-MIXER output	1.4	1.4	
4	FM-MIXER output	–	1.0	
5	$VSTAB_A$	1.4	1.4	
6	$FM\text{-}IF1_I$ input	–	0.73	
7	$AM\text{-}IF2_{I/O}$ input/output	1.4	1.4	

PIN NO.	PIN SYMBOL	DC PIN VOLTAGE (V)		EQUIVALENT CIRCUIT
		AM	FM	
8	FM-IF1$_o$ output	–	0.69	
9	VSTAB$_B$	1.4	1.4	
10	FM-IF2$_I$ input	–	0.73	
11	IFGND	0	0	
12	FM-DEM	–	1.0	
13	AF output	0.6	0.7	
14	AM/FM switch	1.3	0	

PIN NO.	PIN SYMBOL	DC PIN VOLTAGE (V)		EQUIVALENT CIRCUIT
		AM	FM	
15	IND	3.0	3.0	
16	V_P	3.0	3.0	
17	AM-OSC	0	0	
18	FM-OSC	0	0	
19	SUBGND	0	0	
20	FM-RF_o	0	0	
21	AM-AGC/ FM-AFC	0.1	0.7	

PIN NO.	PIN SYMBOL	DC PIN VOLTAGE (V)		EQUIVALENT CIRCUIT
		AM	FM	
22	RIPPLE	2.1	2.1	
23	AM-RF$_I$	0	0	
24	RFGND	0	0	

AM CHARACTERISTICS

f_i = 1 MHz; m = 0.3; f_m = 1 kHz; V_P = 3.0 V; measured in Fig.4 with S1 in position B and S2 in position A, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_P	supply current	no input signal	5.6	7.5	9.9	mA
C_i	input capacitance	V_{21} = 0.2 V	–	3	–	pF
G_c	front-end conversion gain	V_{21} = 0.2 V	1.8	3.3	5.0	
V_{in1}	RF sensitivity	S/N = 26 dB	40	55	70	µV
V_{in2}	IF sensitivity	V_{13} = 30 mV; S_1 in position A	0.13	0.2	0.45	mV
V_{13}	AF output voltage	V_{in2} = 3.16 mV; S_1 in position A	36	45	70	mV
THD	total harmonic distortion	V_{in1} = 1 mV	–	0.8	2.0	%
V_{in1}	large signal handling	m = 0.8; THD ≤ 8 %	150	300	–	mV
I_{IND}	indicator current	V_{in2} = 100 mV; S_1 in position A	2	3.5	6	mA
I_{INDOFF}	indicator OFF current	V_{in2} = 0 V; S_1 in position A	–	0	10	µA

FM CHARACTERISTICS

f_i = 100 MHz; Δf = 22.5 kHz; f_m = 1 kHz; V_P = 3.0 V; measured in Fig.4 with S1 in position B and S2 in position A, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_P	supply current	no input signal	7.3	9.0	11.2	mA
V_{in3}	RF limiting sensitivity	V_{13} = –3 dB	0.4	1.2	3.8	µV
V_{in3}	RF sensitivity	S/N = 26 dB	1.0	2.0	3.8	µV
V_6/V_{in3}	front-end voltage gain	V_{in3} ≤ 1 mV; including ceramic filter K1	12	18	22	dB
V_{in4}	IF sensitivity	S_2 in position B; V_{13} = –3 dB	–	20	30	µV
V_{13}	AF output voltage	V_{in3} = 1 mV	47	58	69	mV
THD	total harmonic distortion	V_{in3} = 1 mV; Δf = 22.5 kHz	–	0.3	0.8	%
V_{in3}	large signal handling	THD ≤ 5 %	–	500	–	mV
I_{IND}	indicator current	V_{in4} = 100 mV; S_2 in position B	2	3.5	6	mA
I_{INDOFF}	indicator OFF current	V_{in4} = 0 V; S_2 in position B	–	0	10	µA

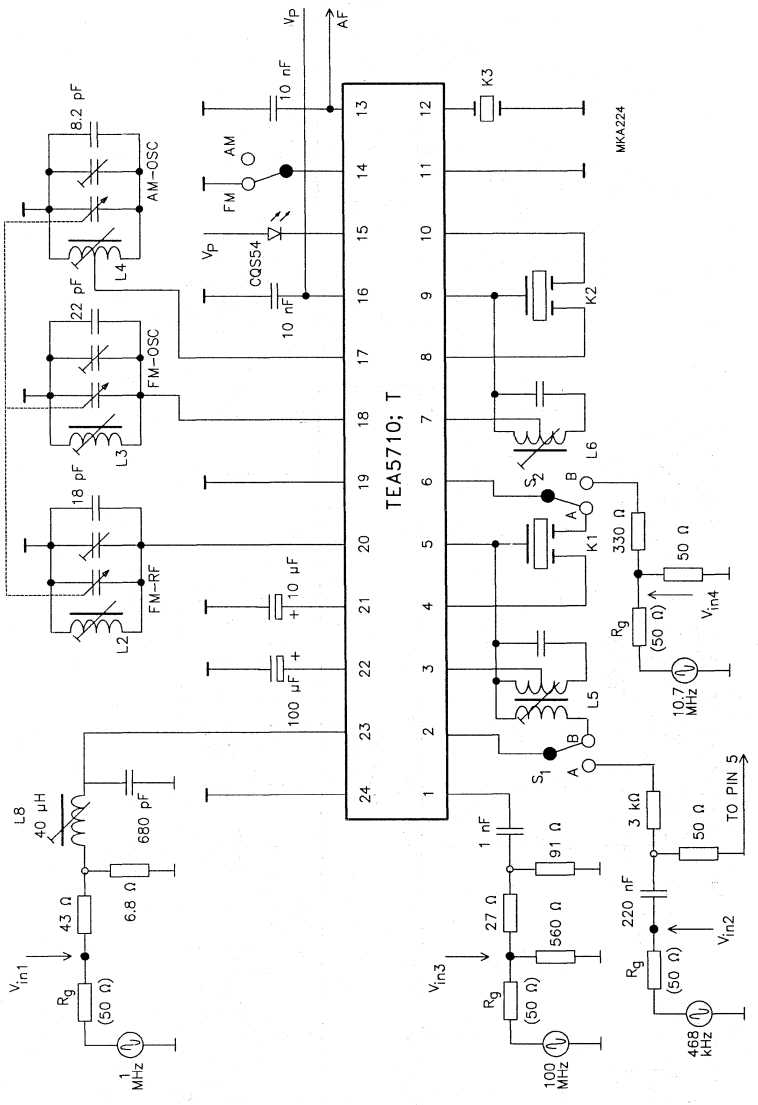


Fig.4 Test circuit.

APPLICATION INFORMATION

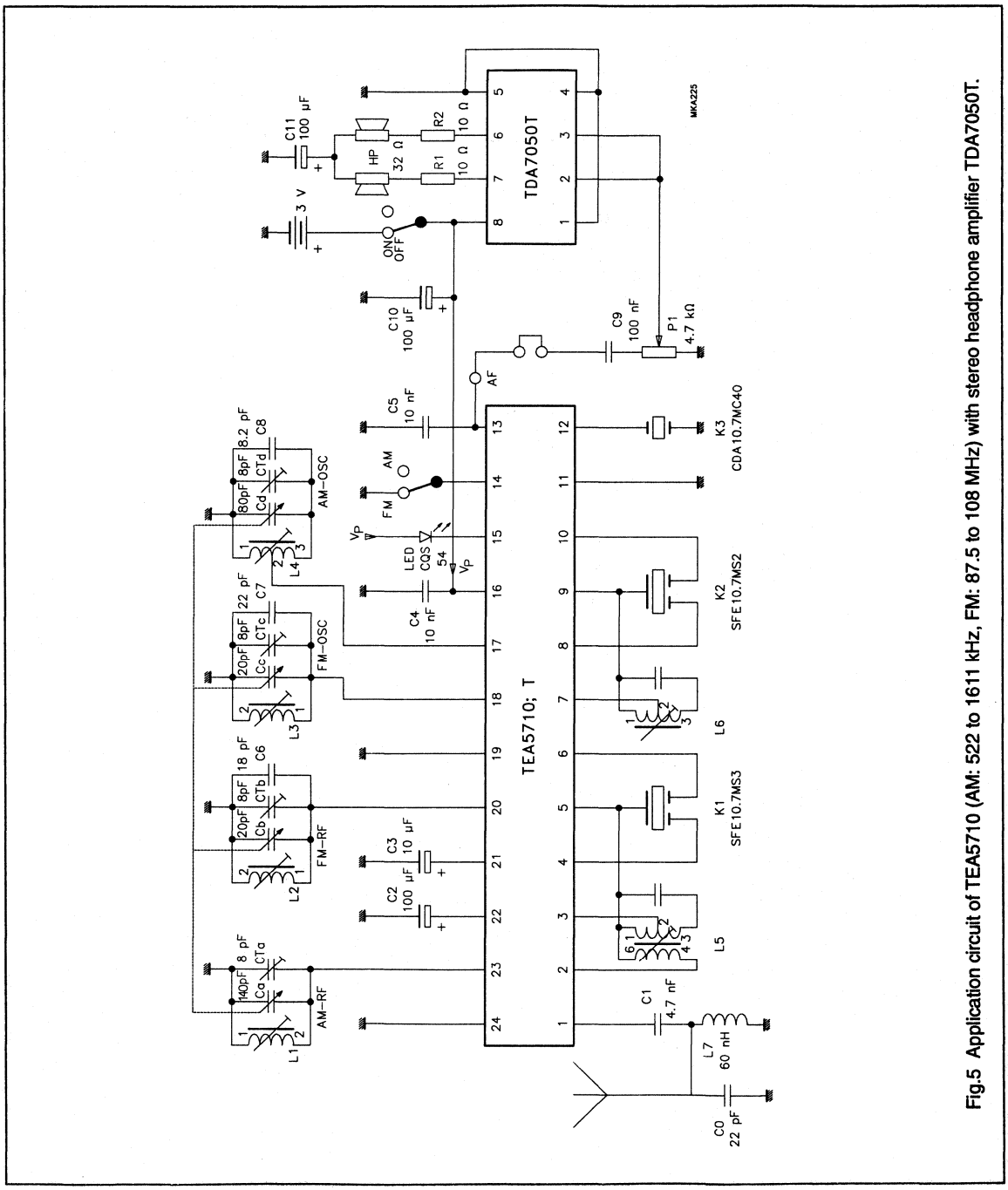


Fig.5 Application circuit of TEA5710 (AM: 522 to 1611 kHz, FM: 87.5 to 108 MHz) with stereo headphone amplifier TDA7050T.

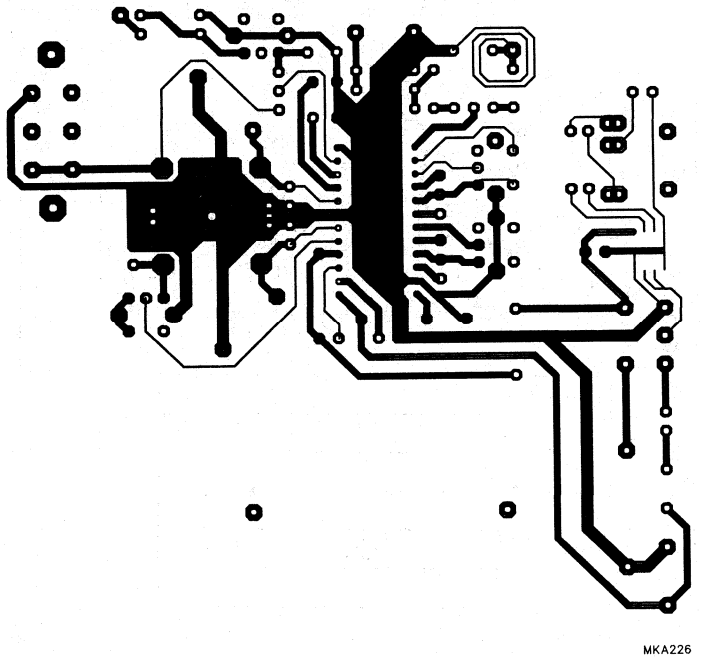


Fig.6 Printed-circuit board layout (track side) for application circuit of Fig.5.

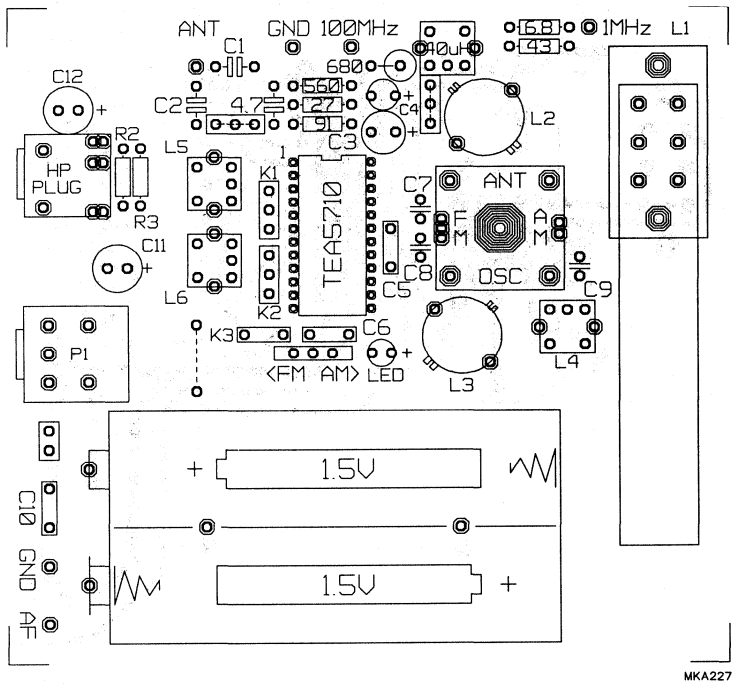
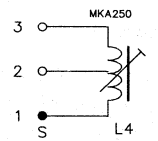
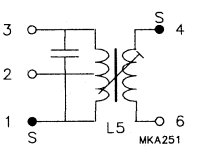
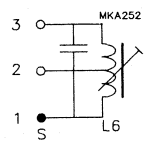
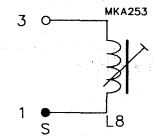


Fig.7 Printed-circuit board layout (component side) for application circuit of Fig.5.

Components for Figs 4 and 5

Coils			
L1	AM-AERIAL	ferroceptor length = 6 cm L1-2 = 625 µH N1-2 = 105 turns	
L2	FM-RF	L1-2 = 66 nH N1-2 = 2.5 turns unloaded Q = 150 TOKO type S18 TOKO no. 301SS-0200	
L3	FM-OSC	L1-2 = 40 nH N1-2 = 1.5 turns unloaded Q = 150 TOKO type S18 TOKO no. 301SS-0100	
L4	AM-OSC	L1-3 = 270 µH N1-2 = 18 N2-3 = 70 unloaded Q = 100 wire diameter 0.07 mm TOKO type 7P material TOKO 7BRS	
L5	AM-IF1	L1-3 = 625 µH N1-2 = 17 turns N2-3 = 141 turns N4-6 = 10 turns C1-3 = 180 pF unloaded Q = 90 wire diameter 0.07 mm TOKO type 7P material TOKO 7MCS	
L6	AM-IF2	L1-3 = 625 µH N1-2 = 28 turns N2-3 = 130 turns C1-3 = 180 pF unloaded Q = 90 wire diameter 0.07 mm TOKO type 7P material TOKO 7MCS	
L7	FM-AERIAL	print-coil L1-2 = 60 nH N1-2 = 2.5 turns	

L8	AM-RF	test circuit only: L1-3 = 40 µH N1-3 = 34 turns unloaded Q = 85 wire diameter 0.09 mm TOKO type 7P material TOKO 7BRS	
Ceramic filters			
K1	FM-IF1	Murata SFE 10.7 MS 3	
K2	FM-IF2	Murata SFE 10.7 MS 2	
K3	FM-DET	Murata CDA 10.7 MC 40	
Capacitors			
C1	VARICON	AM: 140/82 pF FM: 2 x 20 pF trimmer: 4 x 8 pF TOKO type no. HU-22124	

Application notes

1. Short circuiting: **all** pins are short-circuit proof except **pin 1** (FM-RF_I) with respect to the supply voltage pin.
2. Tuning indicator (at pin 15, IND): connect either a tuning indicator (e.g. a LED) between this pin and the supply voltage (pin 16) or connect the pin IND to ground.
3. For an example of PC-board layout: see Figs 6 and 7.

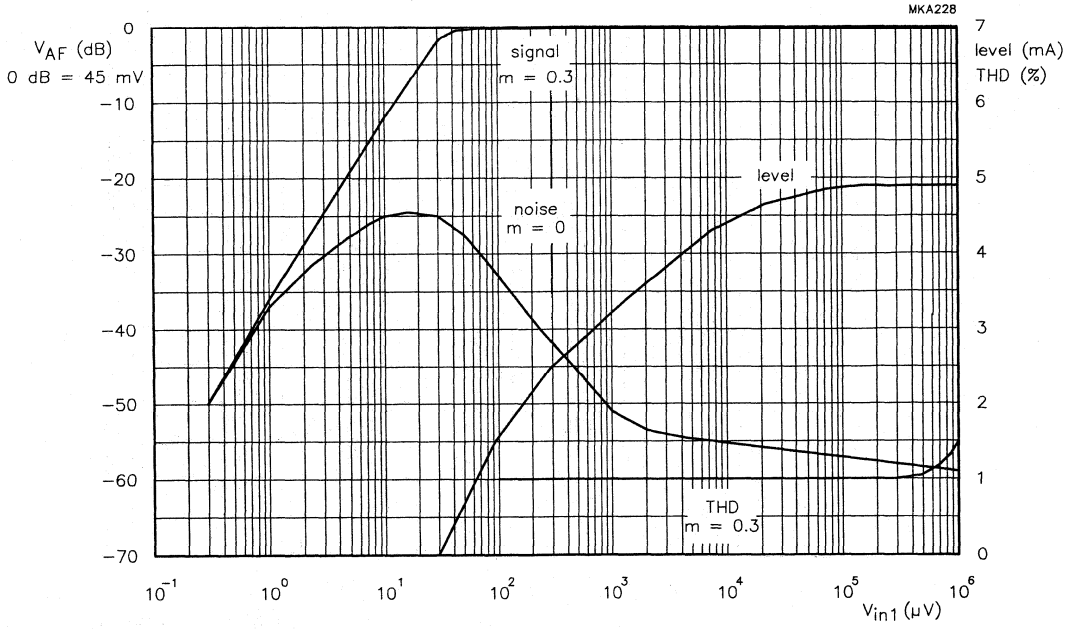


Fig.8 Typical AM audio output voltage (V_{AF}; signal at m = 0.3), noise, THD (at m = 0.3) and indicator current (level) as a function of RF input voltage (V_{in1}; f = 1 kHz). Measured in test circuit of Fig.4 with V_P = 3.0 V.

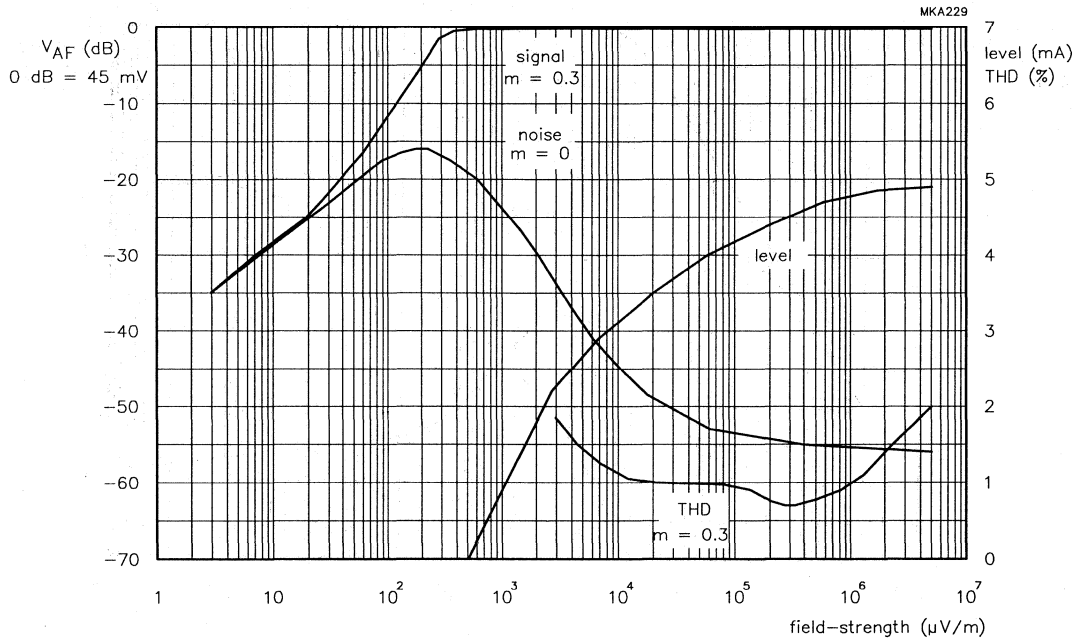


Fig.9 Typical AM audio output voltage (V_{AF}; signal at m = 0.3), noise, THD (at m = 0.3) and indicator current (level) as a function of field-strength (f = 1 kHz). Measured at 1 MHz in application circuit of Fig.5 with V_P = 3 V.

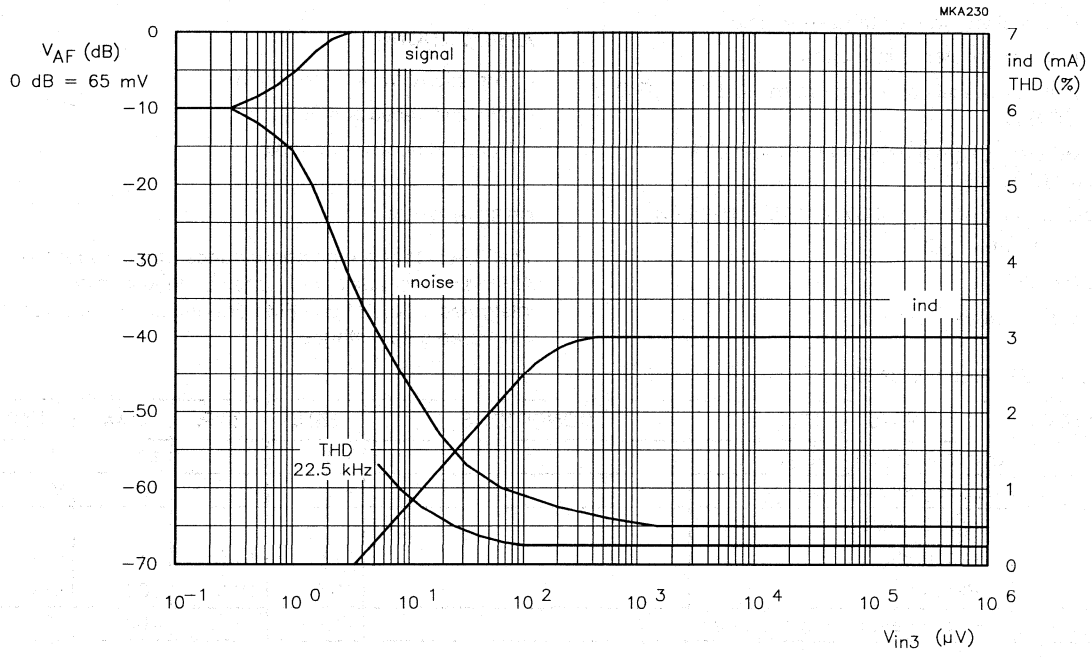


Fig.10 Typical FM audio output voltage (V_{AF}; signal), noise, THD and indicator current (ind) as a function of RF input voltage (V_{in3}; d_f = 22.5 kHz). Measured in test circuit of Fig.4 at V_P = 3 V.

AM/FM stereo radio circuit TEA5711; TEA5711T

FEATURES

- Wide supply voltage range: 1.8 or 2.1 to 12 V
- Low current consumption: 15 mA at AM, 16 mA at FM
- High selectivity with distributed IF gain
- LED driver for stereo indication
- High input sensitivity: 1.6 mV/m (AM), 2.0 μV (FM) for 26 dB S/N
- Good strong signal behaviour: 10 V/m at AM, 500 mV at FM
- Low output distortion: 0.8% at AM, 0.3% at FM
- Signal level output
- Soft mute
- Signal dependent stereo
- Designed for simple and reliable printed-circuit board layout
- High impedance MOSFET input on AM.

APPLICATIONS

- Portable AM/FM stereo radio
- Mini/midi receiver sets
- Personal headphone radio.

DESCRIPTION

The TEA5711 is a high performance Bimos IC for use in AM/FM stereo radios. All necessary functions are integrated: from AM and FM front-end to AM detector and FM stereo output stages.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	TYP.
V_P	dynamic supply voltage		1.8	–	12	V
V_P	static supply voltage		2.1	–	12	V
I_P	supply current					
	AM mode		11.9	15.0	18.9	mA
	FM mode		13.5	16.5	20.2	mA
T_{amb}	operating ambient temperature		−15	–	+60	°C
AM performance						
V_{in1}	RF sensitivity		40	55	70	μV
V_{28}	AF output voltage		36	45	70	mV
THD	total harmonic distortion		–	0.8	2.0	%
FM performance						
V_{in3}	RF sensitivity		1.0	2.0	3.8	μV
V_{28}	AF output voltage		50	61	72	mV
THD	total harmonic distortion		–	0.3	0.8	%
MPX performance						
α_{cs}	channel separation		26	30	–	dB
A_{MPX}	MPX voltage gain	V_{AF-L}/V_{in9}; S5 in position MONO	−1.5	0	+1.0	dB
THD	total harmonic distortion		–	0.5	1.0	%

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TEA5711	SDIP32	plastic shrink dual in-line package; 32 leads (400 mil)	SOT232-1
TEA5711T	SO32	plastic small outline package; 32 leads; body width 7.5 mm	SOT287-1

BLOCK DIAGRAM

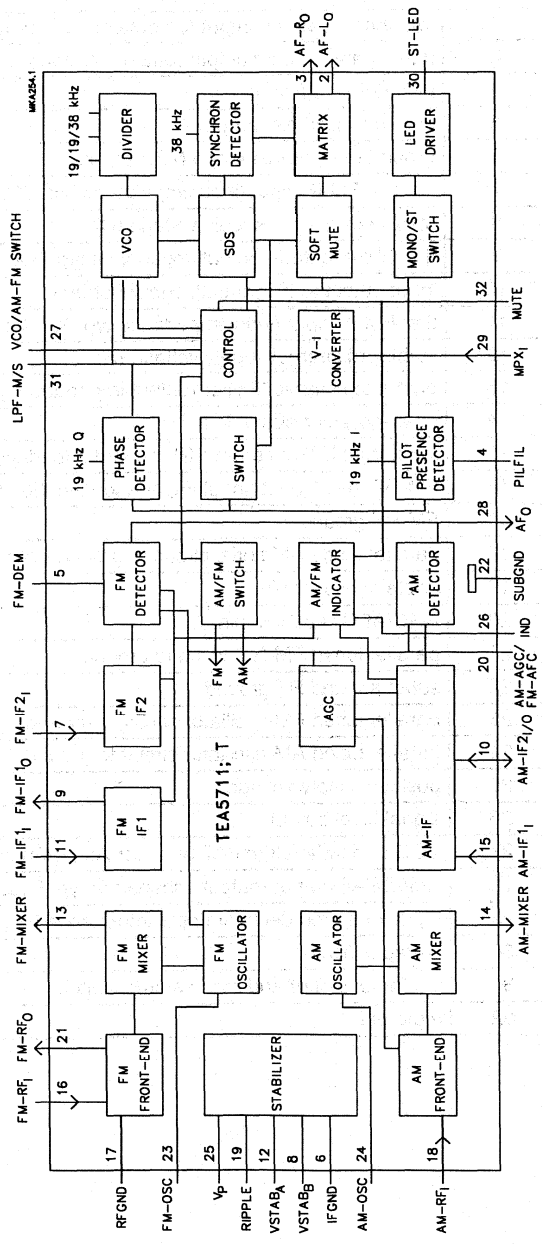


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
n.c.	1	not connected
AF-L_O	2	left channel audio output (output impedance typ. 4.3 kΩ)
AF-R_O	3	right channel audio output (output impedance typ. 4.3 kΩ)
PILFIL	4	pilot detector filter pin
FM-DEM	5	ceramic discriminator pin
IFGND	6	ground of IF, detector and MPX stages
FM-$IF2_I$	7	second FM-IF input (input impedance typ. 330 Ω)
$VSTAB_B$	8	stabilized internal supply voltage (B)
FM-$IF1_O$	9	first FM-IF output (output impedance typ. 330 Ω)
AM-$IF2_{I/O}$	10	input/output to IFT; output: current source
FM-$IF1_I$	11	first FM-IF input (input impedance typ. 330 Ω)
$VSTAB_A$	12	stabilized internal supply voltage (A)
FM-MIXER	13	output to ceramic IF filter (output impedance typ. 330 Ω)
AM-MIXER	14	open-collector output to IFT
AM-$IF1_I$	15	input from IFT or ceramic filter (input impedance typ. 3 kΩ)
FM-RF_I	16	FM-RF aerial input (input impedance typ. 50 Ω)
RFGND	17	FM-RF ground
AM-RF_I	18	parallel tuned AM aerial circuit to ground (total input capacitance typ. 3 pF)
RIPPLE	19	ripple capacitor pin
AM-AGC/FM-AFC	20	AGC/AFC capacitor pin
FM-RF_O	21	parallel tuned FM-RF circuit to ground
SUBGND	22	substrate and RF ground
FM-OSC	23	parallel tuned FM-oscillator circuit to ground
AM-OSC	24	parallel tuned AM-oscillator circuit to ground
V_P	25	positive supply voltage
IND	26	signal level output
VCO/AM-FM SWITCH	27	VCO and switch terminal: open for AM; ground for FM
AF_O	28	AM/FM AF output (output impedance typ. 5 kΩ)
MPX_I	29	input for stereo decoder (input impedance typ. 180 kΩ)
ST-LED	30	stereo indicator
LPF-M/S	31	pin for loop-filter and mono/stereo switch
MUTE	32	mute pin

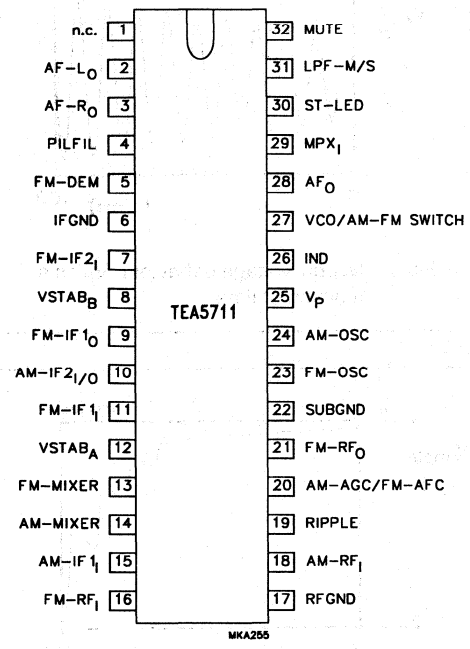


Fig.2 Pin configuration; TEA5711.

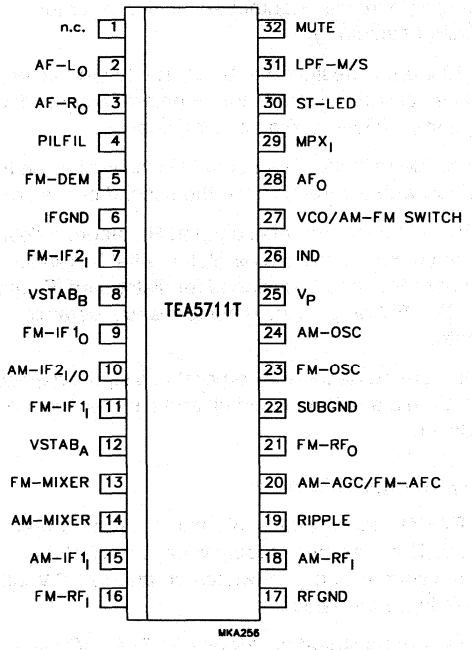


Fig.3 Pin configuration; TEA5711T.

FUNCTIONAL DESCRIPTION

The AM circuit incorporates a double balanced mixer, a one pin low-voltage oscillator (up to 30 MHz) a field-strength indicator output and is designed for distributed selectivity.

The AM input is designed to be connected to the top of a tuned circuit. AGC controls the IF amplification and for large signals it lowers the input impedance.

The first AM selectivity can be an IFT as well as an IFT combined with a ceramic filter; the second one is an IFT.

The FM circuit incorporates a tuned RF stage, a double balanced mixer, a one-pin oscillator, a field-strength indicator output and is designed for distributed IF ceramic filters. The FM quadrature detector uses a ceramic resonator.

The PLL stereo decoder incorporates a signal dependent stereo circuit, a soft-mute circuit and a stereo indicator LED driver.

Supply voltage behaviour

The TEA5711 incorporates internal stabilized power supplies. The maximum supply voltage is 12 V, the minimum voltage can go down temporarily to 1.8 V without any loss in performance.

Due to the capacitor at pin 19 (RIPPLE) the IC gives excellent performance, even when the actual supply voltage at pin 25 (V_P) drops below the voltage at pin 19 (RIPPLE).

Figures 4, 5 and 6 show that V_{stab}, which is dominant for the overall IC performance, remains unaffected, even if V_P drops down to 1.8 V or less. In this typical example the static or average V_P is equal to 2.5 V. Dips in V_{stab} appear only when the peak-to-peak value of the AC-component of $V_P > 2$ V, i.e. when the dynamic value of V_P drops down to 1.5 V for a short moment.

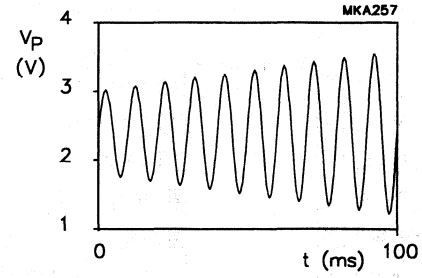


Fig.4 Supply voltage behaviour; V_P as a function of time.

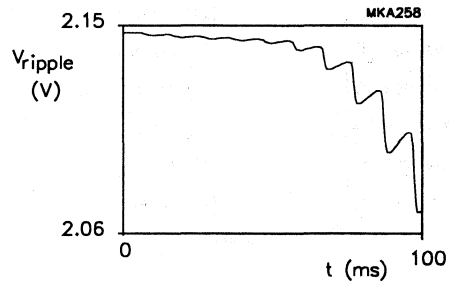


Fig.5 Supply voltage behaviour; V_{ripple} as a function of time.

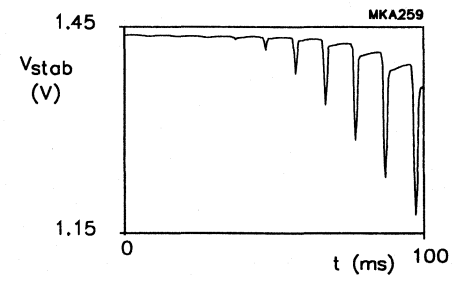


Fig.6 Supply voltage behaviour; V_{stab} as a function of time.

LIMITING VALUES

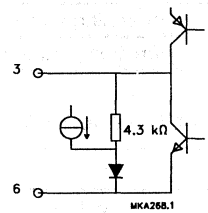
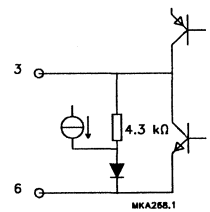
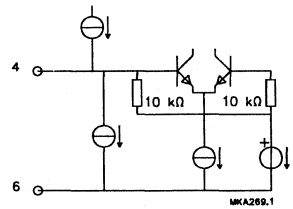
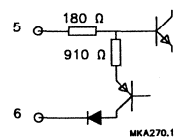
In accordance with the Absolute Maximum Rating System (IEC 134).

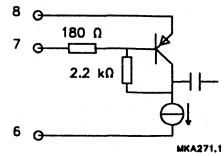
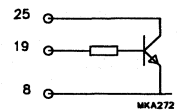
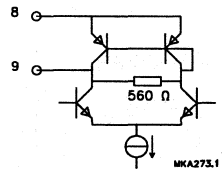
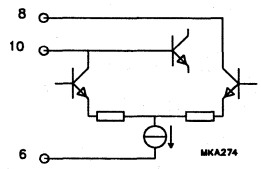
SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_P	supply voltage	0	12	V
T_{stg}	storage temperature	−55	+150	°C
T_{amb}	operating ambient temperature	−15	+60	°C
T_j	junction temperature	−15	+150	°C

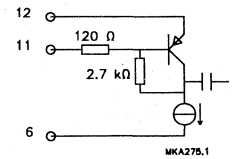
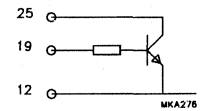
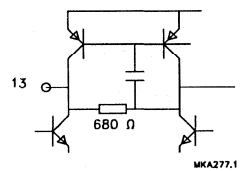
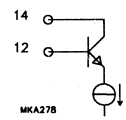
THERMAL CHARACTERISTICS

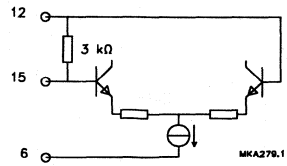
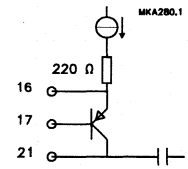
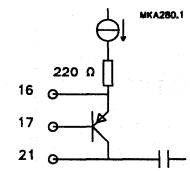
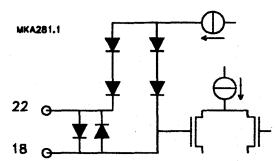
SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air		
	SDIP32	54	K/W
	SO32	68	K/W

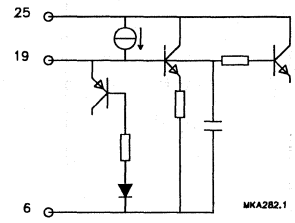
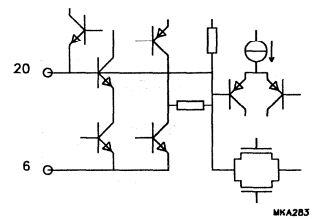
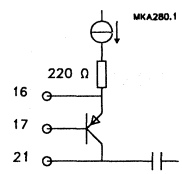
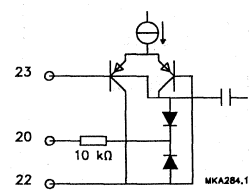
CIRCUIT DESIGN DATA

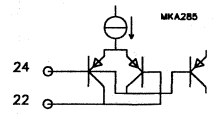
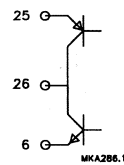
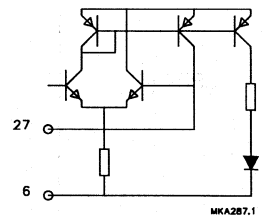
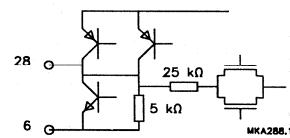
PIN NO.	PIN SYMBOL	DC PIN VOLTAGE (V)		EQUIVALENT CIRCUIT
		AM	FM	
1	n.c.	–	–	
2	AF-L_O output	0.65	0.65	
3	AF-R_O output	0.65	0.65	
4	PILFIL	0.95	0.95	
5	FM-DEM	–	1.0	
6	IFGND	0	0	

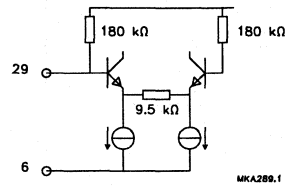
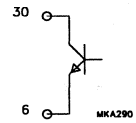
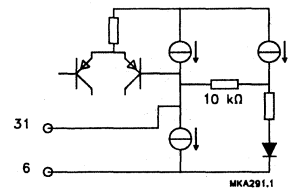
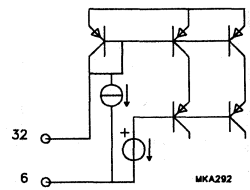
PIN NO.	PIN SYMBOL	DC PIN VOLTAGE (V)		EQUIVALENT CIRCUIT
		AM	FM	
7	$FM\text{-}IF2_I$ input	–	0.73	
8	$VSTAB_B$	1.4	1.4	
9	$FM\text{-}IF1_O$ output	–	0.69	
10	$AM\text{-}IF2_{I/O}$ input/output	1.4	1.4	

PIN NO.	PIN SYMBOL	DC PIN VOLTAGE (V)		EQUIVALENT CIRCUIT
		AM	FM	
11	FM-IF1$_I$ input	–	0.73	
12	VSTAB$_A$	1.4	1.4	
13	FM-MIXER output	–	1.0	
14	AM-MIXER output	1.4	1.4	

PIN NO.	PIN SYMBOL	DC PIN VOLTAGE (V)		EQUIVALENT CIRCUIT
		AM	FM	
15	AM-IF1$_I$ input	1.4	1.4	
16	FM-RF$_I$ input	–	0.73	
17	RFGND	0	0	
18	AM-RF$_I$ input	0	0	

PIN NO.	PIN SYMBOL	DC PIN VOLTAGE (V)		EQUIVALENT CIRCUIT
		AM	FM	
19	RIPPLE	2.1	2.1	
20	AM-AGC/ FM-AFC	0.1	0.7	
21	FM-RF_O	0	0	
22	SUBGND	0	0	
23	FM-OSC	0	0	

PIN NO.	PIN SYMBOL	DC PIN VOLTAGE (V)		EQUIVALENT CIRCUIT
		AM	FM	
24	AM-OSC	0	0	
25	V_P	3.0	3.0	
26	IND output	3.0	3.0	
27	VCO and AM/FM switch	1.3	0.95	
28	AF output	0.6	0.7	

PIN NO.	PIN SYMBOL	DC PIN VOLTAGE (V)		EQUIVALENT CIRCUIT
		AM	FM	
29	MPX input	1.23	1.23	
30	ST-LED	3.0	3.0	
31	LPF-M/S	0.1	0.8	
32	MUTE	0.7	0.7	

AM CHARACTERISTICS

f_i = 1 MHz; m = 0.3; f_m = 1 kHz; V_P = 3.0 V; measured in Fig.7 with S1 in position B, S2 in position A and S7 in position A; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_P	supply current	no input signal	11.9	15.0	18.9	mA
C_i	input capacitance	V_{20} = 0.2 V	–	3	–	pF
G_c	front-end conversion gain	V_{20} = 0.2 V	1.8	3.3	5.0	
V_{in1}	RF sensitivity	S/N = 26 dB	40	55	70	µV
V_{in2}	IF sensitivity	V_{28} = 30 mV; S1 in position A	0.13	0.2	0.45	mV
V_{28}	AF output voltage	V_{in2} = 3.16 mV; S1 in position A	36	45	70	mV
THD	total harmonic distortion	V_{in1} = 1 mV	–	0.8	2.0	%
V_{in1}	large signal handling	m = 0.8; THD ≤ 8%	150	300	–	mV
I_{IND}	indicator current	V_{in2} = 100 mV; S1 in position A	120	170	230	µA
I_{INDOFF}	indicator OFF current	V_{in2} = 0 V; S1 in position A	–	0	10	µA

FM CHARACTERISTICS

f_i = 100 MHz; Δf = 22.5 kHz; f_m = 1 kHz; V_P = 3.0 V; measured in Fig.7 with S1 in position B, S2 in position A and S7 in position A; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_P	supply current	no input signal	13.5	16.5	20.2	mA
V_{in3}	RF limiting sensitivity	V_{28} = –3 dB	0.4	1.2	3.8	µV
V_{in3}	RF sensitivity	S/N = 26 dB	1.0	2.0	3.8	µV
V_{11}/V_{in3}	front-end voltage gain	V_{in3} ≤ 1 mV; including ceramic filter K1	12	18	22	dB
V_{in4}	IF sensitivity	S2 in position B; V_{28} = –3 dB	–	20	30	µV
V_{28}	AF output voltage	V_{in3} = 1 mV	50	61	72	mV
THD	total harmonic distortion	V_{in3} = 1 mV; Δf = 22.5 kHz	–	0.3	0.8	%
V_{in3}	large signal handling	THD ≤ 5%	–	500	–	mV
I_{IND}	indicator current	V_{in4} = 100 mV; S2 in position B	190	255	320	µA
I_{INDOFF}	indicator OFF current	V_{in4} = 0 V; S2 in position B	–	0	2	µA

STEREO DECODER CHARACTERISTICS

f_i = 1 kHz; $V_{in9(L+R)}$ = 195 mv; pilot = 20 mV; V_P = 3.0 V; measured in Fig.7 with S1 in position B, S2 in position A, S6 in position A, S7 in position A and S5 in position STEREO; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
A_{MPX}	MPX voltage gain V_{AF-L}/V_{in9}	S5 in position MONO	–1.5	0	+1.0	dB
THD	total harmonic distortion		–	0.5	1.0	%
(S+N)/N	signal plus noise-to-noise ratio	pilot = 20 mV	–	74	–	dB
α_{cs}	channel separation	L = 1; R = 0 or L = 0; R = 1	26	30	–	dB
SC	stereo control	V_{in3} = 120 µV	–	30	–	dB
		V_{in3} = 10 µV	–	1	–	dB
α_{MUTE}	AF output signal suppression	V_{in3} ≤ 2 µV	–	20	–	dB

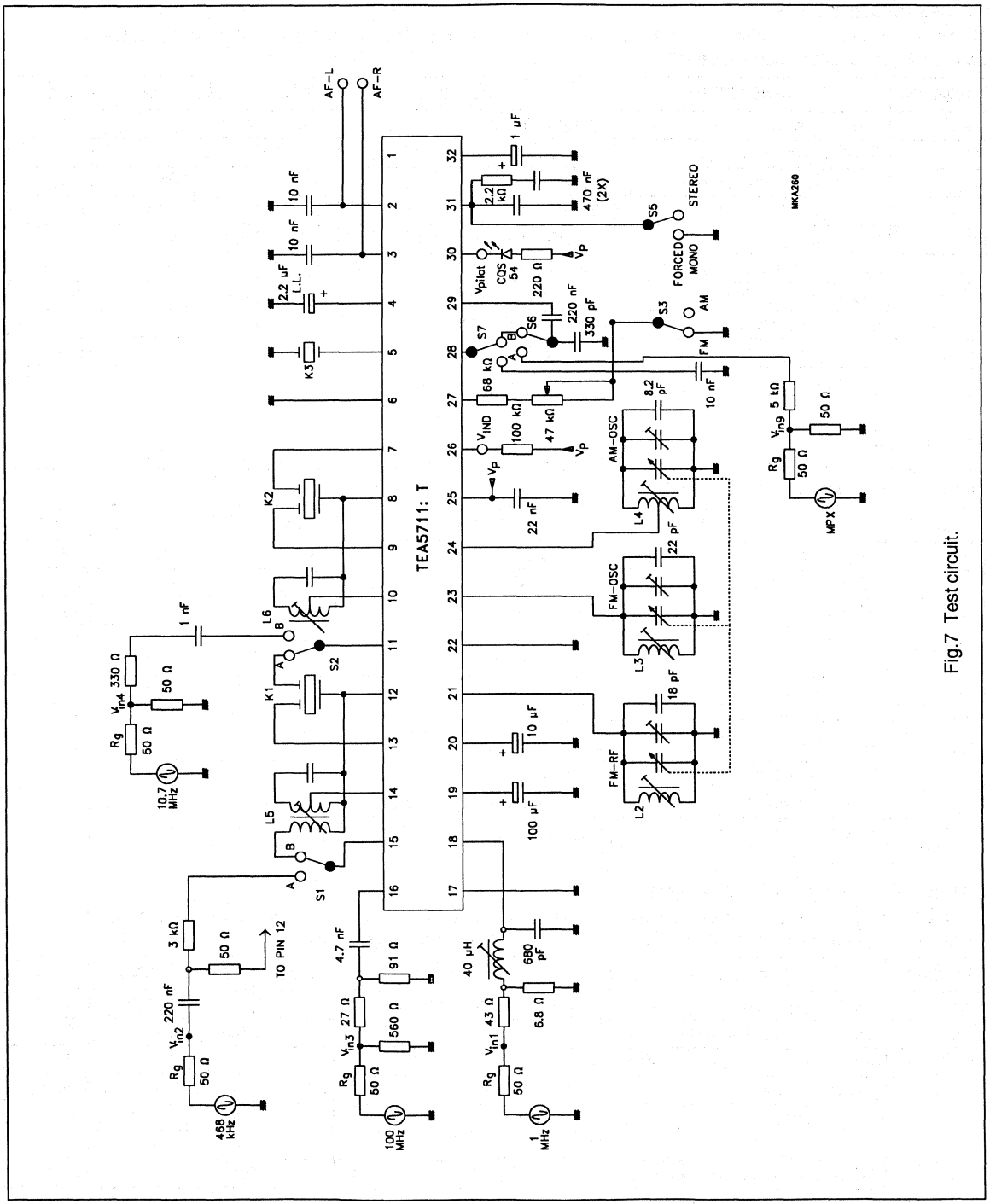


Fig.7 Test circuit.

APPLICATION INFORMATION

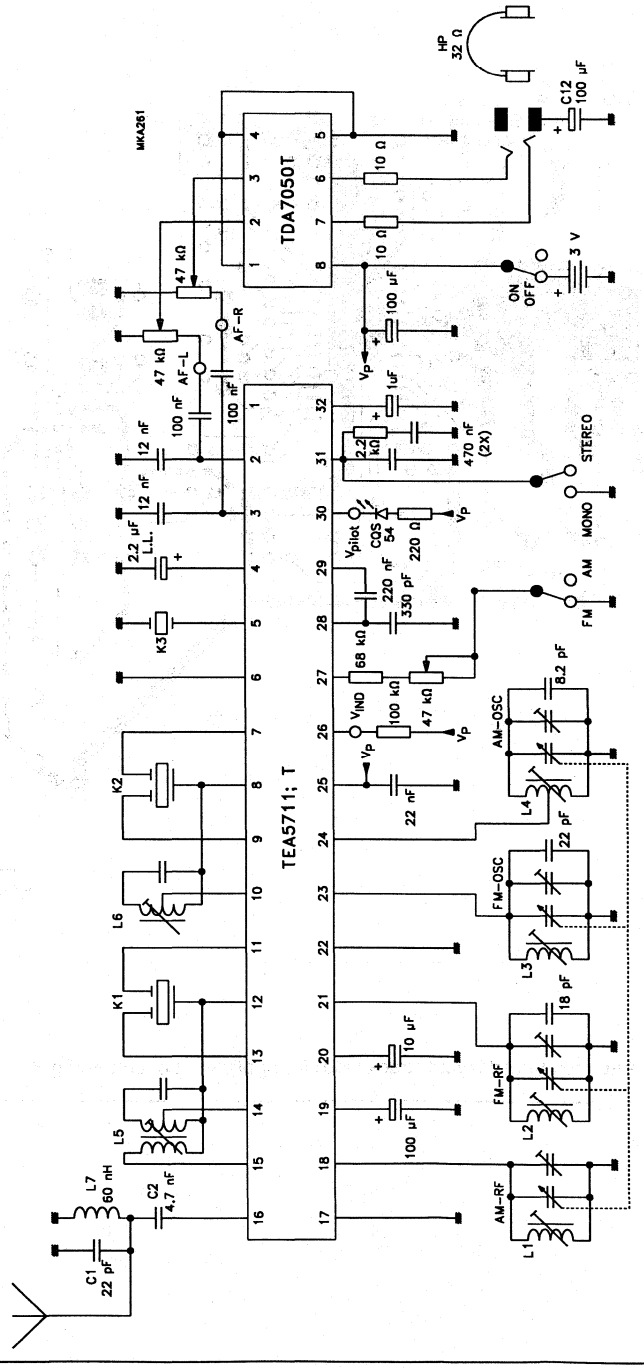


Fig.8 Application circuit of TEA5711 (AM: 522 to 1611 kHz, FM: 87.5 to 108 MHz) with stereo headphone amplifier TDA7050T.

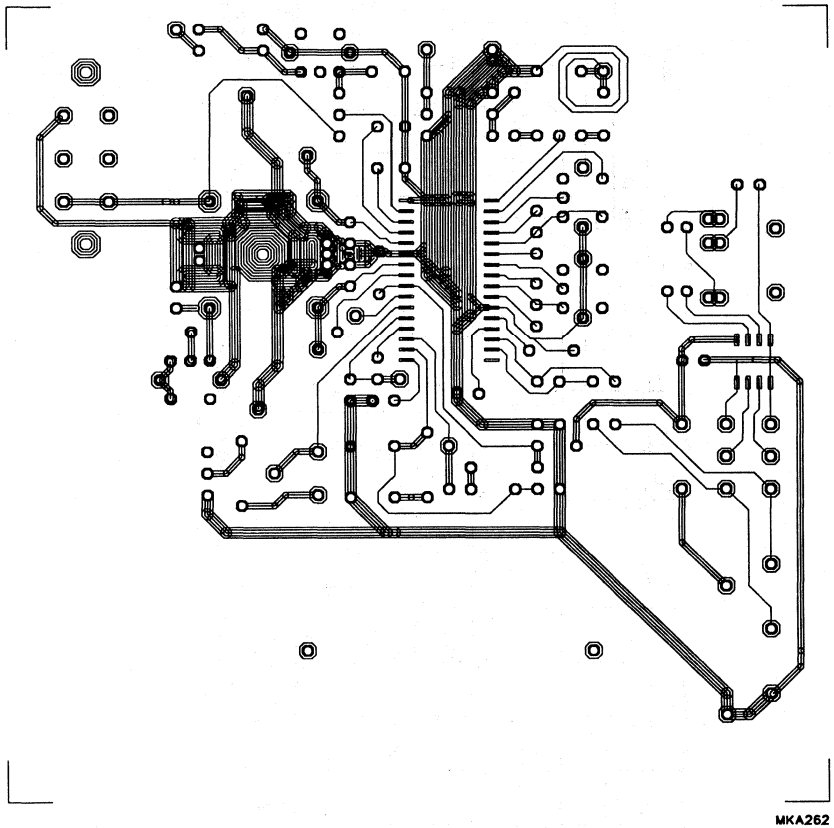


Fig.9 Printed-circuit board layout (track side) for application circuit of Fig.8.

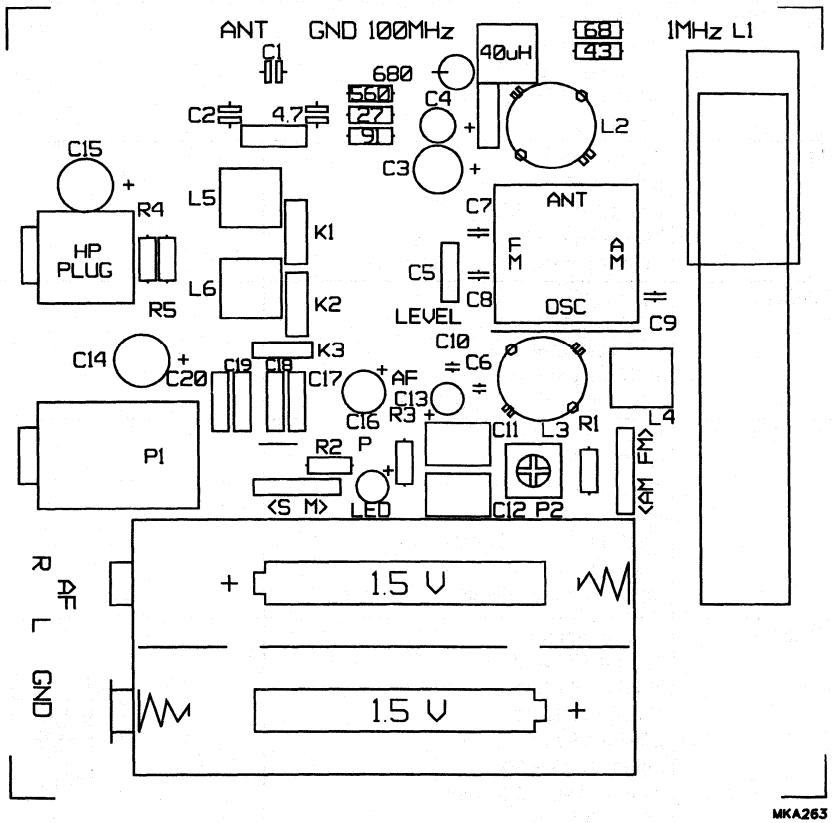
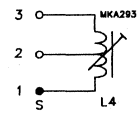
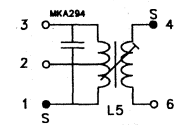
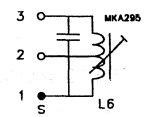
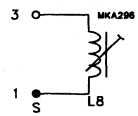


Fig.10 Printed-circuit board layout (component side) for application circuit of Fig.8.

Components for Figs 7 and 8

NUMBER	TYPE	DESCRIPTION	CIRCUIT
Coils			
L1	AM-AERIAL	ferroceptor length = 6 cm L1-2 = 625 µH N1-2 = 105 turns unloaded Q	
L2	FM-RF	L1-2 = 66 nH N1-2 = 2.5 turns unloaded Q = 150T TOKO type S18 TOKO number 301SS-0200	
L3	FM-OSC	L1-2 = 40 nH N1-2 = 1.5 turns unloaded Q = 150 TOKO type S18 TOKO number 301SS-0100	
L4	AM-OSC	L1-3 = 270 µH N1-2 = 18 N2-3 = 70 unloaded Q = 100 wire diameter 0.07 mm TOKO type 7P material TOKO 7BRS	
L5	AM-IF1	L1-3 = 625 µH N1-2 = 17 turns N2-3 = 141 turns N4-6 = 10 turns C1-3 = 180 pF unloaded Q = 90 wire diameter 0.07 mm TOKO type 7P material TOKO 7MCS	
L6	AM-IF2	L1-3 = 625 µH N1-2 = 28 turns N2-3 = 130 turns C1-3 = 180 pF unloaded Q = 90 wire diameter 0.07 mm TOKO type 7P material TOKO 7MCS	
L7	FM-AERIAL	printcoil L1-2 = 60 nH N1-2 = 2.5 turns	

NUMBER	TYPE	DESCRIPTION	CIRCUIT
L8	AM-RF	test circuit only: L1-3 = 40 µH N1-3 = 34 turns unloaded Q = 85 wire diameter 0.09 mm TOKO type 7P material TOKO 7BRS	
Ceramic filters			
K1	FM-IF1	Murata SFE 10.7 MS 2	
K2	FM-IF2	Murata SFE 10.7 MS 2	
K3	FM-DET	Murata CDA 10.7 MC 40	
Capacitors			
C1	VARICON	AM: 140/82 pF FM: 2 × 20 pF trimmer: 4 × 8 pF TOKO type number HU-22124	

Application remarks

- Short circuiting: **all** pins are short-circuit proof except **pin 16** (FM-RF$_I$) with respect to the supply voltage pin.
- For an example of printed-circuit board layout: see Figs 9 and 10.
- Align VCO with aerial signal present.

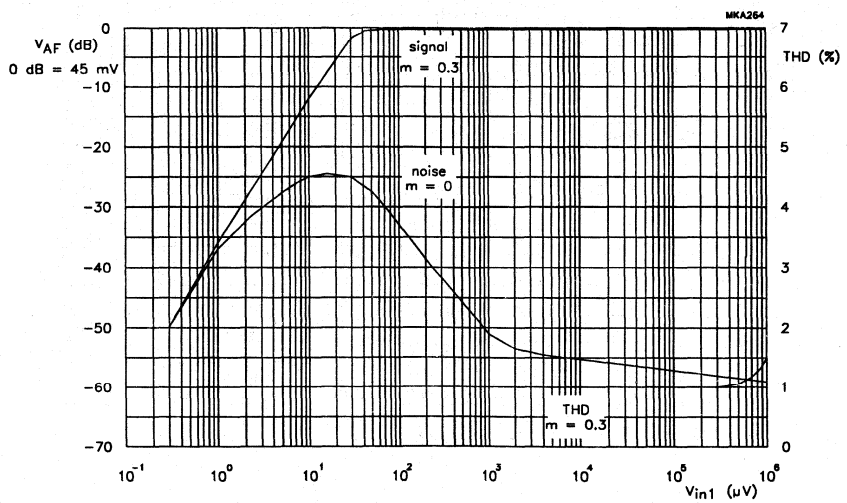


Fig.11 Typical AM audio voltage (V_{AF}; signal at m = 0.3), noise and THD as a function of RF input voltage (V_{in1}; f_i = 1 kHz). Measured in test circuit Fig.7 with V_P = 3.0 V.

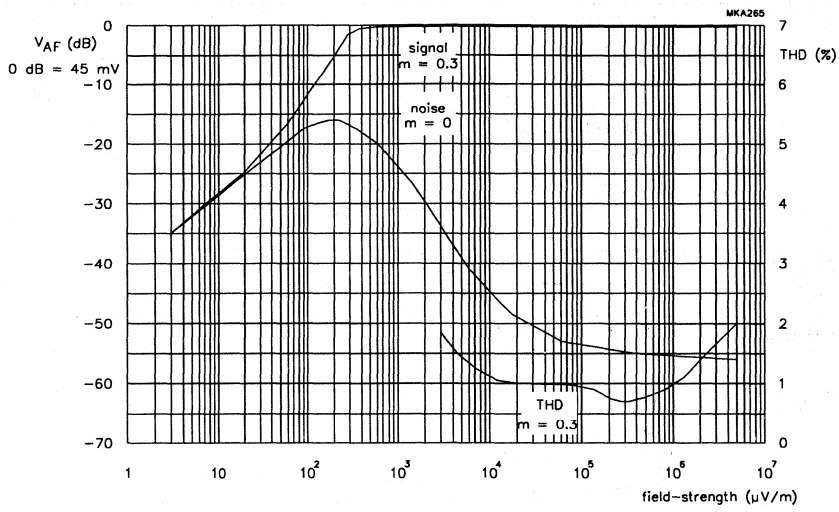


Fig.12 Typical AM audio voltage (V_{AF}; signal at m = 0.3), noise and THD as a function of field-strength (f_i = 1 kHz). Measured in application circuit Fig.8 with V_P = 3.0 V.

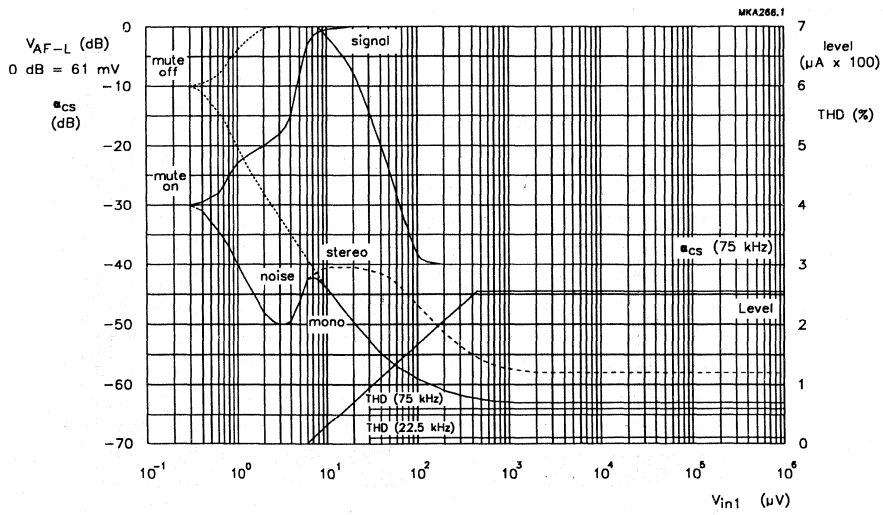


Fig.13 Typical FM audio voltage (V_{AF}; signal), noise, THD (at Δf = 22.5 kHz and Δf = 75 kHz) and indicator current (level) as a function of RF input voltage (V_{in1}; Δf = 22.5 kHz). Curves are shown without mute (mono) and with mute (mono and stereo). Channel separation at Δf = 75 kHz. Measured in test circuit Fig.7 with V_P = 3.0 V.

AM/FM stereo DTS radio circuit TEA5712; TEA5712T

FEATURES

- Wide supply voltage range: 1.8 or 2.1 to 12 V
- Low current consumption: 16 mA at AM, 17 mA at FM
- High selectivity with distributed IF gain
- LED driver for stereo indication
- High input sensitivity: 1.6 mV/m (AM), 2.0 μV (FM) for 26 dB S/N
- Good strong signal behaviour: 10 V/m at AM, 500 mV at FM
- Low output distortion: 0.8% at AM, 0.3% at FM
- Signal level output
- Soft mute
- Signal dependent stereo
- IF output signals available for IF counting
- Designed for simple and reliable printed-circuit board layout
- High impedance MOSFET input on AM.

APPLICATIONS

- Portable AM/FM stereo radio
- Mini/midi receiver sets
- Digitally tuned personal headphone radio.

DESCRIPTION

The TEA5712 is a high performance Bimos IC for use in digitally tuned AM/FM stereo radios. All necessary functions are integrated: from AM and FM front-end to AM detector and FM stereo output stages.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	TYP.
V_P	dynamic supply voltage		1.8	–	12	V
V_P	static supply voltage		2.1	–	12	V
I_P	supply current					
	AM mode		12.8	16.0	20.0	mA
	FM mode		14.3	17.5	21.4	mA
T_{amb}	operating ambient temperature		–15	–	+60	°C
AM performance						
V_{in1}	RF sensitivity		40	55	70	μV
V_{28}	AF output voltage		36	45	70	mV
THD	total harmonic distortion		–	0.8	2.0	%
FM performance						
V_{in3}	RF sensitivity		1.0	2.0	3.8	μV
V_{28}	AF output voltage		50	61	72	mV
THD	total harmonic distortion		–	0.3	0.8	%
MPX performance						
α_{cs}	channel separation		26	30	–	dB
A_{MPX}	MPX voltage gain	V_{AF-L}/V_{in9}; S5 in position MONO	–1.5	0	+1.0	dB
THD	total harmonic distortion		–	0.5	1.0	%

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TEA5712	SDIP32	plastic shrink dual in-line package; 32 leads (400 mil)	SOT232-1
TEA5712T	SO32	plastic small outline package; 32 leads; body width 7.5 mm	SOT287-1

BLOCK DIAGRAM

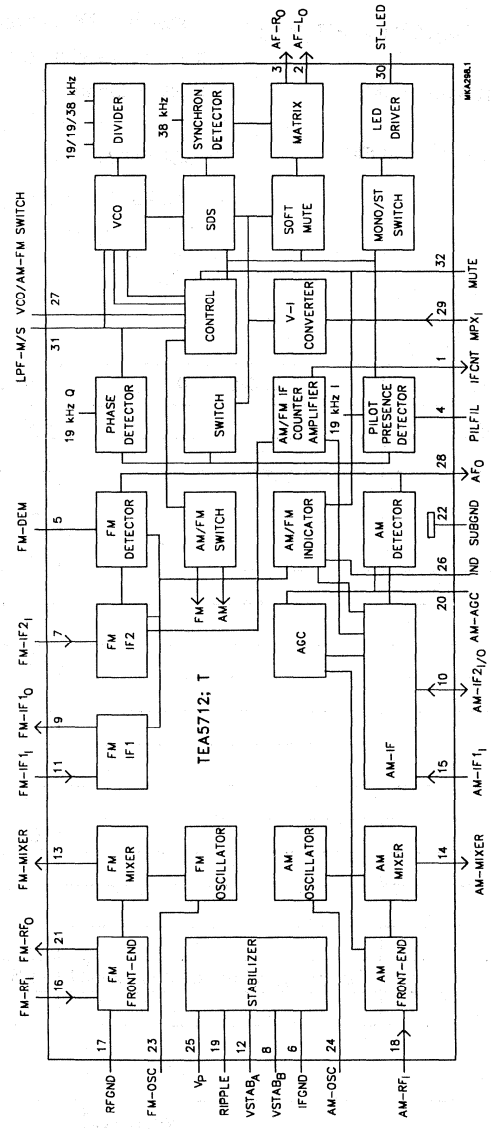


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
IFCNT	1	IF signal output for IF counting
AF-L_O	2	left channel audio output (output impedance typ. 4.3 kΩ)
AF-R_O	3	right channel audio output (output impedance typ. 4.3 kΩ)
PILFIL	4	pilot detector filter pin
FM-DEM	5	ceramic discriminator pin
IFGND	6	ground of IF, detector and MPX stages
FM-IF2_I	7	second FM-IF input (input impedance typ. 330 Ω)
$VSTAB_B$	8	stabilized internal supply voltage (B)
FM-IF1_O	9	first FM-IF output (output impedance typ. 330 Ω)
AM-IF$2_{I/O}$	10	input/output to IFT; output: current source
FM-IF1_I	11	first FM-IF input (input impedance typ. 330 Ω)
$VSTAB_A$	12	stabilized internal supply voltage (A)
FM-MIXER	13	output to ceramic IF filter (output impedance typ. 330 Ω)
AM-MIXER	14	open-collector output to IFT
AM-IF1_I	15	input from IFT or ceramic filter (input impedance typ. 3 kΩ)
FM-RF_I	16	FM-RF aerial input (input impedance typ. 50 Ω)
RFGND	17	FM-RF ground
AM-RF_I	18	parallel tuned AM aerial circuit to ground (total input capacitance typ. 3 pF)
RIPPLE	19	ripple capacitor pin
AM-AGC	20	AGC capacitor pin
FM-RF_O	21	parallel tuned FM-RF circuit to ground
SUBGND	22	substrate and RF ground
FM-OSC	23	parallel tuned FM-oscillator circuit to ground
AM-OSC	24	parallel tuned AM-oscillator circuit to ground
V_P	25	positive supply voltage
IND	26	stop signal output
VCO/AM-FM SWITCH	27	VCO and switch terminal: open for AM; ground for FM
AF_O	28	AM/FM AF output (output impedance typ. 5 kΩ)
MPX_I	29	input for stereo decoder (input impedance typ. 180 kΩ)
ST-LED	30	stereo indicator
LPF-M/S	31	pin for loop-filter and mono/stereo switch
MUTE	32	mute pin

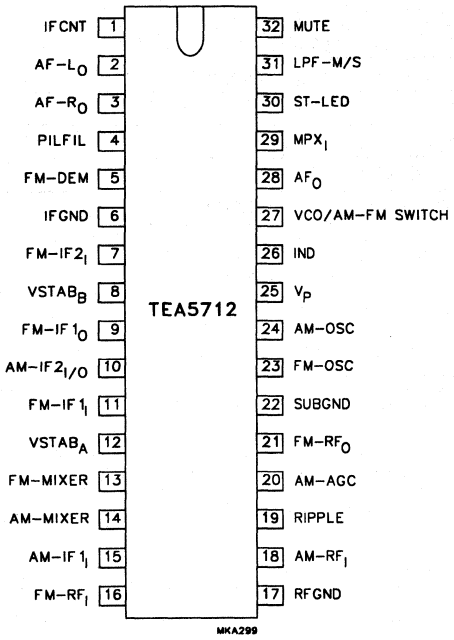


Fig.2 Pin configuration; TEA5712.

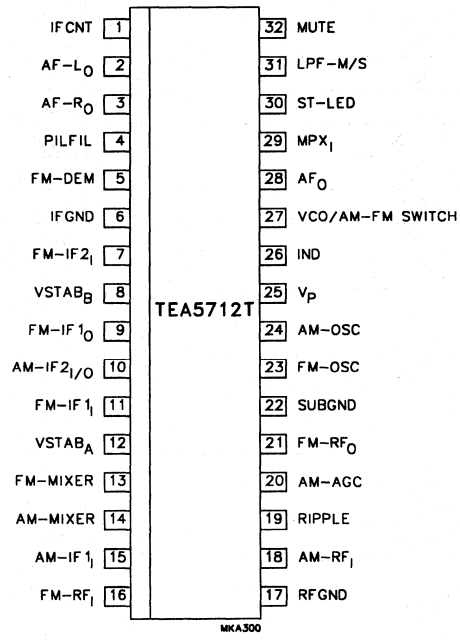


Fig.3 Pin configuration; TEA5712T.

FUNCTIONAL DESCRIPTION

The AM circuit incorporates a double balanced mixer, a one pin low-voltage oscillator (up to 30 MHz) a field-strength indicator output and is designed for distributed selectivity.

The AM input is designed to be connected to the top of a tuned circuit. AGC controls the IF amplification and for large signals it lowers the input impedance.

The first AM selectivity can be an IFT as well as an IFT combined with a ceramic filter; the second one is an IFT.

The FM circuit incorporates a tuned RF stage, a double balanced mixer, a one-pin oscillator, a field-strength indicator output and is designed for distributed IF ceramic filters. The FM quadrature detector uses a ceramic resonator.

The PLL stereo decoder incorporates a signal dependent stereo circuit, a soft-mute circuit and a stereo indicator LED driver.

Supply voltage behaviour

The TEA5712 incorporates internal stabilized power supplies. The maximum supply voltage is 12 V, the minimum voltage can go down temporarily to 1.8 V without any loss in performance.

Due to the capacitor at pin 19 (RIPPLE) the IC gives excellent performance, even when the actual supply voltage at pin 25 (V_P) drops below the voltage at pin 19 (RIPPLE).

Figures 4, 5 and 6 show that V_{stab}, which is dominant for the overall IC performance, remains unaffected, even if V_P drops down to 1.8 V or less. In this typical example the static or average V_P is equal to 2.5 V. Dips in V_{stab} appear only when the peak-to-peak value of the AC-component of $V_P > 2$ V, i.e. when the dynamic value of V_P drops down to 1.5 V for a short moment.

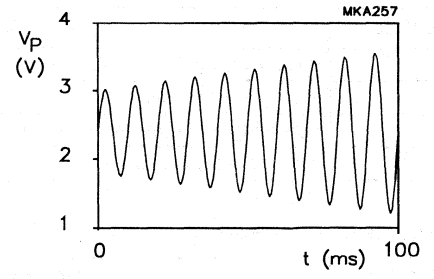


Fig.4 Supply voltage behaviour; V_P as a function of time.

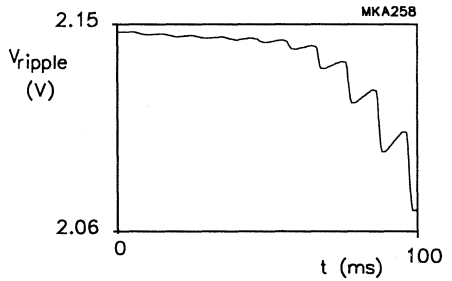


Fig.5 Supply voltage behaviour; V_{ripple} as a function of time.

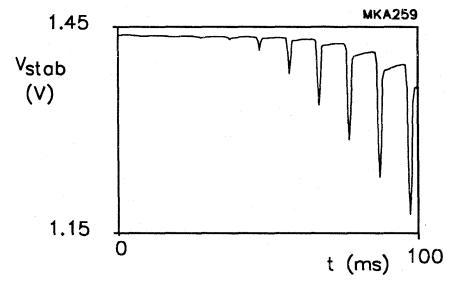


Fig.6 Supply voltage behaviour; V_{stab} as a function of time.

LIMITING VALUES

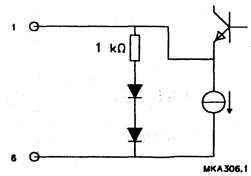
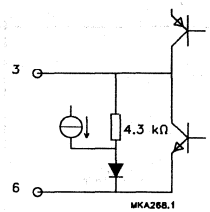
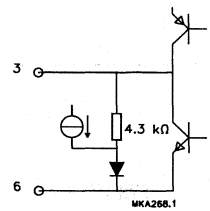
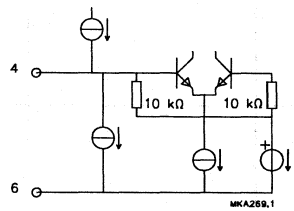
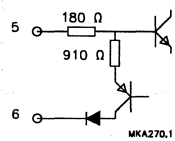
In accordance with the Absolute Maximum Rating System (IEC 134).

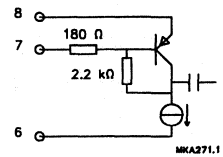
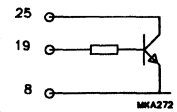
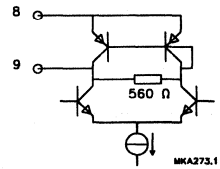
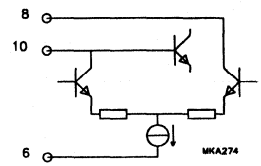
SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_P	supply voltage	0	12	V
T_{stg}	storage temperature	−55	+150	°C
T_{amb}	operating ambient temperature	−15	+60	°C
T_j	junction temperature	−15	+150	°C

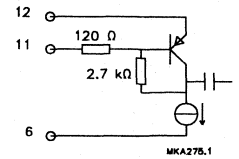
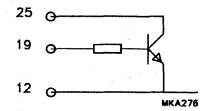
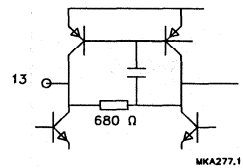
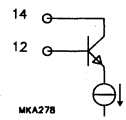
THERMAL CHARACTERISTICS

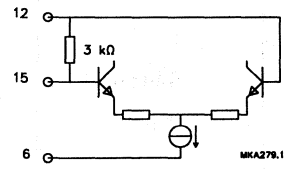
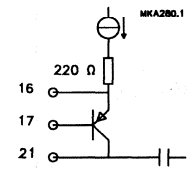
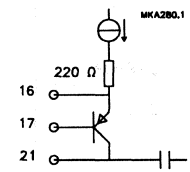
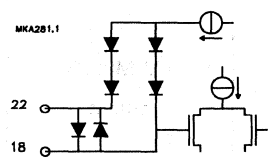
SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air		
	SDIP32	54	K/W
	SO32	68	K/W

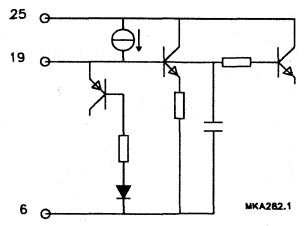
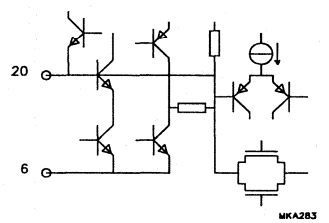
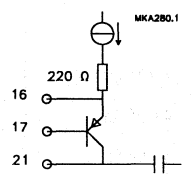
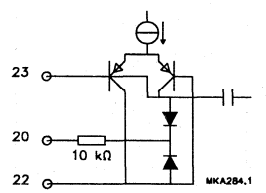
CIRCUIT DESIGN DATA

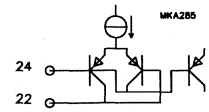
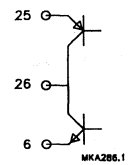
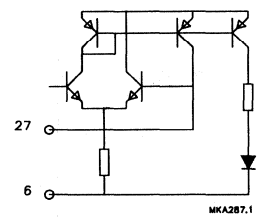
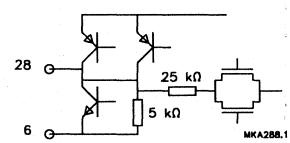
PIN NO.	PIN SYMBOL	DC PIN VOLTAGE (V)		EQUIVALENT CIRCUIT
		AM	FM	
1	IFCNT output	0.3	0.3	
2	AF-L_O output	0.65	0.65	
3	AF-R_O output	0.65	0.65	
4	PILFIL	0.95	0.95	
5	FM-DEM	–	1.0	

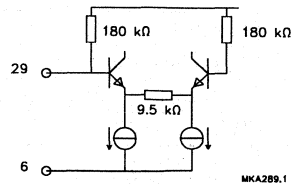
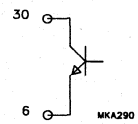
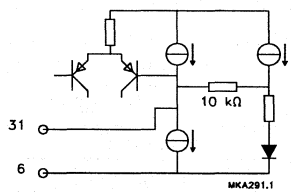
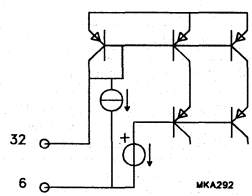
PIN NO.	PIN SYMBOL	DC PIN VOLTAGE (V)		EQUIVALENT CIRCUIT
		AM	FM	
6	IFGND	0	0	
7	$FM\text{-}IF2_I$ input	–	0.73	
8	$VSTAB_B$	1.4	1.4	
9	$FM\text{-}IF1_O$ output	–	0.69	
10	$AM\text{-}IF2_{I/O}$ input/output	1.4	1.4	

PIN NO.	PIN SYMBOL	DC PIN VOLTAGE (V)		EQUIVALENT CIRCUIT
		AM	FM	
11	FM-IF1$_I$ input	–	0.73	
12	VSTAB$_A$	1.4	1.4	
13	FM-MIXER output	–	1.0	
14	AM-MIXER output	1.4	1.4	

PIN NO.	PIN SYMBOL	DC PIN VOLTAGE (V)		EQUIVALENT CIRCUIT
		AM	FM	
15	AM-IF1$_I$ input	1.4	1.4	
16	FM-RF$_I$ input	–	0.73	
17	RFGND	0	0	
18	AM-RF$_I$ input	0	0	

PIN NO.	PIN SYMBOL	DC PIN VOLTAGE (V)		EQUIVALENT CIRCUIT
		AM	FM	
19	RIPPLE	2.1	2.1	
20	AM-AGC	0.1	0.7	
21	FM-RF$_O$	0	0	
22	SUBGND	0	0	
23	FM-OSC	0	0	

PIN NO.	PIN SYMBOL	DC PIN VOLTAGE (V)		EQUIVALENT CIRCUIT
		AM	FM	
24	AM-OSC	0	0	
25	V_P	3.0	3.0	
26	IND output	3.0	3.0	
27	VCO and AM/FM switch	1.3	0.95	
28	AF output	0.6	0.7	

PIN NO.	PIN SYMBOL	DC PIN VOLTAGE (V)		EQUIVALENT CIRCUIT
		AM	FM	
29	MPX input	1.23	1.23	
30	ST-LED	3.0	3.0	
31	LPF-M/S	0.1	0.8	
32	MUTE	0.7	0.7	

AM CHARACTERISTICS

f_i = 1 MHz; m = 0.3; f_m = 1 kHz; V_P = 3.0 V; measured in Fig.7 with S1 in position B, S2 in position A and S7 in position A; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_P	supply current	no input signal	12.8	16.0	20.0	mA
C_i	input capacitance	V_{20} = 0.2 V	–	3	–	pF
G_c	front-end conversion gain	V_{20} = 0.2 V	1.8	3.3	5.0	
V_{in1}	RF sensitivity	S/N = 26 dB	40	55	70	μV
V_{in2}	IF sensitivity	V_{28} = 30 mV; S1 in position A	0.13	0.2	0.45	mV
V_{28}	AF output voltage	V_{in2} = 3.16 mV; S1 in position A	36	45	70	mV
THD	total harmonic distortion	V_{in1} = 1 mV	–	0.8	2.0	%
V_{in1}	large signal handling	m = 0.8; THD ≤ 8%	150	300	–	mV
I_{IND}	indicator current	V_{in2} = 100 mV; S1 in position A	120	170	230	μA
I_{INDOFF}	indicator OFF current	V_{in2} = 0 V; S1 in position A	–	0	10	μA
$V_{IFCNTO(p-p)}$	IF count output signal (peak-to-peak value)	V_{in2} = 10 V; S4 open	–	400	–	mV
V_{IFCNT}	IF count signal	V_{in10} = 3 V; S4 closed	–	–70	–	dB

FM CHARACTERISTICS

f_i = 100 MHz; Δf = 22.5 kHz; f_m = 1 kHz; V_P = 3.0 V; measured in Fig.7 with S1 in position B, S2 in position A and S7 in position A; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_P	supply current	no input signal	14.3	17.5	21.4	mA
V_{in3}	RF limiting sensitivity	V_{28} = –3 dB	0.4	1.2	3.8	μV
V_{in3}	RF sensitivity	S/N = 26 dB	1.0	2.0	3.8	μV
V_{11}/V_{in3}	front-end voltage gain	V_{in3} ≤ 1 mV; including ceramic filter K1	12	18	22	dB
V_{in4}	IF sensitivity	S2 in position B; V_{28} = –3 dB	–	20	30	μV
V_{28}	AF output voltage	V_{in3} = 1 mV	50	61	72	mV
THD	total harmonic distortion	V_{in3} = 1 mV; Δf = 22.5 kHz	–	0.3	0.8	%
V_{in3}	large signal handling	THD ≤ 5%	–	500	–	mV
I_{IND}	indicator current	V_{in4} = 100 mV; S2 in position B	190	255	320	μA
I_{INDOFF}	indicator OFF current	V_{in4} = 0 V; S2 in position B	–	0	2	μA
$V_{IFCNTO(p-p)}$	IF count output signal (peak-to-peak value)	V_{in4} = 10 V; S4 open	–	360	–	mV
V_{IFCNT}	IF count signal	V_{in10} = 3 V; S4 closed	–	–50	–	dB

STEREO DECODER CHARACTERISTICS

f_i = 1 kHz; $V_{in9(L+R)}$ = 195 mv; pilot = 20 mV; V_P = 3.0 V; measured in Fig.7 with S1 in position B, S2 in position A, S6 in position A, S7 in position A and S5 in position STEREO; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
A_{MPX}	MPX voltage gain V_{AF-L}/V_{in9}	S5 in position MONO	−1.5	0	+1.0	dB
THD	total harmonic distortion		–	0.5	1.0	%
(S+N)/N	signal plus noise-to-noise ratio	pilot = 20 mV	–	74	–	dB
α_{cs}	channel separation	L = 1; R = 0 or L = 0; R = 1	26	30	–	dB
SC	stereo control	V_{in3} = 120 μV	–	30	–	dB
		V_{in3} = 10 μV	–	1	–	dB
α_{MUTE}	AF output signal suppression	$V_{in3} \leq 2$ μV	–	20	–	dB

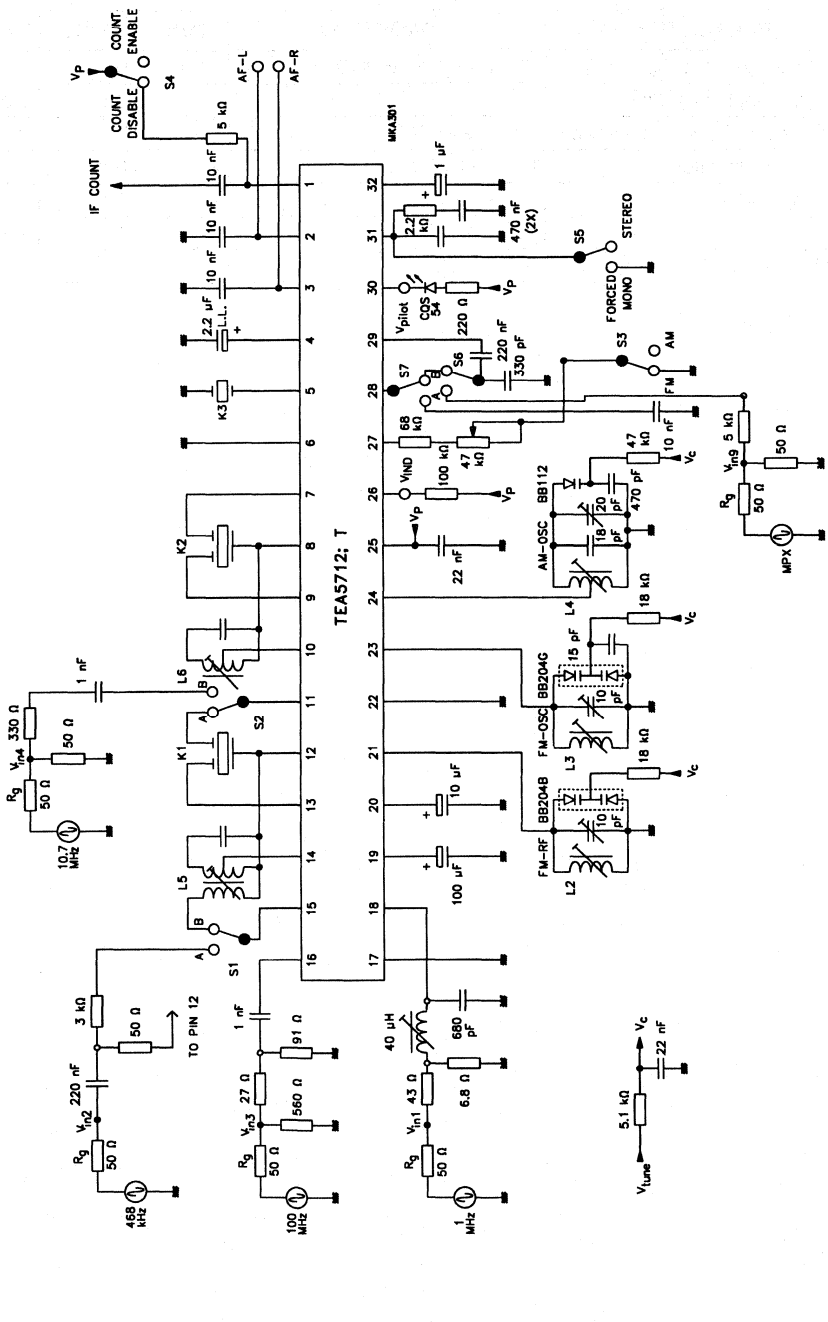


Fig.7 Test circuit.

APPLICATION INFORMATION

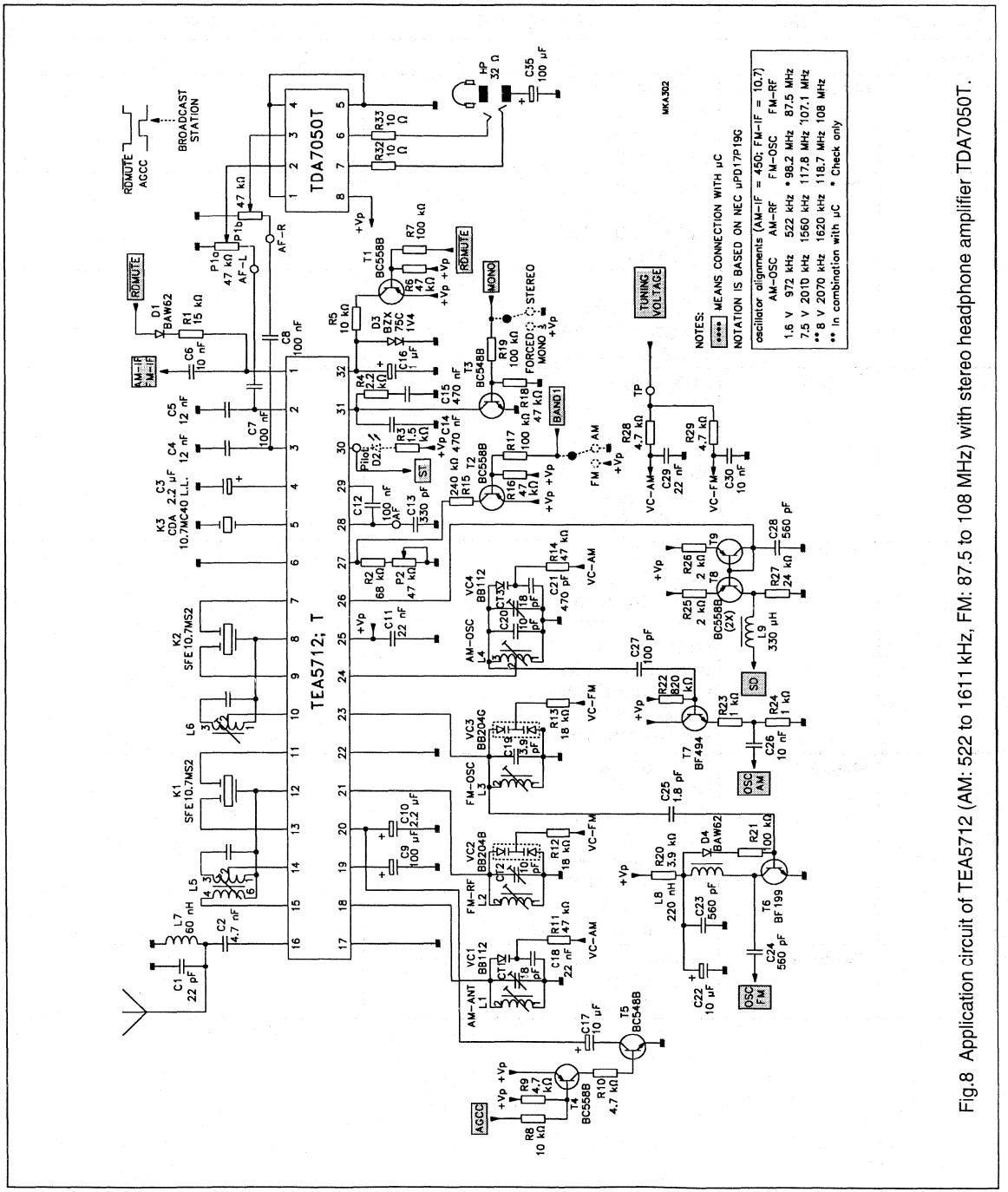
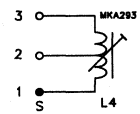
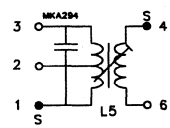
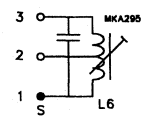
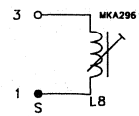


Fig.8 Application circuit of TEA5712 (AM: 522 to 1611 kHz, FM: 87.5 to 108 MHz) with stereo headphone amplifier TDA7050T.

Components for Fig.8

NUMBER	TYPE	DESCRIPTION	CIRCUIT
Coils			
L1	AM-AERIAL	ferroceptor length = 6 cm L1-2 = 203 µH unloaded Q	
L2	FM-RF	L1-2 = 90 nH N1-2 = 2.5 turns unloaded Q = 150T TOKO type S18	
L3	FM-OSC	L1-2 = 70 nH N1-2 = 1.5 turns unloaded Q = 150 TOKO type S18	
L4	AM-OSC	L1-3 = 98 µH N1-2 = 12 N2-3 = 39 unloaded Q = 100 wire diameter 0.07 mm TOKO type 7P material TOKO 7BRS	
L5	AM-IF1	L1-3 = 625 µH N1-2 = 17 turns N2-3 = 141 turns N4-6 = 10 turns C1-3 = 180 pF unloaded Q = 90 wire diameter 0.07 mm TOKO type 7P material TOKO 7MCS	
L6	AM-IF2	L1-3 = 625 µH N1-2 = 28 turns N2-3 = 130 turns C1-3 = 180 pF unloaded Q = 90 wire diameter 0.07 mm TOKO type 7P material TOKO 7MCS	
L7	FM-AERIAL	printcoil L1-2 = 60 nH N1-2 = 2.5 turns	

NUMBER	TYPE	DESCRIPTION	CIRCUIT
L8	AM-RF	test circuit only: L1-3 = 40 µH N1-3 = 34 turns unloaded Q = 85 wire diameter 0.09 mm TOKO type 7P material TOKO 7BRS	
Ceramic filters			
K1	FM-IF1	Murata SFE 10.7 MS 2	
K2	FM-IF2	Murata SFE 10.7 MS 2	
K3	FM-DET	Murata CDA 10.7 MC 40	
Variable capacitance diodes			
	FM-RF	BB204B	
	FM-OSC	BB204G	
	FM-RF	BB112	
	AM-OSC	BB112	

Application remarks

- Short circuiting: **all** pins are short-circuit proof except **pin 16** (FM-RF$_I$) with respect to the supply voltage pin.
- Align VCO with aerial signal present.

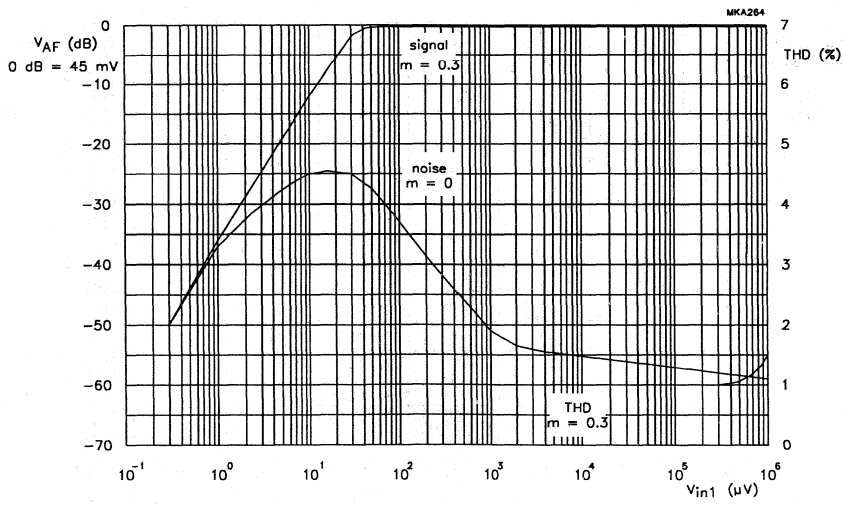


Fig.9 Typical AM audio voltage (V_{AF}; signal at m = 0.3), noise and THD as a function of RF input voltage (V_{in1}; f_i = 1 kHz). Measured in test circuit Fig.7 with V_P = 3.0 V.

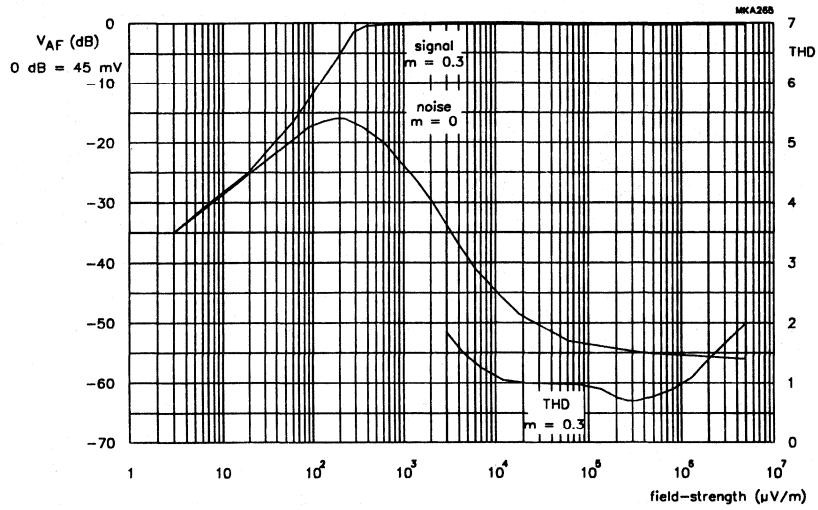


Fig.10 Typical AM audio voltage (V_{AF}; signal at m = 0.3), noise and THD as a function of field-strength (f_i = 1 kHz). Measured in application circuit Fig.8 with V_P = 3.0 V.

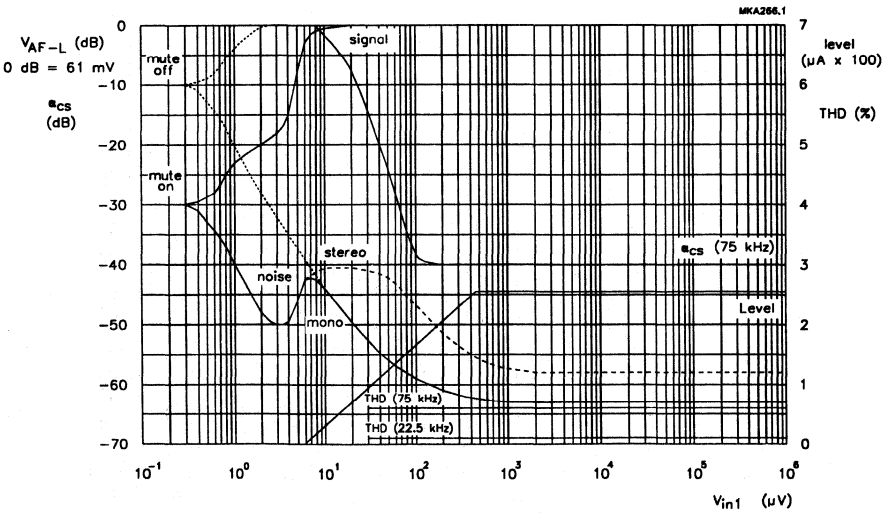


Fig.11 Typical FM audio voltage (V_{AF}; signal), noise, THD (at Δf = 22.5 kHz and Δf = 75 kHz) and indicator current (level) as a function of RF input voltage (V_{in1}; Δf = 22.5 kHz). Curves are shown without mute (mono) and with mute (mono and stereo). Channel separation at Δf = 75 kHz. Measured in test circuit Fig.7 with V_P = 3.0 V.

Self tuned radio TEA5757

FEATURES

- The tuning quality is superior and requires no IF-counter for stop-detection; it is insensitive to ceramic filter tolerances
- The tuning system has an optimized IC partitioning both from application (omitting interferences) and flexibility (removable front panel option) point of view: The tuning synthesizer is on chip with the radio
- Preset mode, manual-search, auto-search and auto-store operations in combination with the microcontroller are fast and consuming low power
- The microcontroller software will be reduced and highly simplified, because of the local (internal) controller function
- The high integration level - radio and tuning synthesizer on one chip - means fewer external components with regard to the communication between the radio and the microcontroller (90% less components compared to the digital tuning application of a radio IC with external PLL tuning function) and a simple and small PCB
- On mentioned quality and high integration level: There will be no application considerations for the tuning system, since there will be no external 100 MHz buffers, no loop filter, no false lock elimination
- The inherent FUZZY LOGIC behaviour of STR (Self Tuned Radio), which mimics hand tuning, yields a potentially fast yet reliable tuning operation
- The level of the incoming signal at which the radio must lock is adjustable (via software as well as analog)
- Two programmable ports
- High selectivity with distributed IF gain
- Soft mute
- Signal dependent stereo-blend
- High impedance MOSFET input on AM
- Wide supply voltage range 2.1 V to 12 V
- Low current consumption 15 mA at AM, 18 mA at FM (including tuning synthesizer)
- High input sensitivity
- Low output distortion
- Due to the new tuning concept the tuning is independent of the channel spacing.

GENERAL DESCRIPTION

The TEA5757 is a 44-pins integrated AM/FM stereo radio circuit including a novel tuning concept. The radio part is identical to the TEA5712.
The new tuning concept combines the advantages of hand tuning with electronic tuning facilities and features. User 'intelligence' is incorparated into the tuning algorithm and an improvement of the analog signal processing is used for the AFC function.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TEA5757H	44	QFP	plastic	SOT307

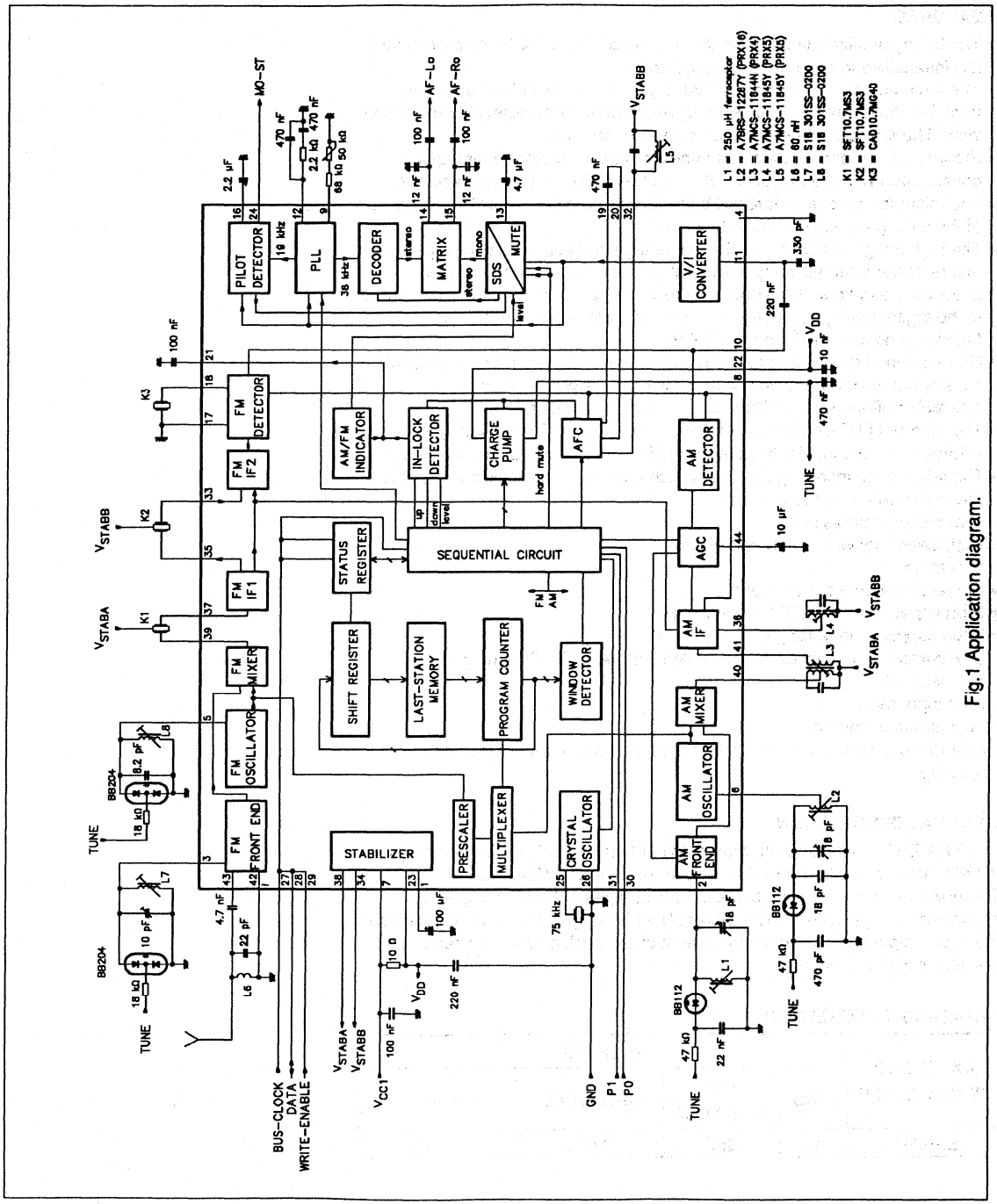


Fig.1 Application diagram.

QUICK REFERENCE DATA

Conditions AM: f_i = 1 MHz; m = 0.3; f_m = 1 kHz; V_{CC1} = 3.0 V; V_{CC2} = 12 V; V_{DD} = 3 V; measured in Fig.11 with S1 in position A, S2 in position B, unless otherwise specified.
Conditions FM: f_i = 100 MHz; Δf = 22.5 kHz; f_m = 1 kHz; V_{CC1} = 3.0 V; V_{CC2} = 12 V; V_{DD} = 3 V; measured in Fig.11 with S2 in position A, S3 in position A and S5 in position A, unless otherwise specified.
Conditions MPX: f_i = 1 kHz; $V_{in3(L+R)}$ = 155 mV; V_{pilot} = 15.5 mV; V_{CC1} = 3.0 V; V_{CC2} = 12 V; V_{DD} = 3 V; measured in Fig.11 with S2 in position B and S3 in position B, unless otherwise specified.

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC1}	static supply voltage	2.1	–	12	V
V_{CC2}	second supply voltage for tuning	–	–	12	V
I_{VCC1}	supply current				
	AM	12	15	18	mA
	FM	13	16	19	mA
I_{VCC2}	supply current V_{CC2}	–	–	640	μA
V_{tune}	tuning voltage	0.7	–	V_{CC2} – 0.75	V
T_{amb}	operating ambient temperature	–15	–	+60	°C
AM performance					
V_{in1}	RF sensitivity	40	55	70	μV
V_{10}	AF output voltage	36	45	70	mV
THD	total harmonic distortion	–	0.8	2.0	%
FM performance					
V_{in5}	RF sensitivity	0.4	1.2	3.8	μV
V_{10}	AF output voltage	40	48	57	mV
THD	total harmonic distortion	–	0.3	0.8	%
MPX performance					
α_{cs}	channel separation	26	30	–	dB

PINNING

SYMBOL	PIN	DESCRIPTION
RIPPLE	1	ripple capacitor pin
AM-RFi	2	AM-RF input
FM-RFo	3	parallel tuned FM-RF circuit to ground
SUBGND	4	substrate and RF ground
FM-OSC	5	parallel tuned FM-oscillator circuit to ground
AM-OSC	6	parallel tuned AM-oscillator circuit to ground
V_{CC1}	7	positive supply voltage
TUNE	8	tuning output current
VCO	9	voltage controlled oscillator pin
AFo	10	AM/FM AF output (output impedance typical 5 kΩ)
MPXi	11	input for stereo decoder (input impedance typical 150 kΩ)
LPF	12	pin for loop-filter
MUTE	13	mute pin
AF-Lo	14	left channel output (output impedance typical 4.3 kΩ)
AF-Ro	15	right channel output (output impedance typical 4.3 kΩ)
PILFIL	16	pilot detector filter pin
IFGND	17	ground of IF, detector and MPX stages
FM-DEM	18	ceramic discriminator pin
AFC-NEG	19	negative output of the AFC
AFC-POS	20	positive output of the AFC
INDICATOR	21	field-strength indicator
V_{CC2}	22	supply voltage for tuning
V_{DD}	23	supply voltage for digital circuits
MO-ST	24	pin for mono/stereo and tuning indication
XTAL	25	crystal input
DGND	26	digital ground
BUS-CLOCK	27	clock input of the bus
DATA	28	data input/output of the bus
WRITE-ENABLE	29	write-enable input of the bus
P0	30	programmable output port (P0)
P1	31	programmable output port (P1)
AFC-AM	32	pin for 450 kHz LC-circuit
FM-IF2i	33	second FM-IF input (input impedance typical 330 Ω)
V_{STABB}	34	internal stabilized supply voltage (B)
FM-IF1o	35	first FM-IF output (output impedance typical 330 Ω)
AM-IF2i/o	36	input/output to IFT; output: current source
FM-IF1i	37	first FM-IF input (input impedance typical 330 Ω)
V_{STABA}	38	internal stabilized supply voltage (A)
FM-MIXER	39	output to ceramic filter (output impedance typical 330 Ω)
AM-MIXER	40	open-collector output to IFT
AM-IF1i	41	input from IFT or ceramic filter (input impedance typical 3 kΩ)
RFGND	42	FM-RF ground
FM-RFi	43	FM-RF aerial input (input impedance typical 50 Ω)
AGC	44	AGC capacitor pin

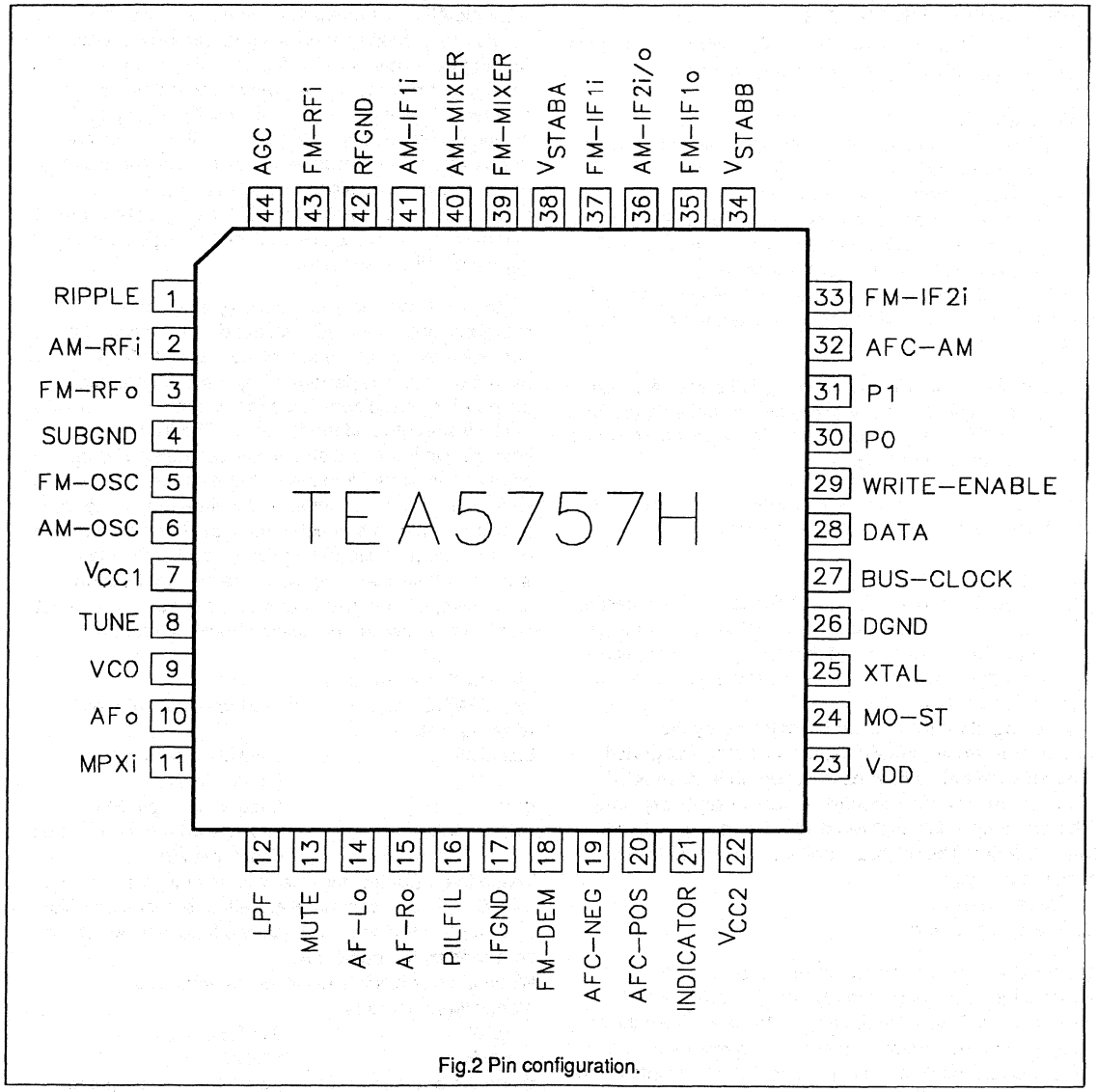


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The TEA5757 is an integrated AM/FM stereo radio circuit including digital tuning and control functions.

The radio

The AM circuit incorporates a double balanced mixer, a one-pin low voltage oscillator (up to 30 MHz) and is designed for distributed selectivity.
The AM input is designed to be connected to the top of a tuned circuit. AGC controls the IF amplification and for large signals it lowers the input impedance.
The first AM selectivity can be an IF-Tank (IFT) as well as an IFT combined with a ceramic filter; the second one is an IFT.

The FM circuit incorporates a tuned RF stage, a double balanced mixer, a one-pin oscillator and is designed for distributed IF ceramic filters. The FM quadrature detector uses a ceramic resonator.

The PLL stereo decoder incorporates a signal dependent stereo-blend circuit and a soft-mute circuit.

Tuning

The tuning-concept of STR (Self Tuned Radio) is based on FUZZY LOGIC: it mimics hand tuning (hand tuning is a combination of coarse and fine tuning to the qualitively best frequency position). As a consequence the tuning system is very fast.
The tuning algorithm, which is controlled by the sequential circuit (see Fig.1), is completely integrated. So there are only a few external components needed. The bus and the microcontroller can be kept very simple. The bus only exists of three wires (bus-clock, data and write enable). The microcontroller must basically give two instructions:
1. Preset operation
2. Search operation

In preset mode, the microcontroller has to load information such as frequency band, frequency and mono/stereo. This information has to be send via the bus to STR. Now the internal algorithm controls the tuning sequence as follows: the information is loaded into a shift register, a last-station memory and the counter.
At first the Automatic Frequency Control (AFC) is switched off. The counter starts counting the frequency and the tuning voltage is varied until the desired frequency roughly equals the real frequency. Subsequently, the AFC will be switched on and the counter will be switched off. The real frequency now is more precisely tuned to the desired frequency: FM ± 1 kHz, AM ± 0.1 kHz.

After the AFC has tuned the real frequency to the desired frequency an in-lock signal can be generated. In order to get a reliable in-lock signal, there are two parameters measured: the field strength and the S-curve. The field strength indicates the strength of the station and by looking at the S-curve the system can distinguish false in-locks from real in-locks (false in-locks occur on the wrong slope of the S-curve).
In case of fading or pulling the in-lock signal becomes '0' and the synthesizer will be switched on again and the algorithm will be repeated.

During a search operation, the only action the microcontroller has to take is: sending the desired band plus the direction of the search operation to STR. The search operation is performed by the charge pump until an in-lock signal is generated (combination of measuring the field strength and the S-curve). The frequency belonging to the found station will be counted by the counter and written into the last-station memory and the shift register of the counter. At this time the frequency is available in the shift register and can eventually be read by the microcontroller. The microcontroller decides whether the frequency is within the desired frequency band. If so, this frequency can be stored under a preset and if not, a new search action should be started.

Description of the bus

The TEA5757 radio has a bus which exists of three wires, namely:

bus-clock	software driven clock (input, pin 27)
data	(input/output, pin 28)
write enable	enables write or read action (input, pin 29)

These three signals, together with the mono/stereo pin (MO-ST, pin 24), communicate with the microcontroller. The mono/stereo indicator has two functions, which are controlled by the bus-clock.
When the bus-clock is LOW, pin 24 indicates mono/stereo operation

LOW	...	STEREO
HIGH	...	MONO

When the bus-clock is HIGH, pin 24 indicates tuning information

LOW	...	tuned
HIGH	...	not tuned

The TEA5757 has a 25-bits shift register with the following configuration:

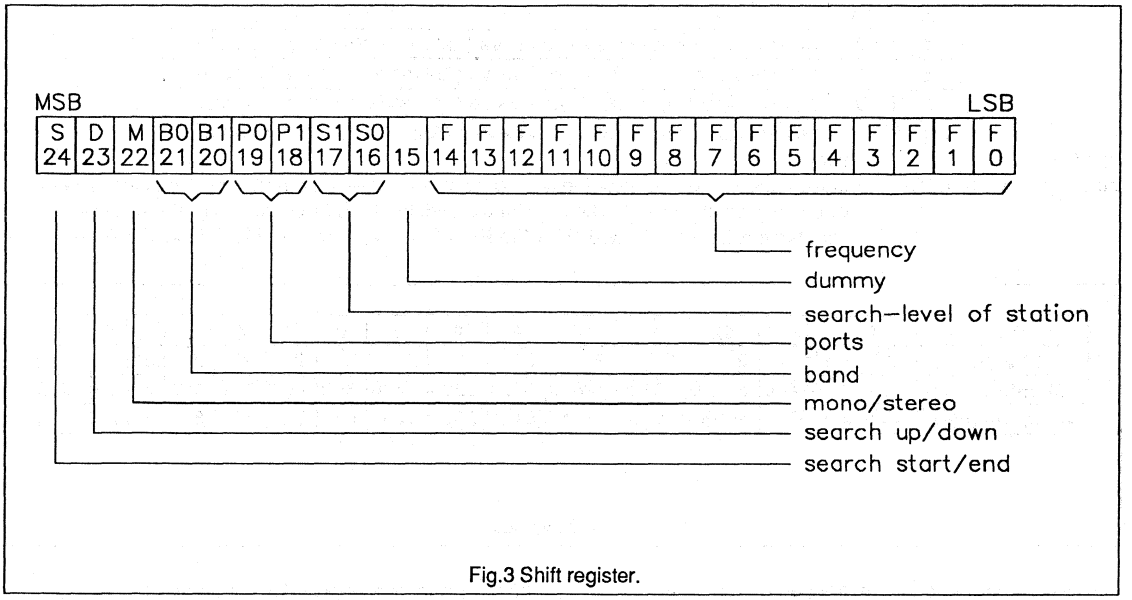


Fig.3 Shift register.

Explanation of the shift register bits:

bit 24 (MSB) : 0 - after a search when a station is found or after a preset
: 1 - during the search action

bit 23 : 0 - indicates whether the radio has to search down
: 1 - indicates whether the radio has to search up

bit 22 : 0 - stereo is allowed
: 1 - mono is required (radio switched to forced mono)

bits 21 and 20 :

B0	B1	band select
0	0	FM
0	1	MW
1	0	LW
1	1	SW

bits 19 and 18 : these bits are user programmable and can e.g. be used as band switch drivers. The truth table can look as follows:

P0	P1	band select
0	0	FM or MW
0	1	LW
1	0	SW

The bits P0 and P1 match to the output pins P0 (pin 30) and P1 (pin 31). The output pins can drive currents up to 5 mA.

bits 17 and 16 : these bits determine the field strength at which the radio during an automatic search, automatic store or manual search must lock.

S0	S1	
0	0	receive signals from 5 μV and above (AM mode: 28 μV and more)
0	1	receive signals from 10 μV and above (AM mode: 40 μV and more)
1	0	receive signals from 30 μV and above (AM mode: 63 μV and more)
1	1	receive signals from 150 μV and above (AM mode: 1000 μV and more)

bit 15 : buffer

bit 14 up to bit 0 (LSB) : these fifteen bits determine the frequency at which the radio has to be / is tuned. The bit values are given in Fig.4. The FM VALUE and the AM VALUE are the values of the affected oscillators. (FM VALUE = FM-RF + FM-IF and AM VALUE = AM-RF + AM-IF)

BIT	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IT value	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}
FM value (kHz)	–	102400	51200	25600	12800	6400	3200	1600	800	400	200	100	50	25	12.5
AM value (kHz)	16384	8192	4096	2048	1024	512	256	128	64	32	16	8	4	2	1

Fig.4 Bit values.

If in search mode no transmitter can be found, all frequency bits of the shift register are set to '1'.

The bus protocol is depicted in Figs 5 and 6.

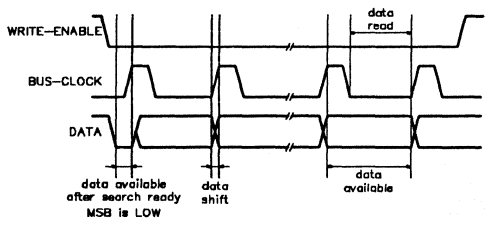


Fig.5 Read data from TEA5757.

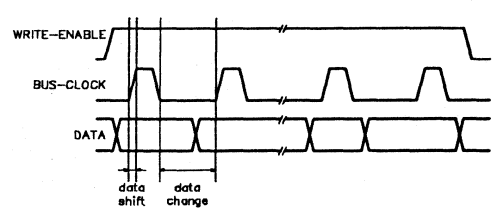


Fig.6 Write data to TEA5757.

Reading data from TEA5757

While write enable is LOW data can be read by the microcontroller. At a rising edge of the bus-clock, data is shifted out of the register. This data is available from the point where the bus-clock is HIGH until the next rising edge of the bus-clock occurs.

To read the entire shift register 24 clock pulses are necessary.

Writing data into TEA5757

While write enable is HIGH the microprocessor can transmit data to the TEA5757 (hard mute is active). At a rising edge of the bus-clock, the register shifts and accepts one bit into LSB. At clock LOW the microprocessor writes data.

To write the entire shift register 25 clock pulses are necessary.

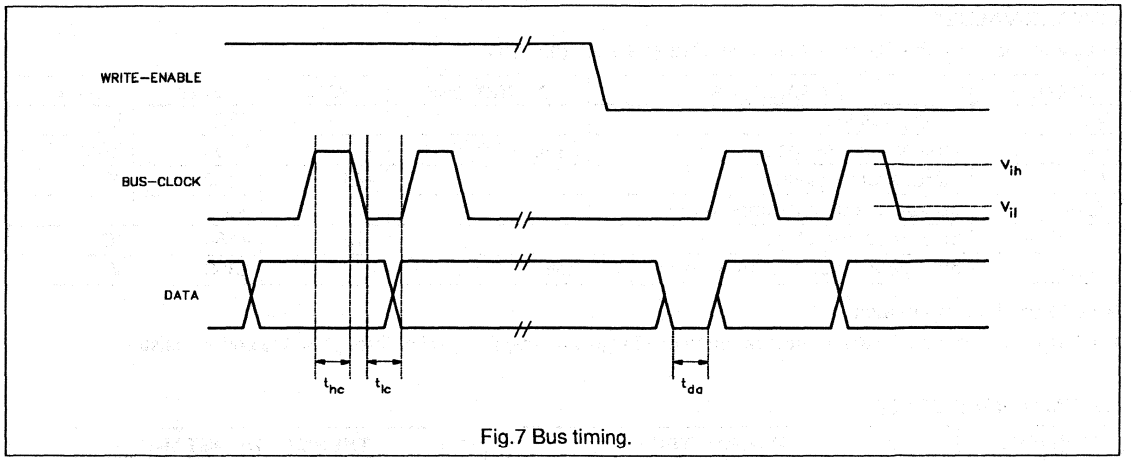


Fig.7 Bus timing.

Table 1 Digital inputs.

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
Digital inputs				
V_{ih}	HIGH level input voltage	1.4	–	V
V_{il}	LOW level input voltage	–	0.6	V
Timing				
F_c	clock input	–	300	kHz
t_{hc}	clock HIGH time	1.67	–	µs
t_{lc}	clock LOW time	1.67	–	µs
t_{da}	shift register available after 'search ready'	–	10	µs

Supply voltage behaviour

The TEA5757 incorporates internal stabilized power supplies. The maximum supply voltage is 12 V, the minimum voltage is 2.1 V. It can temporarily go down to 1.8 V without any loss in performance at the audio output. Due to the capacitor at pin 1 (RIPPLE) the IC gives excellent performance, even when the actual supply voltage at pin 7 (V_{CC1}) drops below the voltage at pin 1 (RIPPLE).

Figs 8 to 10 show that the voltage at pin 38 (V_{STABA}) and pin 34 (V_{STABB}), which is dominant for the overall IC performance, remains unaffected, even if V_{CC1} drops down to 1.8 V or less. In this typical example the static or average V_{CC1} is equal to 2.5 V. Dips in V_{STABA} and V_{STABB} appear only when the peak-to-peak value of the AC-component of V_{CC1} is > 2 V, i.e. when the dynamic value of V_{CC1} drops down to 1.5 V for a short moment.

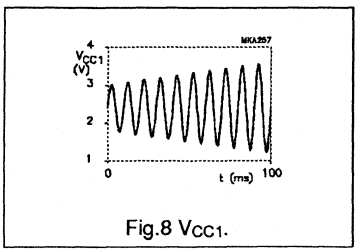


Fig.8 V_{CC1}.

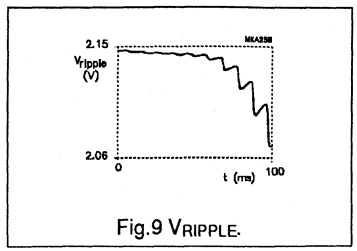


Fig.9 V_{RIPPLE}.

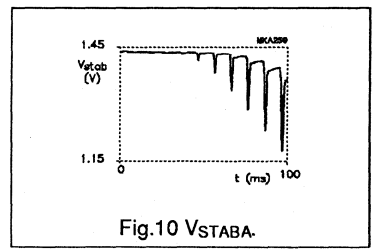


Fig.10 V_{STABA}.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC1}	supply voltage		0	13.2	V
P_{tot}	total power dissipation	T_{amb} = +70 °C	–	250	mW
T_{stg}	storage temperature		–65	+150	°C
T_{amb}	operating ambient temperature		–15	+60	°C
T_j	junction temperature		–15	+150	°C
V_{ESD}	electrostatic handling for all pins	note 1	–	±300	V

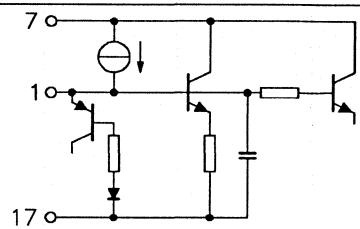
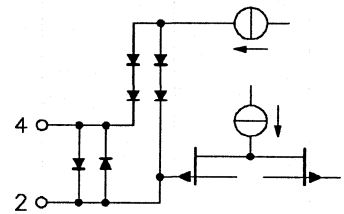
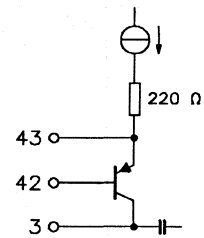
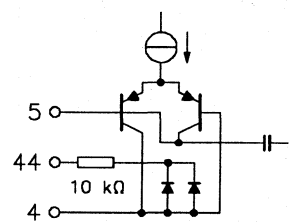
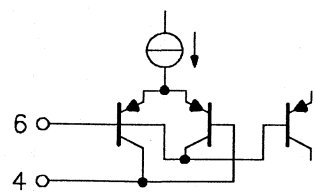
Note to the limiting values

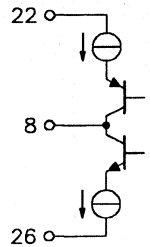
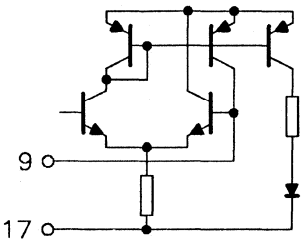
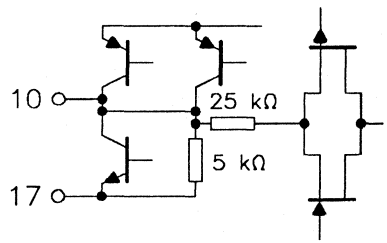
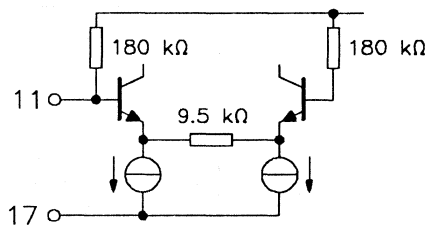
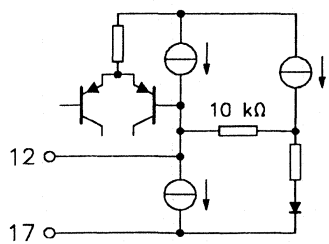
1. Charge device model class B: equivalent to discharging a 200 pF capacitor through a 0 Ω series resistor.

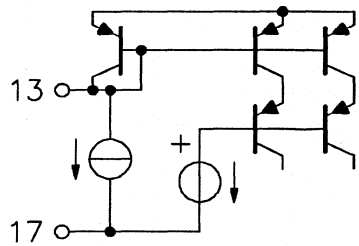
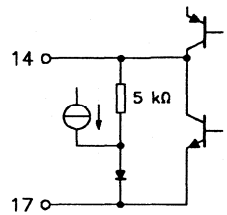
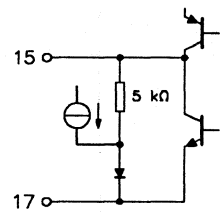
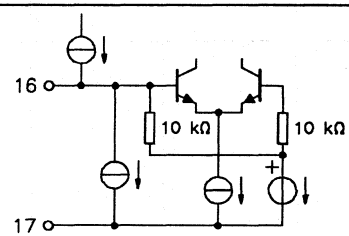
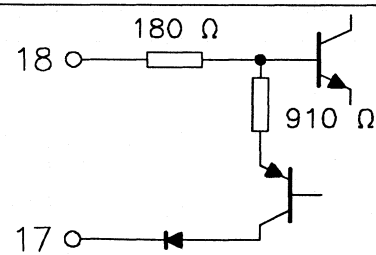
THERMAL RESISTANCE

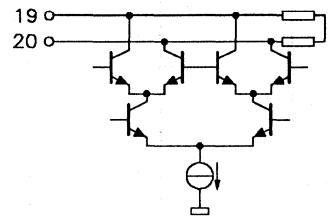
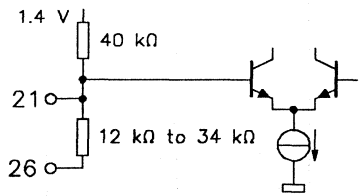
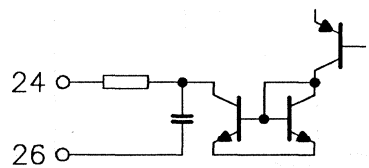
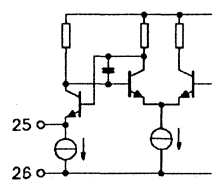
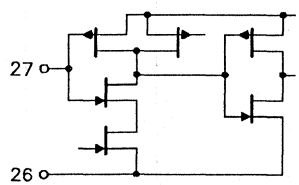
SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient in free air	65 K/W

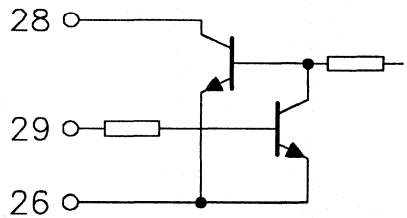
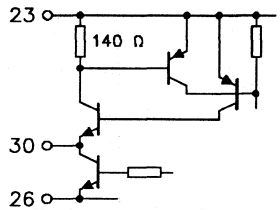
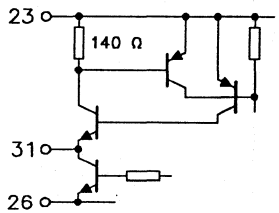
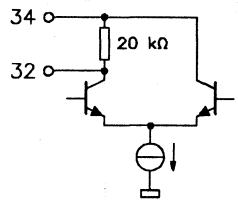
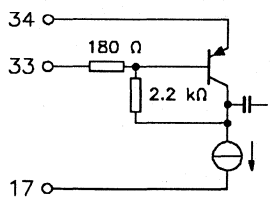
Table 2 Equivalent pin circuits and pin voltages.

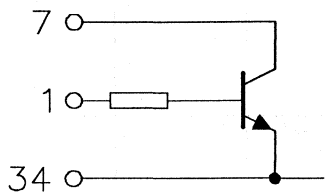
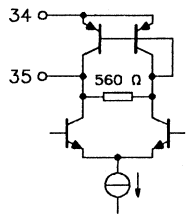
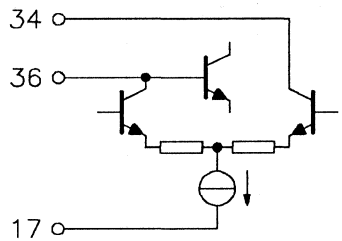
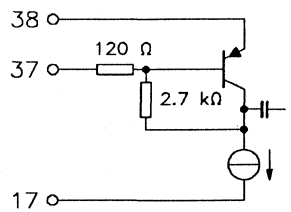
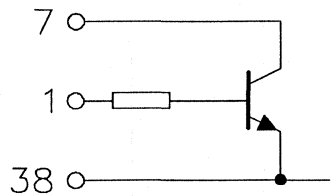
PIN NO.	PIN SYMBOL	DC VOLTAGE (V) AM	DC VOLTAGE (V) FM	EQUIVALENT CIRCUIT
1	RIPPLE	2.1	2.1	
2	AM-RFi	0	0	
3	FM-RFo	0	0	
43	FM-RFi	–	0.73	
4	SUBGND	0	0	
5	FM-OSC	0	0	
6	AM-OSC	0	0	
7	V_{CC1}	3.0	3.0	

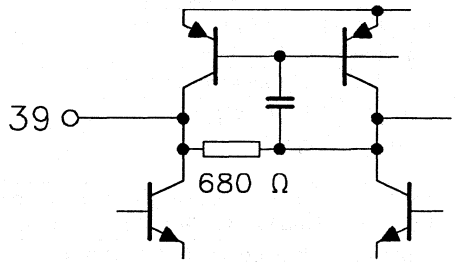
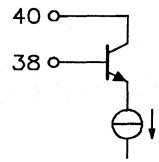
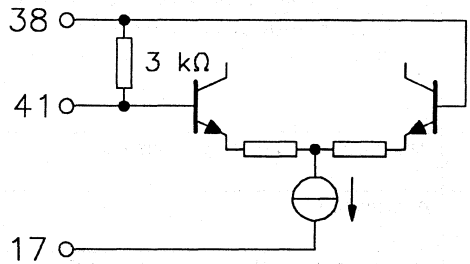
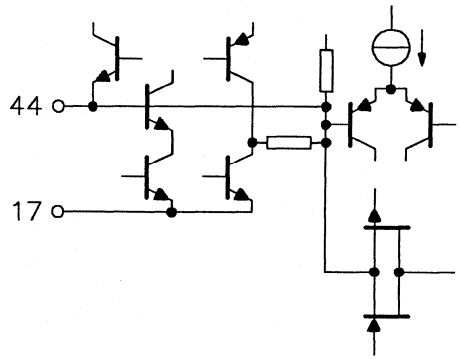
PIN NO.	PIN SYMBOL	DC VOLTAGE (V) AM	DC VOLTAGE (V) FM	EQUIVALENT CIRCUIT
8	TUNE			
9	VCO	1.3	0.95	
10	AFo	0.6	0.7	
11	MPXi	1.23	1.23	
12	LPF	0.1	0.8	

PIN NO.	PIN SYMBOL	DC VOLTAGE (V) AM	DC VOLTAGE (V) FM	EQUIVALENT CIRCUIT
13	MUTE	0.7	0.7	
14	AF-Lo	0.65	0.65	
15	AF-Ro	0.65	0.65	
16	PILFIL	0.95	0.95	
17	IFGND	0	0	
18	FM-DEM	–	1.0	

PIN NO.	PIN SYMBOL	DC VOLTAGE (V)		EQUIVALENT CIRCUIT
		AM	FM	
19	AFC-NEG			
20	AFC-POS			
21	INDICATOR			
22	V_{CC2}			
23	V_{DD}	3.0	3.0	
24	MO-ST			
25	XTAL			
26	DGND	0	0	
27	BUS-CLOCK			

PIN NO.	PIN SYMBOL	DC VOLTAGE (V)		EQUIVALENT CIRCUIT
		AM	FM	
28	DATA			
29	WRITE-ENABLE			
30	P0			
31	P1			
32	AFC-AM			
33	FM-IF2i	–	0.73	

PIN NO.	PIN SYMBOL	DC VOLTAGE (V)		EQUIVALENT CIRCUIT
		AM	FM	
34	V_{STABB}	1.4	1.4	
35	FM-IF1o	–	0.69	
36	AM-IF2i/o	1.4	1.4	
37	FM-IF1i	–	0.73	
38	V_{STABA}	1.4	1.4	

PIN NO.	PIN SYMBOL	DC VOLTAGE (V) AM	DC VOLTAGE (V) FM	EQUIVALENT CIRCUIT
39	FM-MIXER	–	1.0	
40	AM-MIXER	1.4	1.4	
41	AM-IF1i	1.4	1.4	
42	RFGND	0	0	
44	AGC	0.1	0.7	

CHARACTERISTICS

V_{CC1} = 3 V; T_{amb} = +25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC1}	static supply voltage		2.1	–	12	V
	dynamic supply voltage		1.8	–	12	V
V_{CC2}	second supply voltage for tuning		–	–	12	V
V_{DD}	supply voltage for digital part		2.1	–	12	V
V_{tune}	tuning voltage		0.7	–	V_{CC2} – 0.75	V
I_{VCC2}	supply current for tuning in preset mode from one end of the band to the other end of the band		–	–	640	µA
$f_{bus\text{-}clock}$	maximum clock frequency for the bus		–	–	300	kHz
I_{VCC1}	current consumption during acquisition	AM mode	12	15	18	mA
		FM mode	12.5	15.5	18.5	mA
I_{VDD}		AM mode	–	4.8	–	mA
		FM mode	–	5.4	–	mA
I_{VCC1}	current consumption after acquisition	AM mode	12	15	18	mA
		FM mode	13	16	19	mA
I_{VDD}		AM mode	–	3.2	–	mA
		FM mode	–	2.7	–	mA
t	synthesizer auto-search time for empty band	FM mode	–	–	10	s
t	synthesizer preset acquisition time between two bandlimits	FM	–	100	–	ms
		MW	–	200	–	ms
		LW	–	200	–	ms
		SW	–	500	–	ms
f_{band}	frequency range of the synthesizer	AM mode	0.144	–	30	MHz
		FM mode	50	–	150	MHz
Δf_{FM}	AFC accuracy		–	–	10	kHz
Δf_{AM}			–	–	0.5	kHz
$I_{P0/P1}$	software programmable output port P0/P1	V_{CC1} = 5 V				
	sink current		–	–	7	mA
	source current		5	–	7	mA

AM CHARACTERISTICS

Input frequency = 1 MHz; m = 0.3; f_{mod} = 1 kHz; measured in test circuit at pin 10; S2 in position B; V_{in1} measured at input of matching network at pin 2, matching network adjusted to maximum output voltage at low input level; V_{inn} refer to test circuit; V_n refer to pin voltages; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
C_{in}	input capacitance (pin 2)	V_{44} = 0.2 V	–	–	4	pF
I_2	input current (pin 2)	V_{44} = 0.2 V	–	0	–	µA
G_c	front end conversion gain	V_{44} = 0.2 V	5	10	14	dB
		V_{44} = 0.9 V	–26	–14	0	dB
V_{in1}	RF sensitivity	S/N = 26 dB	40	55	70	µV
S/N	maximum signal-to-noise ratio		tbn	50	–	dB
V_{10}	maximun AF output voltage	V_{in1} = 5 mV	36	45	70	mV
THD	total harmonic distortion	V_{in1} = 1 mV	–	0.8	2.0	%
V_{in1}	large signal handling capability	m = 0.8; THD ≤ 8%	150	300	–	mV
$V_{10}/\Delta V_7$	ripple rejection	ΔV_7 = 100 mV (RMS); 100 Hz; V_7 = 3.0 V	–	–47	–	dB
α_{450}	IF suppression	V_{10} = 30 mV	–	56	–	dB

FM CHARACTERISTICS

Input frequency = 100 MHz; Δf = 22.5 kHz; f_{mod} = 1 kHz; measured in test circuit at pin 10 with S2 in position B; V_{inn} refer to test circuit; V_n refer to pin voltages; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{in5}	RF limiting sensitivity	V_{10} = –3 dB; AF_{out} = 0 dB at V_{in5} = 1 mV	0.4	1.2	3.8	µV
V_{in5}	RF sensitivity	S/N = 26 dB	1	2	3.8	µV
V_{37}/V_{in5}	front end conversion gain		12	18	22	dB
S/N	signal-to-noise ratio	V_{in5} = 1 mV	–	62	–	dB
V_{10}	AF output voltage	V_{in5} = 1 mV	40	48	57	mV
THD	total harmonic distortion	IF filter typ SFE10.7MS3A20K-A	–	0.3	0.8	%
V_{in5}	large signal handling capability	THD < 5%	–	500	–	mV
$V_{10}/\Delta V_7$	ripple rejection	ΔV_7 = 100 mV (RMS); 100 Hz; V_7 = 3.0 V	–44	–	–	dB

STEREO DECODER CHARACTERISTICS

f = 1 kHz; $V_{in3(L+R)}$ = 155 mV; V_{pilot} = 15.5 mV; SDS set to maximum level; softmute off (S4 in position A); unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
α_{cs}	channel separation		26	30	–	dB
V_{14}, V_{15}	AF output voltage		–	160	–	mV
V_{AF-L} / V_{in3}	MPX voltage gain		–1.5	–	+1.5	dB
S/N	signal-to-noise ratio	V_{pilot} = 15.5 mV (stereo)	–	74	–	dB
THD	total harmonic distortion		–	0.5	1.0	%
α_{19}	carrier and harmonic suppression	19 kHz (200 mV = 0 dB)	–	–32	–27	dB
α_{38}		38 kHz	–	–21	–16	dB
V_{pilot}	switch to stereo		–	8	12	mV
	switch to mono		2	5	–	mV
α	stereo-blend	V_{in5} = 200 µV	22	30	–	dB
		V_{in5} = 20 µV	–	1	2	dB
	soft mute depth	V_{in5} = 3 µV; $V_{14} = V_{15}$	–1	0	–	dB
		V_{in5} = 1 µV; $V_{14} = V_{15}$	–	–6	–10	dB

TUNING CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
	hard mute	write enable HIGH		–	60	–	dB
	FM levels	$\alpha_{-3\ dB}$-point at V_{in5} = 2 µV					
		S1	S0				
	high (auto-store/search)	1	1	60	150	500	µV
	medium (auto-store/search)	0	1	10	30	55	µV
	low (auto-store/search)	1	0	4	10	20	µV
	nominal (preset mode/tuning indication)	0	0	3	5	9	µV
	AM levels						
		S1	S0				
	high (auto-store/search)	1	1	400	1000	2500	µV
	medium (auto-store/search)	0	1	50	63	80	µV
	low (auto-store/search)	1	0	32	40	50	µV
	nominal (preset mode/tuning indication)	0	0	25	28	40	µV
	AFC-off mode	$\alpha_{-3\ dB}$-point at V_{in5} = 2 µV					
		FM mode		–	3	–	µV
		AM mode		–	25	–	µV

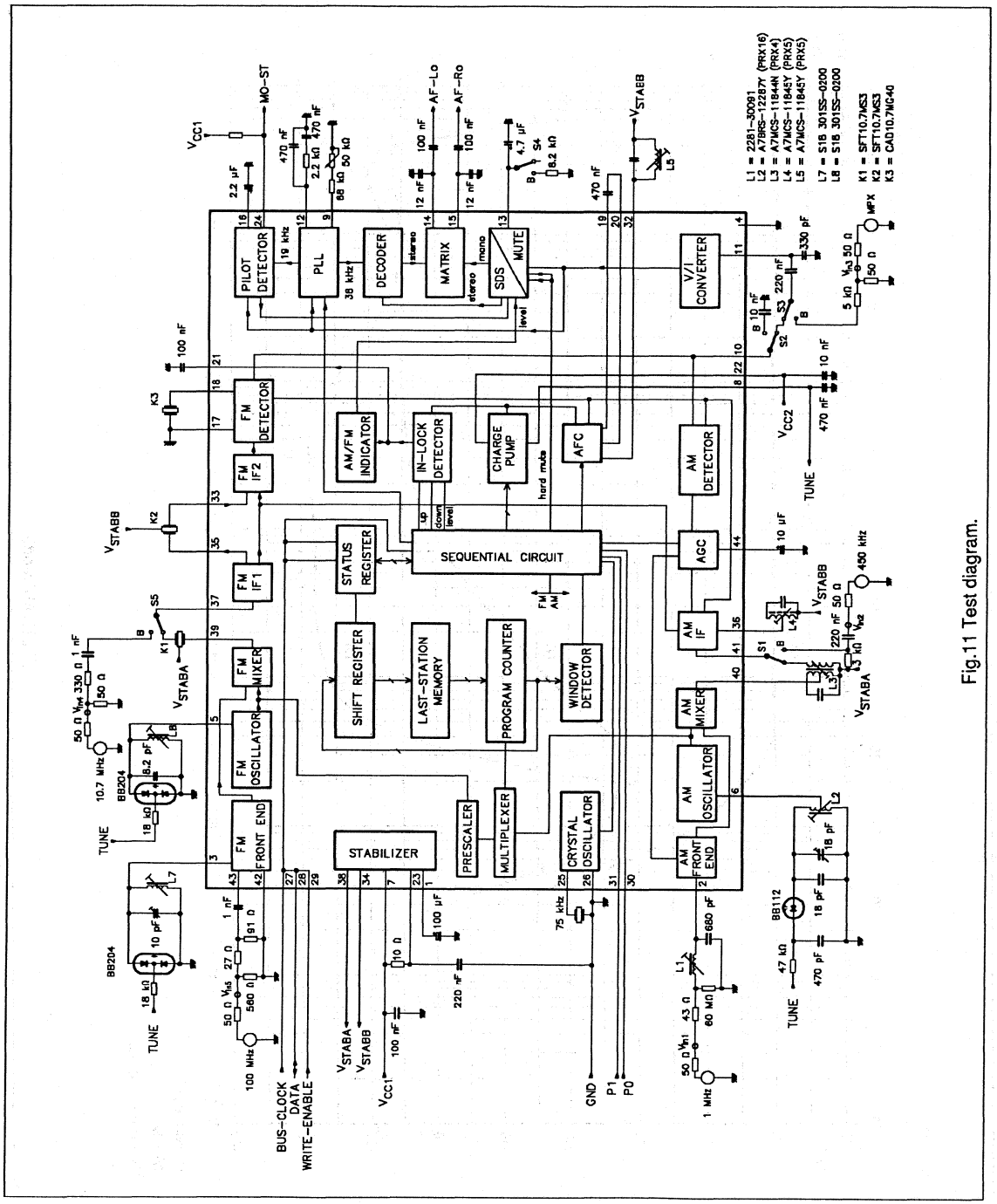


Fig.11 Test diagram.

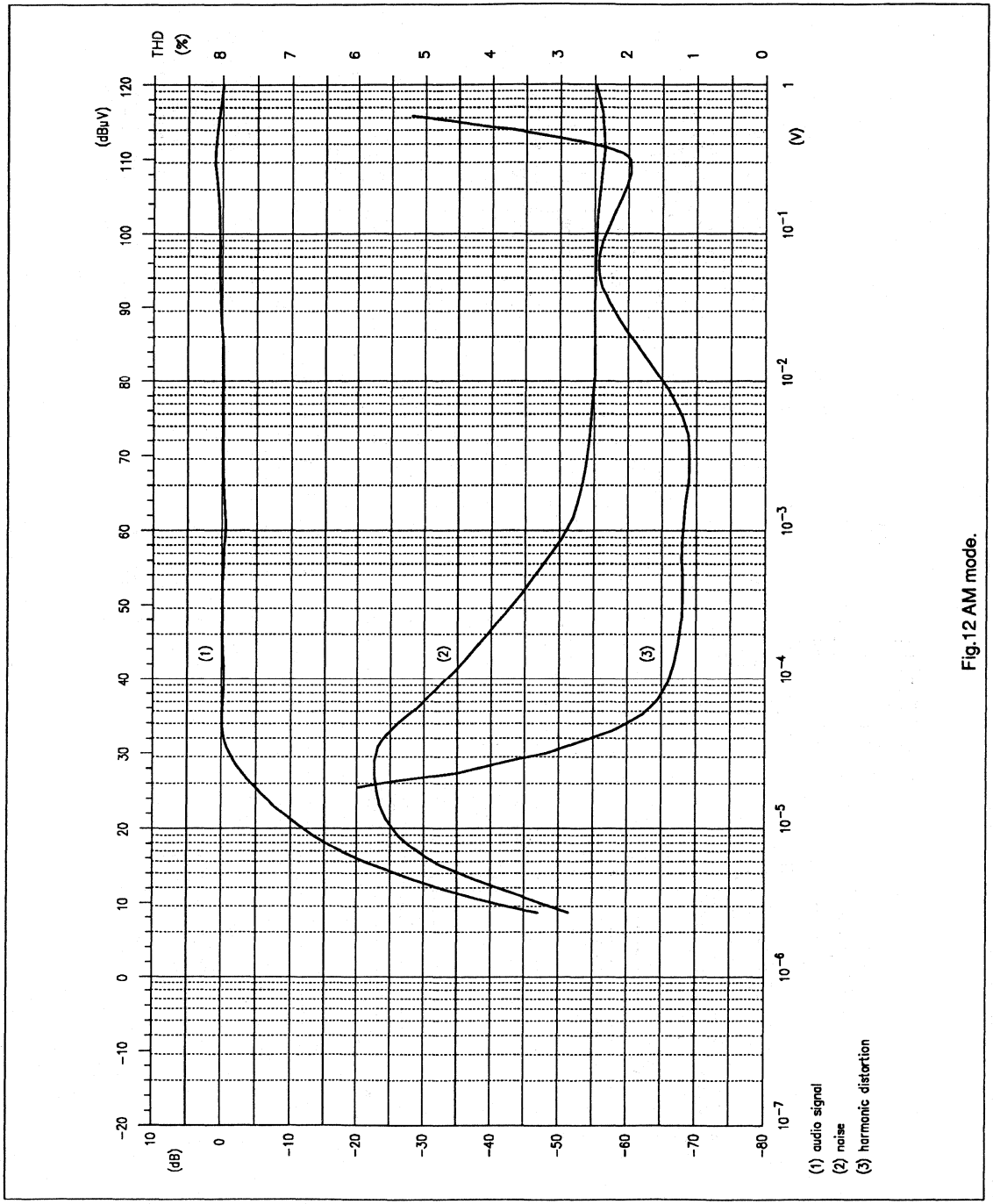


Fig.12 AM mode.

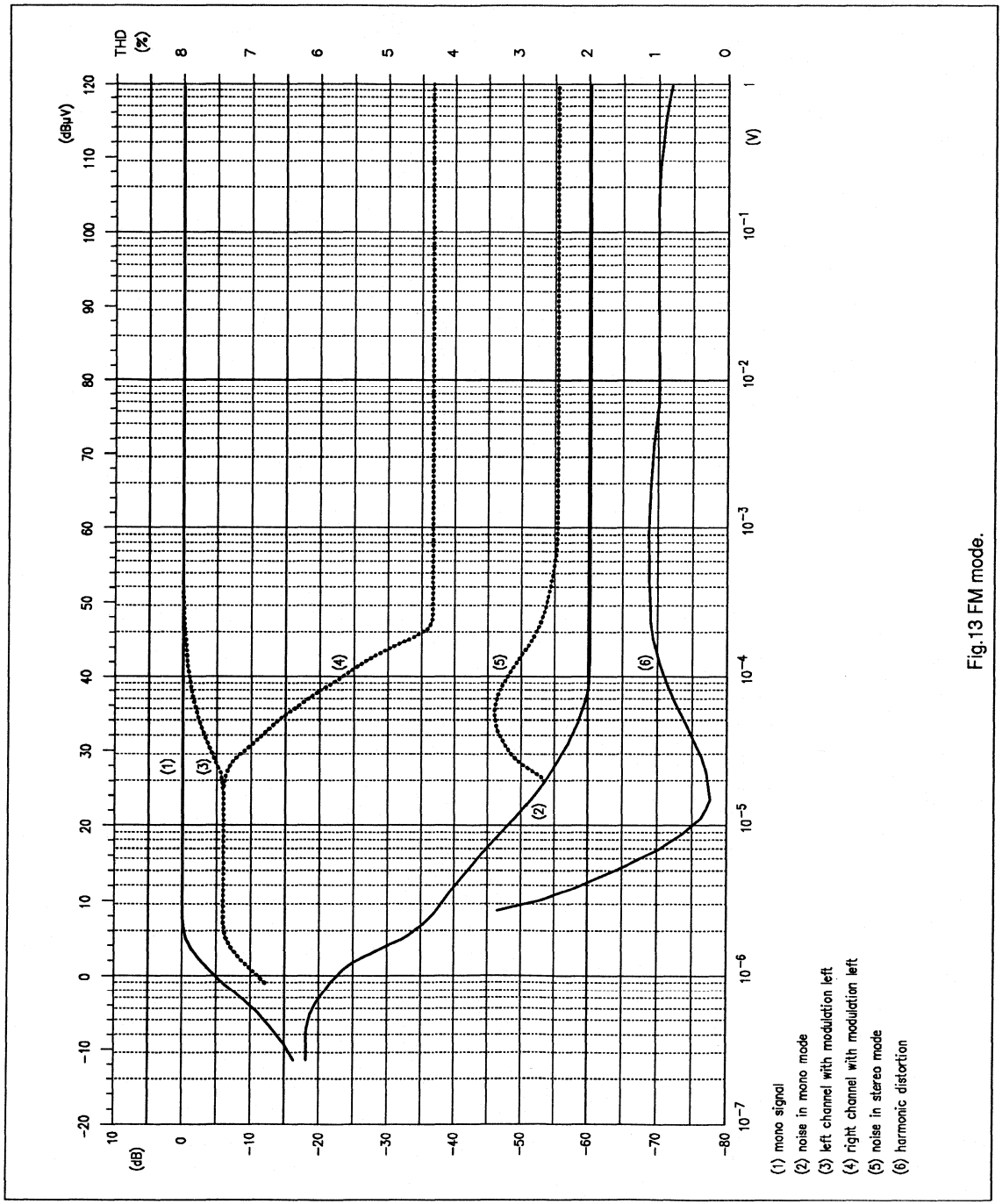


Fig.13 FM mode.

FM/IF SYSTEM AND MICROCOMPUTER-BASED TUNING INTERFACE

GENERAL DESCRIPTION

The TEA6100 is a FM/IF system circuit intended for microcomputer controlled radio receivers. The circuit includes highly sensitive analogue circuitry. The digital circuitry, including an I^2C bus, controls the analogue circuitry and the AM/FM tuning and stop information for the microcomputer.

Features

- 4-stage symmetrical IF limiting amplifier
- Software selectable AM or FM input
- Symmetrical quadrature demodulator
- Single-ended LF output stage
- D.C. output level determined by the input signal
- Semi-adjustable AM and FM level voltage
- Multi-path detector/rectifier/amplifier circuitry
- 3-bit level information and 3-bit multi-path information
- Signal dependent 'soft' muting circuit; externally adjustable
- Reference voltage output (FM mode only)
- 8-bit AM/FM frequency counter with selectable counter resolution
- Possibility to measure the AM IF frequency at 460 kHz (250 Hz resolution) and 10,7 MHz (500 Hz resolution)
- Reference frequency can be directly connected to the reference frequency output of a frequency synthesizer (TSA6057, 40 kHz)

PACKAGE OUTLINE

20-lead DIL; plastic (SOT146).

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage		V_{P1}, V_{P2}	–	8,5	–	V
Supply current		$I_{P1} + I_{P2}$	–	35	–	mA
FM/IF sensitivity	–3 dB before limiting	V_i	–	15	–	μV
Signal plus noise to noise ratio	Δf = 75 kHz; V_I = 10 mV	(S + N)/N	–	85	–	dB
Audio output voltage after limiting	Δf = 22,5 kHz	V_o	–	200	–	mV
AM suppression	V_{IFM} = 600 μV to 600 mV; m = 0,3	AMS	–	60	–	dB
Frequency counter sensitivity						
AM	pin 19, f = 10,7 MHz	$V_{i(AM)}$	–	45	–	μV
	f = 460 kHz	$V_{i(AM)}$	–	20	–	μV
FM	pin 18, f = 10,7 MHz	$V_{i(FM)}$	–	45	–	μV
Resolution of the frequency counter	reference frequency of 40 kHz;					
AM	IF = 460 kHz	f_s (AM)	–	250	–	Hz
	IF = 10,7 MHz	f_s (AM)	–	500	–	Hz
FM		f_s (FM)	–	6,4	–	kHz

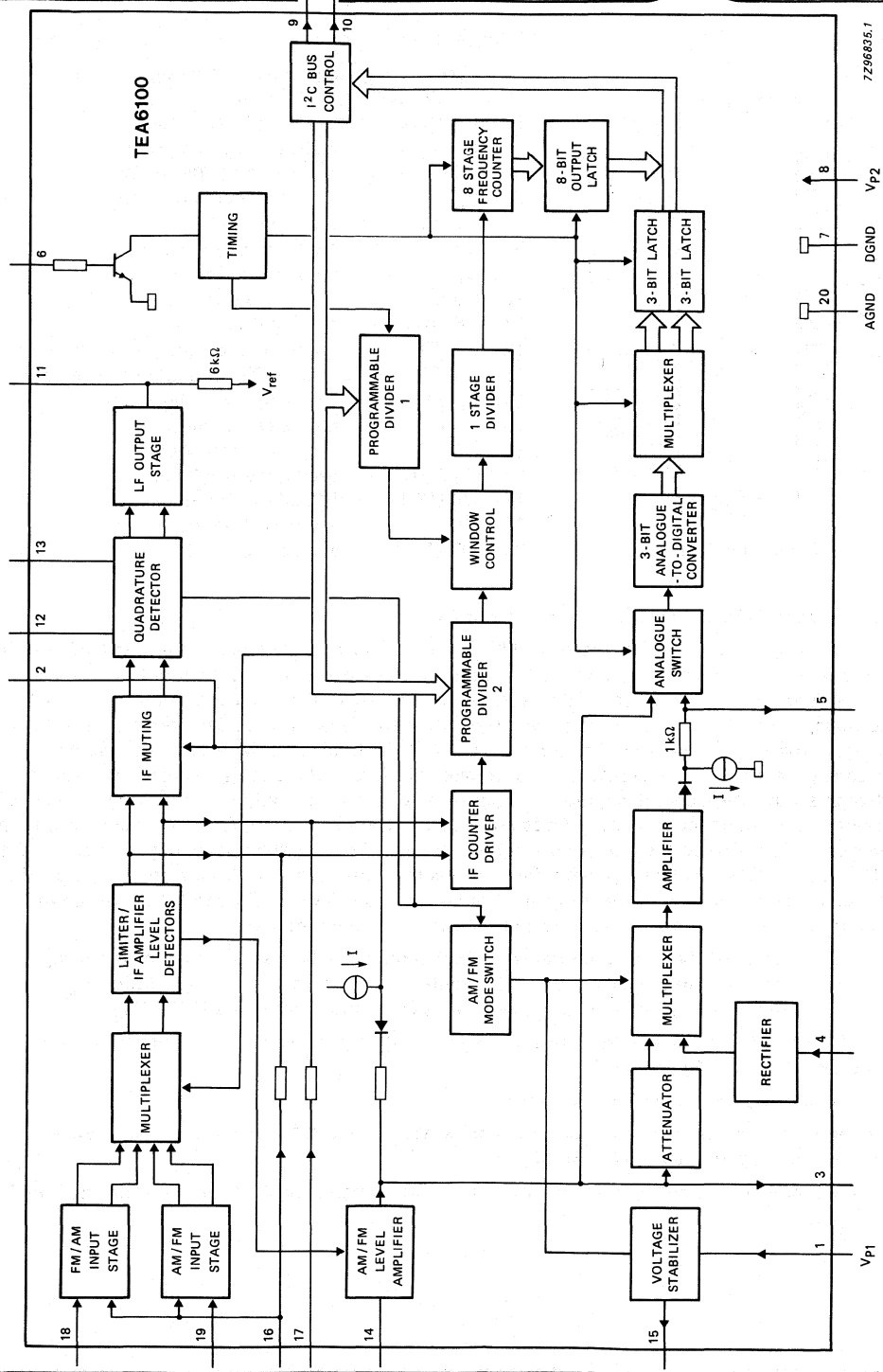


Fig. 1 Block diagram.

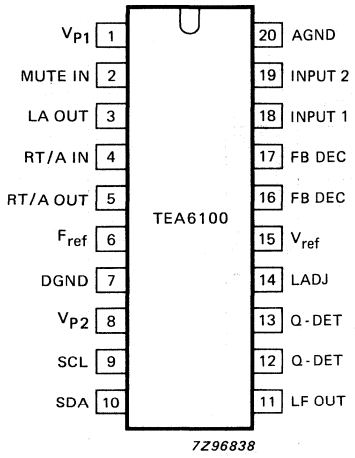


Fig. 2 Pinning diagram.

PINNING

1	V_{P1}	analogue supply voltage
2	MUTE IN	mute input
3	LA OUT	level amplifier output
4	RT/A IN	rectifier/amplifier input
5	RT/A OUT	rectifier/amplifier output
6	F_{ref}	reference frequency input
7	DGND	digital ground
8	V_{P2}	digital supply voltage
9	SCL	serial clock line (I^2C bus)
10	SDA	serial data line (I^2C bus)
11	LF OUT	audio output signal
12	Q-DET	phase shift for quadrature detector
13	Q-DET	phase shift for quadrature detector
14	LADJ	level amplifier adjustment
15	V_{ref}	reference voltage
16	FB DEC	decoupled feedback
17	FB DEC	decoupled feedback
18	INPUT 1	FM/AM IF input
19	INPUT 2	AM/FM IF input
20	AGND	analogue ground

FUNCTIONAL DESCRIPTION (see Figs 1 and 13)

The IF amplifier consists of four balanced limiting amplifier stages, two separate inputs (AM and FM) and one output. Software programming (see Table 2; Figs 4 and 5) allows the input signals (AM/FM) to be inserted on either input (pin 18 or 19). The output drives the frequency counter and via the mute stage, drives the quadrature detector. The output of the quadrature detector is applied to an audio stage (which has a single-ended output). The AM/FM level amplifier, which is driven by 5 IF level detectors, generates a signal dependent d.c. voltage. The level output voltage is used internally to control the mute stage and, if required, the signal can be used externally to control the stereo channel separation and frequency response of a stereo decoder. The signal is also feed to the analogue-to-digital converter (ADC). Due to the front-end spread in the amplification, the level voltage is made adjustable (LADJ, pin 14). The level voltage amplifier controls the mute stage and this insures the −3 dB limiting point remains constant, independent of the front-end spread. AM and FM mode have different front-end circuitry, therefore LADJ must be adjustable for both inputs.

The output voltage of the level amplifier is dependent upon the field strength of the input signal. The multi-path of the FM signal exists in the AM modulation of the input signal. The following method is used to determine the level information and the amount of multi-path (as a DC voltage):

- the IF level detector detects the multi-path and feds the signal, via the level amplifiers, to the external bandpass filter (pin 3) and ADC1
- the signal is then fed to an internal rectifier
- the rectified signal is then fed to an amplifier, so at pin 5 the DC level information is externally available and internally used by ADC2

In the FM mode, the DC information concerning the multi-path is available at pin 5 and the level information is available at pin 3.

In the AM mode, the level information at pin 3 cannot be directly used owing to AM modulation on the output signal of the level amplifier. This signal requires filtering, which is achieved by the following method:

- the multiplexer is switched to a position which causes the signal to be applied to the attenuator
- after attenuation the signal is fed to an amplifier (the resultant gain of attenuator and amplifier is unity), after amplification the signal is filtered by an internal resistor and external capacitor
- after filtering the signal is applied to ADC2 and is externally available

In AM mode pin 5 contains the level information.

The voltages on pin 3 and 5 are converted into two 3-bit digital words by the ADC, which can then be read out by the I^2C bus. The meaning of the 3-bit words is shown in Table 1.

Table 1 3-bit words

	position	
word	FM	AM
1	multipath	level without modulation
2	level	level with modulation

The FM modulated signal is converted into an audio signal by the symmetrical quadrature detector. The main advantage of such a detector is that it requires few external components.

An FM signal requires good AM suppression, and as a result, the IF amplifiers must act as limiters. To achieve good suppression on small input signals the IF amplifiers must have a high gain and thus a high sensitivity. High sensitivity is an undesirable property when used in car radio applications, this problem is solved by having an externally adjustable mute stage to control the overall sensitivity of the device.

The IF mute stage is controlled by the level amplifier (soft muting) and is only active in FM mode. If the input falls below a predetermined level, the mute stage becomes active. To avoid the 'ON/OFF' effect of the audio signal due to fluctuations of the input signal, the mute stage is activated rapidly but de-activated slowly. The mute stage is de-activated slowly, via a current source and an external capacitor at pin 2, to avoid aggressive behaviour of the audio signal. It is possible to adjust the '–3 dB limiting point' of the audio output via the level voltage due to the level signal being externally adjustable. If hard muting is required then pin 2 must be switched to ground.

The 8-bit counter allows accurate stop information to be obtained, because exact tuning is achieved when the measured frequency is equal to the centre frequency of the IF filter.

To measure the input frequency, the number of pulses which occur in a defined time must be counted. This defined time is refered to as 'window'. A wide window indicates a long measuring time and therefore a high accuracy. The counter resolution is defined as Hertz per count. Due to the TEA6100 having to measure the IF frequencies of AM and FM, the counter resolution must be adjustable (different channel spacing). The counter resolution depends on the setting of dividers 1 (N1), divider 2 (N2) and the reference frequency (F_{ref}). The divider ratios of N1 and N2 are controlled by software (see section PROGRAMMING INFORMATION). In Table 3 the window and counter resolution has been calculated for a reference frequency of 40 kHz. The accuracy is controlled by bit 7 of the input word. Although the resolution is the same for bit 7 = logic 0 and bit 7 = logic 1, the width of the window doubles when bit 7 = logic 1.

- bit 7 = 0, accuracy = ± counter resolution
- bit 7 = 1, accuracy = $\pm \frac{1}{2}$ counter resolution

Communication between TEA6100 and the microcomputer is via a two wire bidirectional I²C bus. The power supply lines are fully isolated to avoid cross talk between the digital and analogue parts of the circuit.

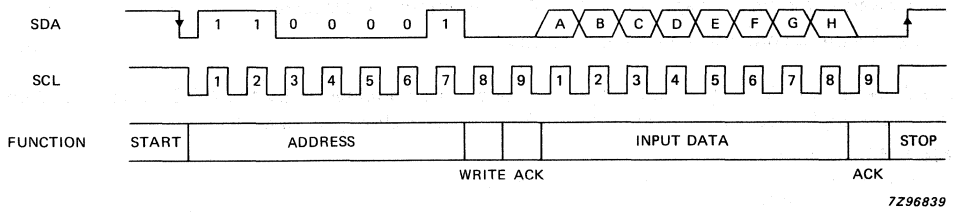


Fig. 3 Input data format waveforms.

Table 2 Input bits

bit	function	logic 0	logic 1	see Figs. 5 and 6
1	reference frequency	32 kHz	40 kHz	A
2	IF mode	AM	FM	B
3	IF input	pin 19	pin 18	C
4	counter input	460 kHz	10,7 MHz	D
5	counter mode	AM	FM	E
6	resolution	divide by 8	divide by 1	F
7	accuracy	LOW	HIGH	G
8	test mode	OFF	ON	H

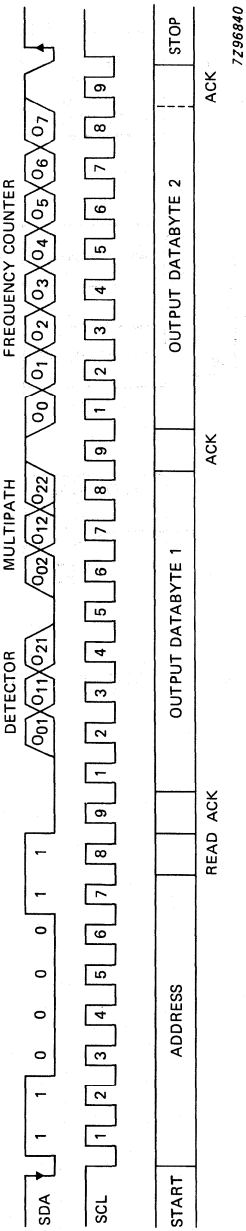


Fig. 4 Output data format waveforms.

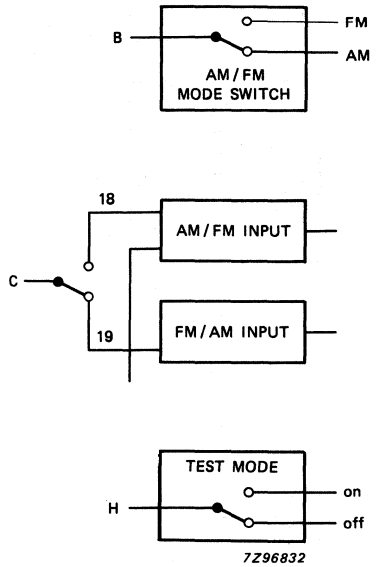


Fig. 5 Switch positions, analogue part (switches drawn in logic 0 state).

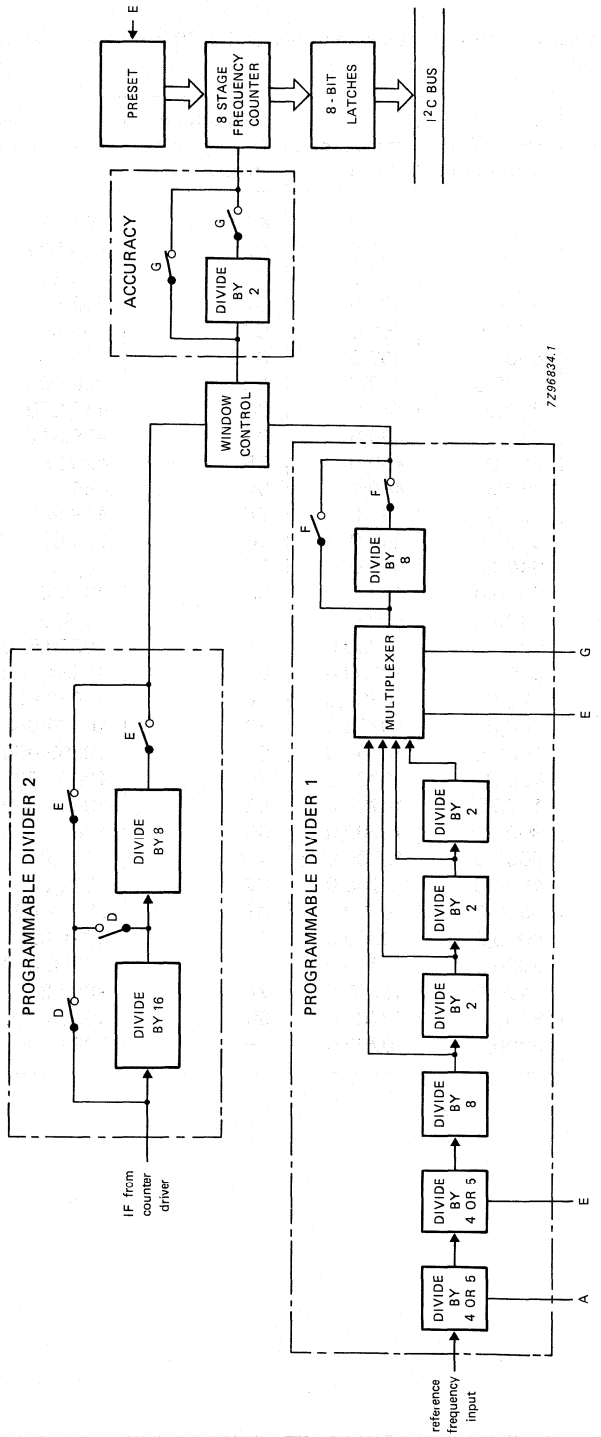


Fig. 6 Switch positions, digital part (switches drawn in logic 0 state, see Tables 2 and 3).

Table 3 Possible window settings and counter resolutions with a 40 kHz reference frequency (see Figs. 5 and 6)

position of switch ADEFG	window (ms)	counter resolution Hz/count	IF frequency (kHz)	read out by IF frequency (hex)	range (kHz)	
					min.	max.
00000	25,6	39,1	460,0	4F	456,914	466,875
10000	32,0	31,3	460,0	CF	453,531	461,500
00001	51,2	39,1	460,0	4F	456,914	466,875
10001	64,0	31,3	460,0	CF	453,531	461,500
00100	128,0	1000,0	460,0	C3	265,000	520,000
10100	160,0	800,0	460,0	36	416,800	620,800
00101	256,0	1000,0	460,0	C3	256,000	520,000
10101	320,0	800,0	460,0	36	416,800	620,800
00010	3,2	312,5	460,0	0F	455,312	535,000
10010	4,0	250,0	460,0	7F	428,250	492,000
00011	6,1	312,5	460,0	0F	455,312	535,000
10011	8,0	250,0	460,0	7F	428,250	492,000
00110	16,0	8000,0	460,0	30	76,000	2116,000
10110	20,0	6400,0	460,0	3F	56,800	1688,800
00111	32,0	8000,0	460,0	30	76,800	2116,000
10111	40,0	6400,0	460,0	3F	56,800	1688,800
01000	25,6	625,0	10700,0	2F	10670,625	10830,000
11000	32,0	500,0	10700,0	E7	10584,500	10712,000
01001	51,2	625,0	10700,0	2F	10670,625	10830,000
11001	64,0	500,0	10700,0	E7	10584,000	10712,000
01100	128,0	1000,0	10700,0	C3	10505,000	10760,000
11100	160,0	800,0	10700,0	36	10656,800	10860,800
01101	256,0	1000,0	10700,0	C3	10505,000	10760,000
11101	320,0	800,0	10700,0	36	10656,800	10860,000
01010	3,2	5000,0	10700,0	AB	9845,000	11120,000
11010	4,0	4000,0	10700,0	C2	9924,000	10944,000
01011	6,4	5000,0	10700,0	AB	9845,000	11120,000
11011	8,0	4000,0	10700,0	C2	9924,000	10944,000
01110	16,0	8000,0	10700,0	30	10316,000	12356,000
11110	20,0	6400,0	10700,0	7F	9887,200	11519,200
01111	32,0	8000,0	10700,0	30	10316,000	12356,000
11111	40,0	6400,0	10700,0	7F	9887,200	11519,200

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage	pins 1 and 8	V_{P1}, V_{P2}	0	13,2	V
Total power dissipation		P_{tot}	see Fig. 7		
Storage temperature range		T_{stg}	−65	+150	°C
Operating ambient temperature range		T_{amb}	−30	+85	°C

THERMAL RESISTANCE

From junction to ambient $R_{th\ j\text{-}a}$ 70 K/W

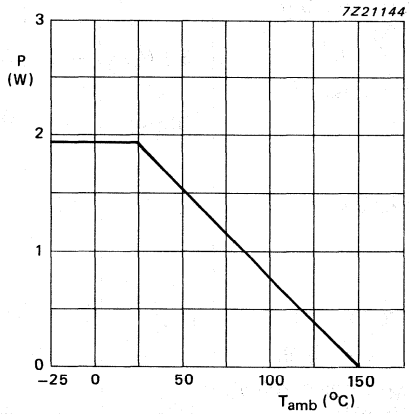


Fig. 7 Power derating curve.

DC CHARACTERISTICS (note)

$V_{P1} = V_{P2} = 8{,}5$ V; $T_{amb} = 25$ °C; all currents positive into the IC; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage	pins 1 and 8	V_{P1}, V_{P2}	7,5	8,5	12	V
Supply current						
FM mode	$V_{ADJ} > 2{,}4$ V	I_{P1}	–	19	25	mA
AM mode	$V_{ADJ} > 2{,}4$ V	I_{P1}	–	15	25	mA
digital part		I_{P2}	–	16	23	mA
Power dissipation		P_d	–	280	–	mW

AC CHARACTERISTICS (note 1)

V_P = 8,5 V; $V_{i(FM)}$ = 1 mV; f = 10,7 MHz; Δf = 22,5 kHz; f_m = 1 kHz; FM mode; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
IF amplifier, quadrature detector and LF amplifier output	pin 11					
Sensitivity	−3 dB before limiting; inactive mute	$V_{i(FM)}$	–	15	30	μV
Sensitivity	S/N = 26 dB; inactive mute	$V_{i(FM)}$	–	12	–	μV
Signal plus noise to noise ratio	$V_{i(FM)}$ = 10 mV; bandwith = 0,3 to 15 kHz; Δf = 75 kHz	(S + N)/N	–	85	–	dB
IF input range	AM suppression > 40 dB	$V_{i(FM)}$	–	0,09 to 1000	–	mV
Audio output voltage after limiting	Δf = 22,5 kHz	V_o	160	200	240	mV
Total harmonic distortion for single tuned circuit	Δf = 75 kHz	THD	–	0,65	–	%
AM suppression	note 2; see Fig. 8;					
	$V_{i(AM)}$ range = 200 μV to 600 mV	AMS	–	60	–	dB
	$V_{i(AM)}$ range = 200 μV to 600 μV	AMS	–	55	–	dB
Supply voltage ripple rejection	200 Hz; 20 log (V_i/V_o)	SVRR	38	40	–	dB
IF counter inputs						
Frequency counter sensitivity	minimum input voltage for a readout ± 1 bit;					
FM mode	10,7 MHz	$V_{i(FM)}$	–	–	60	μV
AM mode	10,7 MHz	$V_{i(AM)}$	–	–	60	μV
AM mode	460 kHz	$V_{i(AM)}$	–	–	45	μV
Maximum input voltage		V_i	–	–	1	V

parameter	conditions	symbol	min.	typ.	max.	unit
FM level performance	see Fig. 9					
Output voltage adjustment range	$V_{i(FM)}$ = 0 V; pins 3 and 14	V_{LFM}	–	0,1 to 4,6	–	V
Maximum output voltage	pins 3 and 14	V_{LFM}	V_P–1,5	–	–	V
Adjustable gain	$V_{i(FM)}/V_{ADJ}$	G_{ADJ}	–	–2	–	dB
Level voltage slope	V_{ADJ} = 2,4 V; $V_{i(FM)}$ = 100 to 10 mV	$S_{i(FM)}$	1,4	1,6	1,8	V/dec *
Output impedance of level amplifier	$V_{LFM} > 1$ V	$\lvert Z_o \rvert$	–	100	–	Ω
AM level performance	see Fig. 10					
Output voltage adjustment range	$V_{i(AM)}$ = 0 V; pins 5 and 14	V_{LFM}	–	0,1 to 4,6	–	V
	$V_{i(AM)}$ = 10 mV; pins 5 and 14	V_{LAM}	6	–	–	V
Adjustable gain	$V_{i(AM)}/V_{ADJ}$	G_{ADJ}	–	–2	–	dB
Level voltage slope	V_{ADJ} = 2,4 V; $V_{i(FM)}$ = 100 to 10 mV	$S_{i(AM)}$	1,3	1,5	1,7	V/dec *
IF soft muting	V_{LFM}; pin 3; see Fig. 11					
Mute operating range		V_{LFM}	–	0,1 to 2,5	–	V
Mute voltage	–3 dB output attenuation	V_{LFM}	1,20	1,45	1,75	V
Maximum muting	V_{LFM} = 0,1 V	V_{MUTE}	–	19	–	dB
IF hard muting	V_{MUTE}; pin 2					
Mute voltage	–60 dB output attenuation	V_{MUTE}	–	460	–	mV
Mute discharge current	V_{MUTE} = 1 V; V_{LEVEL} = 0 V; mute ON; pin 2	$+I_2$	–	270	–	μA
Mute charging current	V_{MUTE} = 0 V; mute OFF	$-I_2$	–	1,5	–	μA

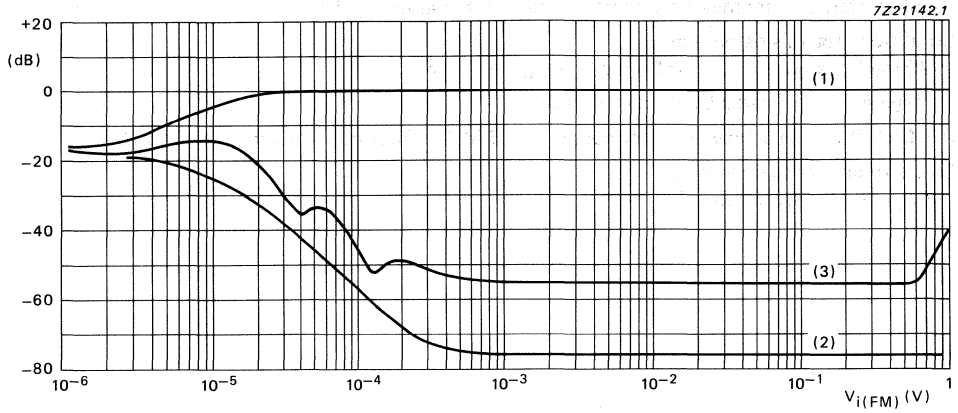
* V/dec = voltage per decade.

AC CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Rectifier/amplifier						
Input impedance	pin 4	$\|Z_i\|$	7	10	13	kΩ
Conversion gain AC to DC	pins 4 and 5; bandwith = 100 Hz to 120 kHz; 20 log $V_{O(MP)}$ (d.c.)/ $V_{i(MP)}$ (a.c.)	G_A	–	30	–	dB
DC output voltage range		$V_{O(MP)}$	–	0,2 to 6	–	V
Output characteristics	see Fig. 13; note 3					
Discharge current		I_o	–	200	–	μA
Output ripple in AM mode (peak-to-peak value)	f_m = 200 Hz; m = 0,8; $V_{i(AM)}$ range = 100 μV to 30 mV	V_{ripple}	–	300	400	mV
Multi-path output	see Fig. 12; note 4					
Reference voltage output	pin 15, FM only					
Output voltage		V_{ref}	–	4,4	–	V
Output sink current		$+I_{15}$	–	–	1,5	mA
Output impedance		$\|Z_O\|$	–	–	10	Ω
Output charge current		$-I_{15}$	5	–	–	mA
Output voltage	AM mode	V_{ref}	–	0	–	V
Output impedance	AM mode	$\|Z_O\|$	–	14	–	kΩ
I^2C bus data format	see Figs 3 and 4; Table 2					
3-bit ADC	multi-path and level information, note 5					
Trip level LOW		V_{TL}	1,20	1,45	1,75	V
Trip level HIGH		V_{TH}	4,25	4,50	4,75	V
Reference frequency input	pin 6					
Reference range		F_{ref}	–	–	40	kHz
Input voltage LOW		V_{IL}	–	–	0,4	V
Input current HIGH		I_{IH}	5	–	–	μA

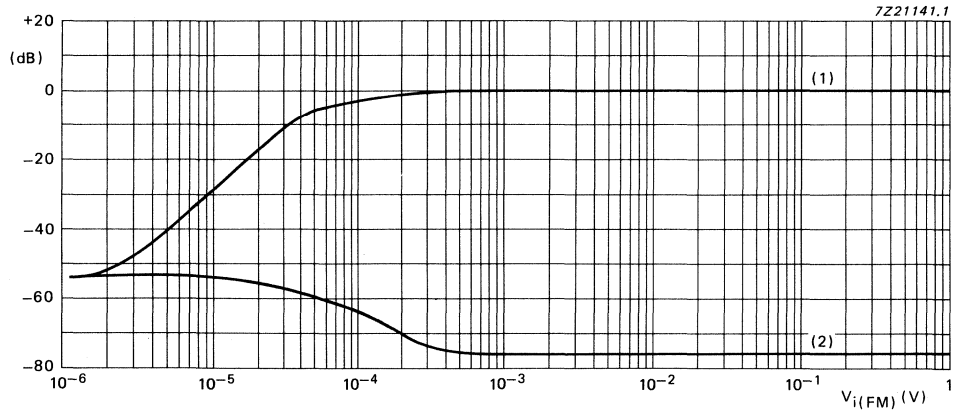
Notes to the characteristics

1. All characteristics are measured from the circuit shown in Fig. 13.
2. Conditions for this parameter are:
   20 log $V_{o(FM)}$; m = 0,3 or 20 log $V_{o(AM)}$; m = 0,3.
3. Voltage source followed by diode and resistor.
4. A DC shift can be achieved by connecting a 1,8 MΩ resistor between pin 4 and pin 15.
5. Step size between trip levels:
   $(V_{TH} - V_{TL})/6 \pm 0{,}07$ V.



(1) Audio (Δf = 22,5 kHz and f_{mod} = 1 kHz) for V_{ADJ} = 0 V.
(2) Noise (with dBA filter) for V_{ADJ} = 0 V.
(3) AM suppression (m = 0,3 and f_{mod} = 1 kHz) for V_{ADJ} = 0 V.

Fig. 8(a) Audio output voltage performance plotted against input signal, $V_{i(FM)}$.



(1) Audio (Δf = 22,5 kHz and f_{mod} = 1 kHz) for V_{ADJ} = 2,4 V.
(2) Noise (with dBA filter) for V_{ADJ} = 2,4 V.

Fig. 8(b) Audio output voltage performance plotted against input signal, $V_{i(FM)}$.

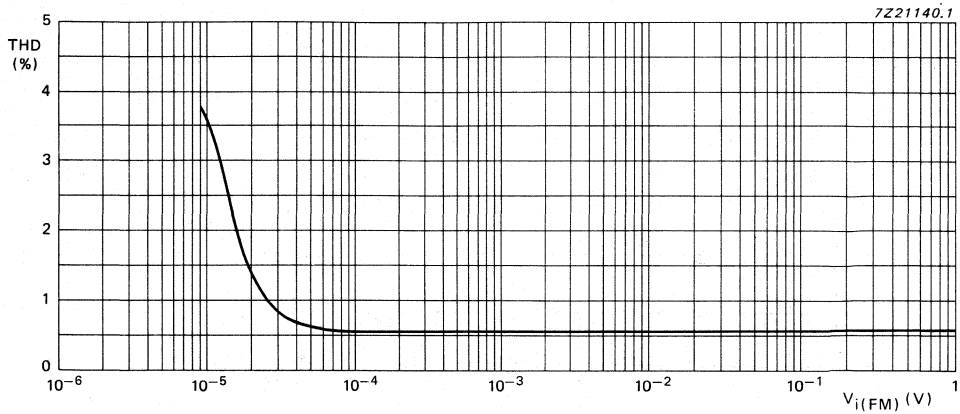
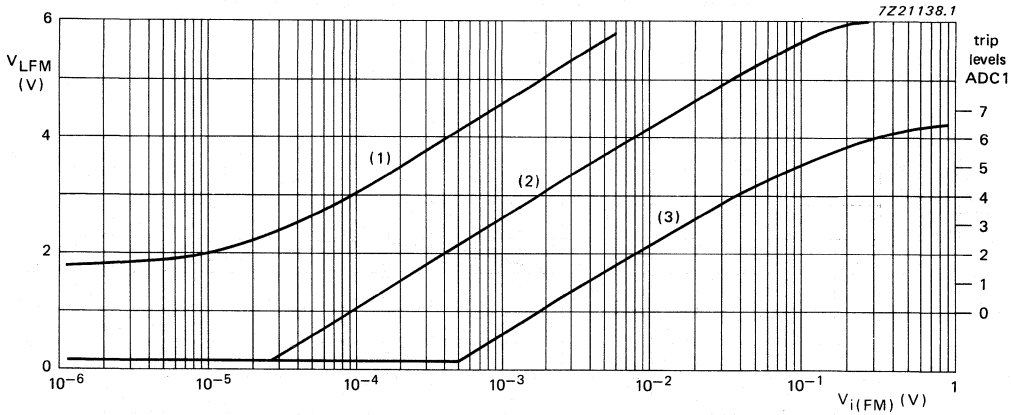
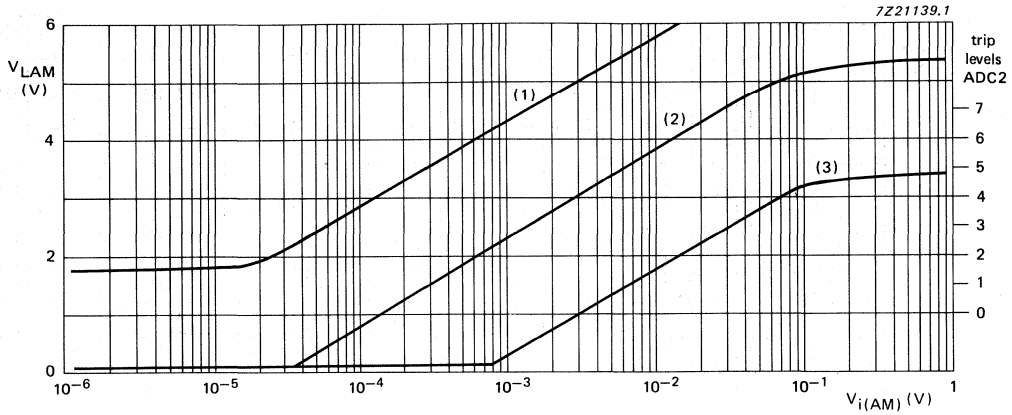


Fig. 8(c) Total harmonic distortion; Δf = 75 kHz, f_{mod} = 1 kHz and V_{ADJ} = 0 V.



(1) V_{ADJ} = 1,4 V.
(2) V_{ADJ} = 2,4 V.
(3) V_{ADJ} = 3,4 V.

Fig. 9 Level voltage output (V_{LFM}) plotted against IF input signal, $V_{i(FM)}$; IF = 10,7 MHz.



(1) V_{ADJ} = 1,4 V.
(2) V_{ADJ} = 2,4 V.
(3) V_{ADJ} = 3,4 V.

Fig. 10 Level voltage output (V_{LAM}) plotted against IF input signal, $V_{i(AM)}$; IF = 10,7 MHz or 460 kHz.

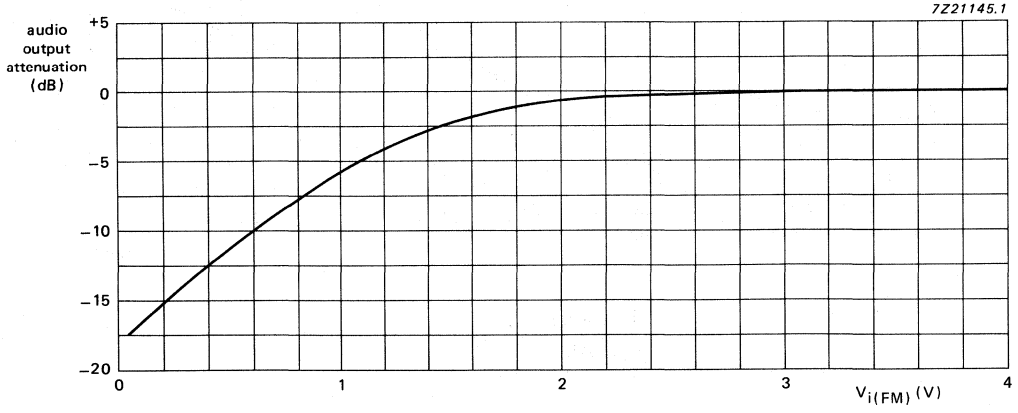
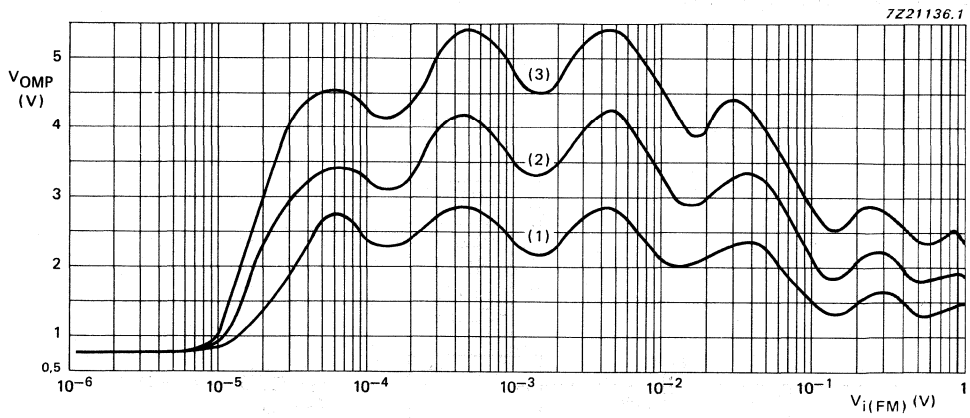
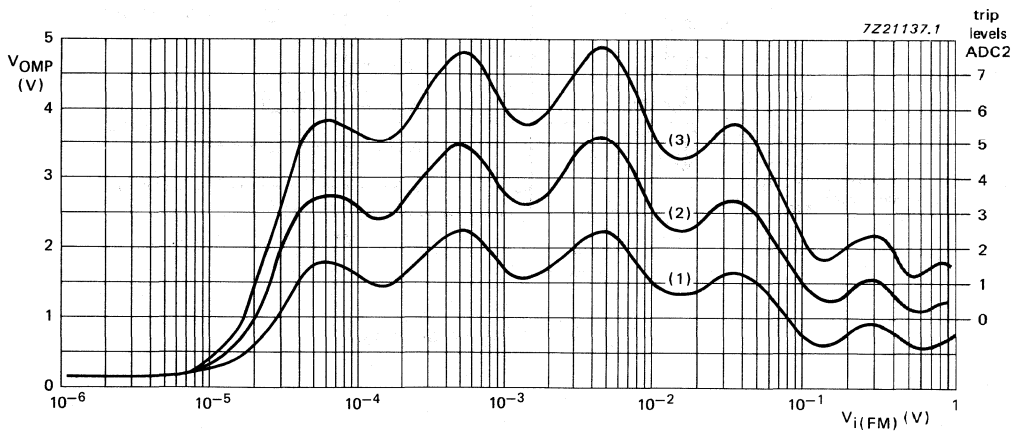


Fig. 11 Soft muting plotted against level output voltage; $V_{i(FM)}$ = 1 mV and Δf = 22,5 kHz.



(1) mod = 0,2
(2) mod = 0,3
(3) mod = 0,4

Fig. 12(a) Multi-path output plotted against IF input signal, $V_{i(FM)}$; f_{mod} = 3 kHz (AM, no FM modulation), V_{ADJ} = 2,4 V and 1,8 MΩ resistor connected between pin 4 and pin 15.



(1) mod = 0,2
(2) mod = 0,3
(3) mod = 0,4

Fig. 12(b) Multi-path output plotted against IF input signal, $V_{i(FM)}$; f_{mod} = 3 kHz (AM, no FM modulation), V_{ADJ} = 2,4 V.

APPLICATION INFORMATION

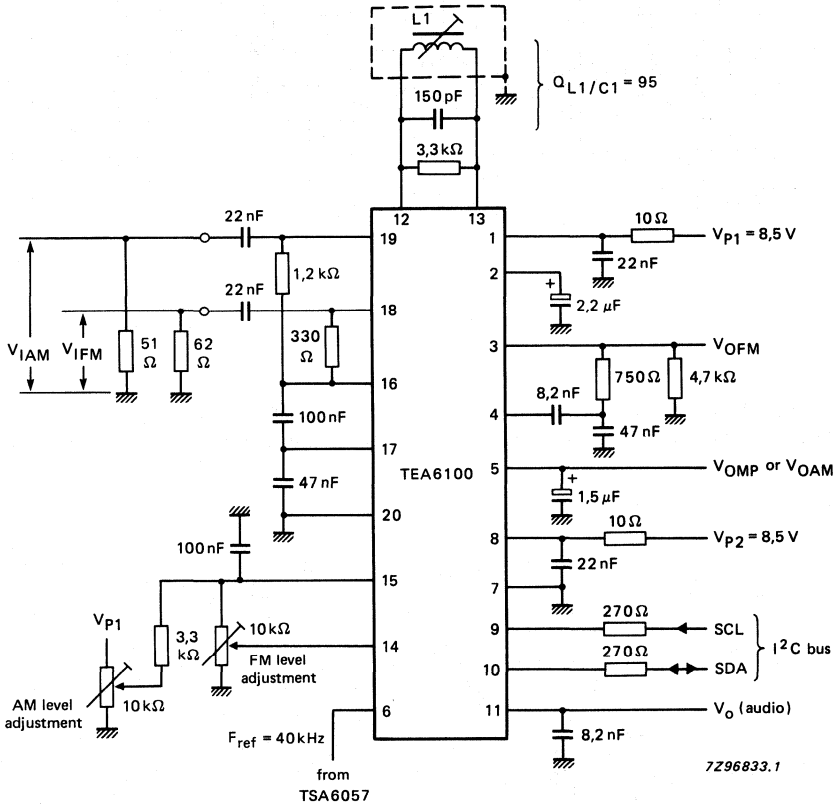


Fig. 13 Application diagram.

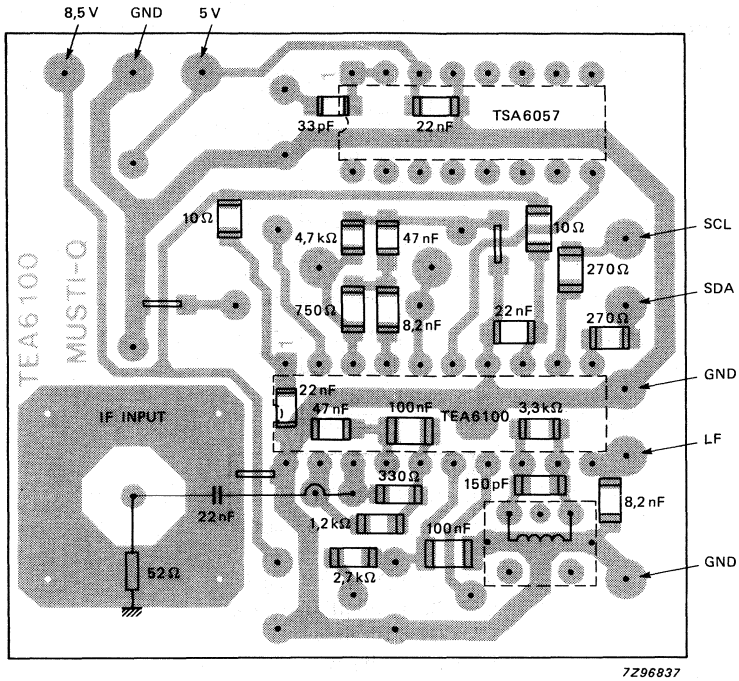


Fig. 14 Track side of printed circuit board.

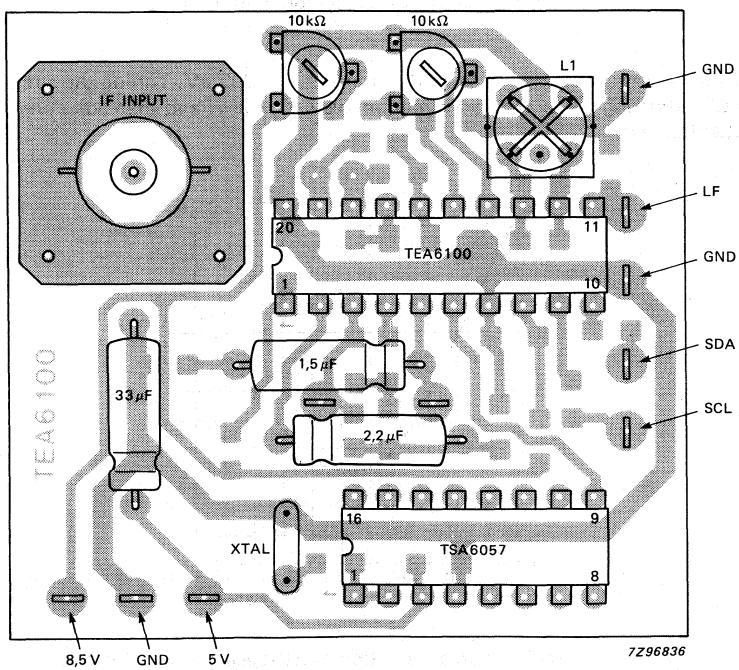
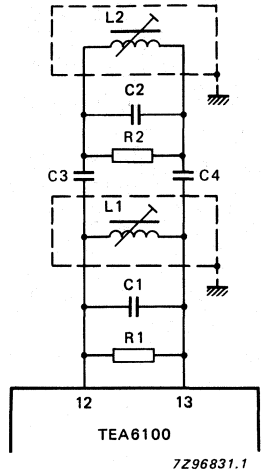


Fig. 15 Component side of printed circuit board.

Double tuned circuit



R1 = 5,1 kΩ, R2 = 1,5 kΩ
C1 = C2 = 150 pF (n = 220)
C3 = C4 = 10 pF
L1 = L2 = 1,6 μH

Fig. 16 Double tuned demodulator circuit.

Alignment of the circuit is obtained with an IF input signal > 200 μV. Tuning the circuit is performed by, detuning L2, adjusting L1 to obtain a minimum distortion level and then adjusting L2 to obtain a minimum distortion level.

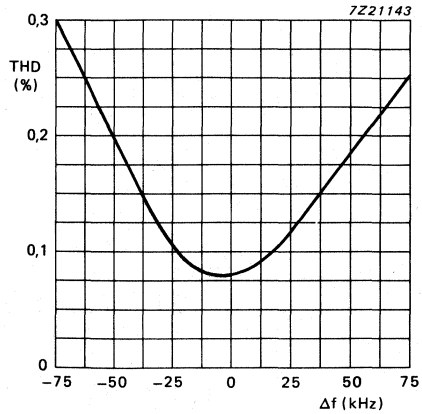


Fig. 17 Total harmonic distortion plotted against IF detuning; for $\Delta f = \pm 75$ kHz, $f_{mod} = 1$ kHz and $V_O = 500$ mV.

PROGRAMMING INFORMATION

Converting the read out of the counters into frequency

The counter resolution at the input is defined as:

- resolution = divider ratio of N2/window

For every increment of the counter the counted frequency increases relative to the resolution in Hertz, as shown in example:

- window = 20 ms; N2 = 128; IF frequency = 10,7 MHz; resolution = 128/0,02 = 6,4 kHz per count

The counter consists of 8 bits. Therefore, the maximum frequency range that can be counted is 256 x resolution = 1,6384 MHz. In the example the frequency to be counted is 10,7 MHz, therefore, the counter will overflow (in the example above, 7 times). The real measured frequency is:

- f_{real} = (read out + overflow x 256) x resolution

The overflow indicates the off-set on the frequency scale which must be added to the read out. Due to the bandwidth of the IF filter, the frequencies at the input to the TEA6100 are known, for example:

- IF filter for FM has a center frequency of 10,7 MHz and −3 dB bandwidth of 300 kHz. Only the frequencies of 10,7 MHz ± 150 kHz occur at the input of the TEA6100. For this reason it is not necessary to count the overflow.

The read out of the counter has to be translated into frequency. This translation depends upon the counter resolution. The preferred way to calculate the input frequency is to:

- calculate the read out of the target IF frequency. Compare this value with that of the measured read out and multiply the difference by the resolution.

The formulae for calculating the target IF read out and the resolution are as follows (A, D, E, F and G refer to the bits of the I^2C bus input data as shown in Figs 3 and 4 and to the counter/timer block diagram shown in Fig. 6. An, Dn, En, Fn and Gn are inverted values of the variables A, D, E, F and G. Table 3 shows the following formulae calculated for a reference frequency of 40 kHz):

- N1 = (An x 4 + A x 5) x (En x 4 + E x 5) x 8 x $(2^{[E \times 2 + G \times 1]})$ x (F x 1 + Fn x 8)
- Window (T) = $N1/F_{ref}$
- N2 = (E x 16 x 8 + En x [Dn x 1 + D x 16]) x (G x 2 + Gn x 1)
- Target decimal read out (TDEC) = T x (TIFF/N2 + (E x 247 + En x 79). TIFF is the symbol for target IF frequency
- Target read out hexadecimal (THEX), convert the target decimal read out to hexadecimal and use the 2 least significant digits (Do not use overflow value). The symbol for measured hexadecimal is MHEX
- Resolution (R) = N2/T
- Measured frequency (F_I) = (TIFF) + R x (MHEX − THEX)

Note

Care should be taken if TIFF + $\frac{1}{2}$ filter bandwidth is greater than the frequency for the read out of hexadecimal value FF, or if TIFF − $\frac{1}{2}$ filter bandwith is less than the frequency at read out for hexadecimal value 00.

- Counter accuracy (AW and AN), with bit 7 (G) the accuracy can be chosen with the same resolution. If bit 7 is logic 1 the accuracy is HIGH and if bit 7 is logic 0 then the accuracy is LOW.

  bit 7 = 0, AN = ± (N2/T)
  bit 7 = 1, AW = ± ($\frac{1}{2}$ x N2/T)

Example

The example uses the following values:

TIFF = 10,7 MHz; accuracy = LOW (G = 0); F_{ref} = 40 kHz (A = 1); IF frequency = 10, 7 MHz (D = 1); resolution = N1 (F = 1) and counter mode = FM (E = 1)

$N1 = (0 \times 4 + 1 \times 5) \times (0 \times 4 + 1 \times 5) \times 8 \times (2^{[1 \times 2 + 0 \times 1]}) \times (1 \times 1 + 0 \times 8) = 800$

$T = 800/40 = 20$ ms

$N2 = (1 \times 16 \times 8 + 0 \times [1 \times 1 + 0 \times 16]) \times (0 \times 2 + 1 \times 1) = 128$

$TDEC = 20 \times 10,7/128 + (1 \times 247 + 0 \times 79) = 1919$

THEX; 1919 is hexadecimal 77F and the least significant 2 digits are 7F, so THEX = 7 F

$R = 128/20 = 6400$ Hz/count

Assume the readout is '6E', the measured frequency will be:

- $F_I = 10,7 + (6E - 7F) \times 6400 = 10,59$ MHz

Assume the readout is '83', the measured frequency will be:

- $F_I = 10,7 + (83 - 7F) \times 6400 = 10,726$

Antenna diversity circuit TEA6101/T

FEATURES

- Ability to switch between up to four antennae
- Switching signal derived from two signals: the audio and the level signals
- Floating switching threshold adjusts switching rate to prevailing circumstances:
  - increasing threshold due to excessive noise
  - increasing threshold due to numerous level variations
- Memory for the most favourable antenna signal to overcome unnecessary switching
- Signal-dependent "soft" muting circuit
- Mode selection to the first antenna receiving an AM signal whilst the diversity system is reset.

APPLICATIONS

- Car radio receivers
- Mobile radio communications equipment

GENERAL DESCRIPTION

Intended for multi-antenna FM car radio reception (antenna diversity system), the TEA6101/T selects the most favourable signal from one of up to four antennae. Founded upon audible signal disturbance the criteria are derived from two signals: high frequency components (e.g. spikes due to noise and multipath reception) and variations in signal level as a result of multipath reception or fluctuations in field strength.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_P	positive supply voltage	–	8.5	–	V
I_P	positive supply current	–	14	–	mA
$V_{I(p-p)}$	audio input voltage (peak-to-peak value)	–	–	3	V
I_{os}	antenna switch output current (source/sink)	–	–	7	mA
V_L	–3 dB audio attenuation (soft mute)	–	1.45	–	V
T_{amb}	operating ambient temperature range	–30	–	+85	°C

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TEA6101	18	DIL	plastic	SOT102
TEA6101T	20	SO	plastic	SOT163A

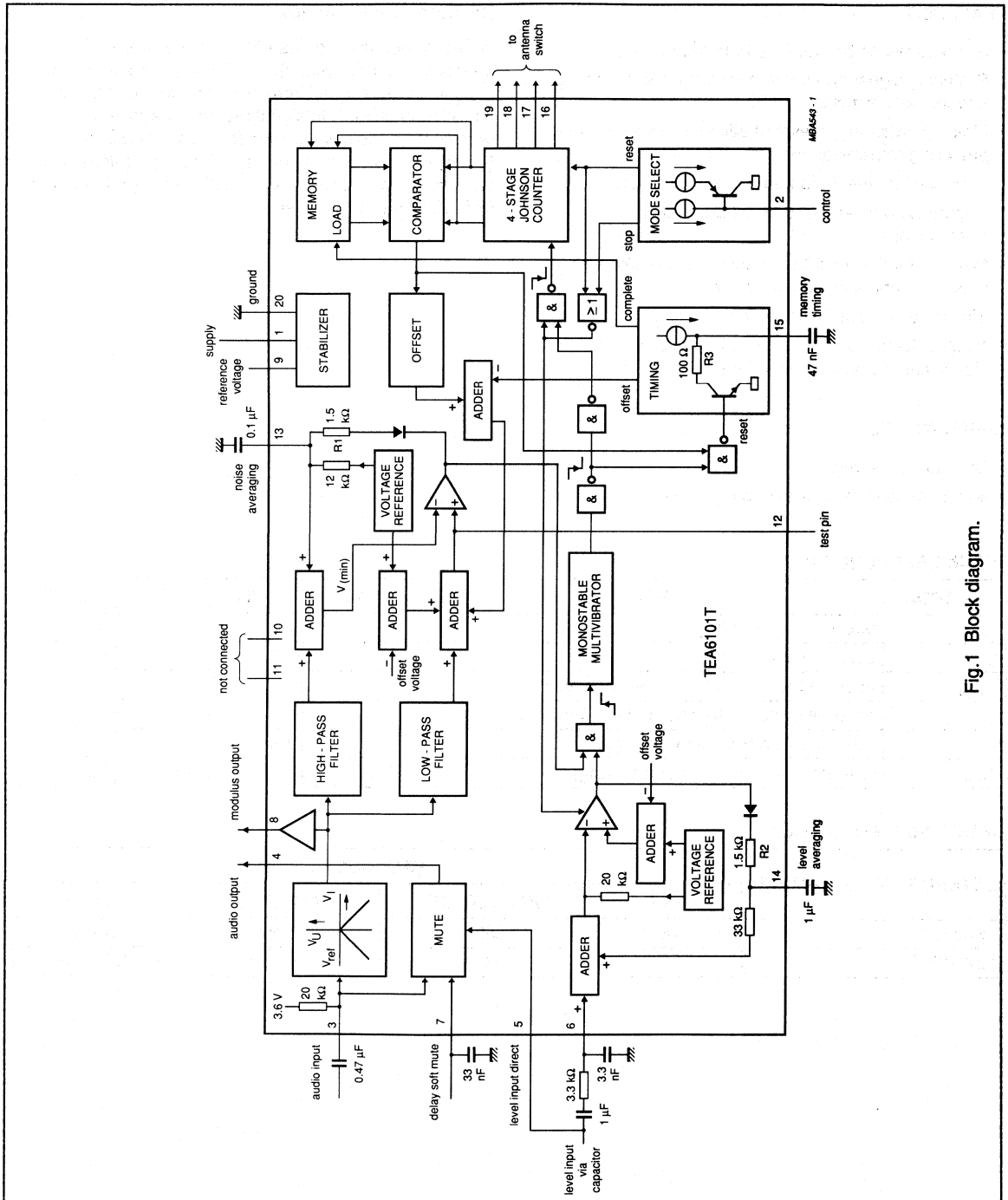


Fig.1 Block diagram.

PINNING

The pin numbers given in parenthesis refer to the TEA6101

SYMBOL	PIN		DESCRIPTION
V_P	1	(1)	positive supply
CTRL	2	(2)	control input
AUDIN	3	(3)	audio input
AUDOUT	4	(4)	audio output
LID	5	(5)	level input direct
LIC	6	(6)	level input via capacitor
DSM	7	(7)	delay soft mute
MODOUT	8	(8)	modulus output
V_{ref}	9	(9)	reference voltage
n.c.	10	–	not connected
n.c.	11	–	not connected
TEST	12	(10)	test pin
NOAV	13	(11)	noise averaging
LEAV	14	(12)	level averaging
MT	15	(13)	memory timing
OUT4	16	(14)	output 4
OUT3	17	(15)	output 3
OUT2	18	(16)	output 2
OUT1	19	(17)	output 1
GND	20	(18)	ground

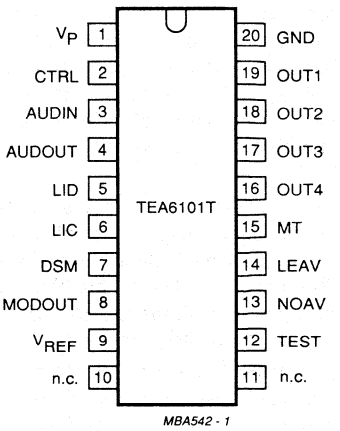


Fig.2 Pin configuration (TEA6101T).

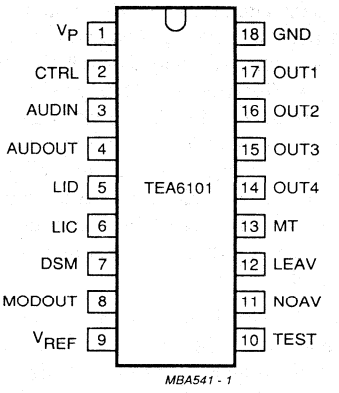


Fig.3 Pin configuration (TEA6101).

FUNCTIONAL DESCRIPTION

Various forms of disturbance can affect signal reception in car radio receivers:

- ignition interference produces spikes on the audio signal. Switching to another antenna will be ineffective. Strong ignition interference, however, will modulate the antenna field strength. In this instance another antenna possessing a directional pattern will suffer less disturbance and switching would be appropriate.
- variation of antenna field strength due to travelling through a zone of variable signal strength will result in a variation in the signal level. Greater noise will be apparent on the audio signal whilst the IF limiter is not limiting. Switching to an alternative antenna input would increase the signal strength.
- multipath reception occurs when a signal reaches the antenna from two or more directions. Often the signals will be of different phase. In certain circumstances the sum of the reflected signals results in zero and a large spike will be evident on the audio signal. It will then be necessary to switch to an alternative antenna from which the sum of the received signals will be different.

The criteria for an antenna diversity system are high frequency components (spikes and noise) on the audio signal in combination with variations in signal level.

Detection of spikes on the audio signal

A rectifier, high pass filter, low pass filter and a comparator are used to detect spikes and noise on the audio signal (see Fig.1). The negative spikes are detected by the rectifier whilst a high pass filter removes the audio signal to leave the high frequency signal components at the negative input to the comparator. The signal at the positive input to the comparator consists of an offset together with an audio signal attenuated by the low pass filter. If the amplitude of the spikes exceed that of the attenuated audio plus offset, the output of the comparator is HIGH.

When the switching rate of the comparator is HIGH, feedback increases the offset via the diode, the resistor R1, and the 100 nF capacitor. The offset is decreased by the 12 kΩ resistor and the 100 nF capacitor (pin 11 or 13). The result is an offset based upon the comparator switching rate, rapid to increase but slow to decrease, therefore permitting only the largest spikes to trigger the comparator (floating threshold).

Should high noise be apparent on the audio signal, the offset is decreased by means of the rectifier and high pass filter. This will result in more frequent switching to an alternative antenna whilst the result of the switching operation will be less audible.

Detection of voltage level variation

A 1 μF input capacitor and 20 kΩ resistor remove the absolute level voltage to leave only variations to be detected. The level comparator output is HIGH when the variations in level voltage are greater than the offset. Similarly to the audio comparator; the feedback diode, resistor R2, the 1 μF capacitor and the 33 kΩ resistor cause the threshold level to float. During periods of high activity the comparator thus switches only on the largest variations.

Switching to an alternative antenna

When both the level and the audio comparator outputs are HIGH, another output of the Johnson counter will be selected. Since switching to an alternative antenna would cause a disturbance of the audio and level signals the monostable multivibrator will prohibit the counter from selecting another antenna input for 21 μs.

Memory and timing

Approximately similar qualities of signal originating from different antennae could result in unnecessary antenna switching. This is prevented by appointing a priority antenna. The selection of an antenna without priority results in the audio offset being decreased by 1.2 V such that the audio comparator will have a HIGH output voltage. During the period of memory timing the offset increases towards the normal offset value. Should level alterations occur during this period another antenna will be selected. If, however, the memory is timed-out without the occurrence of signal variation, priority will be appointed to the selected antenna. Thus a priority antenna will be selected for the majority of the time during reception of almost all similarly weak antenna signals.

Mute

A mute function should not precede the circuit. This function is therefore assumed by the TEA6101. When used in combination with the TEA6100 the 20 kΩ input of the IF IC together with the 6 kΩ output resistor of the TEA6101 cause an attenuation of 3 dB. The mute circuit therefore has 3 dB amplification of level voltages in excess of 2.75 V.

Mode selection

The diversity system is intended for FM reception. To avoid an audible disturbance if it is used with an AM system, the circuit can be reset. In the reset mode antenna 1 (pin 17 (19)) is selected and both comparators are switched off to prevent pulses reaching the output.

For FM search tuning the diversity system may be similarly disabled. The selected antenna will again be retained with the comparators being inhibited.

Test pin

Although intended for test purposes the test pin can be used to increase the audio offset (resistor from pin 10 (12) to ground) or to change the compensation factor (resistor between pin 8 (8) and 10 (12)). These modifications permit the behaviour of the antenna switch to be adapted to alternative IF amplifier IC's.

LIMITING VALUES

In accordance with the absolute maximum system (IEC 134)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_P	positive supply voltage	0	12	V
P_{tot}	total power dissipation	–	see Fig.3	
T_{amb}	operating ambient temperature range	–30	+85	°C
T_{stg}	storage temperature range	–55	+150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ c\text{-}a}$	from crystal to ambient (SOT102)	75 K/W
$R_{th\ c\text{-}a}$	from crystal to ambient (SOT163A)	150 K/W

DC CHARACTERISTICS

Measurements using application circuit (Fig 1) at T_{amb} = 25 °C and V_P = 8.5 V. Voltages with respect to pin 18 (20); pin numbers in parenthesis refer to TEA6101T; all currents positive into the IC unless otherwise specified.

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
V_P	positive supply voltage		7.5	8.5	12	V
I_P	positive supply current	I_{SO} = 0 mA	–	14	–	mA
P_{tot}	total power dissipation		–	119	–	mW
V_{pins}	voltage at pin:					
	1 (1)		–	8.5	–	V
	2 (2)		–	7.8	–	V
	3 (3)		–	3.6	–	V
	4 (4)		–	5.4	–	V
	5 (5)		–	0	–	V
	6 (6)		–	5.3	–	V
	7 (7)		–	0.6	–	V
	8 (8)		–	5.2	–	V
	9 (9)		–	5.4	–	V
	– (10)		–	n.c.	–	
	– (11)		–	n.c.	–	
	10 (12)		–	5.1	–	V
	11 (13)		–	5.4	–	V
	12 (14)		–	5.3	–	V
	13 (15)		–	0	–	V
	14 (16)		–	0	–	V
	15 (17)		–	0	–	V
	16 (18)		–	0	–	V
	17 (19)		–	7.5	–	V
	18 (20)		–	0	–	V

AC CHARACTERISTICS

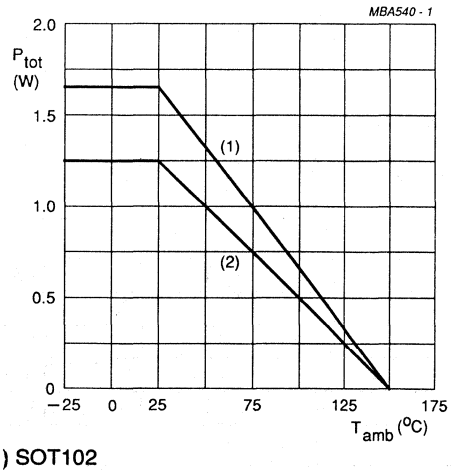
V_P = 8.5 V; T_{amb} = 25 °C; unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Mute						
SOFT MUTE (V_L)						
Z_I	input impedance (pin 3 (3))		–	20	–	kΩ
MR	mute range	note 1	17	19.3	–	V
V_{aud}/V_I	mute gain	V_L = 2.75 V	–	2.7	–	dB
		V_L = 1.45 V	–1	0.6	2	dB
HARD MUTE (VMUTE)						
V_{mute}	–60 dB output attenuation		–	455	–	mV
$+I_m$	mute ON sink current	V_{mute} = 1 V, V_L = 0 V	–	370	–	µA
$-I_m$	mute "OFF" source current	V_{mute} = 0 V	3	–	–	µA
THD	total harmonic distortion	V_i = 200 mV; V_L = 2.5 V	–	0.09	–	%
$V_{I(p-p)}$	audio input voltage (peak-to-peak value)	THD > 10%	–	3	–	V
(S+N)/N	signal-to-noise ratio; measured with dB(A) curve	V_{aud} = 600 mV; 1 kHz; V_L = 3 V	–	95	–	dB
V_{aud}/V_p	ripple rejection	note 2; 300 Hz; 100 mV; V_L = 2.5 V	28	32	–	dB
V_{ref}	output reference voltage		–	5.3	–	V
V_{off1}	audio comparator offset voltage	$V_{off1} = V_{min} - V_{ap}$				
		with priority	–	+250	–	mV
		with no priority				
		V_t = 0 V	–	–1100	–	mV
		V_t = 3 V	–	–348	–	mV
Level comparator						
$V_{ref}-V_{il}$	voltage for high comparator output		–	56	–	mV
t	monostable multivibrator time period	started with both comparator outputs HIGH	16	21	28	µs
Timing/memory						
$-I_t$	source current		–	30	–	µA
C_t	value delay capacitor		–	–	50	nF
T_t	timing duration	C_t = 47 nF	–	6	–	ms
$+I_t$	reset current	V_t = 3 V	–	17.7	–	mA
V_t	change of priority antenna		–	3.7	–	V
Antenna switch outputs						
$-I_{os}$	output source current		–	–	7	mA
$+I_{os}$	output sink current		–	–	7	mA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{SO}	selected output voltage					
		I_{SO} = −10 mA	V_P−2 V	–	–	V
		I_{SO} = 0.5 mA	V_P−1 V	–	–	V
V_{NSO}	not selected output voltage					
		I_{SO} = +10 mA	–	–	0.7	V
		I_{SO} = 0 mA	–	–	0.1	V
Mode selection						
ENABLE						
V_r	all functions active		–	–	1	V
$-I_r$	input current	V_r = 1 V	–	–	12	µA
RESET (ACTIVE AT OPEN INPUT)						
V_r	voltage at first antenna (pin 17 (19))		4.2	–	V_P	V
STOP						
V_r	keep selected antenna voltage		1.6	–	3.5	V

Notes to the AC characteristics

1. $\frac{V_{aud}\,(a\ V_L = 2.75\ V)}{V_{aud}\,(a\ V_L = 0.1\ V)}$
2. When V_P (pin 1 (1)) is filtered with R = 25 Ω and C = 100 µF the ripple rejection becomes 46 dB



(1) SOT102

(2) SOT163A

Fig.4 Derating curve.

INTEGRATED AM UPCONVERSION RECEIVER

GENERAL DESCRIPTION

The TEA6200 is an integrated AM upconversion receiver circuit with an IF of 10.7 MHz. Because of the high dynamic range of the RF prestage there is no tuned prestage. The whole selectivity is provided by crystal filters. The circuit is intended for use in AM radios with synthesizer tuning.
The TEA6200 can handle RF signals up to 2 V RMS.

Features

- No pre-tuned selection is required
- No LW/MW switching
- RF input is protected from static discharge from the aerial
- Electronic standby switch
- Voltage controlled oscillator for synthesizer tuning
- IF output providing level information for search tuning.
- No alignment required.

QUICK REFERENCE DATA

parameter	symbol	min.	typ.	max.	unit
Supply voltage range	V_P	7.6	8.5	9.4	V
Supply current range	I_P	–	50	70	mA
AF output voltage with: RF at 1 MHz and 10 mV f_m at 400 Hz and 30%	V_{af}	–	350	–	mV
AGC start	V_{rf}	30	50	80	μV
AGC range	ΔV_{rf}	–	95	–	dB

PACKAGE OUTLINE

20-lead dual in line; plastic (SOT146).

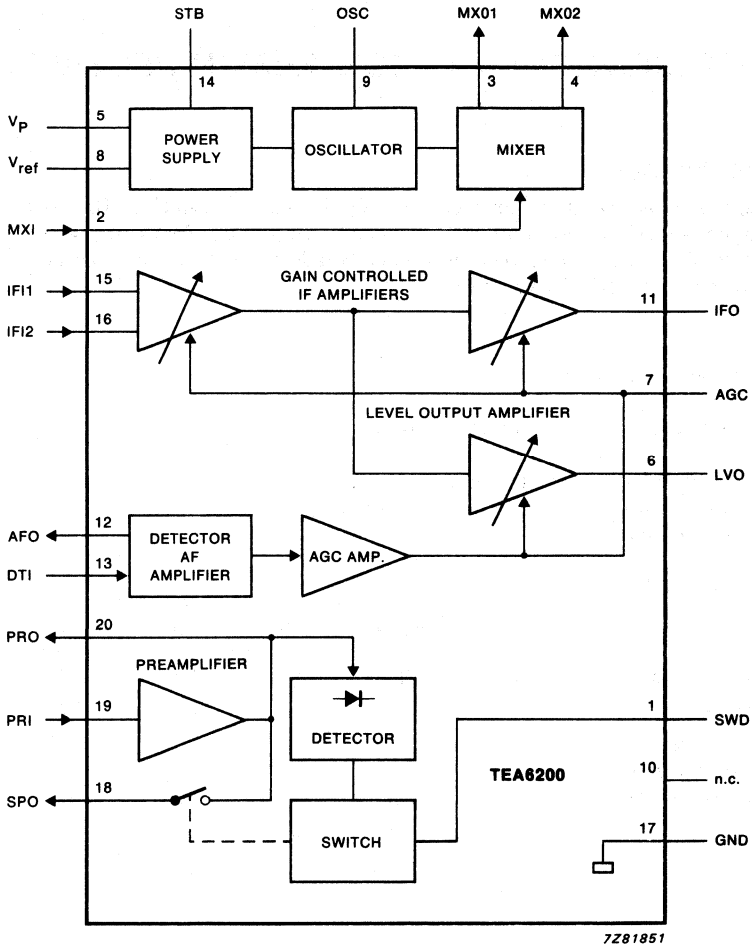


Fig. 1 Block diagram.

PINNING

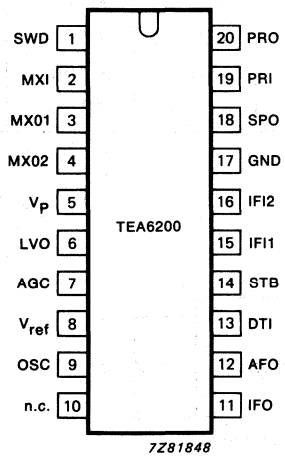


Fig. 2 Pinning diagram.

1	SWD	switching delay
2	MXI	mixer input
3	MXO1	mixer output 1
4	MXO2	mixer output 2
5	V_P	supply voltage
6	LVO	level output
7	AGC	AGC time constant
8	V_{ref}	reference voltage
9	OSC	oscillator
10	n.c.	not internally connected*
11	IFO	IF output
12	AFO	AF output
13	DTI	detector input
14	STB	standby switch
15	IFI1	IF input 1
16	IFI2	IF input 2
17	GND	ground
18	SPO	switched prestage output
19	PRI	prestage input
20	PRO	prestage output

* Pin 10 must be connected to pin 5, 8 or 17.

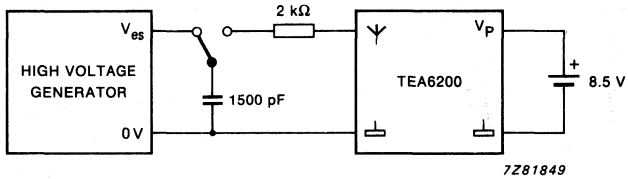
RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage	V_P	–	12	V
Supply current	I_P	–	70	mA
Total power dissipation	P_{tot}	–	850	mW
Operating ambient temperature range	T_{amb}	−30	+ 85	°C
Storage temperature range	T_{stg}	−40	+ 150	°C
Electrostatic discharge voltage	$\pm V_{es}$	–	10	kV

THERMAL RESISTANCE

From junction to ambient $R_{th\ j\text{-}a}$ = 80 K/W



Will tolerate discharge between −10 kV and + 10 kV.

Fig. 3. Test circuit in accordance with IEC 315-1 clause 25.

DC CHARACTERISTICS

V_P = 8.5 V; $V_{14} = V_P$; Signal in OFF condition; all voltages referenced to ground unless otherwise specified.

parameter	conditions	symbol	min.	typ.	max.	unit
Mixer input		V_I	–	4.0	–	V
Mixer output 1		V_O	–	8.5	–	V
Mixer output 2		V_O	–	8.5	–	V
Level output		V_O	–	8.5	–	V
AGC voltage		V_{AGC}	–	0.65	–	V
Reference voltage		V_{ref}	–	4.0	–	V
Oscillator DC voltage		V_{OSC}	–	4.0	–	V
Prestage input		V_I	–	1.2	–	V
Prestage output		V_O	–	3.2	–	V

CHARACTERISTICS

V_P = 8.5 V; T_{amb} = 25 °C; f_{RF} = 1 MHz at 10 mV RMS; Q_{OSC} = 50; modulation = 400 Hz at 30%; insertion loss of filters: crystal filter = 1 dB; ceramic filter = 4 dB, all voltages referenced to ground unless otherwise specified.

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage range		V_P	7.6	8.5	9.4	V
Supply current range		I_P	–	50	70	mA
Guaranteed operating voltage		V_P	7.0	–	10.0	V
Standby switch						
ON voltage		V_{14}	3.2	–	V_P	V
OFF voltage		V_{14}	0	–	1	V
ON current		$\|I_{14}\|$	–	–	10	μA
OFF current		$-I_{14}$	–	–	0.5	mA
Supply current	device OFF	I_P	–	–	10	mA
Prestage	note 1					
Switching threshold	modulation = 80%	V_{rf}	–	320	–	mV
Hysteresis		V_{rf}	1.5	3.5	5.5	dB

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Oscillator						
Frequency range		f_{osc}	10.8	–	17.8	MHz
Oscillator amplitude		V_{osc}	200	420	–	mV
Tuned circuit selectivity		Q_{OSC}	20	50	–	–
Mixer						
Input capacitance		$C_{2\text{-}8}$	–	5	10	pF
Input impedance		$Z_{2\text{-}8}$	10	40	–	kΩ
Conversion transconductance		$I_{3\text{-}4}/V_{2\text{-}8}$	–	3.8	–	S
IF amplifier						
Input impedance		$R_{16\text{-}15}$	10	–	–	kΩ
Input capacitance		$C_{16\text{-}15}$	–	–	5	pF
Output impedance		Z_{11}	230	330	430	Ω
Detector	note 2					
Input impedance		Z_{13}	265	380	500	Ω
Output impedance		Z_{12}	7	10	14	kΩ
Output level		V_{af}	250	350	500	mV
Reference voltage						
Voltage	V_P = 8.5 V	V_8	3.8	4.0	4.2	V
Output impedance		Z_8	–	20	–	Ω
Ripple rejection		$\frac{\Delta V_P}{\Delta V_8}$	40	–	–	dB
Level output pin 6	see Fig. 5					
Output impedance		Z_6	–	1	–	kΩ
Output voltage	V_{rf} = 70 μV	V_6	0.5	0.7	1.0	mV
Output voltage	V_{rf} = 2 mV	V_6	–	15	–	mV

parameter	conditions	symbol	min.	typ.	max.	unit
RF sensitivity						
RF input	(S + N)/N = 6 dB	V_{rf}	–	11	20	μV
	(S + N)/N = 26 dB	V_{rf}	–	110	150	μV
	(S + N)/N = 46 dB	V_{rf}	–	1100	2000	μV
	RF = 150 kHz (S + N)/N = 26 dB	V_{rf}	–	200	–	μV
Output signal						
AF output voltage	V_{rf} = 10 mV	V_{af}	250	350	500	mV
	V_{rf} = 20 μV	V_{af}	–	100	–	mV
Total distortion	V_{rf} = 1 mV; modulation = 80%	d_{tot}	–	3	5	%
Signal plus noise-to-noise ratio	RF = 10 mV to 1 V	(S+N)/N	53	57	–	dB
Ripple rejection	V_P = 8.5 V + V_r 20 Hz < fR < 20 kHz V_{rms} = 40 mV	$\frac{\Delta V_P}{\Delta V_{af}}$	20	–	–	dB
Large signal handling						
Aerial input voltage	THD = 10%; modulation = 80%	V_{rf}	2	3	–	V
AGC range of preamplifier switch			–	12	–	dB
Switching threshold	modulation = 80%	V_{rf}	–	320	–	mV
Hysteresis	modulation = 80%	V_{rf}	1.5	3.5	5.5	dB
Ripple rejection of preamplifier	20 Hz < f_R < 1.5 MHz	$\frac{\Delta V_P}{\Delta V_{20}}$	–	40	–	dB
AGC						
AGC range			–	95	–	dB
Change of V_{af}	100 μV < V_{rf} < 2 V		–	2	3	dB
AGC start		V_{rf}	30	50	80	μV
Intermodulation free dynamic range						
Long wave	350/250 kHz					
second order	input noise level = –99 dBm	IMFDR 2	72	82	–	dB
third order	input noise level = –99 dBm	IMFDR 3	–	86	–	dB
Medium wave	650/1550 kHz					
second order	input noise level = –104 dBm	IMFDR 2	74	84	–	dB
third order	1.25/1.4 MHz input noise level = –104 dBm	IMFDR 3	–	90	–	dB

Notes to the characteristics

1. The prestage is connected to the aerial by a 6 MHz low-pass filter that decouples unwanted aerial cable resonance frequencies. The large dynamic range of the prestage is achieved by use of a transimpedance amplifier with a feedback loop consisting of an equivalent aerial capacitance and a feedback capacitor. When large RF signals are received the feedback capacitance in the loop is increased and the gain subsequently reduced, (see Fig. 4).

   Voltage gain for small signals $G_V = V_{rf} \times \frac{C_{ae}}{C_1}$

   Voltage gain for large signals $G_V = V_{rf} \times \frac{C_{ae}}{C_1 + C_2}$

2. To protect the demodulator and the AGC circuitry, against parasitic oscillation in the IF section, a ceramic filter is connected between the IF output and detector input.

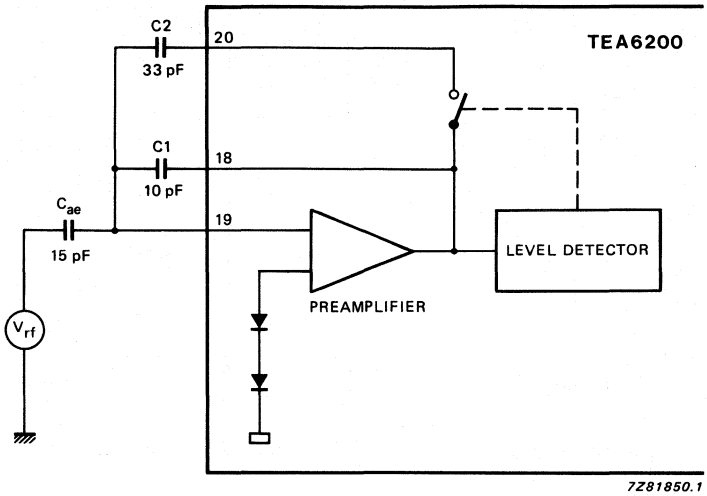


Fig. 4 Prestage circuit.

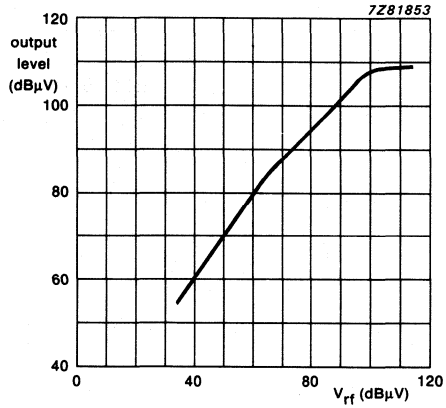


Fig. 5 IF output level.

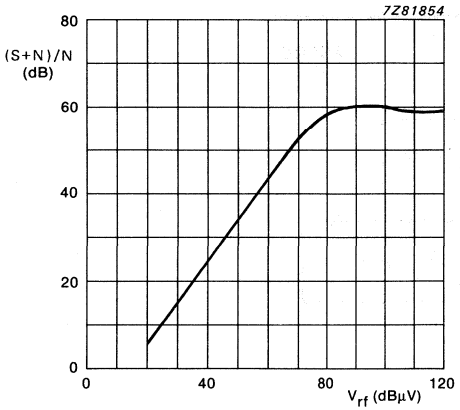


Fig. 6 Signal plus noise-to-noise ratio.

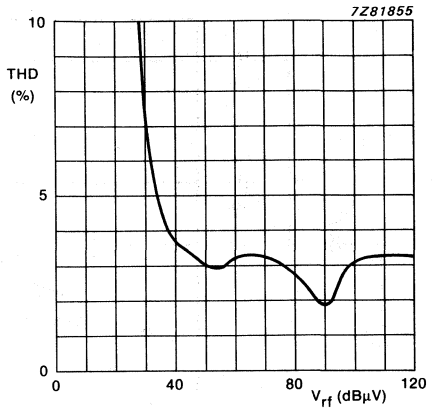


Fig. 7 Total harmonic distortion.

APPLICATION INFORMATION

Notes Fig. 8.

	Component	Circuit identity	Supplier reference
(1)	Crystal filters	XTAL	NDK 10T 7 BA
(2)	Ceramic filter	SFE	Murata E 10 7 S
(3)	Transformer	T1	Toko 7PS-1078 JK
(4)	Variable capacitance diode.	D1	BB609, BB809 or BBY40
(5)	Oscillator coil	L1	Toko 7PS-1077 X

APPLICATION INFORMATION

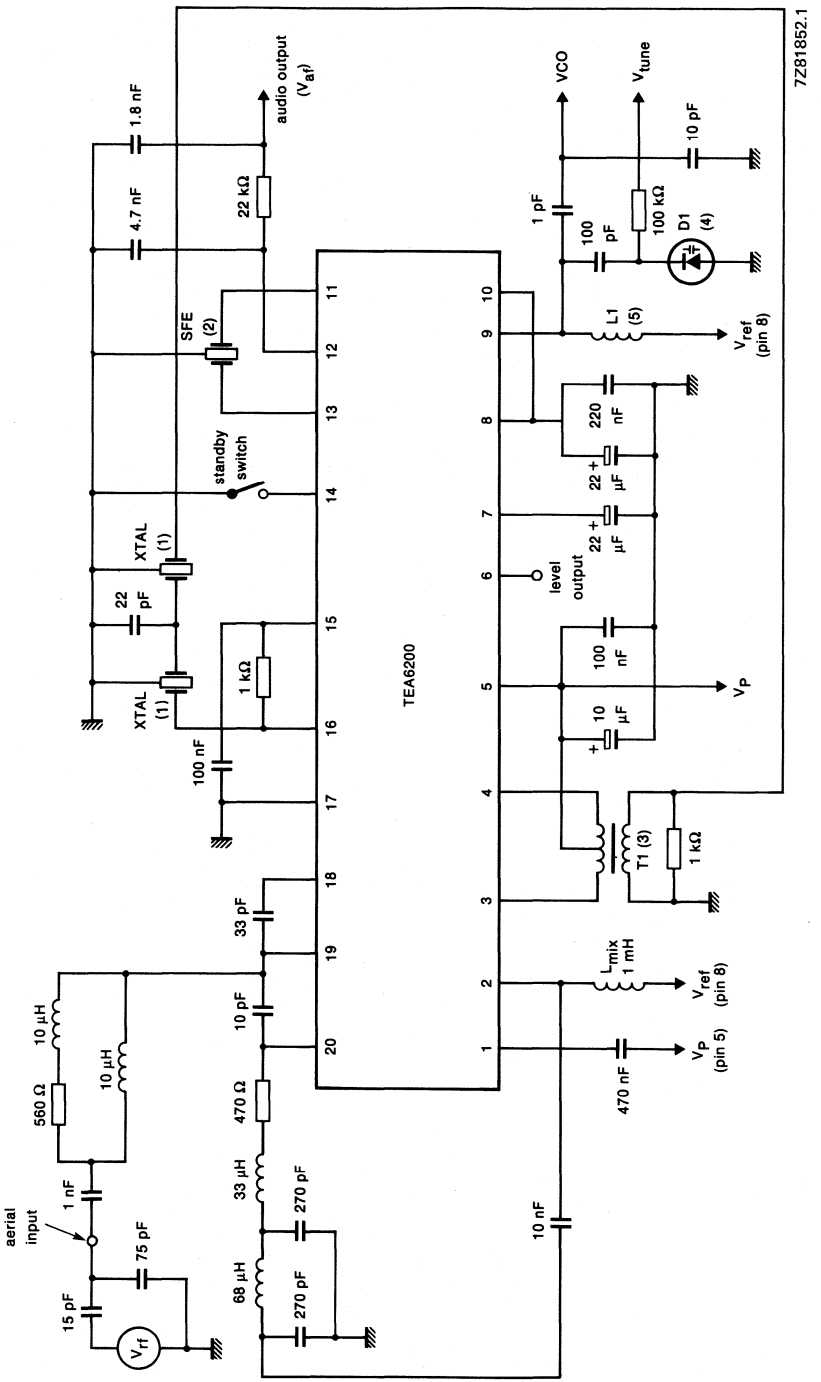


Fig. 8 Application diagram.

SOUND FADER CONTROL CIRCUIT

GENERAL DESCRIPTION

The Sound Fader Control circuit (SOFAC) is an I²C-bus controlled preamplifier for car radios.

Features

- Source selector for three stereo inputs
- Inputs and outputs for noise reduction circuits
- Volume and balance control; control range of 86 dB in steps of 2 dB
- Bass and treble control from + 15 dB (treble 12 dB) to −12 dB in steps of 3 dB
- Fader control from 0 dB to −30 dB in steps of 2 dB
- Fast muting
- Low noise suitable for DOLBY* B and C NR (noise reduction)
- Signal handling suitable for compact disc
- I²C-bus control for all functions
- ESD protected

QUICK REFERENCE DATA

parameter	symbol	min.	typ.	max.	unit
Supply voltage	V_{CC}	7,0	8,5	13,2	V
Input sensitivity for full power at the output stage	$V_{i(rms)}$	–	50	–	mV
Input signal handling	$V_{i(rms)}$	–	1,65	–	V
Frequency response	f_r	35	–	20 000	Hz
Channel separation f = 250 Hz to 10 kHz	α_{CS}	70	92	–	dB
Total harmonic distortion	THD	–	0,05	–	%
Signal plus noise-to-noise ratio	(S+N)/N	–	80	–	dB
Operating ambient temperature range	T_{amb}	−40	–	+ 85	°C

* Dolby is a registered trademark of Dolby Laboratories Licencing Corporation, San Fransisco, California (U.S.A.).

PACKAGE OUTLINES

28-lead dual in-line; plastic (SOT117).
28-lead mini-pack; plastic (SO28; SOT136A).

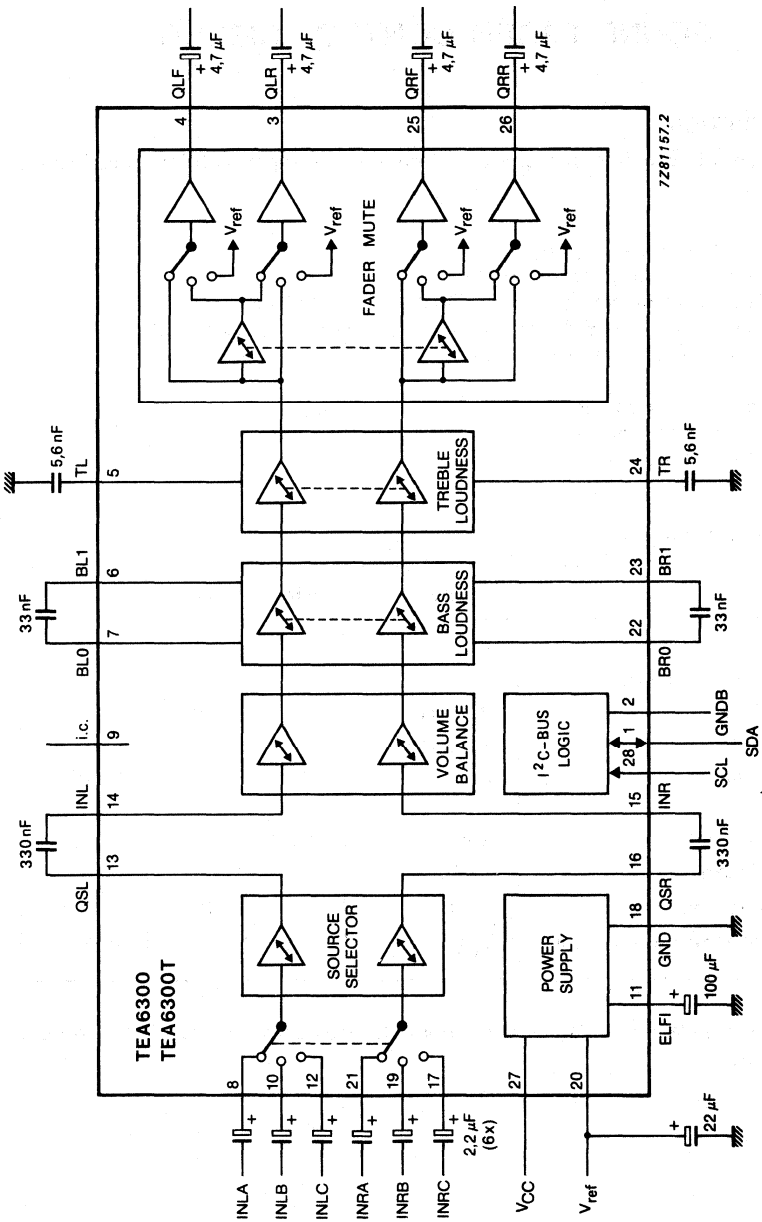


Fig. 1 Block diagram.

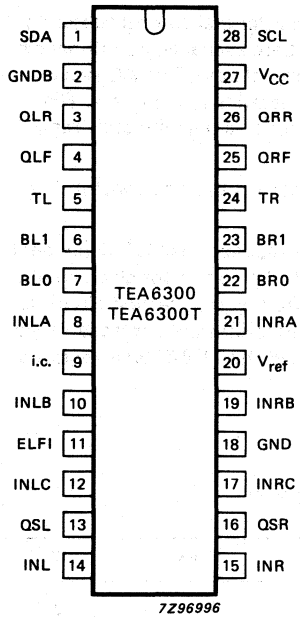


Fig. 2 Pinning diagram.

PINNING

1	SDA	serial data input/output (I^2C-bus)
2	GNDB	ground for I^2C-bus terminals
3	QLR	output left rear
4	QLF	output left front
5	TL	treble control capacitor; left channel
6	BL1	bass control capacitor; left channel
7	BL0	bass control capacitor; left channel
8	INLA	input left source A
9	i.c.	internally connected
10	INLB	input left source B
11	ELFI	electronic filtering for supply
12	INLC	input left source C
13	QSL	output source selector left
14	INL	input left control part
15	INR	input right control part
16	QSR	output source selector right
17	INRC	input right source C
18	GND	ground
19	INRB	input right source B
20	V_{ref}	reference voltage (1/2 V_{CC})
21	INRA	input right source A
22	BR0	bass control capacitor; right channel
23	BR1	bass control capacitor; right channel
24	TR	treble control capacitor; right channel
25	QRF	output right front
26	QRR	output right rear
27	V_{CC}	supply voltage
28	SCL	serial clock input (I^2C-bus)

FUNCTIONAL DESCRIPTION

The source selector selects three stereo channels —RF part (AM/FM), recorder and compact disc. As the outputs of the source selector and the inputs of the main control part are available, additional circuits such as compander and equalizer systems may be inserted into the signal path. The AC signal setting is performed by resistor chains in combination with multi-input operational amplifiers. The advantage of this principle is the combination of low noise, low distortion and a high dynamic range for the circuit.

The separate volume controls of the left and the right channel facilitate correct balance control. The range and balance control is software programmable.

Because the TEA6300 has four outputs a low-level fader is included. The fader control is independent of the volume control and an extra mute position is built in for the front, the rear or for all channels. The last function may be used for muting during preset selection. An extra pop suppression circuit is built in for pop-free switching on and off. As all switching and control functions are controllable via the two-wire I^2C-bus, no external interface between the microcomputer and the TEA6300 is required.

The on-chip power-on-reset sets the TEA6300 to the general mute mode.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage (pin 27-18)	V_{CC}	–	16	V
Maximum power dissipation	P_{tot}	–	1	W
Storage temperature range	T_{stg}	−55	+ 150	°C
Operating ambient temperature range	T_{amb}	−40	+ 85	°C

CHARACTERISTICS

V_{CC} = 8,5 V; R_S = 600 Ω; R_L = 10 kΩ; f = 1 kHz; T_{amb} = 25 °C; test circuit Fig. 10; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply voltage	V_{CC}	7,0	8,5	13,2	V
Supply current	I_{CC}	–	26	–	mA
Supply current at 8,5 V	I_{CC}	–	–	33	mA
Supply current at 13,2 V	I_{CC}	–	–	44	mA
DC voltage inputs, outputs and reference	V_{DC}	0,45	0,5	0,55	V_{CC}
Internal reference voltage (pin 20) V_{ref} = 0,5 V_{CC}	V_{REF}	–	4,25	–	V
Maximum voltage gain bass and treble linear, fader off	G_v	19	20	21	dB
Output voltage level for P_{max} at the output stage for start of clipping	$V_{o(rms)}$ $V_{o(rms)}$	– –	500 1000	– –	mV mV
Input sensitivity at V_o = 500 mV	$V_{i(rms)}$	–	50	–	mV
Frequency response bass and treble linear; roll-off frequency –1 dB	f_r	35	–	20 000	Hz
Channel separation G_v = 0 dB; bass and treble linear; frequency range 250 Hz to 10 kHz	α_{CS}	70	92	–	dB
Total harmonic distortion frequency range 20 Hz to 12,5 kHz					
V_i = 50 mV; G_v = 20 dB	THD	–	0,1	0,3	%
V_i = 500 mV; G_v = 0 dB	THD	–	0,05	0,2	%
V_i = 1,6 V; G_v = –10 dB	THD	–	0,2	0,5	%
Ripple rejection $V_{r(rms)}$ < 200 mV; G_v = 0 dB; bass and treble linear;					
at f = 100 Hz	RR_{100}	–	70	–	dB
at f = 40 Hz to 12,5 kHz	RR_{range}	–	60	–	dB

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Signal plus noise-to-noise ratio bass and treble linear; notes 1 and 2 CCIR 468-2 weighted; quasi peak					
V_i = 50 mV; V_o = 46 mV; P_o = 50 mW	(S + N)/N	–	65	–	dB
V_i = 500 mV; V_o = 45 mV; P_o = 50 mW	(S + N)/N	–	67	–	dB
V_i = 50 mV; V_o = 200 mV; P_o = 1 W	(S + N)/N	65	70	–	dB
V_i = 500 mV; V_o = 200 mV; P_o = 1 W	(S + N)/N	65	78	–	dB
V_i = 50 mV; V_o = 500 mV; P_o = 6 W	(S + N)/N	–	70	–	dB
V_i = 500 mV; V_o = 500 mV; P_o = 6 W	(S + N)/N	–	85	–	dB
Noise output power mute position, only contribution of TEA6300; power amplifier for 25 W	P_{no}	–	–	10	nW
Crosstalk (20 log $V_{bus(p-p)}/V_{o(rms)}$) between bus inputs and signal outputs G_V = 0 dB; bass and treble linear	α_B	–	110	–	dB
Source selector					
Input impedance	Z_i	20	30	40	kΩ
Output impedance	Z_o	–	–	100	Ω
Output load resistance	R_L	10	–	–	kΩ
Output load capacity	C_L	0	–	200	pF
Input isolation not selected source; frequency range 40 Hz to 12,5 kHz	α_S	–	80	–	dB
Voltage gain $R_L \geqslant 10$ kΩ	G_v	–	0	–	dB
Internal bias voltage ratio	$V_{b\,int}/V_{ref}$	–	1	–	
Maximum input voltage level (RMS value) THD < 0,5% THD < 0,5%; V_{CC} = 7,5 V	 $V_{i(rms)}$ $V_{i(rms)}$	 – –	 1,65 1,5	 – –	 V V
Total harmonic distortion V_i = 500 mV; R_L = 10 kΩ	THD	–	–	0,1	%
Noise output voltage weighted CCIR 468-2, quasi peak	V_{no}	–	9	20	μV
DC offset voltage between any inputs	V_o	–	–	10	mV
Control part					
Source selector disconnected, source resistance 600 Ω					
Input impedance	Z_i	35	50	65	kΩ
Output impedance	Z_o	–	100	150	Ω
Output load resistance	R_L	5	–	–	kΩ
Output load capacity	C_L	0	–	2500	pF

parameter	symbol	min.	typ.	max.	unit
Maximum input voltage THD < 0,5%; G_v = −10 dB; bass and treble linear	$V_{i(rms)}$	–	2,0	–	V
Noise output voltage weighted acc CCIR 468-2, quasi peak, bass and treble linear, fader off					
G_v = 20 dB	V_{no}	–	110	220	μV
G_v = 0 dB	V_{no}	–	25	50	μV
G_v = −66 dB	V_{no}	–	19	38	μV
mute position	V_{no}	–	11	22	μV
Volume control					
Continuous control range	G_c	–	86	–	dB
Step resolution		–	2	–	dB
Attenuator set error (G_v = + 20 to −50 dB)	ΔG_a	–	–	2	dB
Attenuator set error (G_v = + 20 to −66 dB)	ΔG_a	–	–	3	dB
Gain tracking error balance in mid position, bass and treble linear	ΔG_t	–	–	2	dB
Mute attenuation	α_m	72	90	–	dB
DC step offset					
Between any adjoining step and any step to mute					
G_v = 0 to −66 dB		–	0,2	10	mV
G_v = 20 to 0 dB		–	2	15	mV
In any treble and fader position G_v = 0 to −66 dB		–	–	10	mV
In any bass position G_v = 0 to −66 dB		–	–	20	mV
Bass control					
Bass control range					
f = 40 Hz; maximum boost	G_b	14	15	16	dB
f = 40 Hz; maximum attenuation	G_b	11	12	13	dB
Step resolution		–	3	–	dB
Step error		–	–	0,5	dB
Treble control					
Treble control range					
f = 15 kHz; maximum boost	G_t	11	12	13	dB
f = 15 kHz; maximum attenuation	G_t	11	12	13	dB
f > 15 kHz; maximum boost	G_t	–	–	15	dB
Step resolution		–	3	–	dB
Step error		–	–	0,5	dB

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Fader control					
Continuous attenuation fader control range	G_f	–	30	–	dB
Step resolution		–	2	–	dB
Attenuator set error		–	–	1,5	dB
Mute attenuation	α_m	74	84	–	dB
Digital part					
Bus terminals					
Input voltage					
HIGH	V_{IH}	3	–	12	V
LOW	V_{IL}	−0,3	–	+ 1,5	V
Input current					
HIGH	I_{IH}	−10	–	+ 10	μA
LOW	I_{IL}	−10	–	+ 10	μA
Output voltage LOW I_L = 3 mA	V_{OL}	–	–	0,4	V
AC characteristics in accordance with the I²C-bus specification					
Power-on-Reset When RESET is active the GMU (general mute) bit is set and the I²C-bus receiver is in RESET position					
Increasing supply voltage					
start of reset	V_{CC}	–	–	2,5	V
end of reset	V_{CC}	5,2	6,0	6,8	V
Decreasing supply voltage					
start of reset	V_{CC}	4,2	5,0	5,8	V

Notes to the characteristics

1. The indicated values for output power assume a 6 W power amplifier with 20 dB gain, connected to the output of the circuit. Signal-to-noise ratios exclude noise contribution of the power amplifier.
2. Signal-to-noise ratios on a CCIR 468-2 average meter reading are 4,5 dB better than on CCIR 468-2 quasi peak.

I²C-BUS FORMAT

S	SLAVE ADDRESS	A	SUBADDRESS	A	DATA	A	P

S = start condition
SLAVE ADDRESS = 1000 0000
A = acknowledge, generated by the slave
SUBADDRESS = see Table 1
DATA = see Table 1
P = STOP condition

If more than 1 byte of DATA is transmitted, then auto-increment of the subaddress is performed.

Table 1 I²C-bus; subaddress/data

function	subaddress	DATA							
		D7	D6	D5	D4	D3	D2	D1	D0
volume left	0 0 0 0 0 0 0 0	X	X	VL5	VL4	VL3	VL2	VL1	VL0
volume right	0 0 0 0 0 0 0 1	X	X	VR5	VR4	VR3	VR2	VR1	VR0
bass	0 0 0 0 0 0 1 0	X	X	X	X	BA3	BA2	BA1	BA0
treble	0 0 0 0 0 0 1 1	X	X	X	X	TR3	TR2	TR1	TR0
fader	0 0 0 0 0 1 0 0	X	X	MFN	FCH	FA3	FA2	FA1	FA0
switch	0 0 0 0 0 1 0 1	GMU	X	X	X	X	SCC	SCB	SCA

Function of the bits:

VL0 to VL5	volume control left
VR0 to VR5	volume control right
BA0 to BA3	bass control
TR0 to TR3	treble control
FA0 to FA3	fader control
FCH	select fader channel (front or rear)
MFN	mute control of the selected fader channel (front or rear)
SCA to SCC	source selector control
GMU	mute control (general mute) for the outputs QLF, QLR, QRF and QRR
X	don't care bits (logic 1 during testing)

Table 2 Bass setting

G_V dB	DATA			
	BA3	BA2	BA1	BA0
+15	1	1	1	1
+15	1	1	1	0
+15	1	1	0	1
+15	1	1	0	0
+12	1	0	1	1
+ 9	1	0	1	0
+ 6	1	0	0	1
+ 3	1	0	0	0
0	0	1	1	1
− 3	0	1	1	0
− 6	0	1	0	1
− 9	0	1	0	0
−12	0	0	1	1
−12	0	0	1	0
−12	0	0	0	1
−12	0	0	0	0

Table 3 Treble setting

G_V dB	DATA			
	TR3	TR2	TR1	TR0
+12	1	1	1	1
+12	1	1	1	0
+12	1	1	0	1
+12	1	1	0	0
+12	1	0	1	1
+ 9	1	0	1	0
+ 6	1	0	0	1
+ 3	1	0	0	0
0	0	1	1	1
− 3	0	1	1	0
− 6	0	1	0	1
− 9	0	1	0	0
−12	0	0	1	1
−12	0	0	1	0
−12	0	0	0	1
−12	0	0	0	0

Table 4 Volume setting LEFT

G_V dB	DATA					
	VL5	VL4	VL3	VL2	VL1	VL0
20	1	1	1	1	1	1
18	1	1	1	1	1	0
16	1	1	1	1	0	1
14	1	1	1	1	0	0
12	1	1	1	0	1	1
10	1	1	1	0	1	0
8	1	1	1	0	0	1
6	1	1	1	0	0	0
4	1	1	0	1	1	1
2	1	1	0	1	1	0
0	1	1	0	1	0	1
− 2	1	1	0	1	0	0
− 4	1	1	0	0	1	1
− 6	1	1	0	0	1	0
− 8	1	1	0	0	0	1
−10	1	1	0	0	0	0
−12	1	0	1	1	1	1
−14	1	0	1	1	1	0
−16	1	0	1	1	0	1
−18	1	0	1	1	0	0
−20	1	0	1	0	1	1
−22	1	0	1	0	1	0
−24	1	0	1	0	0	1
−26	1	0	1	0	0	0
−28	1	0	0	1	1	1
−30	1	0	0	1	1	0
−32	1	0	0	1	0	1
−34	1	0	0	1	0	0
−36	1	0	0	0	1	1
−38	1	0	0	0	1	0
−40	1	0	0	0	0	1
−42	1	0	0	0	0	0
−44	0	1	1	1	1	1
−46	0	1	1	1	1	0
−48	0	1	1	1	0	1
−50	0	1	1	1	0	0
−52	0	1	1	0	1	1
−54	0	1	1	0	1	0
−56	0	1	1	0	0	1
−58	0	1	1	0	0	0
−60	0	1	0	1	1	1
−62	0	1	0	1	1	0
−64	0	1	0	1	0	1
−66	0	1	0	1	0	0
mute left	0	1	0	0	1	1
mute left	0	1	0	0	1	0
.				.		
.				.		
.				.		
mute left	0	0	0	0	0	0

Table 5 Volume setting RIGHT

G_V dB	DATA					
	VR5	VR4	VR3	VR2	VR1	VR0
20	1	1	1	1	1	1
18	1	1	1	1	1	0
16	1	1	1	1	0	1
14	1	1	1	1	0	0
12	1	1	1	0	1	1
10	1	1	1	0	1	0
8	1	1	1	0	0	1
6	1	1	1	0	0	0
4	1	1	0	1	1	1
2	1	1	0	1	1	0
0	1	1	0	1	0	1
− 2	1	1	0	1	0	0
− 4	1	1	0	0	1	1
− 6	1	1	0	0	1	0
− 8	1	1	0	0	0	1
−10	1	1	0	0	0	0
−12	1	0	1	1	1	1
−14	1	0	1	1	1	0
−16	1	0	1	1	0	1
−18	1	0	1	1	0	0
−20	1	0	1	0	1	1
−22	1	0	1	0	1	0
−24	1	0	1	0	0	1
−26	1	0	1	0	0	0
−28	1	0	0	1	1	1
−30	1	0	0	1	1	0
−32	1	0	0	1	0	1
−34	1	0	0	1	0	0
−36	1	0	0	0	1	1
−38	1	0	0	0	1	0
−40	1	0	0	0	0	1
−42	1	0	0	0	0	0
−44	0	1	1	1	1	1
−46	0	1	1	1	1	0
−48	0	1	1	1	0	1
−50	0	1	1	1	0	0
−52	0	1	1	0	1	1
−54	0	1	1	0	1	0
−56	0	1	1	0	0	1
−58	0	1	1	0	0	0
−60	0	1	0	1	1	1
−62	0	1	0	1	1	0
−64	0	1	0	1	0	1
−66	0	1	0	1	0	0
mute right	0	1	0	0	1	1
mute right	0	1	0	0	1	0
.				.		
.				.		
.				.		
mute right	0	0	0	0	0	0

Table 6 Fader function

setting		DATA					
front dB	rear dB	MFN	FCH	FA3	FA2	FA1	FA0
		fader off					
0	0	1	1	1	1	1	1
0	0	0	1	1	1	1	1
		fader front					
− 2	0	1	1	1	1	1	0
− 4	0	1	1	1	1	0	1
− 6	0	1	1	1	1	0	0
− 8	0	1	1	1	0	1	1
−10	0	1	1	1	0	1	0
−12	0	1	1	1	0	0	1
−14	0	1	1	1	0	0	0
−16	0	1	1	0	1	1	1
−18	0	1	1	0	1	1	0
−20	0	1	1	0	1	0	1
−22	0	1	1	0	1	0	0
−24	0	1	1	0	0	1	1
−26	0	1	1	0	0	1	0
−28	0	1	1	0	0	0	1
−30	0	1	1	0	0	0	0
		mute front					
−80	0	0	1	1	1	1	0
.	.			.			
.	.			.			
.	.			.			
−80	0	0	1	0	0	0	0

setting		DATA					
front dB	rear dB	MFN	FCH	FA3	FA2	FA1	FA0
		fader off					
0	0	1	0	1	1	1	1
0	0	0	0	1	1	1	1
		fader rear					
0	− 2	1	0	1	1	1	0
0	− 4	1	0	1	1	0	1
0	− 6	1	0	1	1	0	0
0	− 8	1	0	1	0	1	1
0	−10	1	0	1	0	1	0
0	−12	1	0	1	0	0	1
0	−14	1	0	1	0	0	0
0	−16	1	0	0	1	1	1
0	−18	1	0	0	1	1	0
0	−20	1	0	0	1	0	1
0	−22	1	0	0	1	0	0
0	−24	1	0	0	0	1	1
0	−26	1	0	0	0	1	0
0	−28	1	0	0	0	0	1
0	−30	1	0	0	0	0	0
		mute rear					
0	−80	0	0	1	1	1	0
.	.			.			
.	.			.			
.	.			.			
0	−80	0	0	0	0	0	0

Table 7 Selected inputs

selected inputs	DATA		
	SCC	SCB	SCA
data not allowed	1	1	1
data not allowed	1	1	0
data not allowed	1	0	1
INLC, INRC	1	0	0
data not allowed	0	1	1
INLB, INRB	0	1	0
INLA, INRA	0	0	1
data not allowed	0	0	0

Table 8 Mute control

MUTE control	DATA GMU	remarks
active	1	outputs QLF, QLR QRF and QRR are muted
passive	0	no general mute

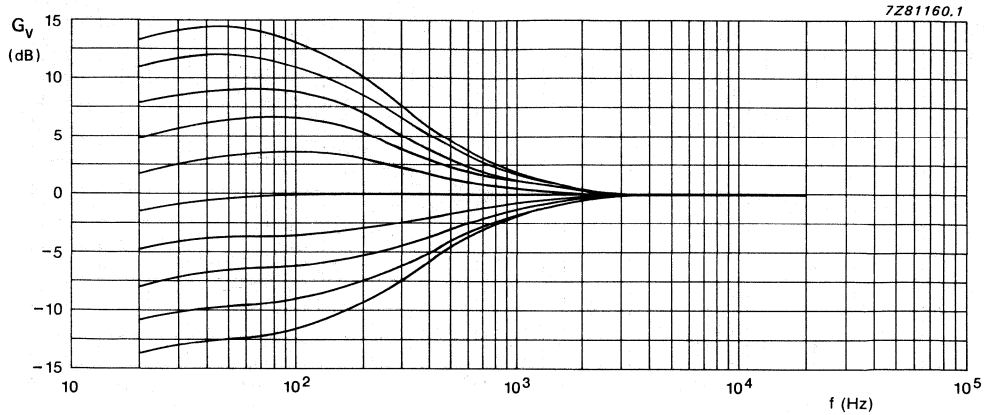


Fig. 3 Bass control without T-pass filter.

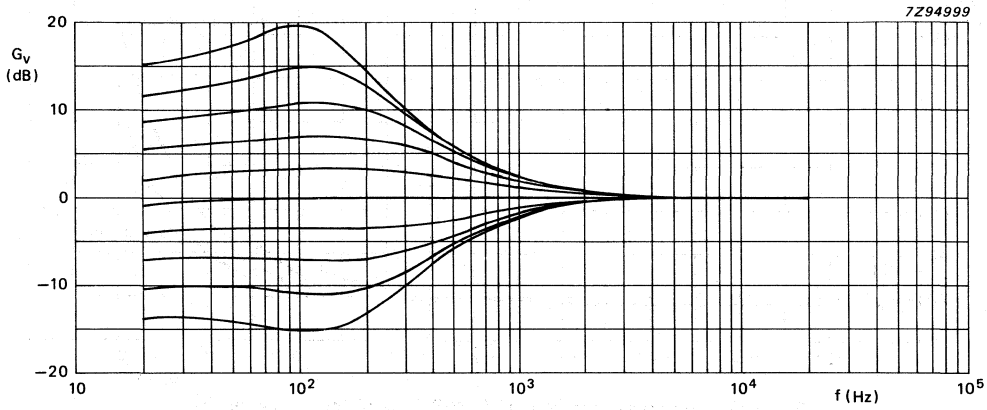
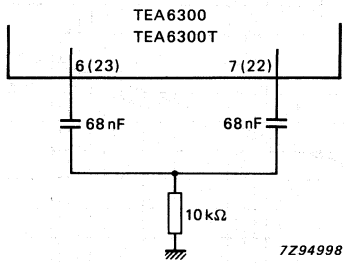


Fig. 4 Bass control with T-pass filter.



Pin numbers in parenthases refer to the bass control, right channel.

Fig. 5 T-pass filter.

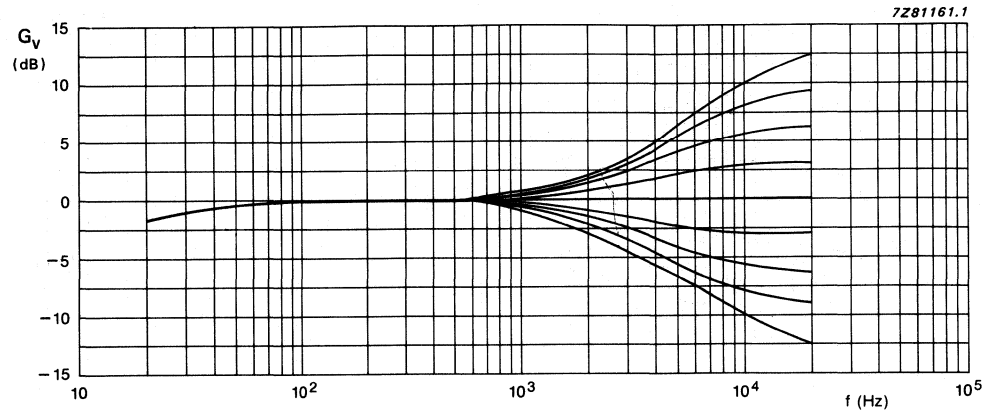


Fig. 6 Treble control.

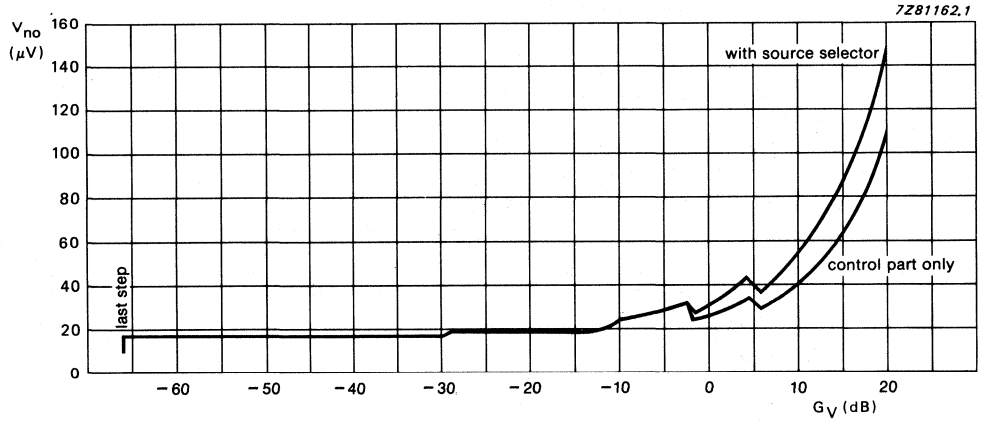


Fig. 7 Output noise voltage (CCIR 468-2 weighted: quasi peak).

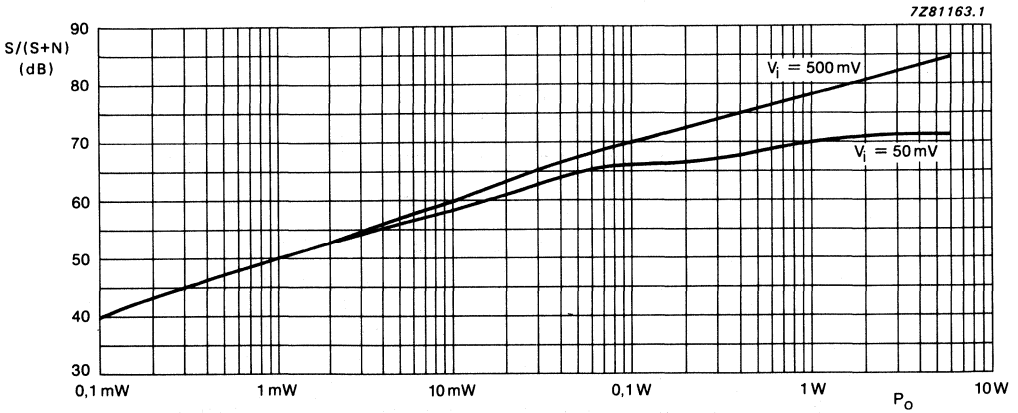


Fig. 8 Signal-to-noise ratio (CCIT 468-2 weighted; quasi peak) with a 6 W power amplifier (gain 20 dB) without noise contribution of the power amplifier (see Fig. 9).

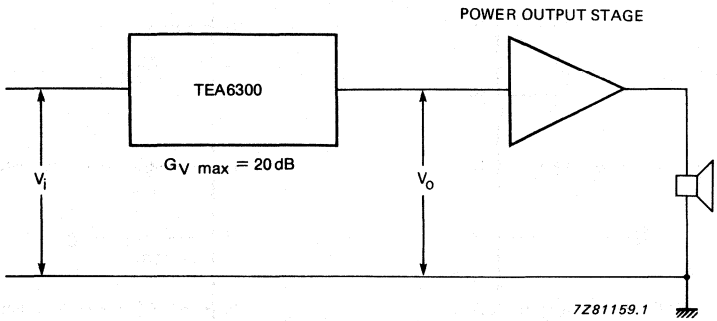


Fig. 9 Recommended level diagram; $V_{i\ min}$ = 50 mV, V_o = 500 mV for P_{max}.

APPLICATION INFORMATION

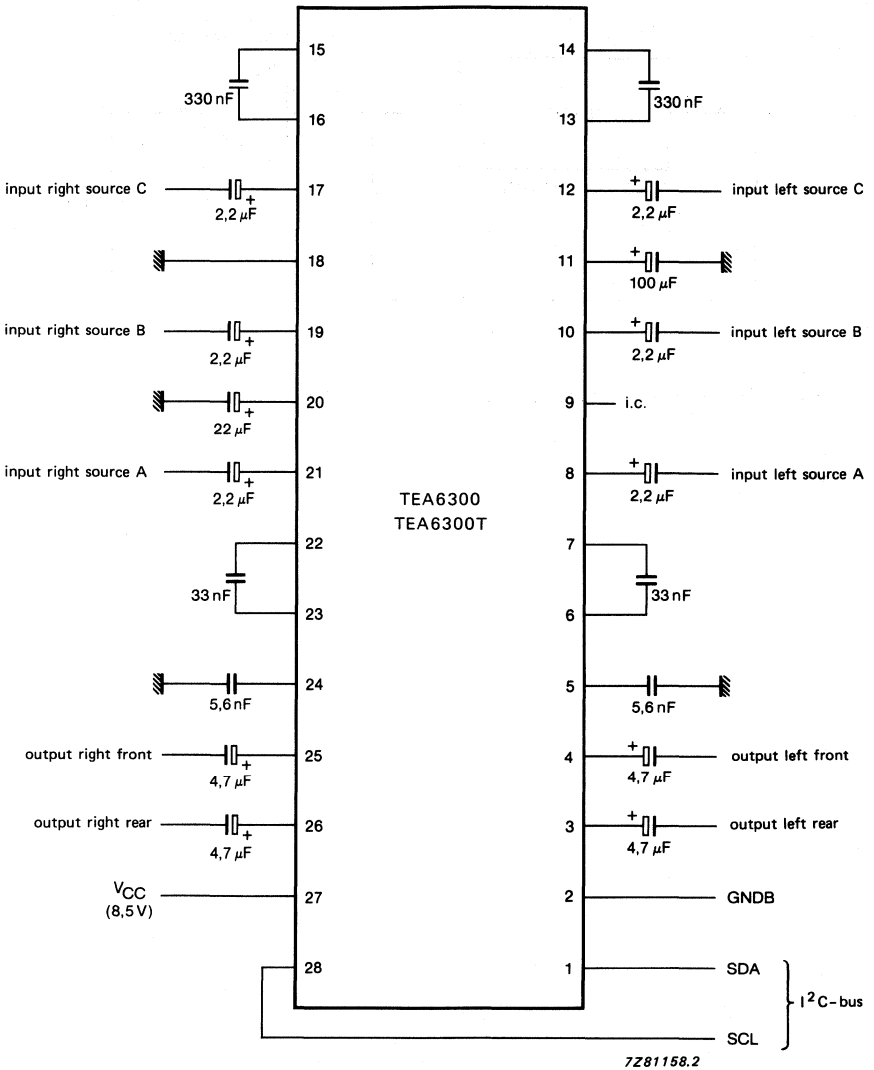


Fig. 10 Test and application circuit.

SOUND FADER CONTROL CIRCUIT

GENERAL DESCRIPTION

The Sound Fader Control circuit (SOFAC) is an I²C-bus controlled tone and volume control circuit for car radios.

Features

- Volume and balance control; control range of 86 dB in steps of 2 dB
- Bass and treble control from +15 dB (treble 12 dB) to −12 dB in steps of 3 dB
- Fader control form 0 dB to −30 dB in steps of 2 dB
- Fast muting
- Low noise suitable for Dolby* B and C NR (noise reduction)
- Signal handling suitable for compact disc
- I²C-bus control for all functions
- ESD protected

QUICK REFERENCE DATA

parameter	symbol	min.	typ.	max.	unit
Supply voltage	V_{CC}	7,0	8,5	13,2	V
Input sensitivity for full power at the output stage	$V_{i(rms)}$	–	50	–	mV
Input signal handling	$V_{i(rms)}$	–	1,65	–	V
Frequency response	f_r	35	–	20 000	Hz
Channel separation f = 250 Hz to 10 kHz	α_{CS}	70	96	–	dB
Total harmonic distortion	THD	–	0,05	–	%
Signal plus noise-to-noise ratio	(S+N)/N	–	80	–	dB
Operating ambient temperature range	T_{amb}	−40	–	+ 85	°C

* Dolby is a registered trademark of Dolby Laboratories Licencing Corporation, San Fransisco, California (U.S.A.).

PACKAGE OUTLINE

28-lead mini-pack; plastic (SO28; SOT136A).

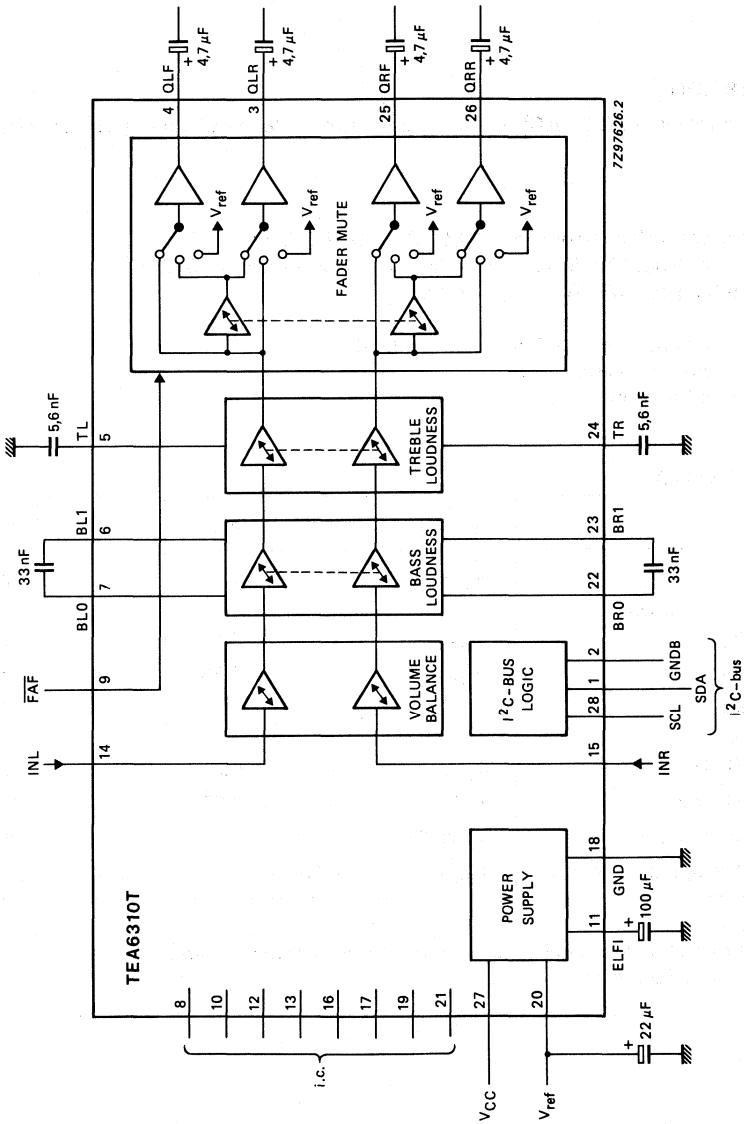


Fig. 1 Block diagram.

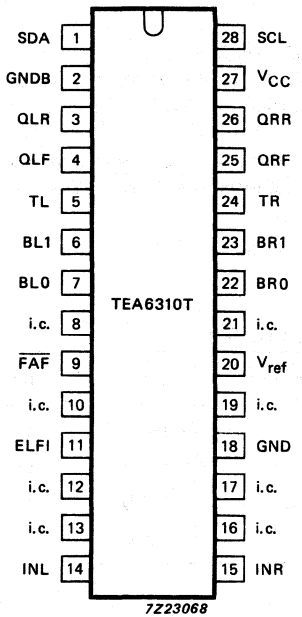


Fig. 2 Pinning diagram

PINNING

1	SDA	serial data input/output (I^2C-bus)
2	GNDB	ground for I^2C-bus terminals
3	QLR	output left rear
4	QLF	output left front
5	TL	treble control capacitor; left channel
6	BL1	bass control capacitor; left channel
7	BL0	bass control capacitor; left channel
8	i.c.	internally connected
9	$\overline{FAF}$	fader off control input
10	i.c.	internally connected
11	ELFI	electronic filtering for supply
12	i.c.	internally connected
13	i.c.	internally connected
14	INL	input left control part
15	INR	input right control part
16	i.c.	internally connected
17	i.c.	internally connected
18	GND	ground
19	i.c.	internally connected
20	V_{ref}	reference voltage (1/2 V_{CC})
21	i.c.	internally connected
22	BR0	bass control capacitor; right channel
23	BR1	bass control capacitor; right channel
24	TR	treble control capacitor; right channel
25	QRF	output right front
26	QRR	output right rear
27	V_{CC}	supply voltage
28	SCL	serial clock input (I^2C-bus)

FUNCTIONAL DESCRIPTION

The AC signal setting is performed by resistor chains in combination with multi-input operational amplifiers. The advantage of this principle is the combination of low noise, low distortion and a high dynamic range for the circuit.

The separate volume controls of the left and the right channel facilitate correct balance control. The range and balance control is software programmable.

Because the TEA6310T has four outputs a low level fader is included. The fader control is independent of the volume control and an extra mute position is built in for the front, the rear or for all channels. The last function may be used for muting during preset selection. The Fader function can be disabled by an input signal at $\overline{FAF}$ (pin 9).
An extra pop suppression circuit is built in for pop-free switching on and off. As all switching and control functions are controllable via the two-wire I^2C-bus, no external interface between the micro-computer and the TEA6310T is required.

The on-chip power-on-reset sets the TEA6310T to the general mute mode.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage (pin 27-18)	V_{CC}	–	16	V
Maximum power dissipation	P_{tot}	–	1	W
Storage temperature range	T_{stg}	−55	+150	°C
Operating ambient temperature range	T_{amb}	−40	+ 85	°C

CHARACTERISTICS

V_{CC} = 8,5 V; R_S = 600 Ω; R_L = 10 kΩ; f = 1 kHz; T_{amb} = 25 °C; test circuit Fig. 10; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply voltage	V_{CC}	7,0	8,5	13,2	V
Supply current	I_{CC}	–	26	–	mA
Supply current at 8,5 V	I_{CC}	–	–	30	mA
Supply current at 13,2 V	I_{CC}	–	–	44	mA
DC voltage inputs, outputs and reference	V_{DC}	0,45	0,5	0,55	V_{CC}
Internal reference voltage (pin 20) V_{ref} = 0,5 V_{CC}	V_{REF}	–	4,25	–	V
Maximum voltage gain bass and treble linear, fader off	G_v	19	20	21	dB
Output voltage level for P_{max} at the output stage	$V_{o(rms)}$	–	500	–	mV
for start of clipping	$V_{o(rms)}$	–	1000	–	mV
Input sensitivity at V_o = 500 mV	$V_{i(rms)}$	–	50	–	mV
Frequency response bass and treble linear; roll-off frequency −1 dB	f_r	35	–	20 000	Hz
Channel separation G_v = 0 dB; bass and treble linear; frequency range 250 Hz to 10 kHz	α_{CS}	70	96	–	dB
Total harmonic distortion frequency range 20 Hz to 12,5 kHz					
V_i = 50 mV; G_v = 20 dB	THD	–	0,1	0,3	%
V_i = 500 mV; G_v = 0 dB	THD	–	0,05	0,2	%
V_i = 1,6 V; G_v = −10 dB	THD	–	0,2	0,5	%
Ripple rejection $V_{r(rms)}$ <200 mV; G_v = 0 dB; bass and treble linear;					
at f = 100 Hz	RR_{100}	–	70	–	dB
at f = 40 Hz to 12,5 kHz	RR_{range}	–	60	–	dB

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Signal-to-noise ratio; bass and treble linear; notes 1 and 2; CCIR 468-2 weighted; quasi peak;					
V_i = 50 mV; V_o = 46 mV; P_o = 50 mW	S/(S + N)	–	65	–	dB
V_i = 500 mV; V_o = 45 mV; P_o = 50 mW	S/(S + N)	–	67	–	dB
V_i = 50 mV; V_o = 200 mV; P_o = 1 W	S/(S + N)	65	72	–	dB
V_i = 500 mV; V_o = 200 mV; P_o = 1 W	S/(S + N)	65	78	–	dB
V_i = 50 mV, V_o = 500 mV; P_o = 6 W	S/(S + N)	–	72	–	dB
V_i = 500 mV; V_o = 500 mV; P_o = 6 W	S/(S + N)	–	86	–	dB
Noise output power mute position, only contribution of TEA310T, power amplifier for 25 W	P_{no}	–	–	10	nW
Crosstalk (20 log $V_{bus(p-p)}/V_{o(rms)}$) between bus inputs and signal outputs G_v = 0 dB; bass and treble linear;	α_B	–	110	–	dB
Control part					
Input impedance	Z_i	35	50	65	kΩ
Output impedance	Z_o	–	100	150	Ω
Output load resistance	R_L	5	–	–	kΩ
Output load capacity	C_L	0	–	2500	pF
Maximum input voltage; THD < 0,5%; G_v = −10 dB; bass and treble linear	$V_{i(rms)}$	–	2,0	–	V
Noise output voltage; weighted acc CCIR 468-2, quasi peak, bass and treble linear, fader off;					
G_v = 20 dB	V_{no}	–	110	220	μV
G_v = 0 dB	V_{no}	–	25	50	μV
G_v = −66 dB	V_{no}	–	19	38	μV
mute position	V_{no}	–	11	22	μV
Volume control					
Continuous control range	G_c	–	86	–	dB
Step resolution		–	2	–	dB
Attenuator set error; (G_v = + 20 to −50 dB)	ΔG_a	–	–	2	dB
Attenuator set error; (G_v = + 20 to −66 dB)	ΔG_a	–	–	3	dB
Gain tracking error; balance in mid position, bass and treble linear	ΔG_t	–	–	2	dB
Mute attenuation	α_m	76	90	–	dB

parameter	symbol	min.	typ.	max.	unit
DC step offset					
Between any adjoining step and any step to mute					
G_v = 0 to −66 dB		–	0,2	10	mV
G_v = 20 to 0 dB		–	2	15	mV
In any treble and fader position					
G_v = 0 to −66 dB		–	–	10	mV
In any bass position					
G_v = 0 to −66 dB		–	–	20	mV
Bass control					
Bass control range;					
f = 40 Hz; maximum boost	G_b	14	15	16	dB
f = 40 Hz; maximum attenuation	G_b	11	12	13	dB
Step resolution		–	3	–	dB
Step error		–	–	0,5	dB
Treble control					
Treble control range					
f = 15 kHz; maximum boost	G_t	11	12	13	dB
f = 15 kHz; maximum attenuation	G_t	11	12	13	dB
f > 15 kHz; maximum boost	G_t	–	–	15	dB
Step resolution		–	3	–	dB
Step error		–	–	0,5	dB
Fader control					
Continous attenuation fader control range	G_f	–	30	–	dB
Step resolution		–	2	–	dB
Attenuator set error		–	–	1,5	dB
Mute attenuation	α_m	74	84	–	dB
Fader enable/disable control (pin 9)					
Fader enabled					
Input voltage HIGH	$V_{9\text{-}18}$	3	–	12	V
Fader disabled					
Input voltage LOW	$V_{9\text{-}18}$	−0,3	–	1,5	V
Input current					
HIGH	I_9	−10	–	+10	μA
LOW	I_9	−10	–	+10	μA

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Digital part					
Bus terminals					
Input voltage					
HIGH	V_{IH}	3	–	12	V
LOW	V_{IL}	−0,3	–	1,5	V
Input current					
HIGH	I_{IH}	−10	–	+10	μA
LOW	I_{IL}	−10	–	+10	μA
Output voltage LOW I_L = 3 mA	V_{OL}	–	–	0,4	V
AC characteristics					
in accordance with the I^2C-bus specification					
Power-on-Reset					
When RESET is active the GMU (general mute) bit is set and the I^2C-bus receiver is in RESET position					
Increasing supply voltage					
start of reset	V_{CC}	–	–	2,5	V
end of reset	V_{CC}	5,2	6,0	6,8	V
Decreasing supply voltage start of reset	V_{CC}	4,2	5,0	5,8	V

Notes to the characteristics

1. The indicated values for output power assume a 6 W power amplifier with 20 dB gain, connected to the output of the circuit. Signal-to-noise ratios exclude noise contribution of the power amplifier.
2. Signal-to-noise ratios on a CCIR 468-2 average meter reading are 4,5 dB better than on CCIR 468-2 quasi peak.

I²C-BUS FORMAT

S	SLAVE ADDRESS	A	SUBADDRESS	A	DATA	A	P

S = start condition
SLAVE ADDRESS = 10000 0000
A = acknowledge, generated by the slave
SUBADDRESS = see Table 1
DATA = see Table 1
P = STOP condition

If more than 1 byte DATA are transmitted, then auto-increment of the subaddress is performed.

Table 1 I²C-bus; subaddress/data

function	subaddress	DATA							
		D7	D6	D5	D4	D3	D2	D1	D0
volume left	0 0 0 0 0 0 0 0	X	X	VL5	VL4	VL3	VL2	VL1	VL0
volume right	0 0 0 0 0 0 0 1	X	X	VR5	VR4	VR3	VR2	VR1	VR0
bass	0 0 0 0 0 0 1 0	X	X	X	X	BA3	BA2	BA1	BA0
treble	0 0 0 0 0 0 1 1	X	X	X	X	TR3	TR2	TR1	TR0
fader	0 0 0 0 0 1 0 0	X	X	MFN	FCH	FA3	FA2	FA1	FA0
switch	0 0 0 0 0 1 0 1	GMU	X	X	X	X	X	X	X

Function of the bits:

VL0 to VL5	volume control left
VR0 to VR5	volume control right
BA0 to BA3	bass control
TR0 to TR3	treble control
FA0 to FA3	fader control
FCH	select fader channel (front or rear)
MFN	mute control of the selected fader channel (front or rear)
GMU	mute control (general mute) for the outputs QLF, QLR, QRF and QRR
X	don't care bits (logic 1 during testing)

Table 2 Bass setting

G_V dB	DATA			
	BA3	BA2	BA1	BA0
+ 15	1	1	1	1
+ 15	1	1	1	0
+ 15	1	1	0	1
+ 15	1	1	0	0
+ 12	1	0	1	1
+ 9	1	0	1	0
+ 6	1	0	0	1
+ 3	1	0	0	0
0	0	1	1	1
− 3	0	1	1	0
− 6	0	1	0	1
− 9	0	1	0	0
−12	0	0	1	1
−12	0	0	1	0
−12	0	0	0	1
−12	0	0	0	0

Table 3 Treble setting

G_V dB	DATA			
	TR3	TR2	TR1	TR0
+ 12	1	1	1	1
+ 12	1	1	1	0
+ 12	1	1	0	1
+ 12	1	1	0	0
+ 12	1	0	1	1
+ 9	1	0	1	0
+ 6	1	0	0	1
+ 3	1	0	0	0
0	0	1	1	1
− 3	0	1	1	0
− 6	0	1	0	1
− 9	0	1	0	0
−12	0	0	1	1
−12	0	0	1	0
−12	0	0	0	1
−12	0	0	0	0

Table 4 Volume setting LEFT

G_V dB	DATA					
	VL5	VL4	VL3	VL2	VL1	VL0
20	1	1	1	1	1	1
18	1	1	1	1	1	0
16	1	1	1	1	0	1
14	1	1	1	1	0	0
12	1	1	1	0	1	1
10	1	1	1	0	1	0
8	1	1	1	0	0	1
6	1	1	1	0	0	0
4	1	1	0	1	1	1
2	1	1	0	1	1	0
0	1	1	0	1	0	1
− 2	1	1	0	1	0	0
− 4	1	1	0	0	1	1
− 6	1	1	0	0	1	0
− 8	1	1	0	0	0	1
−10	1	1	0	0	0	0
−12	1	0	1	1	1	1
−14	1	0	1	1	1	0
−16	1	0	1	1	0	1
−18	1	0	1	1	0	0
−20	1	0	1	0	1	1
−22	1	0	1	0	1	0
−24	1	0	1	0	0	1
−26	1	0	1	0	0	0
−28	1	0	0	1	1	1
−30	1	0	0	1	1	0
−32	1	0	0	1	0	1
−34	1	0	0	1	0	0
−36	1	0	0	0	1	1
−38	1	0	0	0	1	0
−40	1	0	0	0	0	1
−42	1	0	0	0	0	0
−44	0	1	1	1	1	1
−46	0	1	1	1	1	0
−48	0	1	1	1	0	1
−50	0	1	1	1	0	0
−52	0	1	1	0	1	1
−54	0	1	1	0	1	0
−56	0	1	1	0	0	1
−58	0	1	1	0	0	0
−60	0	1	0	1	1	1
−62	0	1	0	1	1	0
−64	0	1	0	1	0	1
−66	0	1	0	1	0	0
mute left	0	1	0	0	1	1
mute left	0	1	0	0	1	0
.				.		
.				.		
.				.		
mute left	0	0	0	0	0	0

Table 5 Volume setting RIGHT

G_V dB	DATA					
	VR5	VR4	VR3	VR2	VR1	VR0
20	1	1	1	1	1	1
18	1	1	1	1	1	0
16	1	1	1	1	0	1
14	1	1	1	1	0	0
12	1	1	1	0	1	1
10	1	1	1	0	1	0
8	1	1	1	0	0	1
6	1	1	1	0	0	0
4	1	1	0	1	1	1
2	1	1	0	1	1	0
0	1	1	0	1	0	1
− 2	1	1	0	1	0	0
− 4	1	1	0	0	1	1
− 6	1	1	0	0	1	0
− 8	1	1	0	0	0	1
−10	1	1	0	0	0	0
−12	1	0	1	1	1	1
−14	1	0	1	1	1	0
−16	1	0	1	1	0	1
−18	1	0	1	1	0	0
−20	1	0	1	0	1	1
−22	1	0	1	0	1	0
−24	1	0	1	0	0	1
−26	1	0	1	0	0	0
−28	1	0	0	1	1	1
−30	1	0	0	1	1	0
−32	1	0	0	1	0	1
−34	1	0	0	1	0	0
−36	1	0	0	0	1	1
−38	1	0	0	0	1	0
−40	1	0	0	0	0	1
−42	1	0	0	0	0	0
−44	0	1	1	1	1	1
−46	0	1	1	1	1	0
−48	0	1	1	1	0	1
−50	0	1	1	1	0	0
−52	0	1	1	0	1	1
−54	0	1	1	0	1	0
−56	0	1	1	0	0	1
−58	0	1	1	0	0	0
−60	0	1	0	1	1	1
−62	0	1	0	1	1	0
−64	0	1	0	1	0	1
−66	0	1	0	1	0	0
mute right	0	1	0	0	1	1
mute right	0	1	0	0	1	0
.				.		
.				.		
.				.		
mute right	0	0	0	0	0	0

Table 6 Fader function

setting front dB	setting rear dB	DATA MFN	FCH	FA3	FA2	FA1	FA0
		fader off					
0	0	1	1	1	1	1	1
0	0	0	1	1	1	1	1
		fader front					
− 2	0	1	1	1	1	1	0
− 4	0	1	1	1	1	0	1
− 6	0	1	1	1	1	0	0
− 8	0	1	1	1	0	1	1
−10	0	1	1	1	0	1	0
−12	0	1	1	1	0	0	1
−14	0	1	1	1	0	0	0
−16	0	1	1	0	1	1	1
−18	0	1	1	0	1	1	0
−20	0	1	1	0	1	0	1
−22	0	1	1	0	1	0	0
−24	0	1	1	0	0	1	1
−26	0	1	1	0	0	1	0
−28	0	1	1	0	0	0	1
−30	0	1	1	0	0	0	0
		mute front					
−80	0	0	1	1	1	1	0
.	.			.			
.	.			.			
.	.			.			
−80	0	0	1	0	0	0	0

setting front dB	setting rear dB	DATA MFN	FCH	FA3	FA2	FA1	FA0
		fader off					
0	0	1	0	1	1	1	1
0	0	0	0	1	1	1	1
		fader rear					
0	− 2	1	0	1	1	1	0
0	− 4	1	0	1	1	0	1
0	− 6	1	0	1	1	0	0
0	− 8	1	0	1	0	1	1
0	−10	1	0	1	0	1	0
0	−12	1	0	1	0	0	1
0	−14	1	0	1	0	0	0
0	−16	1	0	0	1	1	1
0	−18	1	0	0	1	1	0
0	−20	1	0	0	1	0	1
0	−22	1	0	0	1	0	0
0	−24	1	0	0	0	1	1
0	−26	1	0	0	0	1	0
0	−28	1	0	0	0	0	1
0	−30	1	0	0	0	0	0
		mute rear					
0	−80	0	0	1	1	1	0
.	.			.			
.	.			.			
.	.			.			
0	−80	0	0	0	0	0	0

Table 7 Mute control

MUTE control	DATA GMU	remarks
active	1	outputs QLF, QLR QRF and QRR are muted
passive	0	no general mute

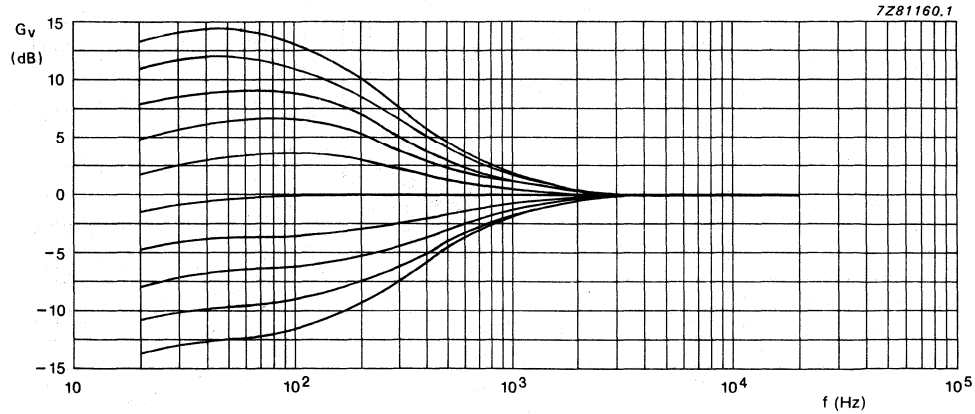


Fig. 3 Bass control without T-pass filter.

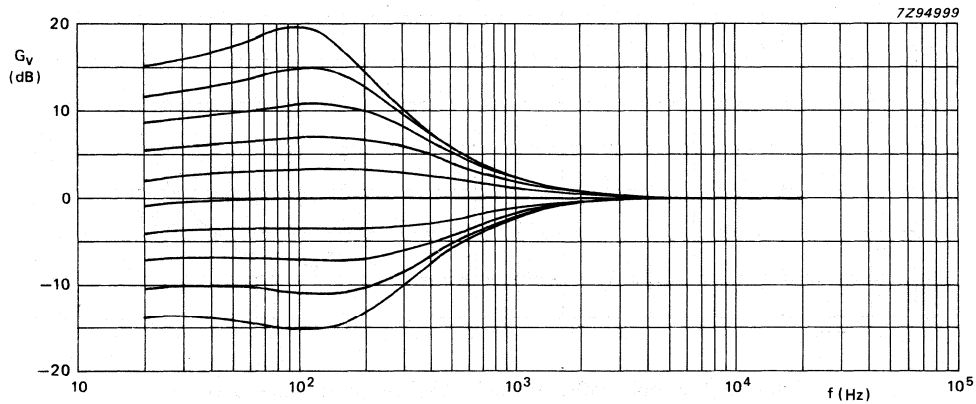
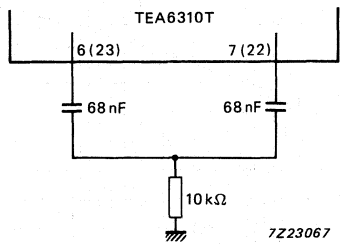


Fig. 4 Bass control with T-pass filter.



Pin numbers in parentheses refer to the bass control, right channel.

Fig. 5 T-pass filer.

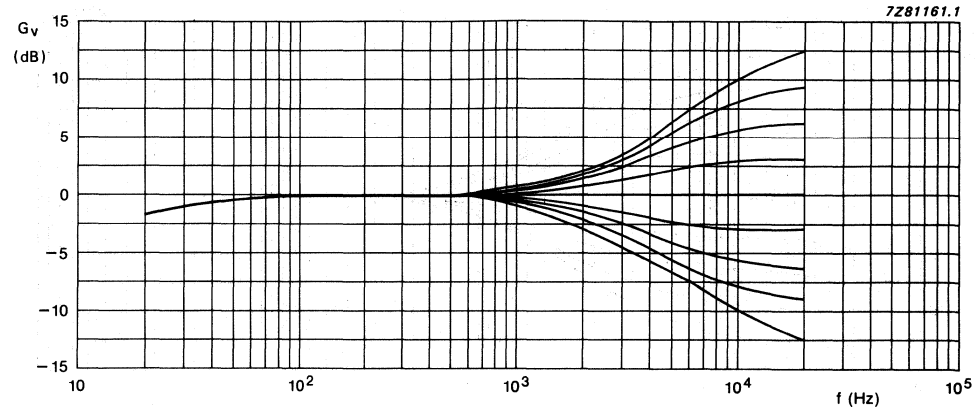


Fig. 6 Treble control.

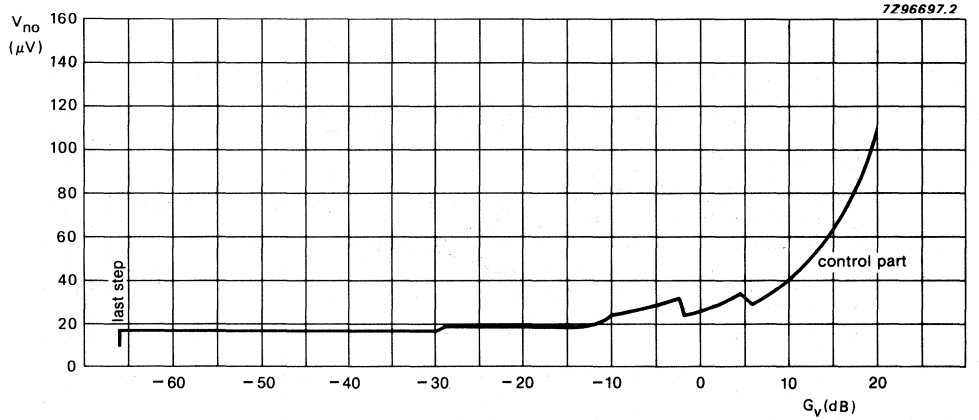


Fig. 7 Output noise voltage (CCIR 468-2 weighted: quasi peak).

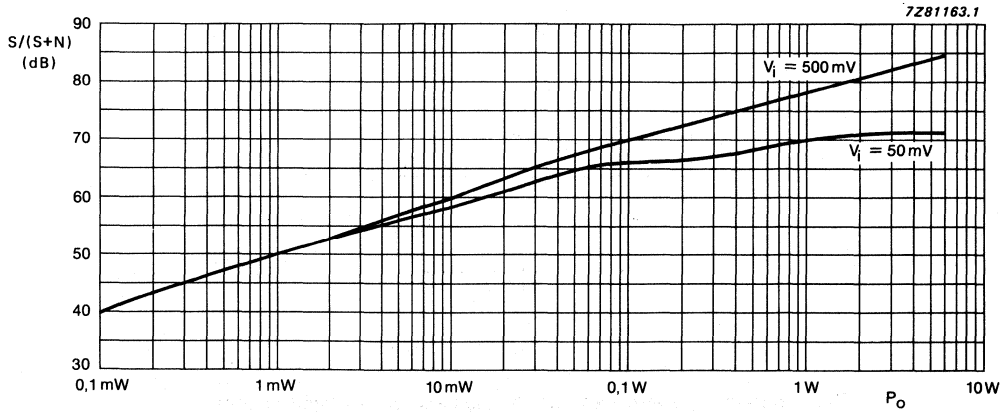


Fig. 8 Signal-to-noise ratio (CCIT 468-2 weighted; quasi peak) with a 6 W power amplifier (gain 20 dB) without noise contribution of the power amplifier (see Fig. 9).

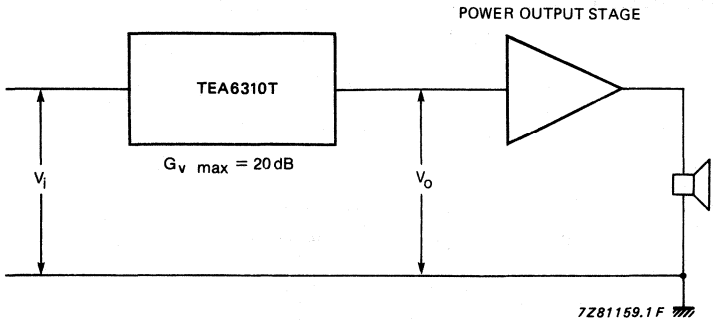


Fig. 9 Recommended level diagram; $V_{i\,min}$ = 50 mV, V_o = 500 mV for P_{max}.

APPLICATION INFORMATION

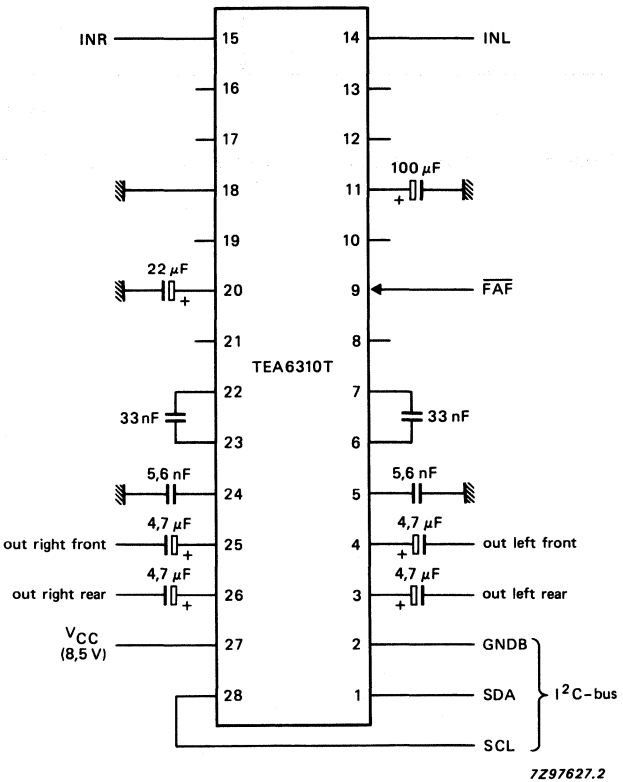


Fig. 10 Test and application circuit.

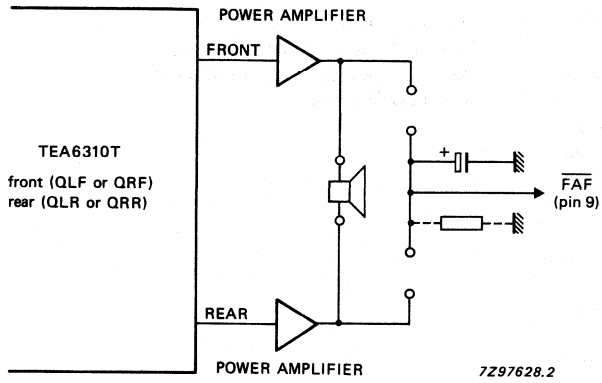


Fig. 11 Automatic FADER control; P_o = 24 W, $V_{9\text{-}18}$ = 0 V (FADER disabled).

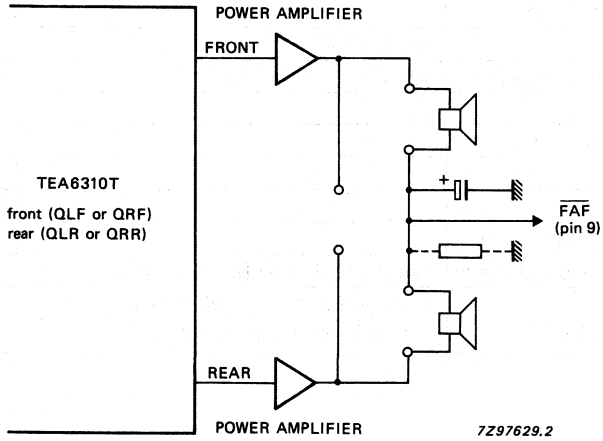


Fig. 12 Automatic FADER control; P_o = 2 x 6 W, $V_{9\text{-}18}$ = 7 V (FADER enabled).

Sound fader control circuit TEA6320

FEATURES

- Source selector for four stereo and one mono inputs
- Interface for noise reduction circuits
- Interface for external equalizer
- Volume, balance and fader control
- Special loudness characteristic automatically controlled in combination with volume setting
- Bass and treble control
- Mute control at audio signal zero crossing
- Fast mute control via I^2C-bus
- Fast mute control via pin
- I^2C-bus control for all functions
- Power supply with internal power-on reset

GENERAL DESCRIPTION

The sound fader control circuit TEA6320 is an I^2C-bus controlled stereo preamplifier for car radio hi-fi sound applications.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}	positive supply voltage		7.5	8.5	9.5	V
I_{CC}	supply current	V_{CC} = 8.5 V	–	26	–	mA
$V_{o(RMS)}$	maximum output voltage level	V_{CC} = 8.5 V; THD ≤ 0.1%	–	2000	–	mV
G_v	volume gain		–86	–	+20	dB
G_{step}	step resolution (volume)		–	1	–	dB
G_b	bass control		–15	–	+15	dB
G_t	treble control		–12	–	+12	dB
G_{step}	step resolution (bass, treble)		–	1.5	–	dB
(S+N)/N	signal-plus-noise to noise ratio	V_o = 2.0 V; G_v = 0 dB; unweighted	–	105	–	dB
RR_{100}	ripple rejection	$V_{r(RMS)}$ < 200 mV; f = 100 Hz; G_v = 0 dB	–	75	–	dB
α_{cs}	channel separation	250 Hz ≤ f ≤ 10 kHz; G_v = 0 dB	90	96	–	dB

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TEA6320	32	SDIL	plastic	SOT232AG
TEA6320T	32	SO	plastic	SOT287AH

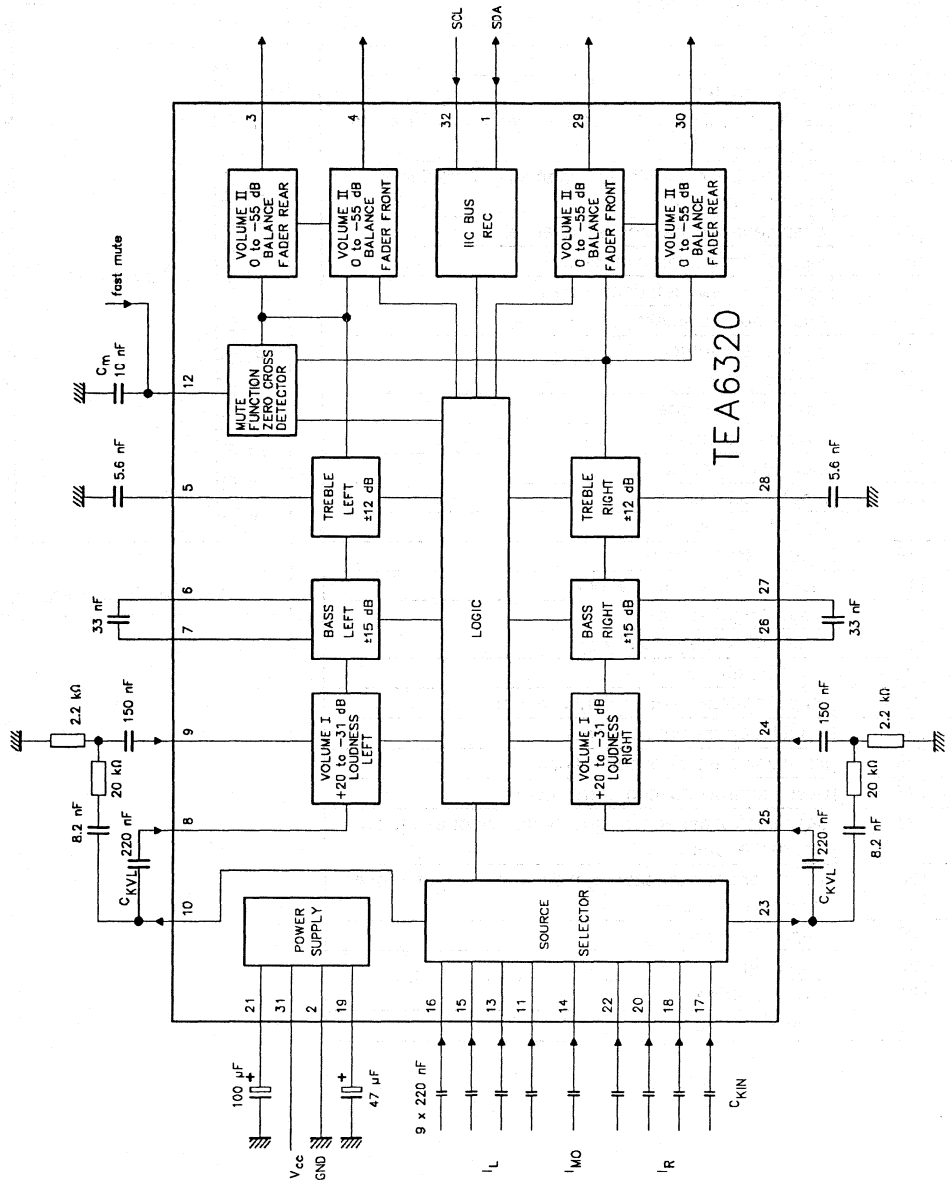


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
SDA	1	serial data input/output
GND	2	ground
OUTLR	3	output left rear
OUTLF	4	output left front
TL	5	treble control capacitor left channel or input from an external equalizer
B2L	6	bass control capacitor left channel or output to an external equalizer
B1L	7	bass control capacitor, left channel
IVL	8	input volume I, left control part
ILL	9	input loudness, left control part
QSL	10	output source selector, left channel
IDL	11	input D left source
MUTE	12	mute control
ICL	13	input C left source
IMO	14	input mono source
IBL	15	input B left source
IAL	16	input A left source
IAR	17	input A right source
IBR	18	input B right source
CAP	19	electronic filtering for supply
ICR	20	input C right source
V_{ref}	21	reference voltage ($0.5V_{CC}$)
IDR	22	input D right source
QSR	23	output source selector right channel
ILR	24	input loudness right channel
IVR	25	input volume I, right control part
B1R	26	bass control capacitor right channel
B2R	27	bass control capacitor right channel or output to an external equalizer
TR	28	treble control capacitor right channel or input from an external equalizer
OUTRF	29	output right front
OUTRR	30	output right rear
V_{CC}	31	supply voltage
SCL	32	serial clock input

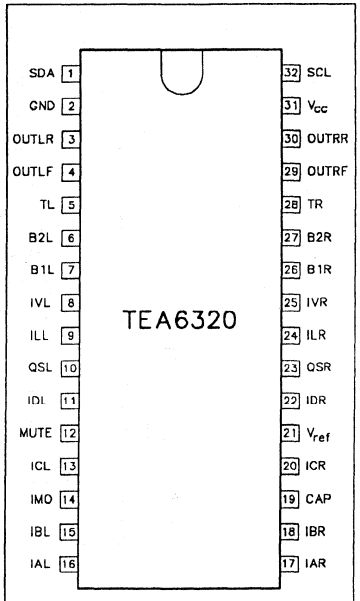


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The source selector selects one of 4 stereo inputs or the mono input. The maximum input signal voltage is $V_{i\,(RMS)}$ = 2 V. The outputs of the source selector and the inputs of the following volume control parts are available at pins 8 and 10 for the left channel and pins 23 and 25 for the right channel. This offers the possibility of interfacing a noise reduction system.

The volume control function is split into two sections: volume I control block and volume II control block.

The control range of volume I is between +20 dB and –31 dB in steps of 1 dB. The volume II control range is between 0 dB and –55 dB in steps of 1 dB. Although the theoretical possible control range is 106 dB (+20 dB to –86 dB), in practice a range of 86 dB (+20 dB to –66 dB) is recommended. The gain/attenuation setting of the volume I control blocks is common for both channels.

The volume I control blocks operate in combination with the loudness control. The filter is linear when the maximum gain for the volume I control (+20 dB) is selected. The filter characteristic increases automatically over a range of 32 dB down to a setting of –12 dB. That means the maximum filter characteristic is obtained at –12 dB setting of volume I. Further reduction of the volume does not further influence the filter characteristic (see Fig.5). The maximum selected filter characteristic is determined by external components. The proposed application gives a maximum boost of 17 dB for bass and 4.5 dB for treble. The loudness may be switched on or off via I²C-bus control (Table 7).

The volume I control block is followed by the bass control block. A single external capacitor of 33 nF for each channel in combination with internal resistors, provides the frequency response of the bass control (see Fig.3). The adjustable range is between –15 dB and +15 dB in steps of 1.5 dB at 40 Hz.

Both, loudness and bass control result in a maximum bass boost of 32 dB for low volume settings.

The treble control block offers a control range between –12 dB and +12 dB in steps of 1.5 dB at 15 kHz. The filter characteristic is determined by a single capacitor of 5.6 nF for each channel in combination with internal resistors (see Fig.4).

The basic step width of bass and treble control is 3 dB. The intermediate steps are obtained by switching 1.5 dB boost and 1.5 dB attenuation steps.

The bass and treble control functions can be switched off via I²C-bus. In this event the internal signal flow is disconnected. The connections B2L / B2R are outputs and TL / TR are inputs for inserting an external equalizer.

The last section of the circuit is the volume II block. The balance and fader functions are performed using the same control blocks. This is realized by 4 independently controllable attenuators, one for each output. The control range of these attenuators is 55 dB in steps of 1 dB with an additional mute step.

The circuit provides 3 mute modes.
1) Zero crossing mode mute via I²C-bus using 2 independent zero crossing detectors (ZCM, see Tables 2 and 9 and Fig.15).
2) Fast mute via mute pin (see Fig.9).
3) Fast mute via I²C-bus either by general mute (GMU see Tables 2 and 9) or volume II block setting (see Table 4).
The mute function is performed immediately if ZCM is cleared (ZCM = 0). If the bit is set (ZCM = 1) the mute is activated after changing the GMU bit. The actual mute switching is delayed until the next zero crossing of the audio frequency signal. As the two audio channels (left and right) are independent, two comparators (window detectors) are required to control independent mute switches.

To avoid a large delay of the muting switching when very low frequencies are processed, the maximum delay time is limited to typically 100 ms by an integrated timing circuit and an external capacitor (C_m = 10 nF, see Fig.9). This timing circuit is triggered by reception of a new data word for the switch function which includes the GMU bit. After a discharge and charge period of an external capacitor the muting switch follows the GMU bit if no zero crossing was detected during that time.

The mute function can also be controlled externally. If the mute pin is switched to ground all outputs are muted immediately (hardware mute). This mute request overwrites all mute controls via the I²C-bus for the time the pin is held low.
The hardware mute position is not stored in the TEA6320.

For the turn on/off behaviour the following explanation is generally valid. To avoid AF output caused by the input signal coming from preceding stages, which produce output during drop of V_{CC}. The mute has to be set, before the V_{CC} will drop. This can be achieved by I²C-bus control or by grounding the mute pin.

For use where there is no mute in the application before turn off, a supply voltage drop of more than 1 x V_{BE} will result in a mute during the voltage drop.

The power supply should include a V_{CC} buffer capacitor, which provides a discharging time constant. If the input signal does not disappear after turn off the input will become audible after a certain time. A 4.7 kΩ resistor discharges the V_{CC} buffer capacitor, because the internal current of the IC does not discharge it completely.

The hardware mute function is favourable for use in RDS (Radio Data System) applications. The zero crossing mute avoids modulation plops. This feature is an advantage for mute during changing presets and/or sources (e. g. traffic announcement during cassette playback).

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	supply voltage		0	10	V
T_{amb}	operating ambient temperature range		–40	+85	°C
T_{stg}	storage temperature range		–65	+150	°C
V_{es}	electrostatic handling	see note 1			
V_n	voltage at pins: pin 1 to 2 and 3 - 32 to 2		0	V_{CC}	V

Note to the limiting values

1. Human body model: C = 100 pF; R = 1.5 kΩ; V ≥ 2 kV
   Charge device model: C = 200 pF; R = 0 Ω; V ≥ 500 V

CHARACTERISTICS

V_{CC} = 8.5 V; R_S = 600 Ω, R_L = 10 kΩ, C_L = 2.5 nF, AC coupled; f = 1 kHz; T_{amb} = +25 °C; gain control G_v = 0 dB; bass linear; treble linear; fader off; balance in mid position; loudness off; unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage		7.5	8.5	9.5	V
I_{CC}	supply current		–	26	33	mA
V_{DC}	internal DC voltage at inputs and outputs		3.83	4.25	4.68	V
V_{ref}	internal reference voltage at pin 21		–	4.25	–	V
G_v	maximum voltage gain	R_S = 0 Ω; R_L = ∞	19	20	21	dB
$V_{o(RMS)}$	output voltage level for					
	P_{max} at the power output stage	THD ≤ 0.1%; see Fig.10	–	2000	–	mV
	start of clipping	THD = 1%	2300	–	–	mV
		R_L = 2 kΩ; C_L = 10 nF; THD = 1%	2000	–	–	mV
$V_{i(RMS)}$	input sensitivity	V_o = 2000 mV; G_v = 20 dB	–	200	–	mV
B	roll-off frequencies	C_{KIN} = 220 nF; C_{KVL} = 220 nF; $Z_i = Z_{i\,min}$				
		low frequency (–1 dB)	60	–	–	Hz
		low frequency (–3 dB)	30	–	–	Hz
		high frequency (–1 dB)	20000	–	–	Hz
		C_{KIN} = 470 nF; C_{KVL} = 100 nF; $Z_i = Z_{i\,typ}$				
		low frequency (–3 dB)	17	–	–	Hz
α_{CS}	channel separation	V_i = 2 V; frequency range 250 Hz to 10 kHz	90	96	–	dB
THD	total harmonic distortion	frequency range 20 Hz to 12.5 kHz				
		V_i = 100 mV; G_v = 20 dB	–	0.1	–	%
		V_i = 1000 mV; G_v = 0 dB	–	0.05	tbn	%
		V_i = 2000 mV; G_v = 0 dB	–	0.1	–	%
		V_i = 2000 mV; G_v = –10 dB	–	0.1	–	%
RR	ripple rejection	$V_{r(RMS)}$ < 200 mV				
		f = 100 Hz	tbn	76	–	dB
		f = 40 Hz to 12.5 kHz	–	66	–	dB
(S+N)/N	signal-plus-noise to noise ratio	unweighted; 20 Hz to 20 kHz RMS; V_o = 2.0 V; see Fig.6	–	105	–	dB
		CCIR 468-2 weighted; quasi peak; V_o = 2.0 V				
		G_v = 0 dB	–	95	–	dB
		G_v = 12 dB	–	88	–	dB
		G_v = 20 dB	–	81	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$P_{no(RMS)}$	noise output power (RMS value) only contribution of TEA6320; power amplifier for 6 W	mute position; note 1	–	–	10	nW
α_B	crosstalk (20 log $V_{bus(p-p)}$ / $V_{o(RMS)}$) between bus inputs and signal outputs	note 2	–	110	–	dB
Source selector						
Z_i	input impedance		25	35	45	kΩ
α_S	input isolation of one selected source to any other input	f = 1 kHz	–	105	–	dB
		f = 12.5 kHz	–	95	–	dB
$V_{i(RMS)}$	maximum input voltage (RMS value)	THD < 0.5%; V_{CC} = 8.5 V	–	2.15	–	V
		THD < 0.5%; V_{CC} = 7.5 V	–	1.8	–	V
$V_{DC\ OFF}$	DC offset voltage at source selector out by selection of any inputs		–	–	10	mV
Z_o	output impedance		–	80	120	Ω
R_L	output load resistance		10	–	–	kΩ
C_L	output load capacity		0	–	2500	pF
G_v	voltage gain, source selector		–	0	–	dB
Control part (source selector disconnected; source resistance 600 Ω)						
Z_i	input impedance volume input		100	150	200	kΩ
	input impedance loudness input		25	33	40	kΩ
Z_o	output impedance		–	80	120	Ω
R_L	output load resistance		2	–	–	kΩ
C_L	output load capacity		0	–	10	nF
$V_{i(RMS)}$	maximum input voltage (RMS value)	THD < 0.5%	–	2.15	–	V
V_{no}	noise output voltage	CCIR 468-2 weighted; quasi peak				
		G_v = 20 dB	–	110	220	μV
		G_v = 0 dB	–	33	50	μV
		G_v = –66 dB	–	13	22	μV
		mute position	–	10	–	μV
G_c	total continuous control range		–	106	–	dB
	recommended control range		–	86	–	dB
G_{step}	step resolution		–	1	–	dB
	step error between any adjoining step		–	–	0.5	dB
ΔG_a	attenuator set error	G_v = +20 to –50 dB	–	–	2	dB
		G_v = –51 to –66 dB	–	–	3	dB
ΔG_t	gain tracking error	G_v = +20 to –50 dB	–	–	2	dB
α_m	mute attenuation	see Fig.8	100	110	–	dB
$V_{DC\ OFF}$	DC step offset	G_v = 0 to –66 dB	–	0.2	10	mV
	between any adjoining step	G_v = 20 to 0 dB	–	tbn	15	mV
	between any step to mute	G_v = 0 to –66 dB	–	–	10	mV

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Volume I control and loudness						
G_c	continuous volume control range		–	51	–	dB
G_v	volume gain		–31	–	20	dB
G_{step}	step resolution		–	1	–	dB
L_B	maximum loudness boost	loudness on; referred to loudness off; boost is determined by external components				
		f = 40 Hz	–	17	–	dB
		f = 10 kHz	–	4.5	–	dB
Bass control						
G_b	bass control, maximum boost	f = 40 Hz	14	15	16	dB
	maximum attenuation	f = 40 Hz	14	15	16	dB
G_{step}	step resolution (toggle switching)	f = 40 Hz	–	1.5	–	dB
	step error between any adjoining step	f = 40 Hz	–	–	0.5	dB
$V_{DC\ OFF}$	DC step offset in any bass position		–	–	20	mV
Treble control						
G_t	treble control, maximum boost	f = 15 kHz	11	12	13	dB
	maximum attenuation	f = 15 kHz	11	12	13	dB
	maximum boost	f > 15 kHz	–	–	15	dB
G_{step}	step resolution (toggle switching)	f = 15 kHz	–	1.5	–	dB
	step error between any adjoining step	f = 15 kHz	–	–	0.5	dB
$V_{DC\ OFF}$	DC step offset in any treble position		–	–	10	mV
Volume II, balance and fader control						
G_f	continuous attenuation fader and volume control range		53.5	55	56.5	dB
G_{step}	step resolution		–	1	2	dB
	attenuation set error		–	–	1.5	dB
Mute function (see Fig.9)						
a) Hardware mute						
V_{SW}	mute switch level (2 x V_{BE})		–	1.45	–	V
mute active:						
$V_{SW\ LOW}$	input level		–	–	1.0	V
I_{CH}	input current	$V_{SW\ LOW}$ = 1 V	–300	–	–	µA
mute passive: level internally defined						
$V_{SW\ HIGH}$	saturation voltage		–	–	V_{CC}	V
t_{DMU}	delay until mute passive		–	–	0.5	ms
b) Zero crossing mute						
I_D	discharge current		0.3	0.6	1.2	µA
I_{CH}	charge current		–300	–150	–	µA
V_{SWDEL}	delay switch level (3 x V_{BE})		–	2.2	–	V
t_{DEV}	delay time	C_m = 10 nF	–	100	–	ms
V_{WIND}	window for audio signal zero crossing detection		–	30	40	mV

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Muting at power supply drop						
$V_{CC-DROP}$	supply drop for mute active		–	$V_{19} - 0.7$	–	V
Power on reset (when reset is active the GMU-bit (general mute) is set and the I^2C-bus receiver is in reset position)						
V_{CC}	increasing supply voltage start of reset		–	–	2.5	V
	end of reset		5.2	6.0	6.8	V
	decreasing supply voltage start of reset		4.2	5.0	5.8	V
Digital part						
I^2C-bus pins; see note 3						
V_{IH}	HIGH level input voltage		3	–	9.5	V
V_{IL}	LOW level input voltage		–0.3	–	+1.5	V
I_{IH}	HIGH level input current		–10	–	+10	μA
I_{IL}	LOW level input current		–10	–	+10	μA
V_{OL}	LOW level output voltage	I_L = 3 mA	–	–	0.4	V

Notes to the characteristics

1. The indicated values for output power assume a 6 W power amplifier at 4 Ω with 20 dB gain and a fixed attenuator of 12 dB in front of it. Signal-to-noise ratios exclude noise contribution of the power amplifier.
2. The transmission contains: total initialization with MAD and Subaddress for volume and 8 data words, see also definition of characteristics, clock frequency = 50 kHz, repetition burst rate = 400 Hz, maximum bus signal amplitude = 5 V_{p-p}
3. The AC characteristics are in accordance with the I^2C-bus specification. Full specification of I^2C-bus will be supplied on request.

I^2C-BUS PROTOCOL

I^2C-bus format

S	SLAVE ADDRESS	A	SUBADDRESS	A	DATA	A	P

Where:

S = start condition
SLAVE ADDRESS (MAD) = 1000 0000
A = acknowledge, generated by the slave
SUBADDRESS (SAD) = see Table 1
DATA = see Table 1
P = STOP condition

If more than 1 byte of DATA is transmitted, then auto-increment of the significant subaddress is performed.

Subaddress

Table 1 Second byte after MAD

FUNCTION	BIT	MSB 7	6	5	4	3	2	1	LSB 0
volume/loudness	V	0	0	0	0	0	0	0	0
fader front right	FFR	0	0	0	0	0	0	0	1
fader front left	FFL	0	0	0	0	0	0	1	0
fader rear right	FRR	0	0	0	0	0	0	1	1
fader rear left	FRL	0	0	0	0	0	1	0	0
bass	BA	0	0	0	0	0	1	0	1
treble	TR	0	0	0	0	0	1	1	0
switch	S	0	0	0	0	0	1	1	1
							significant subaddress		

Definition of third byte

Table 2 Third byte after MAD and SAD

FUNCTION	BIT	MSB 7	6	5	4	3	2	1	LSB 0
volume/loudness	V	ZCM	LOFF	V5	V4	V3	V2	V1	V0
fader front right	FFR	X	X	FFR5	FFR4	FFR3	FFR2	FFR1	FFR0
fader front left	FFL	X	X	FFL5	FFL4	FFL3	FFL2	FFL1	FFL0
fader rear right	FRR	X	X	FRR5	FRR4	FRR3	FRR2	FRR1	FRR0
fader rear left	FRL	X	X	FRL5	FRL4	FRL3	FRL2	FRL1	FRL0
bass	BA	X	X	X	BA4	BA3	BA2	BA1	BA0
treble	TR	X	X	X	TR4	TR3	TR2	TR1	TR0
switch	S	GMU	X	X	X	X	SC2	SC1	SC0

Function of the bits:

V0 to V5	volume control
LOFF	switch loudness on/off
FRR0 to FRR5	fader control front right
FFL0 to FFL5	fader control front left
FRR0 to FRR5	fader control rear right
FRL0 to FRL5	fader control rear left
BA0 to BA4	bass control
TR0 to TR4	treble control
SC0 to SC2	source selector control
GMU	mute control for all outputs (general mute)
ZCM	zero crossing mode
X	don't care bits (logic 1 during testing)

Table 3 Volume setting

G_v (dB)	DATA					
	V5	V4	V3	V2	V1	V0
20	1	1	1	1	1	1
19	1	1	1	1	1	0
18	1	1	1	1	0	1
17	1	1	1	1	0	0
16	1	1	1	0	1	1
15	1	1	1	0	1	0
14	1	1	1	0	0	1
13	1	1	1	0	0	0
12	1	1	0	1	1	1
11	1	1	0	1	1	0
10	1	1	0	1	0	1
9	1	1	0	1	0	0
8	1	1	0	0	1	1
7	1	1	0	0	1	0
6	1	1	0	0	0	1
5	1	1	0	0	0	0
4	1	0	1	1	1	1
3	1	0	1	1	1	0
2	1	0	1	1	0	1
1	1	0	1	1	0	0
0	1	0	1	0	1	1
−1	1	0	1	0	1	0
−2	1	0	1	0	0	1
−3	1	0	1	0	0	0
−4	1	0	0	1	1	1
−5	1	0	0	1	1	0
−6	1	0	0	1	0	1
−7	1	0	0	1	0	0
−8	1	0	0	0	1	1
−9	1	0	0	0	1	0
−10	1	0	0	0	0	1
−11	1	0	0	0	0	0

Loudness on: the increment of the loudness characteristic is linear at every volume step in the range from +20 dB to −11 dB.

Table 3 Volume setting (continued)

G_v (dB)	DATA					
	V5	V4	V3	V2	V1	V0
−12	0	1	1	1	1	1
−13	0	1	1	1	1	0
−14	0	1	1	1	0	1
−15	0	1	1	1	0	0
−16	0	1	1	0	1	1
−17	0	1	1	0	1	0
−18	0	1	1	0	0	1
−19	0	1	1	0	0	0
−20	0	1	0	1	1	1
−21	0	1	0	1	1	0
−22	0	1	0	1	0	1
−23	0	1	0	1	0	0
−24	0	1	0	0	1	1
−25	0	1	0	0	1	0
−26	0	1	0	0	0	1
−27	0	1	0	0	0	0
−28	0	0	1	1	1	1
−29	0	0	1	1	1	0
−30	0	0	1	1	0	1
−31	0	0	1	1	0	0

Loudness characteristic is constant in a range from −11 dB to −31 dB.

Table 3 Volume setting (continued)

G_v (dB)	DATA					
	V5	V4	V3	V2	V1	V0
−28	0	0	1	0	1	1
. . .						
−31	0	0	0	0	0	0

Repetition of steps in a range from −28 dB to −31 dB.

Table 4 Fader setting

G_v (dB)	DATA					
	FRR5 FRL5 FFL5 FFR5	FRR4 FRL4 FFL4 FFR4	FRR3 FRL3 FFL3 FFR3	FRR2 FRL2 FFL2 FFR2	FRR1 FRL1 FFL1 FFR1	FRR0 FRL0 FFL0 FFR0
0	1	1	1	1	1	1
–1	1	1	1	1	1	0
–2	1	1	1	1	0	1
–3	1	1	1	1	0	0
–4	1	1	1	0	1	1
–5	1	1	1	0	1	0
–6	1	1	1	0	0	1
–7	1	1	1	0	0	0
–8	1	1	0	1	1	1
–9	1	1	0	1	1	0
–10	1	1	0	1	0	1
–11	1	1	0	1	0	0
–12	1	1	0	0	1	1
–13	1	1	0	0	1	0
–14	1	1	0	0	0	1
–15	1	1	0	0	0	0
–16	1	0	1	1	1	1
–17	1	0	1	1	1	0
–18	1	0	1	1	0	1
–19	1	0	1	1	0	0
–20	1	0	1	0	1	1
–21	1	0	1	0	1	0
–22	1	0	1	0	0	1
–23	1	0	1	0	0	0
–24	1	0	0	1	1	1
–25	1	0	0	1	1	0
–26	1	0	0	1	0	1
–27	1	0	0	1	0	0
–28	1	0	0	0	1	1
–29	1	0	0	0	1	0
–30	1	0	0	0	0	1
–31	1	0	0	0	0	0
–32	0	1	1	1	1	1
–33	0	1	1	1	1	0
–34	0	1	1	1	0	1
–35	0	1	1	1	0	0
–36	0	1	1	0	1	1
–37	0	1	1	0	1	0
–38	0	1	1	0	0	1

G_v (dB)	DATA					
	FRR5 FRL5 FFL5 FFR5	FRR4 FRL4 FFL4 FFR4	FRR3 FRL3 FFL3 FFR3	FRR2 FRL2 FFL2 FFR2	FRR1 FRL1 FFL1 FFR1	FRR0 FRL0 FFL0 FFR0
–39	0	1	1	0	0	0
–40	0	1	0	1	1	1
–41	0	1	0	1	1	0
–42	0	1	0	1	0	1
–43	0	1	0	1	0	0
–44	0	1	0	0	1	0
–45	0	1	0	0	1	0
–46	0	1	0	0	0	1
–47	0	1	0	0	0	0
–48	0	0	1	1	1	1
–49	0	0	1	1	1	0
–50	0	0	1	1	0	1
–51	0	0	1	1	0	0
–52	0	0	1	0	1	1
–53	0	0	1	0	1	0
–54	0	0	1	0	0	1
–55	0	0	1	0	0	0
mute	0	0	0	1	1	1
mute	0	0	0	1	1	0
mute	0	0	0	1	0	1
mute	0	0	0	1	0	0
mute	0	0	0	0	1	1
mute	0	0	0	0	1	0
mute	0	0	0	0	0	1
mute	0	0	0	0	0	0

For a particular range the data is always the same, only the subaddress changes.

Table 5 Bass setting

G_v (dB)	DATA				
	BA4	BA3	BA2	BA1	BA0
15	1	1	1	1	1
13.5	1	1	1	1	0
15	1	1	1	0	1
13.5	1	1	1	0	0
15	1	1	0	1	1
13.5	1	1	0	1	0
12	1	1	0	0	1
10.5	1	1	0	0	0
9	1	0	1	1	1
7.5	1	0	1	1	0
6	1	0	1	0	1
4.5	1	0	1	0	0
3	1	0	0	1	1
1.5	1	0	0	1	0
0 *	1	0	0	0	1
0 **	1	0	0	0	0
–1.5	0	1	1	1	1
–3	0	1	1	1	0
–4.5	0	1	1	0	1
–6	0	1	1	0	0
–7.5	0	1	0	1	1
–9	0	1	0	1	0
–10.5	0	1	0	0	1
–12	0	1	0	0	0
–13.5	0	0	1	1	1
–15	0	0	1	1	0
–13.5	0	0	1	0	1
–15	0	0	1	0	0
***	0	0	0	1	1
***	0	0	0	1	0
***	0	0	0	0	1
*** ****	0	0	0	0	0

* Recommended data word for step 0 dB.

** Result of 1.5 dB boost and 1.5 dB attenuation.

*** The last four bass control data words mute the bass response.

**** The last bass control and treble control data words (00000) enable the external equalizer connection.

Table 6 Treble setting

G_v (dB)	DATA				
	TR4	TR3	TR2	TR1	TR0
12	1	1	1	1	1
10.5	1	1	1	1	0
12	1	1	1	0	1
10.5	1	1	1	0	0
12	1	1	0	1	1
10.5	1	1	0	1	0
12	1	1	0	0	1
10.5	1	1	0	0	0
9	1	0	1	1	1
7.5	1	0	1	1	0
6	1	0	1	0	1
4.5	1	0	1	0	0
3	1	0	0	1	1
1.5	1	0	0	1	0
0 *	1	0	0	0	1
0 **	1	0	0	0	0
−1.5	0	1	1	1	1
−3	0	1	1	1	0
−4.5	0	1	1	0	1
−6	0	1	1	0	0
−7.5	0	1	0	1	1
−9	0	1	0	1	0
−10.5	0	1	0	0	1
−12	0	1	0	0	0
***	0	0	1	1	1
***	0	0	1	1	0
***	0	0	1	0	1
***	0	0	1	0	0
***	0	0	0	1	1
***	0	0	0	1	0
***	0	0	0	0	1
*** ****	0	0	0	0	0

* Recommended data word for step 0 dB.
** Result of 1.5 dB boost and 1.5 dB attenuation.
*** The last eight treble control data words select treble cut.
**** The last treble control and bass control data words (00000) enable the external equalizer connection.

Table 7 Loudness setting

CHARACTERISTIC	DATA L OFF
with loudness	0
linear	1

Table 8 Selected inputs

INPUTS	DATA		
	SC2	SC1	SC0
IAL, IAR stereo	1	1	1
IBL, IBR stereo	1	1	0
ICC, ICR stereo	1	0	1
IDL, IDR stereo	1	0	0
IMO, mono	0	X	X

Table 9 Mute mode

GMU	ZCM	mode
0	0	direct mute off
0	1	mute off delayed until the next zero crossing
1	0	direct mute
1	1	mute delayed until the next zero crossing

X = don't care bits (logic 1 during testing)

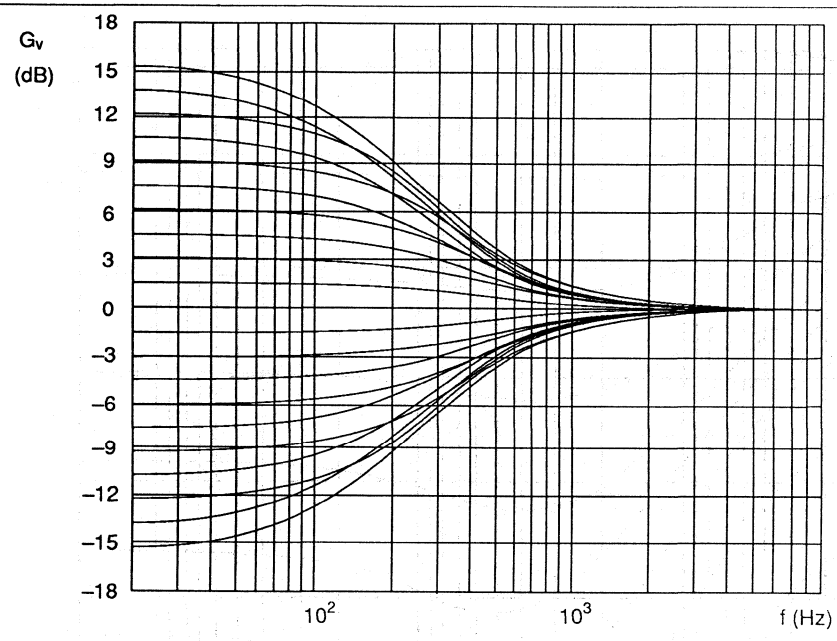


Fig.3 Bass control.

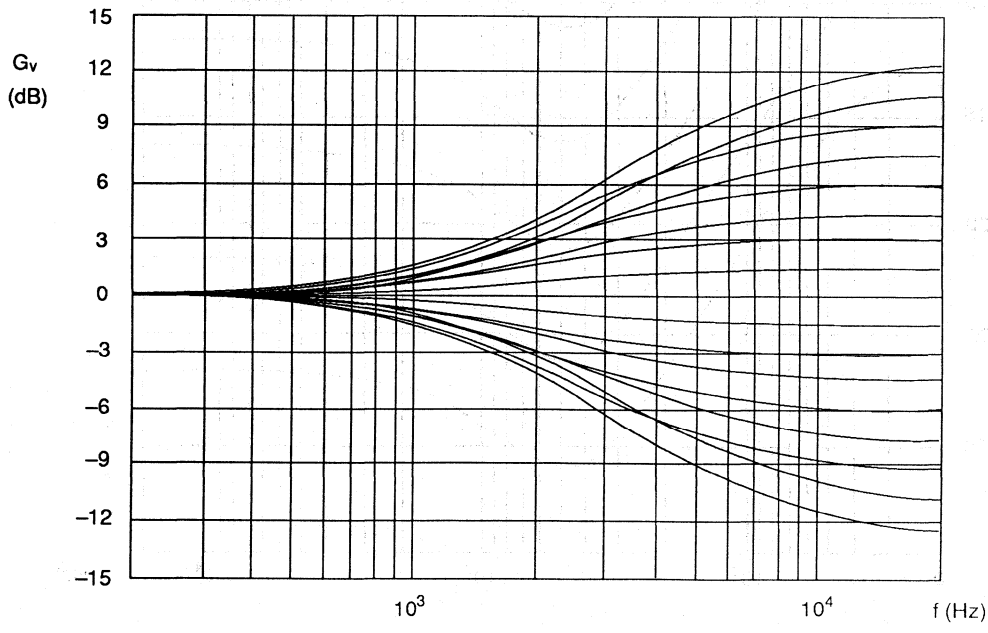


Fig.4 Treble control.

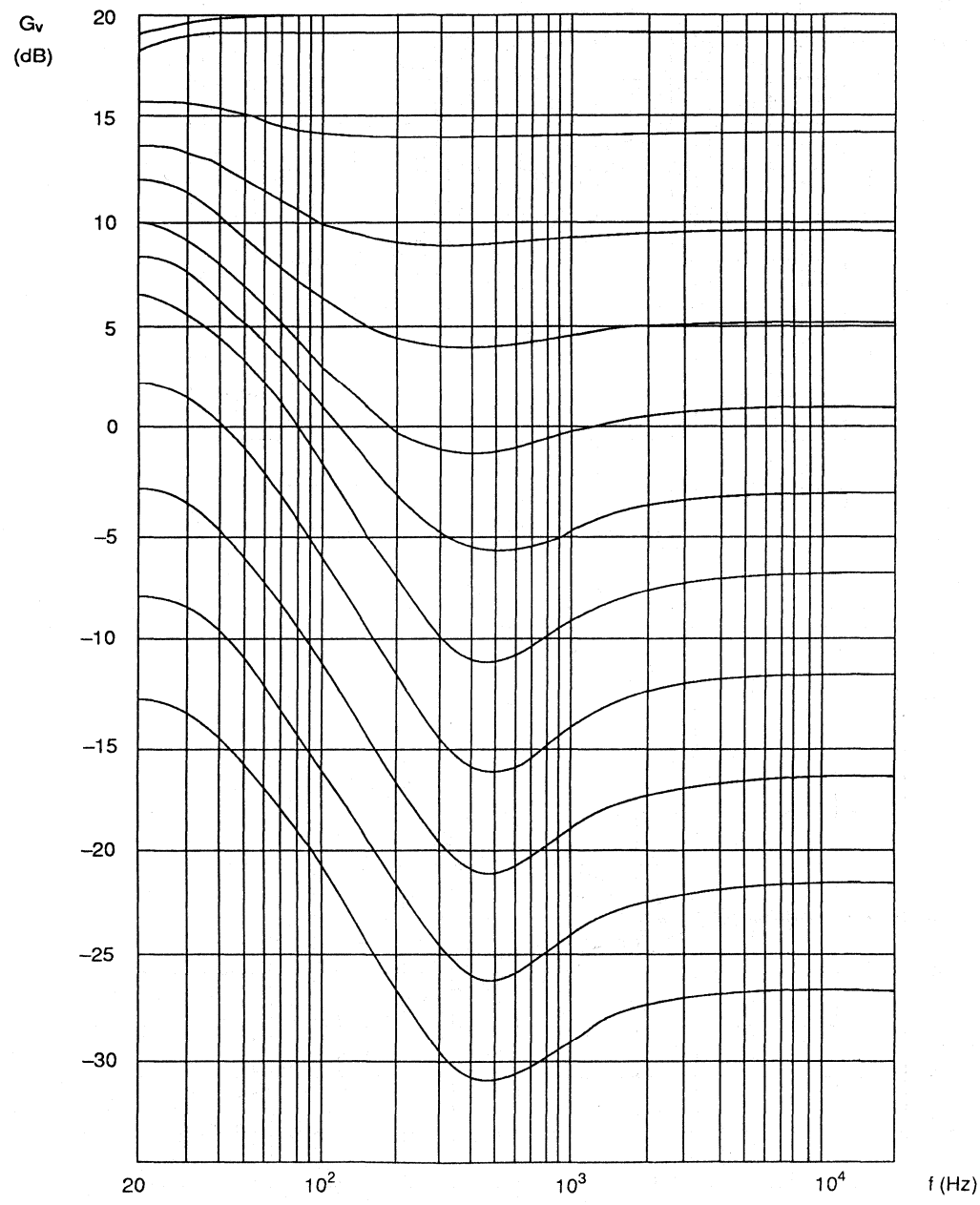
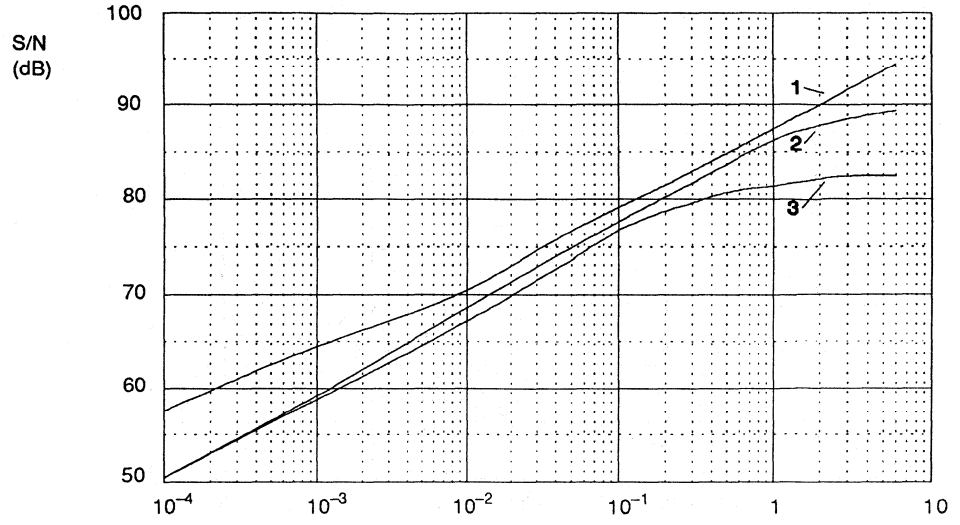
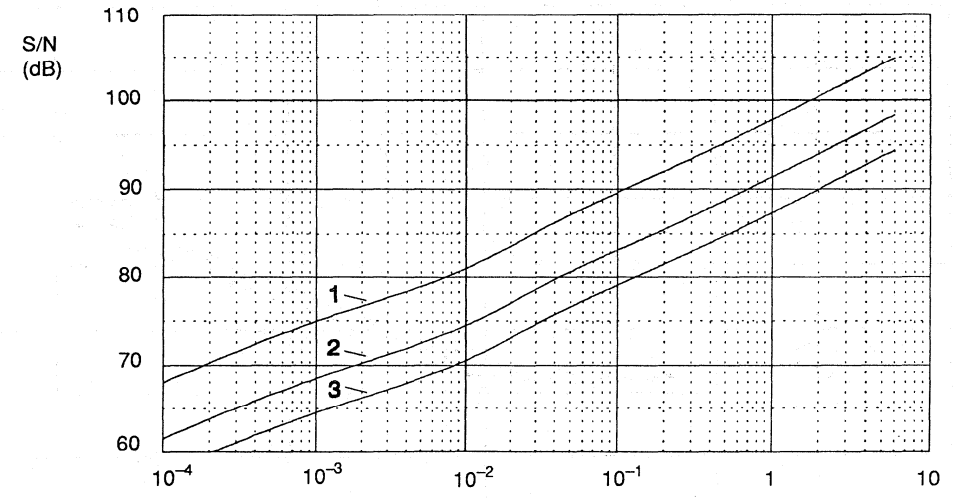


Fig.5 Volume control with loudness (including low roll-off frequency).



1: V_i = 2.0 V
2: V_i = 0.5 V
3: V_i = 0.2 V

Fig.6(a) Signal-to-noise ratio; noise weighted: CCIR468-2, quasi peak.



1: unweighted RMS
2: CCIR468-2 RMS
3: CCIR468-2 quasi peak

Fig.6(b) Signal-to-noise ratio; V_i = 2 V; P_{max} = 6 W.

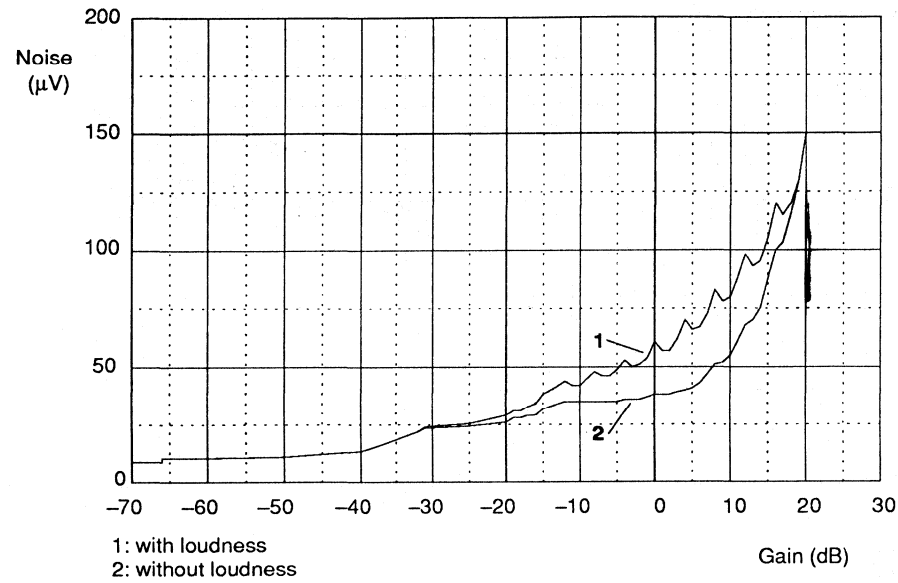


Fig.7 Noise output voltage; CCIR468-2, quasi peak.

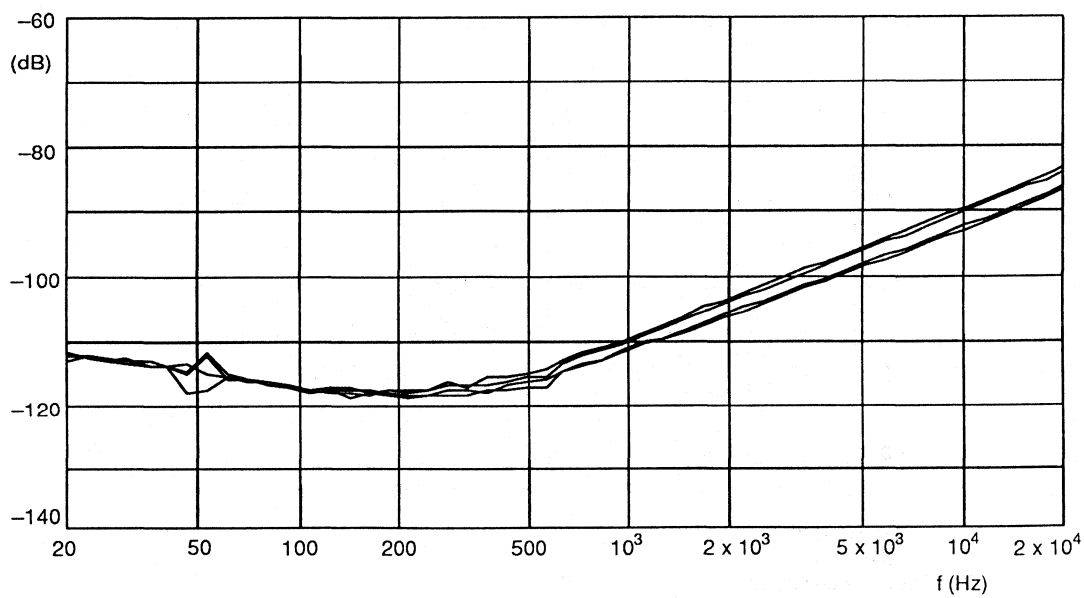
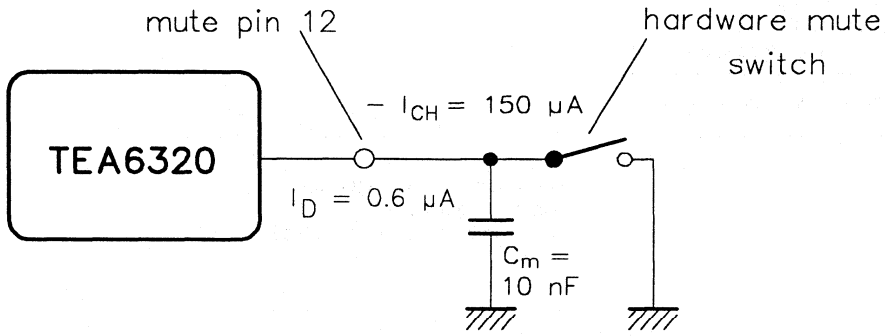
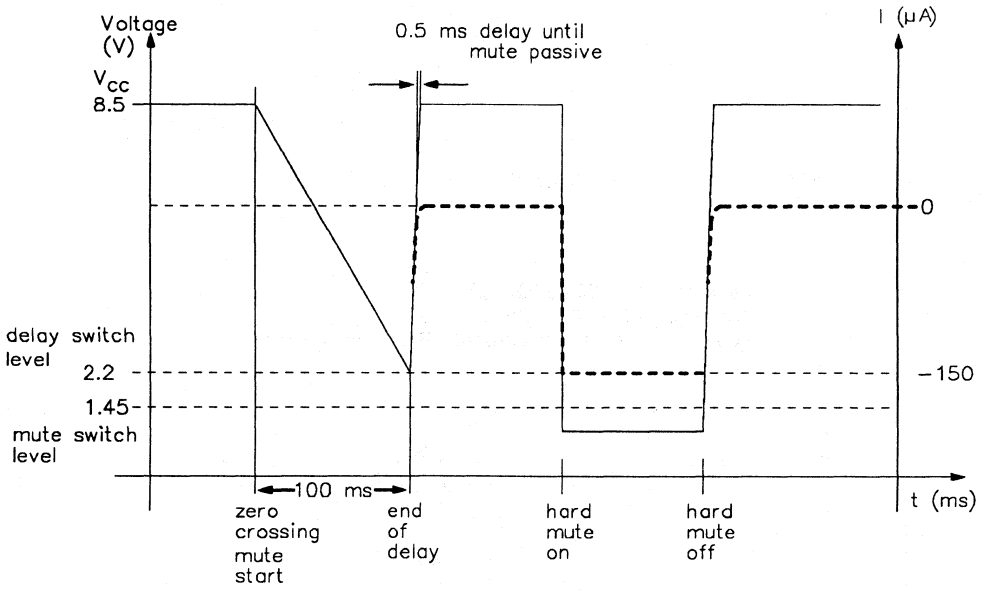


Fig.8 Muting.



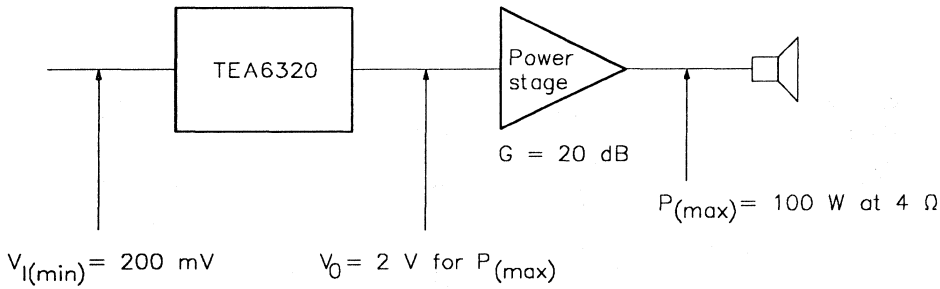


delay switch level voltage is typically 2.2 V and is referenced to 3 x V_{BE}

Fig.9 Mute function diagram.

If the 20 dB gain is not required for the maximum volume position, it will be an advantage to use the maximum boost gain and then increased attenuation in the last section, Volume II.
Therefore the loudness will be at the correct place and a lower noise and offset voltage will be achieved.

gain volume I = 20 dB ($G_{v\,max}$)
gain volume II = 0 dB
fader and balance range = 55 dB



gain volume I = 20 dB ($G_{v\,max}$)
gain volume II = −6 dB global setting
fader and balance range now 49 dB, previously 55 dB

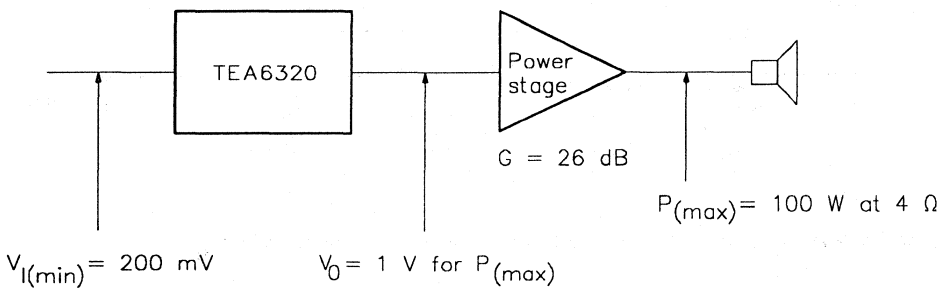


Fig.10 Level diagram.

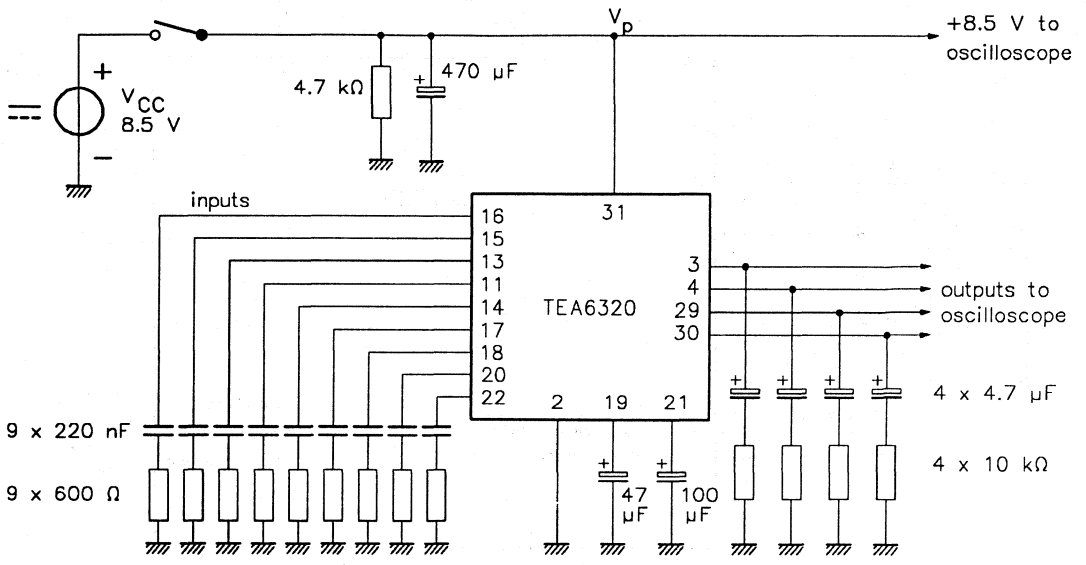


Fig.11 Turn-on/off power supply circuit diagram.

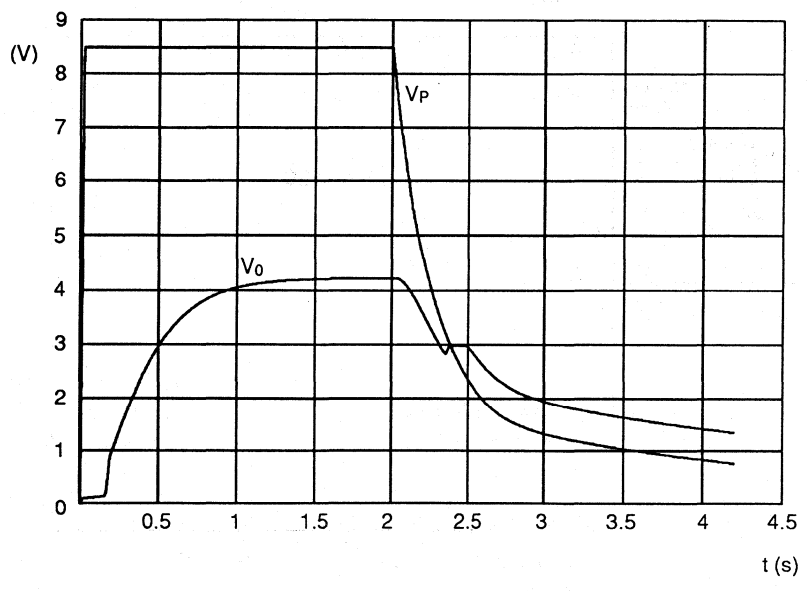


Fig.12 Turn-on/off behaviour.

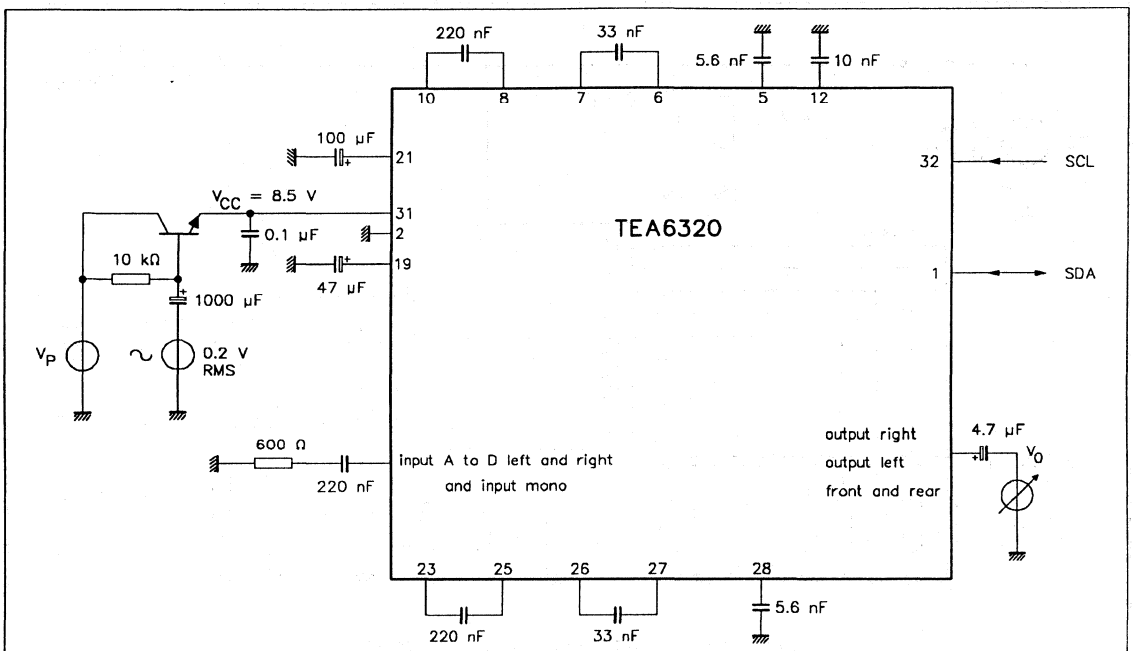


Fig.13 Test circuit for power supply ripple rejection (RR).

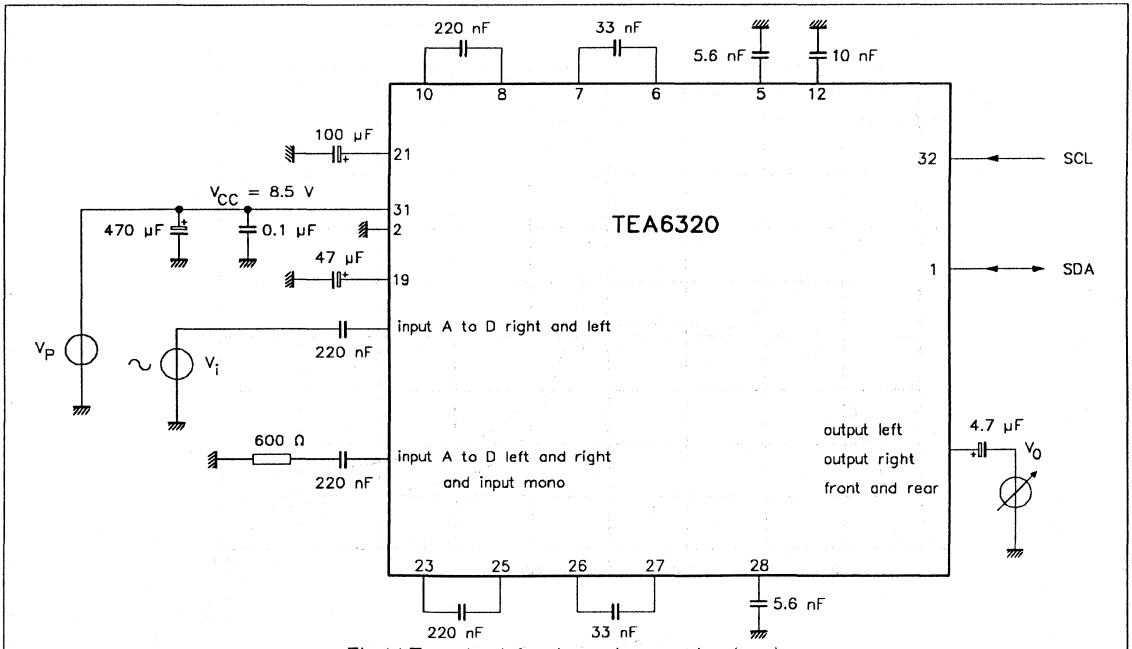


Fig.14 Test circuit for channel separation (α_{CS}).

Selection of input signals by using the zero crossing mute mode

A selection from input A (IAL) to input B (IBL) left sources produces a modulation click depending on the difference of the signal values at the time of switching.
At t_1 the maximum possible difference between signals is 7 $V_{(p-p)}$ and gives a large click. Using the zero cross detector no modulation click is audible.

For example: The selection is enabled at t_1, the microcontroller sets the zero cross bit (ZCM = 1) and then the mute bit (GMU = 1) via the I^2C-bus. The output signal follows the input A signal, until the next zero crossing occurs and then activates mute.
After a fixed delay time at t_2, the microcontroller sends the bits for input switching and mute inactive.

The output signal remains muted until the next signal zero crossing of input B (IBL) occurs, and then follows that signal.
The delay time $t_2 - t_1$ is e. g. 40 ms. Therefore is the capacity CM = 3.3 nF. The zero cross function is working at the lowest frequency of 40 Hz determined by the CM capacitor.

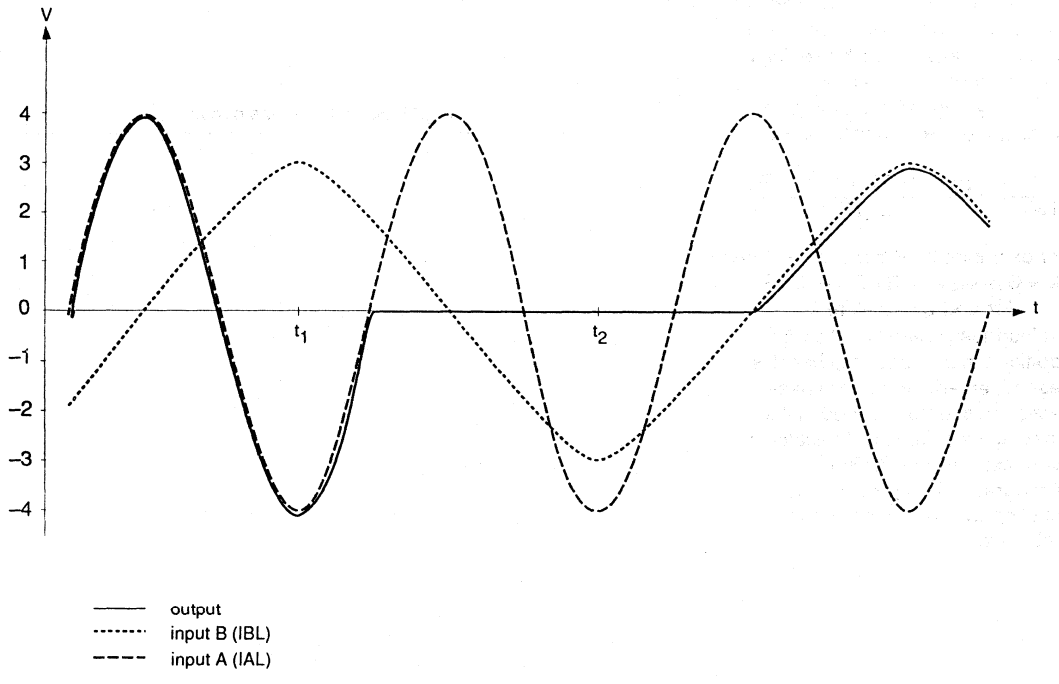


Fig.15 Zero cross function; only one channel shown.

Loudness filter calculation example

Fig.16 shows the basic loudness circuit with an external low pass filter application. R_1 allows an attenuation range of 21 dB while the boost is determined by the gain stage V_2. Both result in a loudness control range of +20 dB to −12 dB. Defining $f_{reference}$ as the frequency where the level does not change while switching loudness on/off. The external resistor R_3 for $f_{reference} \rightarrow \infty$ can be calculated as

$$R_3 = R_1 \frac{10^{G_v/20}}{1 - 10^{G_v/20}}$$

with $G_v = -21$ dB and $R_1 = 33\ k\Omega$ $R_3 = 3.2\ k\Omega$ is generated.

For the low pass filter characteristic the value of the external capacitor C_1 can be determined by setting a specific boost for a defined frequency and referring the gain to G_v at $f_{reference}$ as indicated above.

$$\left|\frac{1}{j\omega C_1}\right| = \frac{(R_1 + R_3) \times 10^{G_v/20} - R_3}{1 - 10^{G_v/20}}$$

For example: 3 dB boost at f = 1 kHz
$G_v = G_{v\,reference} + 3\ dB = -18\ dB$;
f = 1 kHz and $C_1 = 100$ nF

If a loudness characteristic with additional high frequency boost is desired, an additional high pass section has to be included in the external filter circuit as indicated in the block diagram. A filter configuration that provides AC coupling avoids offset voltage problems.

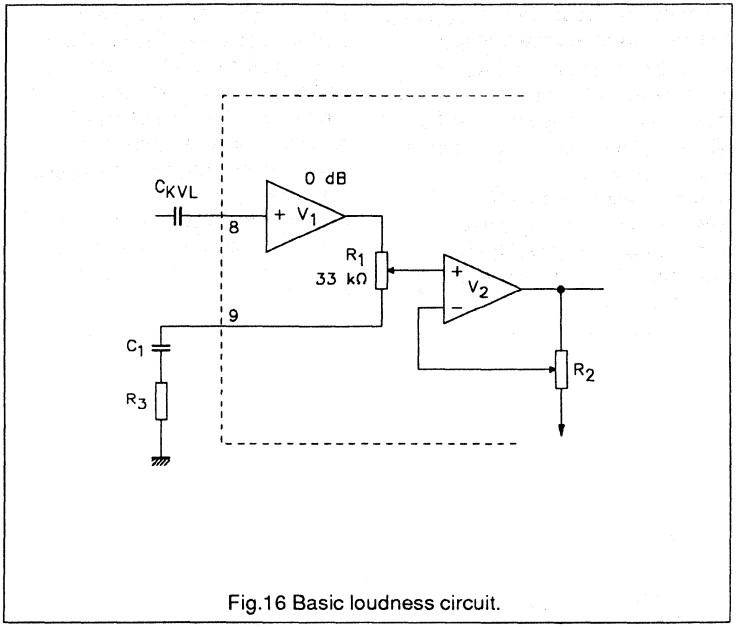
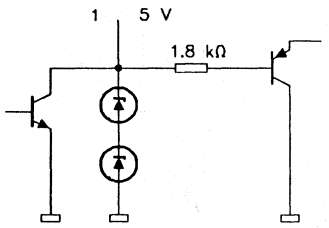
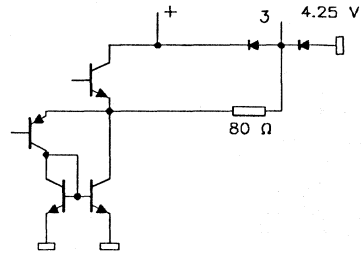


Fig.16 Basic loudness circuit.

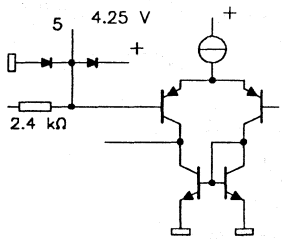
INTERNAL PIN CONFIGURATIONS



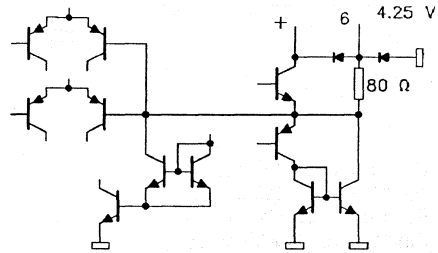
Pin 1: SDA (I^2C-bus data)



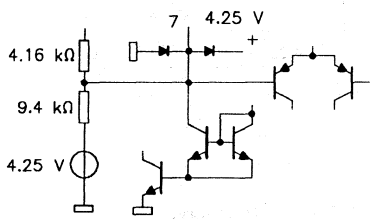
Pin 3: Output left, rear
Pin 4: Output left, front
Pin 29: Output right, front
Pin 30: Output right, rear



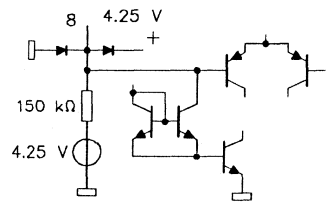
Pin 5: Treble control capacitor, left channel
Pin 28: Treble control capacitor, right channel



Pin 6: Bass control capacitor output, left channel
Pin 27: Bass control capacitor output, right channel



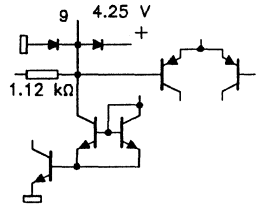
Pin 7: Bass control capacitor input, left channel
Pin 27: Bass control capacitor input, right channel



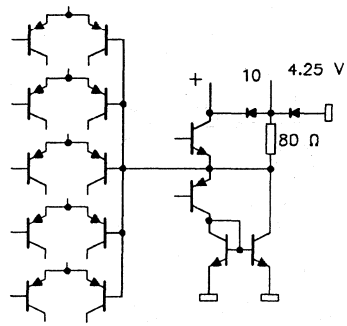
Pin 8: Input volume 1 left, control part
Pin 25: Input volume 1 right, control part

Pin equivalent circuits
V_{CC} = 8.5 V
(All values shown are typical DC values)

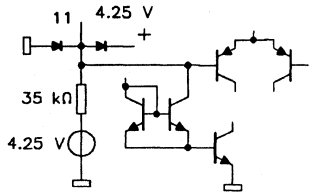
Fig.17(a) Internal circuits (continued in Fig.17(b)).



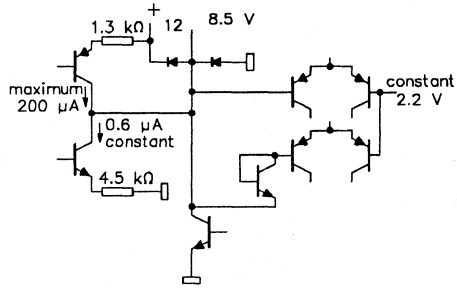
Pin 9: Input loudness left, control part
Pin 24: Input loudness right, control part



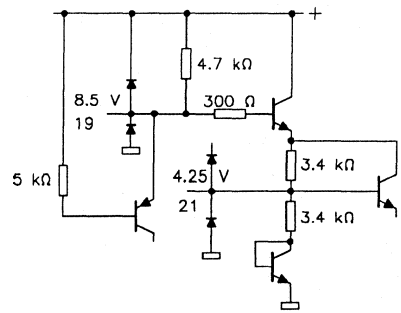
Pin 10: Output source selector, left channel
Pin 23: Output source selector, right channel



Pin 11: Input D left source
Pin 13: Input C left source
Pin 14: Input mono source
Pin 15: Input B left source
Pin 16: Input A left source
Pin 17: Input A right source
Pin 18: Input B right source
Pin 20: Input C right source
Pin 22: Input D right source



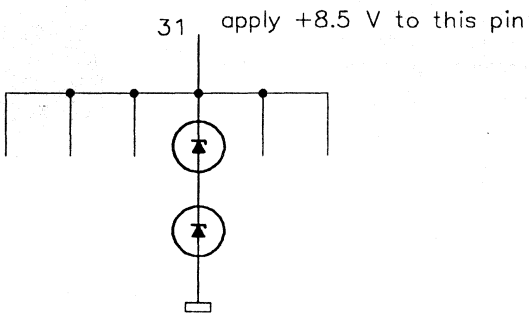
Pin 12: Mute control



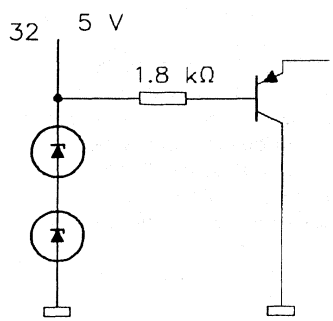
Pin 19: Filtering for supply
Pin 21: Reference voltage

Pin equivalent circuits
V_{CC} = 8.5 V
(All values shown are typical DC values)

Fig.17(b) Internal circuits (continued from Fig.17(a)).



Pin 31: Supply voltage



Pin 32: SCL (I^2C-bus clock)

Pin equivalent circuits
V_{CC} = 8.5 V
(All values shown are typical DC values)

Fig.17(c) Internal circuits (continued from Fig.17(b)).

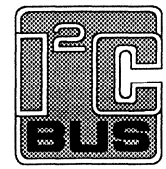
Sound fader control circuit TEA6321

FEATURES

- Source selector for four stereo and one mono inputs
- Interface for noise reduction circuits
- Interface for external equalizer
- Volume, balance and fader control
- Special loudness characteristic automatically controlled in combination with volume setting
- Bass control with equalizer filters
- Treble control
- Mute control at audio signal zero crossing
- Fast mute control via I²C-bus
- Fast mute control via pin
- I²C-bus control for all functions
- Power supply with internal power-on reset.

GENERAL DESCRIPTION

The sound fader control circuit TEA6321 is an I²C-bus controlled stereo preamplifier for car radio hi-fi sound applications.



QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}	positive supply voltage		7.5	8.5	9.5	V
I_{CC}	supply current	V_{CC} = 8.5 V	–	26	–	mA
$V_{o(RMS)}$	maximum output voltage level	V_{CC} = 8.5 V; THD ≤ 0.1%	–	2000	–	mV
G_v	volume gain		–86	–	+20	dB
G_{step}	step resolution (volume)		–	1	–	dB
G_b	bass control		–18	–	+18	dB
G_t	treble control		–12	–	+12	dB
G_{step}	step resolution (treble)		–	1.5	–	dB
(S+N)/N	signal-plus-noise to noise ratio	V_o = 2.0 V; G_v = 0 dB; unweighted	–	105	–	dB
RR_{100}	ripple rejection	$V_{r(RMS)}$ < 200 mV; f = 100 Hz; G_v = 0 dB	–	75	–	dB
α_{cs}	channel separation	250 Hz ≤ f ≤ 10 kHz; G_v = 0 dB	90	96	–	dB

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TEA6321T	32	SO	plastic	SOT287AH

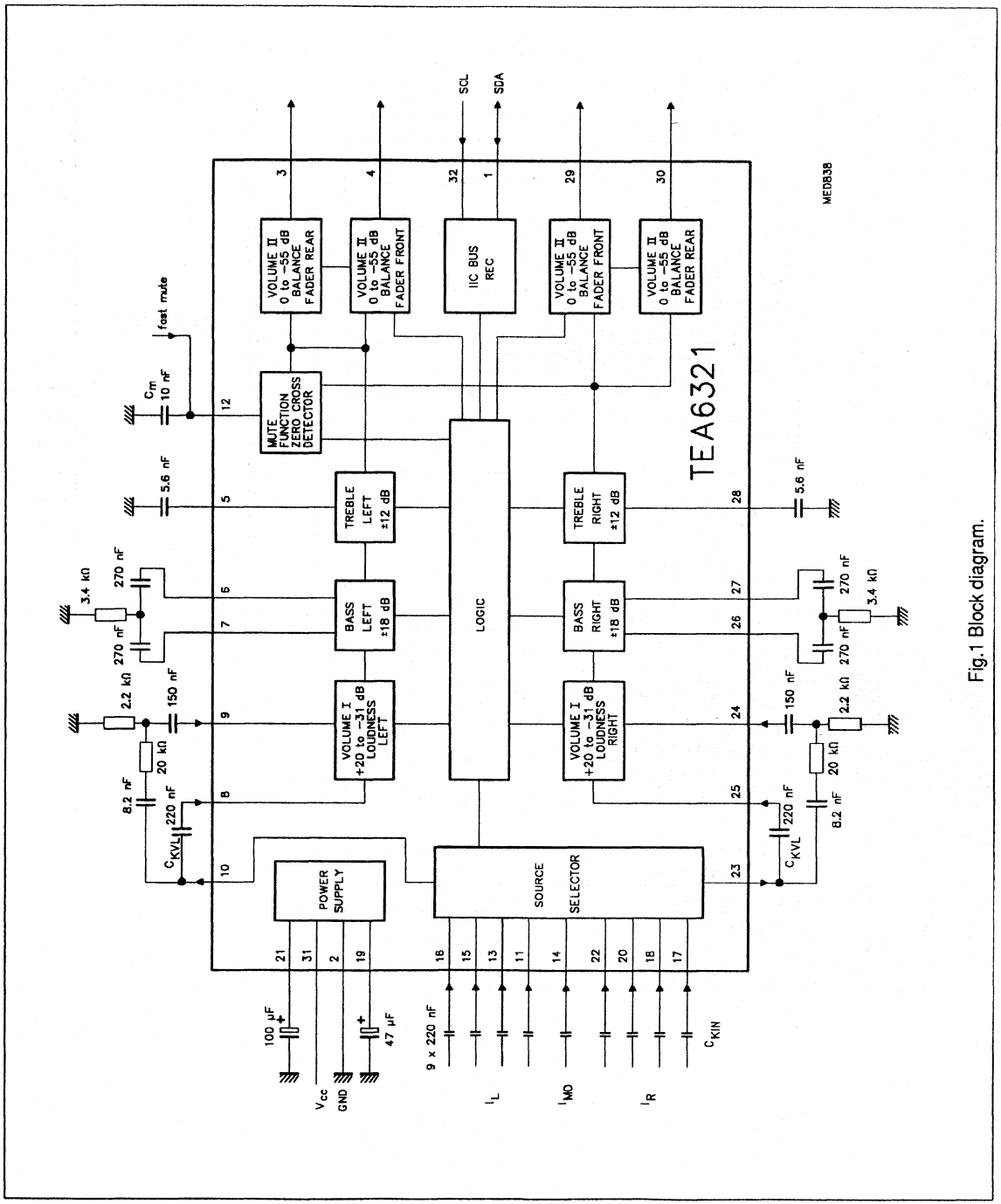


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
SDA	1	serial data input/output
GND	2	ground
OUTLR	3	output left rear
OUTLF	4	output left front
TL	5	treble control capacitor left channel or input from an external equalizer
B2L	6	bass control left channel or output to an external equalizer
B1L	7	bass control, left channel
IVL	8	input volume I, left control part
ILL	9	input loudness, left control part
QSL	10	output source selector, left channel
IDL	11	input D left source
MUTE	12	mute control
ICL	13	input C left source
IMO	14	input mono source
IBL	15	input B left source
IAL	16	input A left source
IAR	17	input A right source
IBR	18	input B right source
CAP	19	electronic filtering for supply
ICR	20	input C right source
V_{ref}	21	reference voltage (0.5V_{CC})
IDR	22	input D right source
QSR	23	output source selector right channel
ILR	24	input loudness right channel
IVR	25	input volume I, right control part
B1R	26	bass control right channel
B2R	27	bass control right channel or output to an external equalizer
TR	28	treble control capacitor right channel or input from an external equalizer
OUTRF	29	output right front
OUTRR	30	output right rear
V_{CC}	31	supply voltage
SCL	32	serial clock input

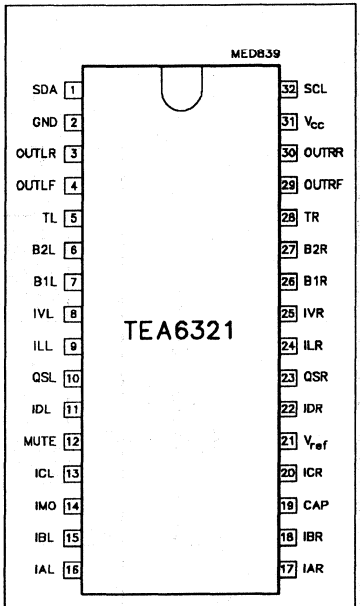


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The source selector selects one of 4 stereo inputs or the mono input. The maximum input signal voltage is $V_{i\,(RMS)}$ = 2 V. The outputs of the source selector and the inputs of the following volume control parts are available at pins 8 and 10 for the left channel and pins 23 and 25 for the right channel. This offers the possibility of interfacing a noise reduction system.

The volume control function is split into two sections: volume I control block and volume II control block.

The control range of volume I is between +20 dB and –31 dB in steps of 1 dB. The volume II control range is between 0 dB and –55 dB in steps of 1 dB. Although the theoretical possible control range is 106 dB (+20 dB to –86 dB), in practice a range of 86 dB (+20 dB to –66 dB) is recommended. The gain/attenuation setting of the volume I control blocks is common for both channels.

The volume I control blocks operate in combination with the loudness control. The filter is linear when the maximum gain for the volume I control (+20 dB) is selected. The filter characteristic increases automatically over a range of 32 dB down to a setting of –12 dB. That means the maximum filter characteristic is obtained at –12 dB setting of volume I. Further reduction of the volume does not further influence the filter characteristic (see Fig.5). The maximum selected filter characteristic is determined by external components. The proposed application gives a maximum boost of 17 dB for bass and 4.5 dB for treble. The loudness may be switched on or off via I²C-bus control (Table 7).

The volume I control block is followed by the bass control block. An external filter for each channel in combination with internal resistors, provides the frequency response of the bass control (see Fig.3). The adjustable range is between –18 dB and +18 dB in steps of 1.8 dB at 46 Hz.

Both, loudness and bass control result in a maximum bass boost of 35 dB for low volume settings.

The treble control block offers a control range between –12 dB and +12 dB in steps of 1.5 dB at 15 kHz. The filter characteristic is determined by a single capacitor of 5.6 nF for each channel in combination with internal resistors (see Fig.4).

The basic step width of treble control is 3 dB. The intermediate steps are obtained by switching 1.5 dB boost and 1.5 dB attenuation steps.

The bass and treble control functions can be switched off via I²C-bus. In this event the internal signal flow is disconnected. The connections B2L / B2R are outputs and TL / TR are inputs for inserting an external equalizer.

The last section of the circuit is the volume II block. The balance and fader functions are performed using the same control blocks. This is realized by 4 independently controllable attenuators, one for each output. The control range of these attenuators is 55 dB in steps of 1 dB with an additional mute step.

The circuit provides 3 mute modes.
1) Zero crossing mode mute via I²C-bus using 2 independent zero crossing detectors (ZCM, see Tables 2 and 9 and Fig.16).
2) Fast mute via mute pin (see Fig.10).
3) Fast mute via I²C-bus either by general mute (GMU see Tables 2 and 9) or volume II block setting (see Table 4).
The mute function is performed immediately if ZCM is cleared (ZCM = 0). If the bit is set (ZCM = 1) the mute is activated after changing the GMU bit. The actual mute switching is delayed until the next zero crossing of the audio frequency signal. As the two audio channels (left and right) are independent, two comparators (window detectors) are required to control independent mute switches.

To avoid a large delay of the muting switching when very low frequencies are processed, the maximum delay time is limited to typically 100 ms by an integrated timing circuit and an external capacitor (C_m = 10 nF, see Fig.10). This timing circuit is triggered by reception of a new data word for the switch function which includes the GMU bit. After a discharge and charge period of an external capacitor the muting switch follows the GMU bit if no zero crossing was detected during that time.

The mute function can also be controlled externally. If the mute pin is switched to ground all outputs are muted immediately (hardware mute). This mute request overwrites all mute controls via the I²C-bus for the time the pin is held low.
The hardware mute position is not stored in the TEA6321.

For the turn on/off behaviour the following explanation is generally valid. To avoid AF output caused by the input signal coming from preceding stages, which produce output during drop of V_{CC}. The mute has to be set, before the V_{CC} will drop. This can be achieved by I²C-bus control or by grounding the mute pin.

For use where there is no mute in the application before turn off, a supply voltage drop of more than 1 x V_{BE} will result in a mute during the voltage drop.

The power supply should include a V_{CC} buffer capacitor, which provides a discharging time constant. If the input signal does not disappear after turn off the input will become audible after a certain time. A 4.7 kΩ resistor discharges the V_{CC} buffer capacitor, because the internal current of the IC does not discharge it completely.

The hardware mute function is favourable for use in RDS (Radio Data System) applications. The zero crossing mute avoids modulation plops. This feature is an advantage for mute during changing presets and/or sources (e. g. traffic announcement during cassette playback).

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	supply voltage		0	10	V
T_{amb}	operating ambient temperature		–40	+85	°C
T_{stg}	storage temperature		–65	+150	°C
V_{es}	electrostatic handling	note 1			
V_n	voltage at pins: pin 1 to 2 and 3 - 32 to 2		0	V_{CC}	V

Note to the limiting values

1. Human body model: C = 100 pF; R = 1.5 kΩ; V ≥ 2 kV
   Charge device model: C = 200 pF; R = 0 Ω; V ≥ 500 V.

CHARACTERISTICS

V_{CC} = 8.5 V; R_S = 600 Ω, R_L = 10 kΩ, C_L = 2.5 nF, AC coupled; f = 1 kHz; T_{amb} = +25 °C; gain control G_v = 0 dB; bass linear; treble linear; fader off; balance in mid position; loudness off; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage		7.5	8.5	9.5	V
I_{CC}	supply current		–	26	33	mA
V_{DC}	internal DC voltage at inputs and outputs		3.83	4.25	4.68	V
V_{ref}	internal reference voltage at pin 21		–	4.25	–	V
G_v	maximum voltage gain	R_S = 0 Ω; R_L = ∞	19	20	21	dB
$V_{o(RMS)}$	output voltage level for P_{max} at the power output stage start of clipping	THD ≤ 0.1%; see Fig.11	–	2000	–	mV
		THD = 1%	2300	–	–	mV
		R_L = 2 kΩ; C_L = 10 nF; THD = 1%	2000	–	–	mV
$V_{i(RMS)}$	input sensitivity	V_o = 2000 mV; G_v = 20 dB	–	200	–	mV
B	roll-off frequencies	C_{KIN} = 220 nF; C_{KVL} = 220 nF; $Z_i = Z_{i\,min}$				
		low frequency (–1 dB)	60	–	–	Hz
		low frequency (–3 dB)	30	–	–	Hz
		high frequency (–1 dB)	20000	–	–	Hz
		C_{KIN} = 470 nF; C_{KVL} = 100 nF; $Z_i = Z_{i\,typ}$				
		low frequency (–3 dB)	17	–	–	Hz
α_{CS}	channel separation	V_i = 2 V; frequency range 250 Hz to 10 kHz	90	96	–	dB
THD	total harmonic distortion	frequency range 20 Hz to 12.5 kHz				
		V_i = 100 mV; G_v = 20 dB	–	0.1	–	%
		V_i = 1000 mV; G_v = 0 dB	–	0.05	tbn	%
		V_i = 2000 mV; G_v = 0 dB	–	0.1	–	%
		V_i = 2000 mV; G_v = –10 dB	–	0.1	–	%
RR	ripple rejection	$V_{r(RMS)}$ < 200 mV				
		f = 100 Hz	tbn	76	–	dB
		f = 40 Hz to 12.5 kHz	–	66	–	dB
(S+N)/N	signal-plus-noise to noise ratio	unweighted; 20 Hz to 20 kHz RMS; V_o = 2.0 V; see Figs 6 and 7	–	105	–	dB
		CCIR 468-2 weighted; quasi peak; V_o = 2.0 V				
		G_v = 0 dB	–	95	–	dB
		G_v = 12 dB	–	88	–	dB
		G_v = 20 dB	–	81	–	dB

YMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
o(RMS)	noise output power (RMS value) only contribution of TEA6321; power amplifier for 6 W	mute position; note 1	–	–	10	nW
B	crosstalk (20 log $V_{bus(p-p)}$ / $V_{o(RMS)}$) between bus inputs and signal outputs	note 2	–	110	–	dB
Source selector						
Z_i	input impedance		25	35	45	kΩ
α_S	input isolation of one selected source to any other input	f = 1 kHz	–	105	–	dB
		f = 12.5 kHz	–	95	–	dB
$V_{i(RMS)}$	maximum input voltage (RMS value)	THD < 0.5%; V_{CC} = 8.5 V	–	2.15	–	V
		THD < 0.5%; V_{CC} = 7.5 V	–	1.8	–	V
$V_{DC\ OFF}$	DC offset voltage at source selector out by selection of any inputs		–	–	10	mV
Z_o	output impedance		–	80	120	Ω
R_L	output load resistance		10	–	–	kΩ
C_L	output load capacity		0	–	2500	pF
G_v	voltage gain, source selector		–	0	–	dB
Control part (source selector disconnected; source resistance 600 Ω)						
Z_i	input impedance volume input		100	150	200	kΩ
	input impedance loudness input		25	33	40	kΩ
Z_o	output impedance		–	80	120	Ω
R_L	output load resistance		2	–	–	kΩ
C_L	output load capacity		0	–	10	nF
R_{DCL}	DC load resistance at output to ground		4.7	–	–	kΩ
$V_{i(RMS)}$	maximum input voltage (RMS value)	THD < 0.5%	–	2.15	–	V
V_{no}	noise output voltage	CCIR 468-2 weighted; quasi peak				
		G_v = 20 dB	–	110	220	μV
		G_v = 0 dB	–	33	50	μV
		G_v = –66 dB	–	13	22	μV
		mute position	–	10	–	μV
G_c	total continuous control range		–	106	–	dB
	recommended control range		–	86	–	dB
G_{step}	step resolution		–	1	–	dB
	step error between any adjoining step		–	–	0.5	dB
ΔG_a	attenuator set error	G_v = +20 to –50 dB	–	–	2	dB
		G_v = –51 to –66 dB	–	–	3	dB
ΔG_t	gain tracking error	G_v = +20 to –50 dB	–	–	2	dB
α_m	mute attenuation	see Fig.9	100	110	–	dB
$V_{DC\ OFF}$	DC step offset	G_v = 0 to –66 dB	–	0.2	10	mV
	between any adjoining step	G_v = 20 to 0 dB	–	2	15	mV
	between any step to mute	G_v = 0 to –66 dB	–	–	10	mV

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Volume I control and loudness						
G_c	continuous volume control range		–	51	–	dB
G_v	volume gain		–31	–	20	dB
G_{step}	step resolution		–	1	–	dB
L_B	maximum loudness boost	loudness on; referred to loudness off; boost is determined by external components				
		f = 40 Hz	–	17	–	dB
		f = 10 kHz	–	4.5	–	dB
Bass control						
G_b	bass control, maximum boost	f = 46 Hz	17	18	19	dB
	maximum attenuation	f = 46 Hz	17	18	19	dB
G_{step}	step resolution (toggle switching)	f = 46 Hz	–	1.8	–	dB
	step error between any adjoining step	f = 46 Hz	–	–	0.5	dB
$V_{DC\ OFF}$	DC step offset in any bass position		–	–	10	mV
Treble control						
G_t	treble control, maximum boost	f = 15 kHz	11	12	13	dB
	maximum attenuation	f = 15 kHz	11	12	13	dB
	maximum boost	f > 15 kHz	–	–	15	dB
G_{step}	step resolution (toggle switching)	f = 15 kHz	–	1.5	–	dB
	step error between any adjoining step	f = 15 kHz	–	–	0.5	dB
$V_{DC\ OFF}$	DC step offset in any treble position		–	–	10	mV
Volume II, balance and fader control						
G_f	continuous attenuation fader and volume control range		53.5	55	56.5	dB
G_{step}	step resolution		–	1	2	dB
	attenuation set error		–	–	1.5	dB
Mute function (see Fig.10)						
a) Hardware mute						
V_{SW}	mute switch level (2 x V_{BE})		–	1.45	–	V
mute active:						
$V_{SW\ LOW}$	input level		–	–	1.0	V
I_{CH}	input current	$V_{SW\ LOW}$ = 1 V	–300	–	–	µA
mute passive: level internally defined						
$V_{SW\ HIGH}$	saturation voltage		–	–	V_{CC}	V
t_{DMU}	delay until mute passive		–	–	0.5	ms
b) Zero crossing mute						
I_D	discharge current		0.3	0.6	1.2	µA
I_{CH}	charge current		–300	–150	–	µA
V_{SWDEL}	delay switch level (3 x V_{BE})		–	2.2	–	V
t_{DEV}	delay time	C_m = 10 nF	–	100	–	ms
V_{WIND}	window for audio signal zero crossing detection		–	30	40	mV

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Muting at power supply drop						
$V_{CC-DROP}$	supply drop for mute active		–	$V_{19} - 0.7$	–	V
Power on reset (when reset is active the GMU-bit (general mute) is set and the I^2C-bus receiver is in reset position)						
V_{CC}	increasing supply voltage start of reset		–	–	2.5	V
	end of reset		5.2	6.0	6.8	V
	decreasing supply voltage start of reset		4.2	5.0	5.8	V
Digital part						
I^2C-bus pins; see note 3						
V_{IH}	HIGH level input voltage		3	–	9.5	V
V_{IL}	LOW level input voltage		–0.3	–	+1.5	V
I_{IH}	HIGH level input current		–10	–	+10	μA
I_{IL}	LOW level input current		–10	–	+10	μA
V_{OL}	LOW level output voltage	I_L = 3 mA	–	–	0.4	V

Notes to the characteristics

1. The indicated values for output power assume a 6 W power amplifier at 4 Ω with 20 dB gain and a fixed attenuator of 12 dB in front of it. Signal-to-noise ratios exclude noise contribution of the power amplifier.
2. The transmission contains: total initialization with MAD and Subaddress for volume and 8 data words, see also definition of characteristics, clock frequency = 50 kHz, repetition burst rate = 400 Hz, maximum bus signal amplitude = 5 V_{p-p}.
3. The AC characteristics are in accordance with the I^2C-bus specification. Full specification of I^2C-bus will be supplied on request.

I^2C-BUS PROTOCOL

I^2C-bus format

S	SLAVE ADDRESS	A	SUBADDRESS	A	DATA	A	P

Where:

S = start condition
SLAVE ADDRESS (MAD) = 1000 0000
A = acknowledge, generated by the slave
SUBADDRESS (SAD) = see Table 1
DATA = see Table 1
P = STOP condition

If more than 1 byte of DATA is transmitted, then auto-increment of the significant subaddress is performed.

Subaddress

Table 1 Second byte after MAD.

FUNCTION	BIT	MSB 7	6	5	4	3	2	1	LSB 0
volume/loudness	V	0	0	0	0	0	0	0	0
fader front right	FFR	0	0	0	0	0	0	0	1
fader front left	FFL	0	0	0	0	0	0	1	0
fader rear right	FRR	0	0	0	0	0	0	1	1
fader rear left	FRL	0	0	0	0	0	1	0	0
bass	BA	0	0	0	0	0	1	0	1
treble	TR	0	0	0	0	0	1	1	0
switch	S	0	0	0	0	0	1	1	1
							significant subaddress		

Definition of third byte

Table 2 Third byte after MAD and SAD.

FUNCTION	BIT	MSB 7	6	5	4	3	2	1	LSB 0
volume/loudness	V	ZCM	LOFF	V5	V4	V3	V2	V1	V0
fader front right	FFR	X	X	FFR5	FFR4	FFR3	FFR2	FFR1	FFR0
fader front left	FFL	X	X	FFL5	FFL4	FFL3	FFL2	FFL1	FFL0
fader rear right	FRR	X	X	FRR5	FRR4	FRR3	FRR2	FRR1	FRR0
fader rear left	FRL	X	X	FRL5	FRL4	FRL3	FRL2	FRL1	FRL0
bass	BA	X	X	X	BA4	BA3	BA2	BA1	BA0
treble	TR	X	X	X	TR4	TR3	TR2	TR1	TR0
switch	S	GMU	X	X	X	X	SC2	SC1	SC0

Function of the bits:

V0 to V5	volume control
LOFF	switch loudness on/off
FRR0 to FRR5	fader control front right
FFL0 to FFL5	fader control front left
FRR0 to FRR5	fader control rear right
FRL0 to FRL5	fader control rear left
BA0 to BA4	bass control
TR0 to TR4	treble control
SC0 to SC2	source selector control
GMU	mute control for all outputs (general mute)
ZCM	zero crossing mode
X	don't care bits (logic 1 during testing)

Table 3 Volume setting.

G_V (dB)	DATA					
	V5	V4	V3	V2	V1	V0
20	1	1	1	1	1	1
19	1	1	1	1	1	0
18	1	1	1	1	0	1
17	1	1	1	1	0	0
16	1	1	1	0	1	1
15	1	1	1	0	1	0
14	1	1	1	0	0	1
13	1	1	1	0	0	0
12	1	1	0	1	1	1
11	1	1	0	1	1	0
10	1	1	0	1	0	1
9	1	1	0	1	0	0
8	1	1	0	0	1	1
7	1	1	0	0	1	0
6	1	1	0	0	0	1
5	1	1	0	0	0	0
4	1	0	1	1	1	1
3	1	0	1	1	1	0
2	1	0	1	1	0	1
1	1	0	1	1	0	0
0	1	0	1	0	1	1
−1	1	0	1	0	1	0
−2	1	0	1	0	0	1
−3	1	0	1	0	0	0
−4	1	0	0	1	1	1
−5	1	0	0	1	1	0
−6	1	0	0	1	0	1
−7	1	0	0	1	0	0
−8	1	0	0	0	1	1
−9	1	0	0	0	1	0
−10	1	0	0	0	0	1
−11	1	0	0	0	0	0

Loudness on: the increment of the loudness characteristic is linear at every volume step in the range from +20 dB to −11 dB.

Table 3 Volume setting (continued).

G_v (dB)	DATA					
	V5	V4	V3	V2	V1	V0
–12	0	1	1	1	1	1
–13	0	1	1	1	1	0
–14	0	1	1	1	0	1
–15	0	1	1	1	0	0
–16	0	1	1	0	1	1
–17	0	1	1	0	1	0
–18	0	1	1	0	0	1
–19	0	1	1	0	0	0
–20	0	1	0	1	1	1
–21	0	1	0	1	1	0
–22	0	1	0	1	0	1
–23	0	1	0	1	0	0
–24	0	1	0	0	1	1
–25	0	1	0	0	1	0
–26	0	1	0	0	0	1
–27	0	1	0	0	0	0
–28	0	0	1	1	1	1
–29	0	0	1	1	1	0
–30	0	0	1	1	0	1
–31	0	0	1	1	0	0

Loudness characteristic is constant in a range from –11 dB to –31 dB.

Table 3 Volume setting (continued).

G_v (dB)	DATA					
	V5	V4	V3	V2	V1	V0
–28	0	0	1	0	1	1
.			.			
.			.			
.			.			
–31	0	0	0	0	0	0

Repetition of steps in a range from –28 dB to –31 dB.

4 Fader setting.

v (dB)	DATA					
	FRR5 FRL5 FFL5 FFR5	FRR4 FRL4 FFL4 FFR4	FRR3 FRL3 FFL3 FFR3	FRR2 FRL2 FFL2 FFR2	FRR1 FRL1 FFL1 FFR1	FRR0 FRL0 FFL0 FFR0
0	1	1	1	1	1	1
–1	1	1	1	1	1	0
–2	1	1	1	1	0	1
–3	1	1	1	1	0	0
–4	1	1	1	0	1	1
–5	1	1	1	0	1	0
–6	1	1	1	0	0	1
–7	1	1	1	0	0	0
–8	1	1	0	1	1	1
–9	1	1	0	1	1	0
–10	1	1	0	1	0	1
–11	1	1	0	1	0	0
–12	1	1	0	0	1	1
–13	1	1	0	0	1	0
–14	1	1	0	0	0	1
–15	1	1	0	0	0	0
–16	1	0	1	1	1	1
–17	1	0	1	1	1	0
–18	1	0	1	1	0	1
–19	1	0	1	1	0	0
–20	1	0	1	0	1	1
–21	1	0	1	0	1	0
–22	1	0	1	0	0	1
–23	1	0	1	0	0	0
–24	1	0	0	1	1	1
–25	1	0	0	1	1	0
–26	1	0	0	1	0	1
–27	1	0	0	1	0	0
–28	1	0	0	0	1	1
–29	1	0	0	0	1	0
–30	1	0	0	0	0	1
–31	1	0	0	0	0	0
–32	0	1	1	1	1	1
–33	0	1	1	1	1	0
–34	0	1	1	1	0	1
–35	0	1	1	1	0	0
–36	0	1	1	0	1	1
–37	0	1	1	0	1	0
–38	0	1	1	0	0	1

G_v (dB)	DATA					
	FRR5 FRL5 FFL5 FFR5	FRR4 FRL4 FFL4 FFR4	FRR3 FRL3 FFL3 FFR3	FRR2 FRL2 FFL2 FFR2	FRR1 FRL1 FFL1 FFR1	FRR0 FRL0 FFL0 FFR0
–39	0	1	1	0	0	0
–40	0	1	0	1	1	1
–41	0	1	0	1	1	0
–42	0	1	0	1	0	1
–43	0	1	0	1	0	0
–44	0	1	0	0	1	0
–45	0	1	0	0	1	0
–46	0	1	0	0	0	1
–47	0	1	0	0	0	0
–48	0	0	1	1	1	1
–49	0	0	1	1	1	0
–50	0	0	1	1	0	1
–51	0	0	1	1	0	0
–52	0	0	1	0	1	1
–53	0	0	1	0	1	0
–54	0	0	1	0	0	1
–55	0	0	1	0	0	0
mute	0	0	0	1	1	1
mute	0	0	0	1	1	0
mute	0	0	0	1	0	1
mute	0	0	0	1	0	0
mute	0	0	0	0	1	1
mute	0	0	0	0	1	0
mute	0	0	0	0	0	1
mute	0	0	0	0	0	0

For a particular range the data is always the same, only the subaddress changes.

Table 5 Bass setting.

G_v (dB)	DATA				
	BA4	BA3	BA2	BA1	BA0
18	1	1	1	1	1
16.2	1	1	1	1	0
18	1	1	1	0	1
16.2	1	1	1	0	0
18	1	1	0	1	1
16.2	1	1	0	1	0
14.4	1	1	0	0	1
12.6	1	1	0	0	0
10.8	1	0	1	1	1
9	1	0	1	1	0
7.2	1	0	1	0	1
5.4	1	0	1	0	0
3.6	1	0	0	1	1
1.8	1	0	0	1	0
0 *	1	0	0	0	1
0 **	1	0	0	0	0
–1.8	0	1	1	1	1
–3.6	0	1	1	1	0
–5.4	0	1	1	0	1
–7.2	0	1	1	0	0
–9	0	1	0	1	1
–10.8	0	1	0	1	0
–12.6	0	1	0	0	1
–14.4	0	1	0	0	0
–16.2	0	0	1	1	1
–18	0	0	1	1	0
–16.2	0	0	1	0	1
–18	0	0	1	0	0
***	0	0	0	1	1
***	0	0	0	1	0
***	0	0	0	0	1
*** ****	0	0	0	0	0

* Recommended data word for step 0 dB.

** Result of 1.8 dB boost and 1.8 dB attenuation.

*** The last four bass control data words mute the bass response.

**** The last bass control and treble control data words (00000) enable the external equalizer connection.

Table 6 Treble setting.

G_v (dB)	DATA				
	TR4	TR3	TR2	TR1	TR0
12	1	1	1	1	1
10.5	1	1	1	1	0
12	1	1	1	0	1
10.5	1	1	1	0	0
12	1	1	0	1	1
10.5	1	1	0	1	0
12	1	1	0	0	1
10.5	1	1	0	0	0
9	1	0	1	1	1
7.5	1	0	1	1	0
6	1	0	1	0	1
4.5	1	0	1	0	0
3	1	0	0	1	1
1.5	1	0	0	1	0
0 *	1	0	0	0	1
0 **	1	0	0	0	0
–1.5	0	1	1	1	1
–3	0	1	1	1	0
–4.5	0	1	1	0	1
–6	0	1	1	0	0
–7.5	0	1	0	1	1
–9	0	1	0	1	0
–10.5	0	1	0	0	1
–12	0	1	0	0	0
***	0	0	1	1	1
***	0	0	1	1	0
***	0	0	1	0	1
***	0	0	1	0	0
***	0	0	0	1	1
***	0	0	0	1	0
***	0	0	0	0	1
*** ****	0	0	0	0	0

* Recommended data word for step 0 dB.

** Result of 1.5 dB boost and 1.5 dB attenuation.

*** The last eight treble control data words select treble cut.

**** The last treble control and bass control data words (00000) enable the external equalizer connection.

Table 7 Loudness setting.

CHARACTERISTIC	DATA L OFF
with loudness	0
linear	1

Table 8 Selected inputs.

INPUTS	DATA		
	SC2	SC1	SC0
IAL, IAR stereo	1	1	1
IBL, IBR stereo	1	1	0
ICC, ICR stereo	1	0	1
IDL, IDR stereo	1	0	0
IMO, mono	0	X	X

Table 9 Mute mode.

GMU	ZCM	mode
0	0	direct mute off
0	1	mute off delayed until the next zero crossing
1	0	direct mute
1	1	mute delayed until the next zero crossing

X = don't care bits (logic 1 during testing)

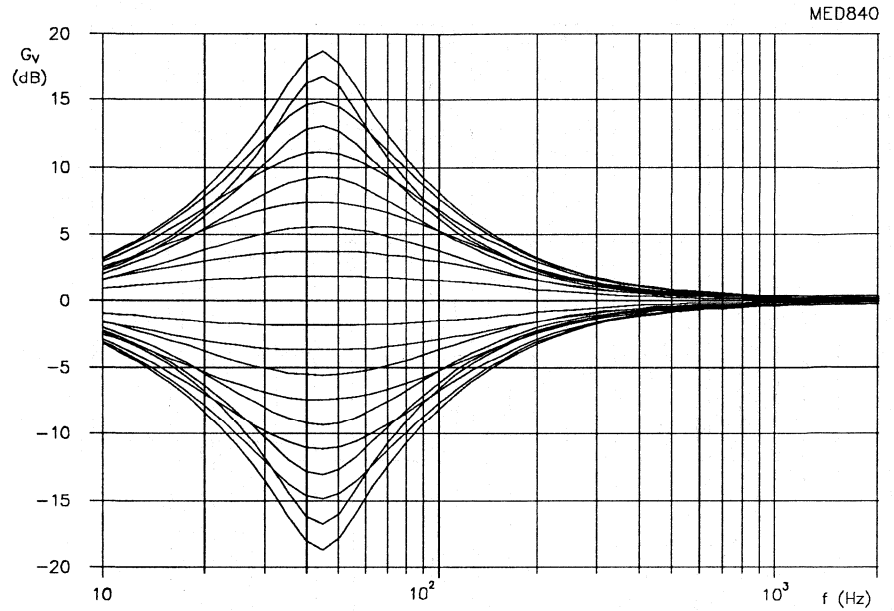


Fig.3 Bass control.

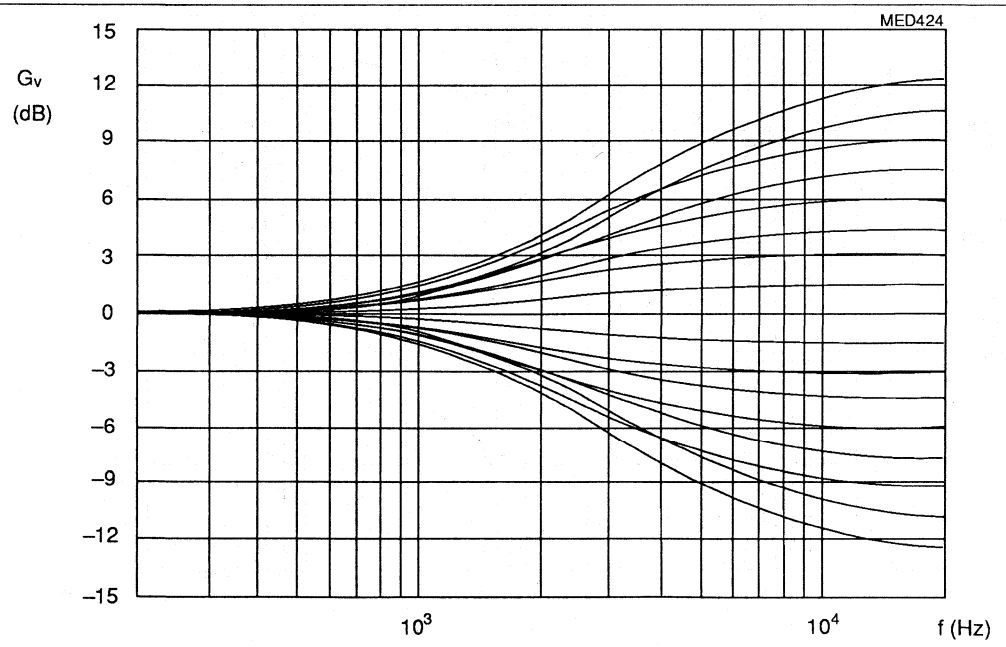


Fig.4 Treble control.

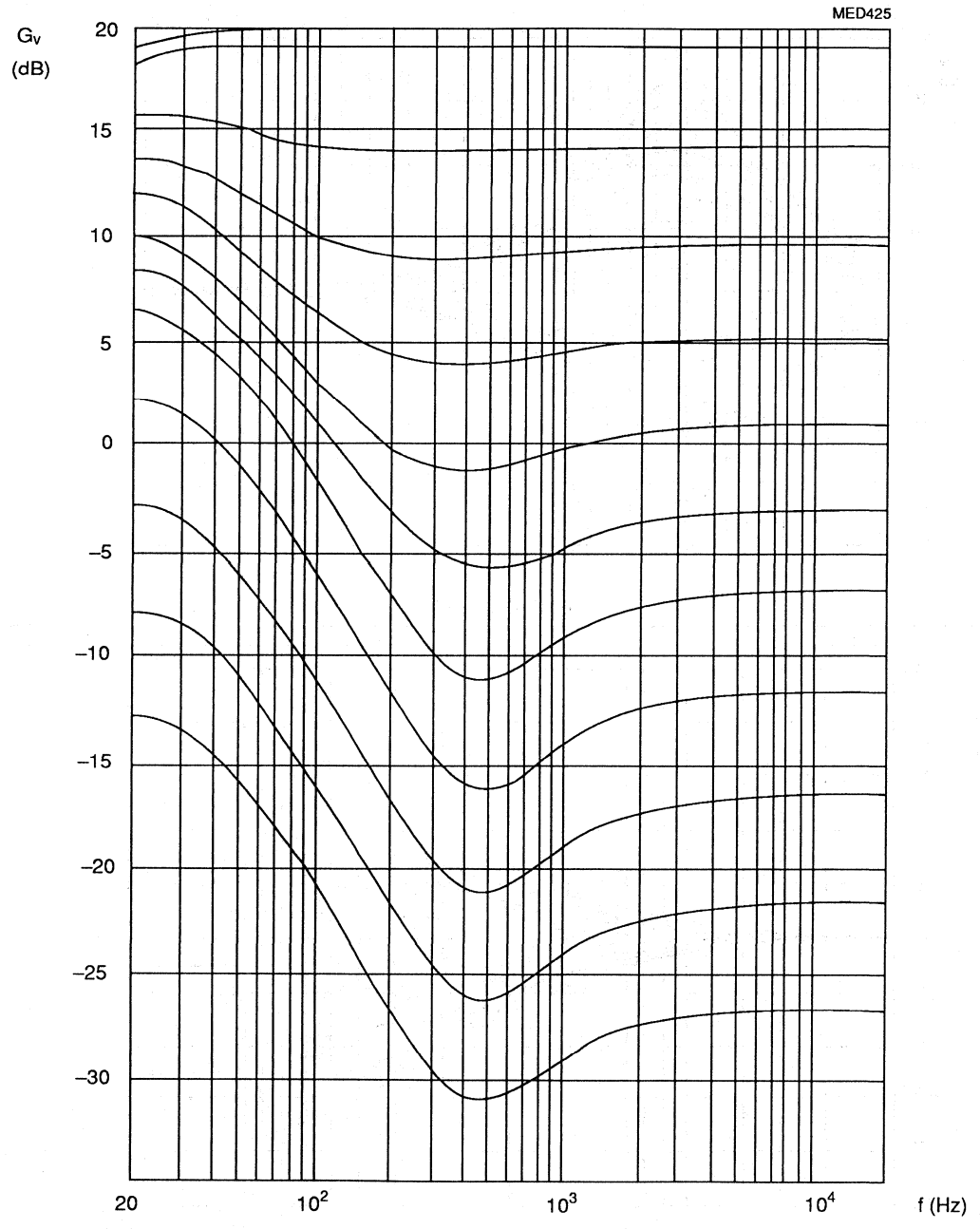
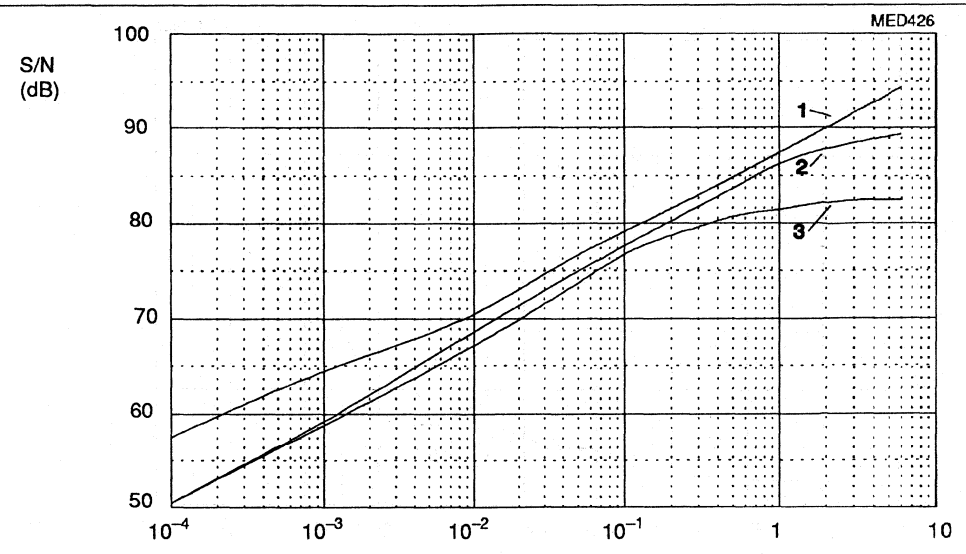
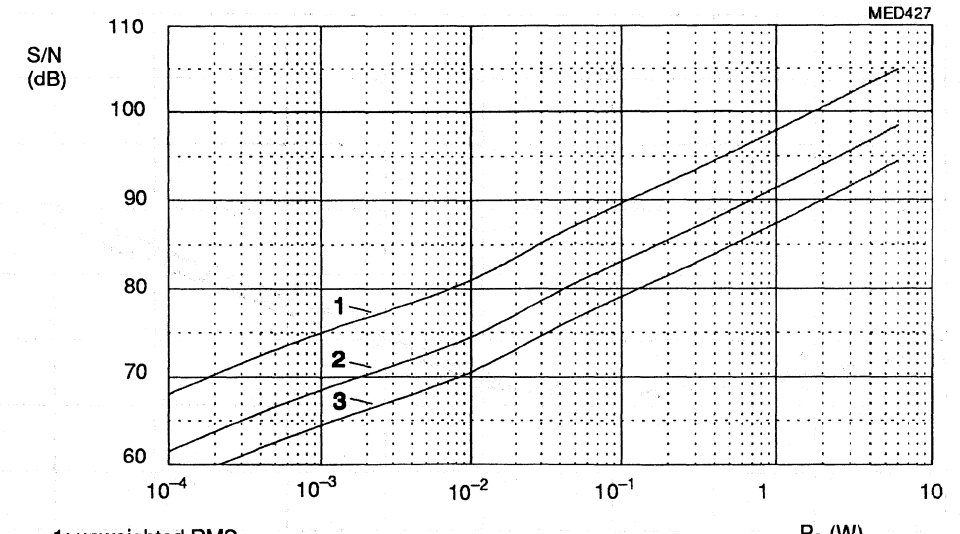


Fig.5 Volume control with loudness (including low roll-off frequency).



1: V_i = 2.0 V
2: V_i = 0.5 V
3: V_i = 0.2 V

Fig.6 Signal-to-noise ratio; noise weighted: CCIR468-2, quasi peak.



1: unweighted RMS
2: CCIR468-2 RMS
3: CCIR468-2 quasi peak

Fig.7 Signal-to-noise ratio; V_i = 2 V; P_{max} = 6 W.

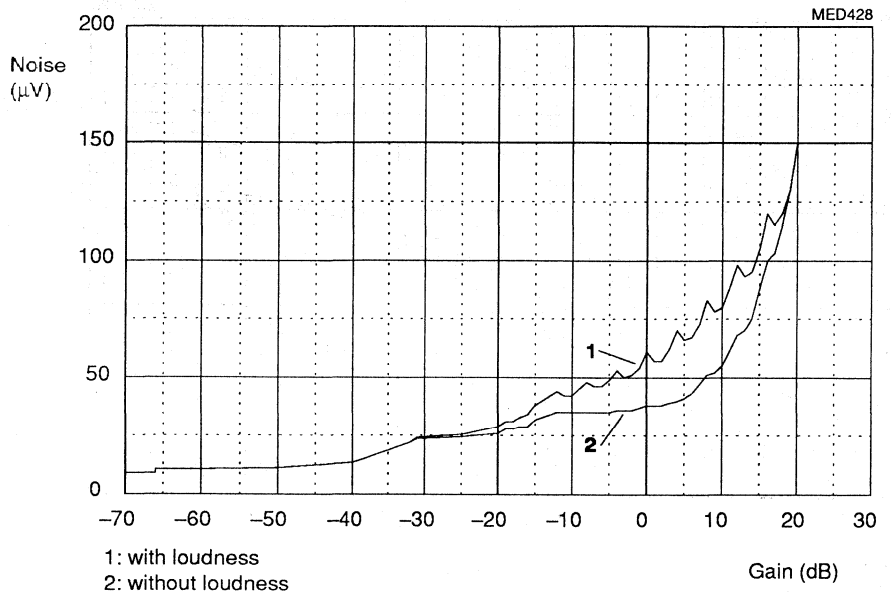


Fig.8 Noise output voltage; CCIR468-2, quasi peak.

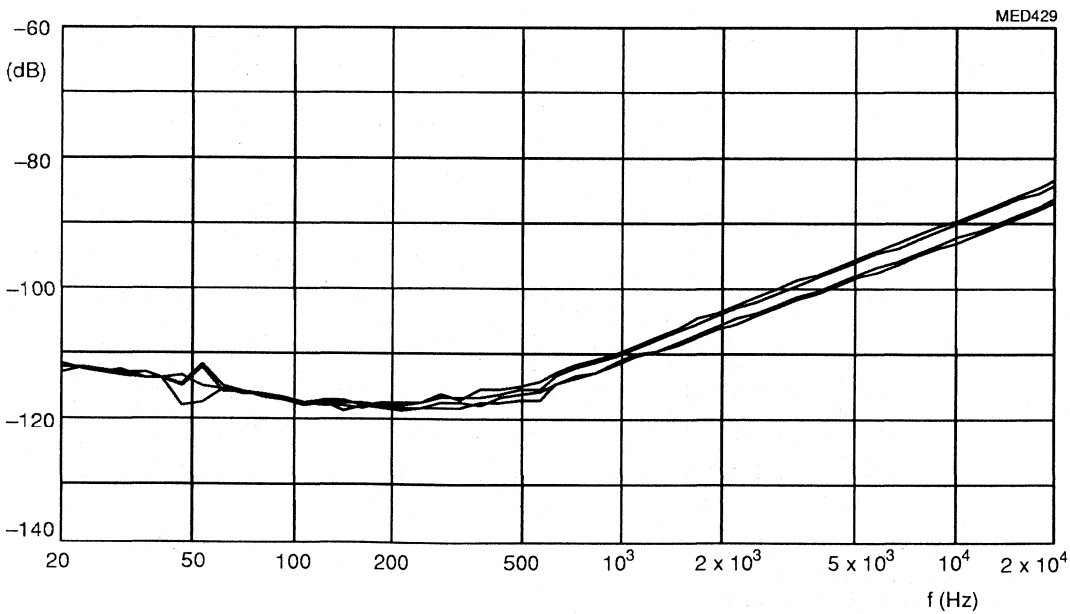
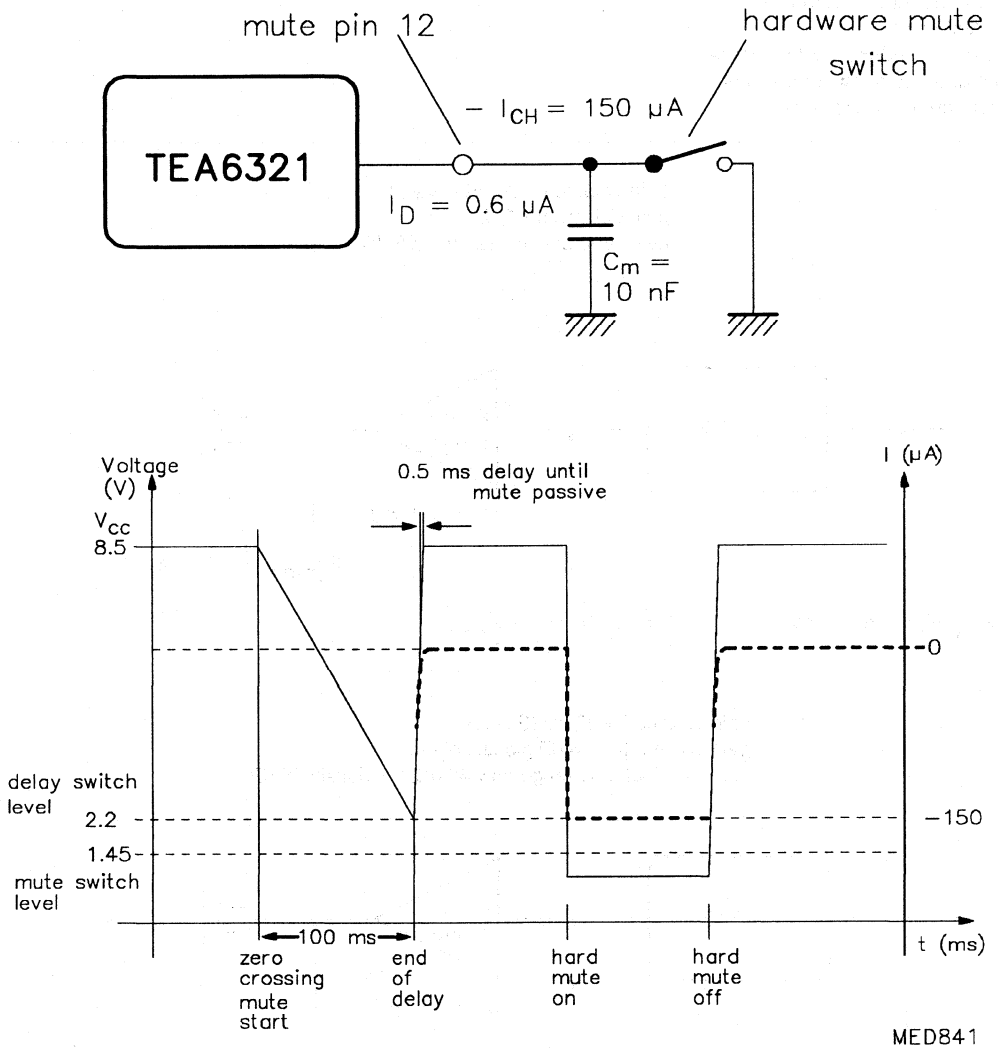


Fig.9 Muting.



delay switch level voltage is typically 2.2 V and is referenced to 3 x V_{BE}

Fig.10 Mute function diagram.

If the 20 dB gain is not required for the maximum volume position, it will be an advantage to use the maximum boost gain and then increased attenuation in the last section, Volume II.
Therefore the loudness will be at the correct place and a lower noise and offset voltage will be achieved.

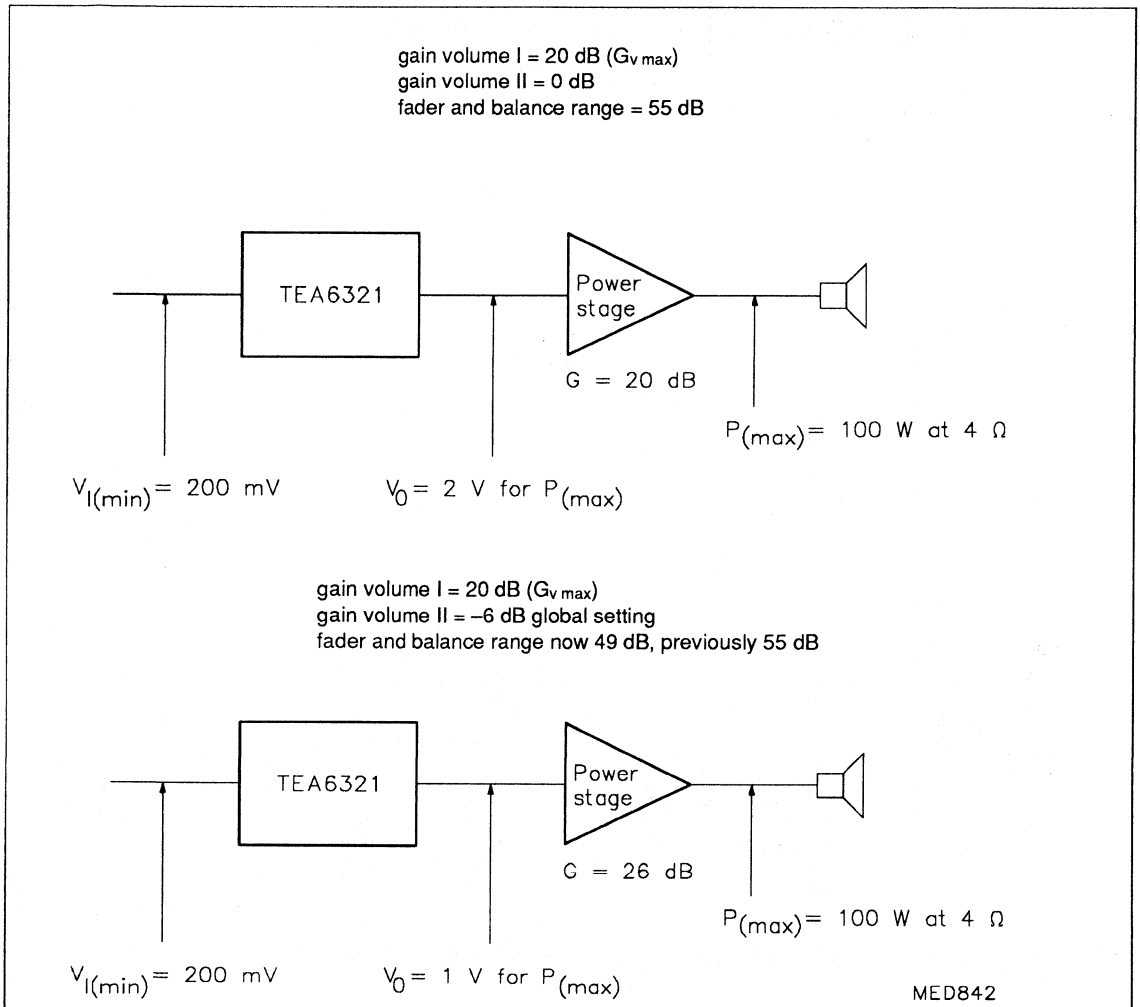


Fig.11 Level diagram.

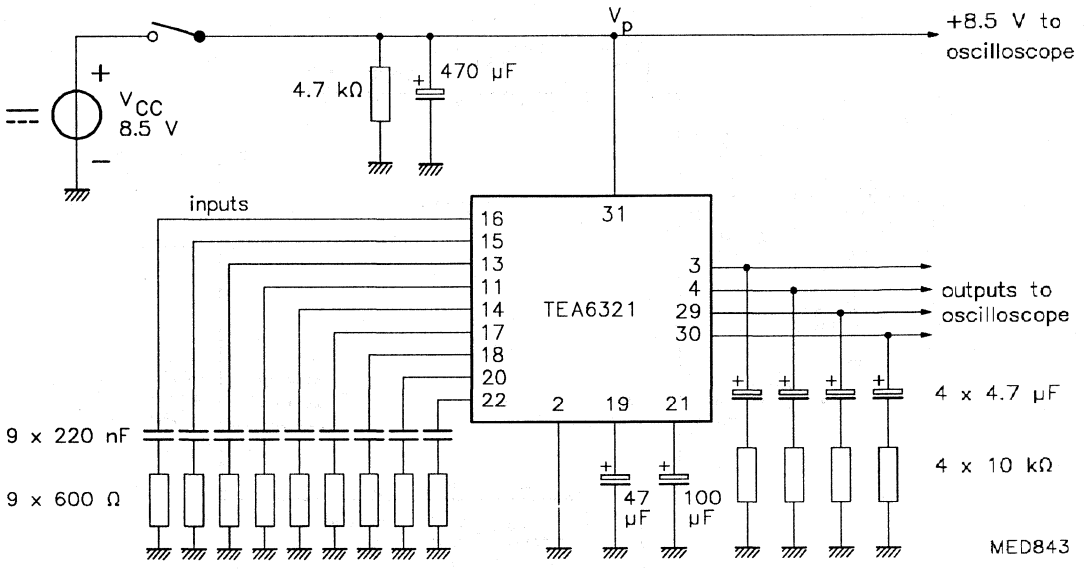


Fig.12 Turn-on/off power supply circuit diagram.

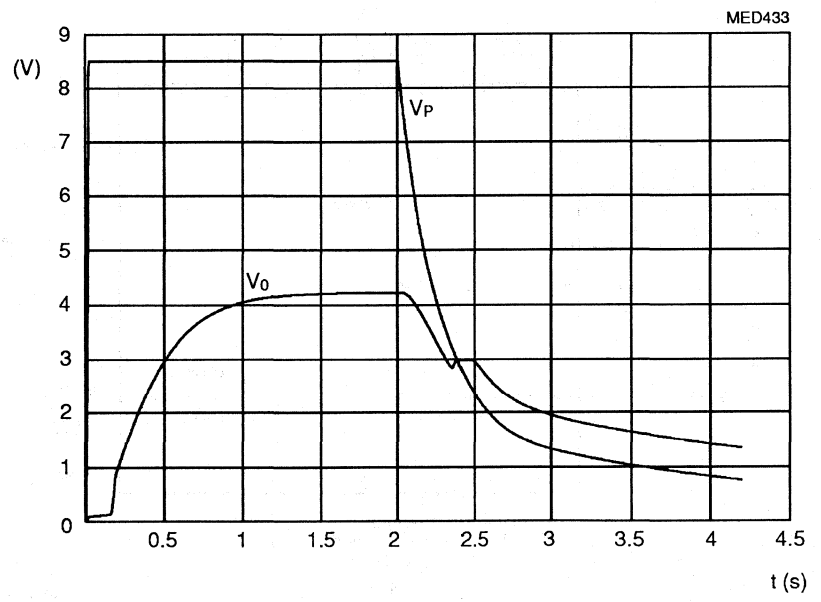


Fig.13 Turn-on/off behaviour.

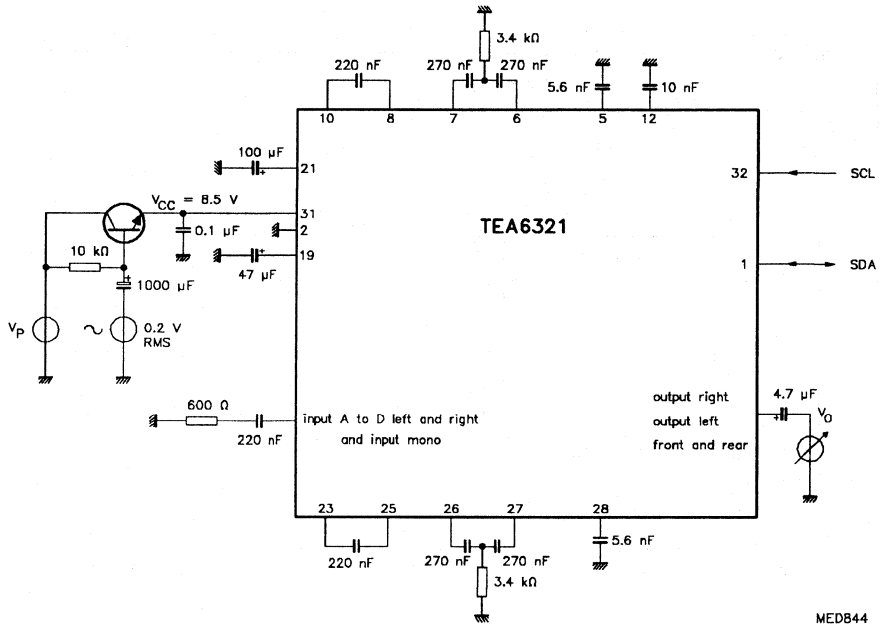


Fig.14 Test circuit for power supply ripple rejection (RR).

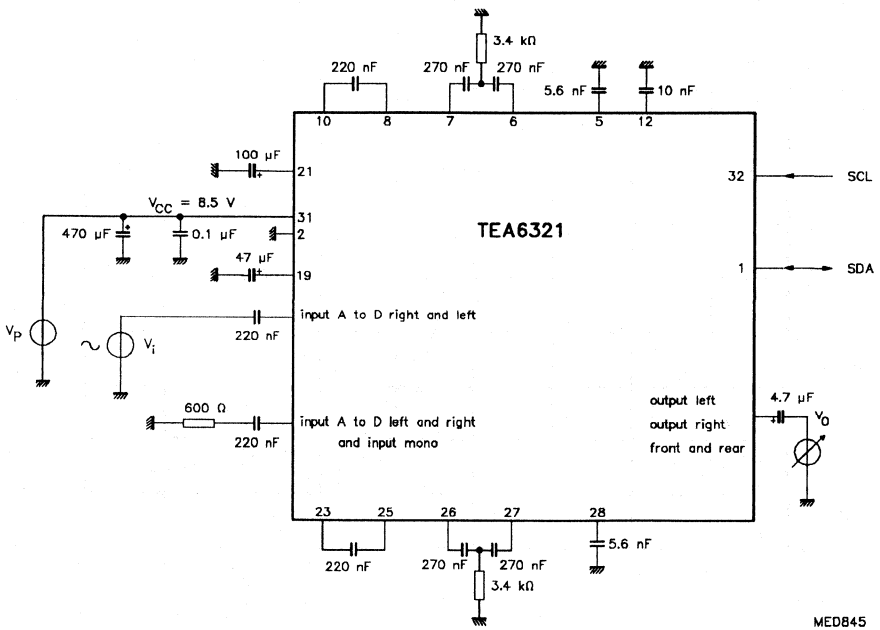


Fig.15 Test circuit for channel separation (α_{cs}).

Selection of input signals by using the zero crossing mute mode

A selection from input A (IAL) to input B (IBL) left sources produces a modulation click depending on the difference of the signal values at the time of switching.
At t_1 the maximum possible difference between signals is 7 $V_{(p-p)}$ and gives a large click. Using the zero cross detector no modulation click is audible.

For example: The selection is enabled at t_1, the microcontroller sets the zero cross bit (ZCM = 1) and then the mute bit (GMU = 1) via the I^2C-bus. The output signal follows the input A signal, until the next zero crossing occurs and then activates mute.
After a fixed delay time at t_2, the microcontroller sends the bits for input switching and mute inactive.

The output signal remains muted until the next signal zero crossing of input B (IBL) occurs, and then follows that signal.
The delay time $t_2 - t_1$ is e. g. 40 ms. Therefore is the capacity CM = 3.3 nF. The zero cross function is working at the lowest frequency of 40 Hz determined by the CM capacitor.

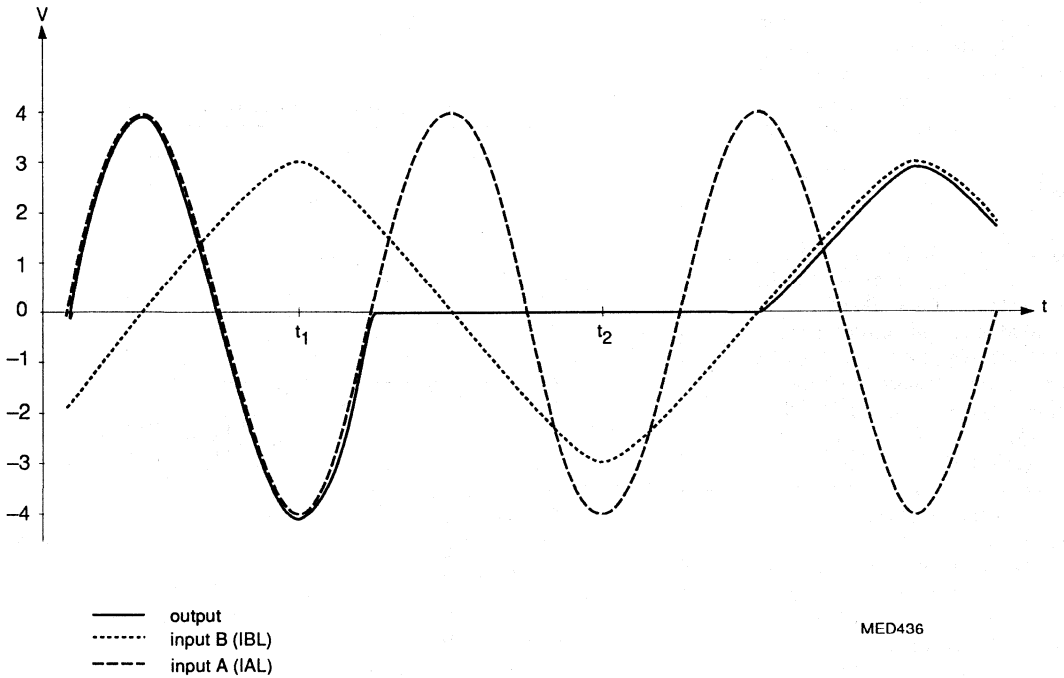


Fig.16 Zero cross function; only one channel shown.

Loudness filter calculation example

Fig.17 shows the basic loudness circuit with an external low pass filter application. R_1 allows an attenuation range of 21 dB while the boost is determined by the gain stage V_2. Both result in a loudness control range of +20 dB to −12 dB.
Defining $f_{reference}$ as the frequency where the level does not change while switching loudness on/off. The external resistor R_3 for $f_{reference} \rightarrow \infty$ can be calculated as

$$R_3 = R_1 \frac{10^{G_v/20}}{1 - 10^{G_v/20}}$$

with G_v = −21 dB and R_1 = 33 kΩ
R_3 = 3.2 kΩ is generated.
For the low pass filter characteristic the value of the external capacitor C_1 can be determined by setting a specific boost for a defined frequency and referring the gain to G_v at $f_{reference}$ as indicated above.

$$\left|\frac{1}{j\omega C_1}\right| = \frac{(R_1 + R_3) \times 10^{G_v/20} - R_3}{1 - 10^{G_v/20}}$$

For example: 3 dB boost at f = 1 kHz
$G_v = G_{v\,reference}$ + 3 dB = −18 dB;
f = 1 kHz and C_1 = 100 nF
If a loudness characteristic with additional high frequency boost is desired, an additional high pass section has to be included in the external filter circuit as indicated in the block diagram. A filter configuration that provides AC coupling avoids offset voltage problems.
Fig.18 shows an example of the loudness circuit with bass and treble boost. The calculation of this network is numeric.

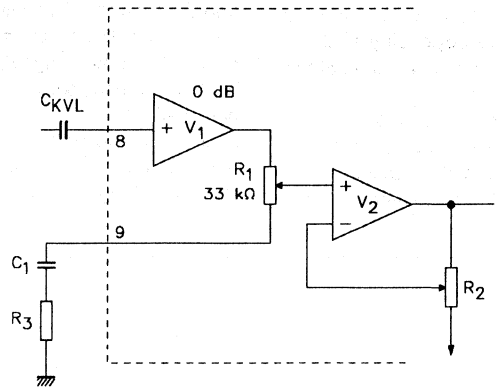


Fig.17 Basic loudness circuit.

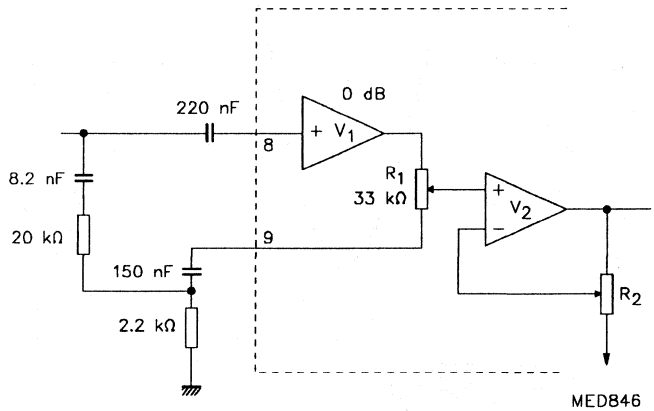
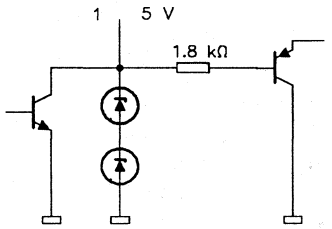
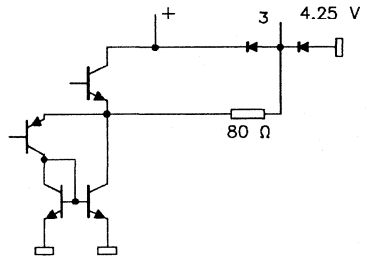


Fig.18 Loudness circuit with bass and treble boost.

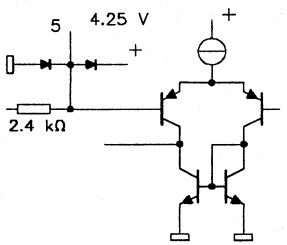
INTERNAL PIN CONFIGURATIONS



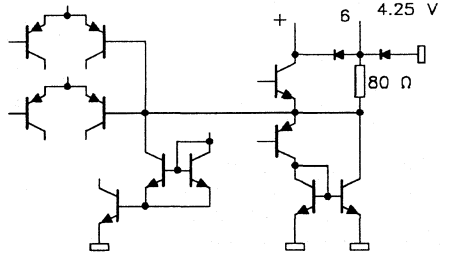
Pin 1: SDA (I^2C-bus data)



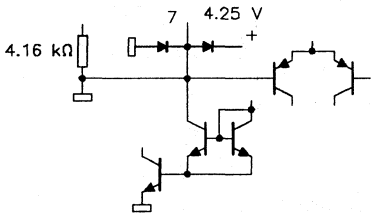
Pin 3: Output left, rear
Pin 4: Output left, front
Pin 29: Output right, front
Pin 30: Output right, rear



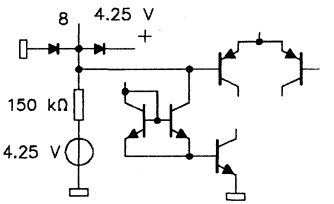
Pin 5: Treble control capacitor, left channel
Pin 28: Treble control capacitor, right channel



Pin 6: Bass control output, left channel
Pin 27: Bass control output, right channel



Pin 7: Bass control input, left channel
Pin 26: Bass control input, right channel

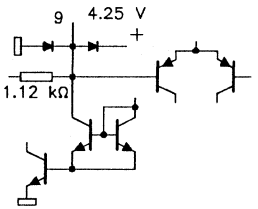


Pin 8: Input volume 1 left, control part
Pin 25: Input volume 1 right, control part

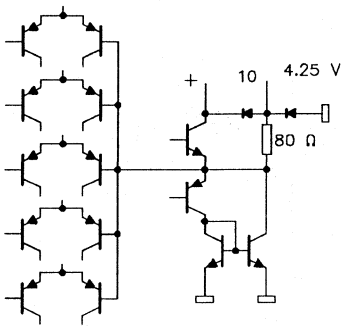
MED847

Pin equivalent circuits
V_{CC} = 8.5 V
(All values shown are typical DC values)

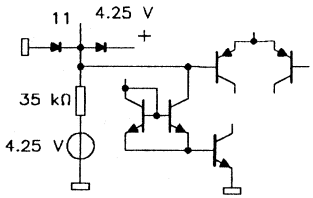
Fig.19 Internal circuits (continued in Fig.20).



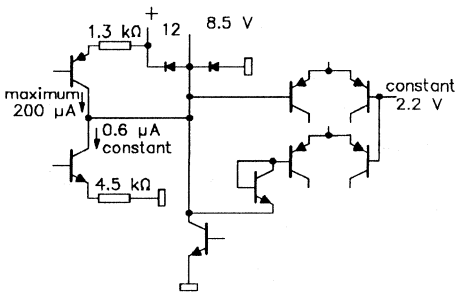
Pin 9: Input loudness left, control part
Pin 24: Input loudness right, control part



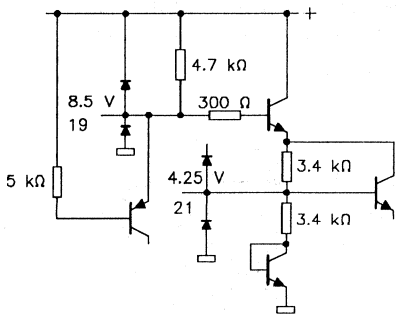
Pin 10: Output source selector, left channel
Pin 23: Output source selector, right channel



Pin 11: Input D left source
Pin 13: Input C left source
Pin 14: Input mono source
Pin 15: Input B left source
Pin 16: Input A left source
Pin 17: Input A right source
Pin 18: Input B right source
Pin 20: Input C right source
Pin 22: Input D right source



Pin 12: Mute control

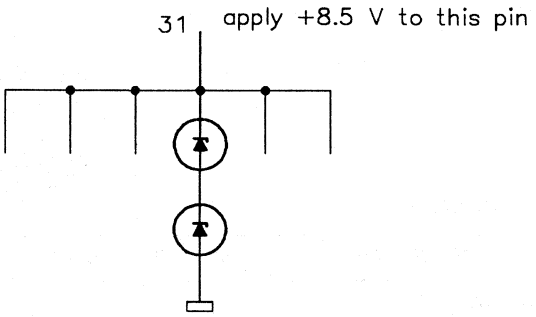


Pin 19: Filtering for supply
Pin 21: Reference voltage

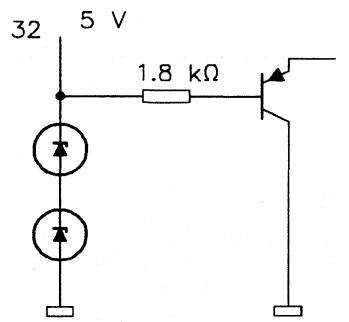
Pin equivalent circuits
V_{CC} = 8.5 V
(All values shown are typical DC values)

MED439

Fig.20 Internal circuits (continued from Fig.19).



Pin 31: Supply voltage



Pin 32: SCL (I^2C-bus clock)

MED440

Pin equivalent circuits
V_{CC} = 8.5 V
(All values shown are typical DC values)

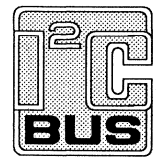
Fig.21 Internal circuits (continued from Fig.20).

Philips Semiconductors

Data sheet	
status	Preliminary specification
date of issue	January 1992
supersedes data sheet of June 1991	

TEA6330T

Sound fader control circuit for car radios



FEATURES

- Stereo/hi-fi processor for car radios performed with volume, balance, bass and treble controls
- Sound fader control (front/rear) down to –30 dB in steps of 2 dB
- Fast muting via bus or via setting the muting pin
- Suitable for external audio equalizers, can be looped-in controlled by the I²C-bus
- Power-on reset on chip sets the device into general mute position
- AC and DC short-circuit protected concerning neighbouring pins
- I²C-bus control for all functions.

GENERAL DESCRIPTION

This bipolar IC is an I²C-bus controlled sound/volume controller for car radios, in addition with fader function and the possibility of an external equalizer.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage	7	8.5	10	V
I_P	supply current	-	26	-	mA
V_i	maximum AF input signal (RMS value)	2	-	-	V
V_o	maximum AF output signal (RMS value)	1.1	-	-	V
ΔG_v	volume control range, separated	–66	-	+20	dB
	fader control range, separated	0	-	–30	dB
	bass control range	–12	-	+15	dB
	treble control range	–12	-	+12	dB
THD	total harmonic distortion	-	-	0.2	%
S/N(W)	weighted signal-to-noise ratio	-	67	-	dB
α_{CR}	crosstalk attenuation	-	90	-	dB
B	frequency response (–1 dB)	-	35 to 20000	-	Hz

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TEA6330T	20	SO	plastic	SOT163A

Sound fader control circuit for car radios

TEA6330T

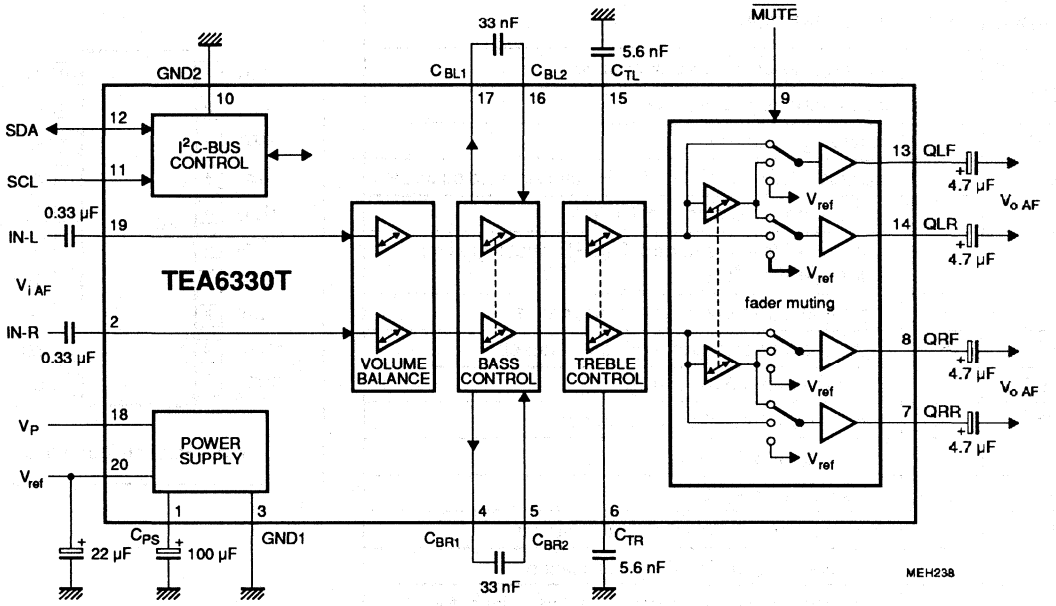


Fig.1 Block and test circuit.

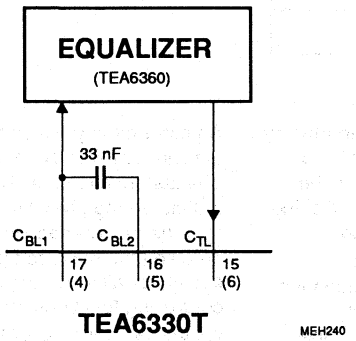


Fig.2 Connection of equalizer (Table 7). In application with equalizer circuit TEA6360 coupling capacitors are not necessary. Connectors for RIGHT in brackets.

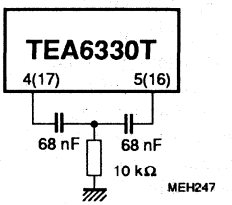


Fig.3 T-filter for enhanced bass control (Fig.5). Connectors for LEFT in brackets.

PINNING

SYMBOL	PIN	DESCRIPTION
C_{PS}	1	filtering capacitor for power supply
IN-R	2	audio input signal RIGHT
GND1	3	analog ground (0 V)
C_{BR1}	4	capacitor for bass control RIGHT and signal to equalizer
C_{BR2}	5	capacitor for bass control RIGHT
C_{TR}	6	capacitor for treble control RIGHT, input signal for equalizer RIGHT
QRR	7	right audio output signal of rear channel
QRF	8	right audio output signal of front channel
MUTE	9	input to set mute externally
GND2	10	digital ground (0 V) for bus control
SCL	11	clock signal of I²C-bus
SDA	12	data signal of I²C-bus
QLF	13	left audio output signal of front channel
QLR	14	left audio output signal of rear channel
C_{TL}	15	capacitor for treble control LEFT, input signal for equalizer LEFT
C_{BL2}	16	capacitor for bass control LEFT
C_{BL1}	17	capacitor for bass control LEFT and signal to equalizer
V_P	18	+8.5 V supply voltage
IN-L	19	audio input signal LEFT
V_{ref}	20	reference voltage output (V_P/2)

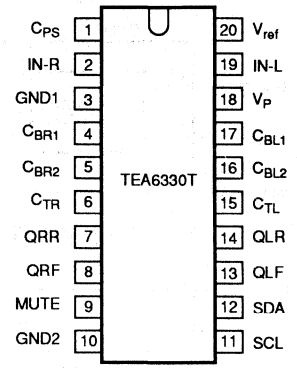


Fig.4 Pin configuration.

FUNCTIONAL DESCRIPTION

This bipolar IC is an I²C-bus controlled sound/volume controller for car radios including fader function and the possibility of an external equalizer. The sound signal setting is performed by resistor chains in combination with multi-input operational amplifiers. The advantages of this principle are the combination of low noise, low distortion and a high dynamic range. The separated volume controls of the left and the right channel make the balance control possible. The value and the characteristic of the balance is controlled via the I²C-bus.

The contour function is performed by setting an extra bass control and optional treble, depending on the actual volume position. Its switching points and its range are also controllable via the I²C-bus.
An interface is assigned behind the volume control to loop-in an equalizer (Fig.2). In this case the treble control is switched off, and the bass control can be used to set the contour.

Low level control fader is included independent of the volume controls, because the TEA6330T has four driver outputs (for front and rear).

An extra mute position for the front, the rear or for all channels is built in. The last function may be used for muting during preset selection.
No external interface is required between the microcomputer and this circuit, for all switching and controlling functions are controllable via the two-wire I²C-bus.

The separate mute-pin allows to switch the fader into mute position without using the I²C-bus.
The on chip power-on reset sets the TEA6330T into the general mute mode.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).
Ground pins 3 and 10 connected together.

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_P	supply voltage (pin 18)	0	10	V
P_{tot}	total power dissipation	0	700	mW
T_{stg}	storage temperature range	–55	150	°C
T_{amb}	operating ambient temperature range	–40	85	°C
V_{ESD}	electrostatic handling* for all pins	-	±300	V
	electrostatic handling** for all pins	-	±4000	V

* Equivalent to discharging a 200 pF capacitor through a 0 Ω series resistor.
** Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

CHARACTERISTICS

V_P = 8.5 V; load resistors at audio outputs 10 kΩ, f_i = 1 kHz (R_S = 600 Ω), bass and treble in linear position, fader in off position and T_{amb} = 25 °C; measurements taken in Fig.1 unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage range (pin 18)		7	8.5	10	V
I_P	supply current		-	26	-	mA
V_{ref}	reference voltage (pin 20)		0.45 V_P	0.5 V_P	0.55 V_P	V
V_O	DC voltage at output (pins 7, 8, 13, 14)		-	0.5 V_P	-	V
Measurements over all						
V_i	maximum AF input level for THD = 2 % at pins 2 and 19 (RMS value)	G_v = –66 to –6 dB and V_P = 8.1 V	2	-	-	V
V_o	maximum AF output level for THD = 2 % at pins 7, 8, 13, 14 (RMS value)	G_v = –4 to +20 dB and V_P = 8.1 V	1.1	-	-	V
G_v	maximum gain by volume setting		19	20	21	dB
B	frequency response	–1 dB roll-off frequency	-	35 to 20000	-	Hz
α_{CR}	crosstalk attenuation	f = 250 to 10000 Hz G_v = 0 dB	70	90	-	dB
THD	total harmonic distortion	f = 20 to 12500 Hz				
	$V_{i\,(RMS)}$ = 50 mV	G_v = +20 dB	-	0.1	0.3	%
	$V_{i\,(RMS)}$ = 500 mV	G_v = 0 dB	-	0.05	0.2	%
	$V_{i\,(RMS)}$ = 1.6 V	G_v = –10 dB	-	0.2	0.5	%
RR	ripple rejection for V_R < 200 mV RMS	G_v = 0 dB				
		f = 100 Hz	-	70	-	dB
		f = 40 Hz to 3 kHz	-	60	-	dB
		f = 3 to 12.5 kHz	-	50	-	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
P_N	noise power at output of a 25 W power stage with 26 dB gain (only contribution of TEA6330T)	mute position (V_9 = 0)	-	-	10	nW
α_{BUS}	crosstalk attenuation between SDA, SCL and signal output (20 log V_{BUS} (p-p)/ V_o RMS)	G_v = 0 dB	-	110	-	dB
S/N(W)	weighted signal-to-noise ratio for	CCIR 468-2 quasi peak for 6 W power amplifier				
	V_i = 50 mV RMS	P_o = 50 mW	-	65	-	dB
	V_i = 500 mV RMS	P_o = 50 mW	-	67	-	dB
	V_i = 50 mV RMS	P_o = 1 W	65	72	-	dB
	V_i = 500 mV RMS	P_o = 1 W	71	78	-	dB
	V_i = 50 mV RMS	P_o = 6 W; Fig.9	-	72	-	dB
	V_i = 500 mV RMS	P_o = 6 W; Fig.9	-	86	-	dB
Audio frequency outputs QLF, QRF, QLR and QRR						
V_o	maximum output signal (RMS value)		1.1	-	-	V
R_o	output resistance (pins 7, 8, 13 and 14)		-	100	150	Ω
R_L	admissible output load resistor	to ground or V_{CC}	7.5	-	-	kΩ
C_L	admissible output load capacitor		-	-	2.5	nF
$V_{N(W)}$	weighted noise voltage at output	CCIR 468-2 ; Fig.8 quasi peak				
	for maximim gain	G_v = +20 dB	-	110	220	μV
	for 0 dB gain	G_v = 0 dB	-	25	50	μV
	for minimum gain	G_v = –66 dB	-	19	38	μV
	for mute position	(V_9 = 0)	-	11	22	μV
Volume control		R_G = 600 Ω				
R_I	input resistance (pins 2 and 19)		35	50	65	kΩ
G_v	volume control range	Table 2	–66	-	+20	dB
ΔG_v	step width		-	2	-	dB
	gain set error	G_v = –50 to +20 dB	-	-	2	dB
		G_v = –66 to –50 dB	-	-	3	dB
	gain tracking error	balance in mid position	-	-	2	dB
α_{mute}	mute attenuation at volume mute	set mute-bits	76	90	-	dB
Bass control						
G_v	controllable bass range	Table 3; Fig.6				
	maximum boost	f = 40 Hz	14	15	16	dB
	maximum boost	f = 100 Hz	12	13	14	dB
	maximum attenuation	f = 40 Hz	11	12	13	dB
	maximum attenuation	f = 100 Hz	10	11	12	dB
ΔG_v	step width	f = 40 Hz	2.5	3	3.5	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Treble control						
G_v	controllable treble range	Table 4; Fig.7				
	maximum boost	f = 10 kHz	9	10	11	dB
	maximum boost	f = 15 kHz	11	12	13	dB
	maximum boost	f > 15 kHz	-	-	15	dB
	maximum attenuation	f = 10 kHz	9	10	11	dB
	maximum attenuation	f = 15 kHz	11	12	13	dB
ΔG_v	step width	f = 15 kHz	2.5	3	3.5	dB
Fader control						
G_v	fader control range	Table 5	-	0 to –30	-	dB
	step width		1.5	2	2.5	dB
α_{MUTE}	mute attenuation	GMB-bit = 1; Table 6	74	84	-	dB
ΔV_o	DC offset output voltage (pins 7, 8, 13, 14)					
	between any adjoining volume step and any step to mute	G_v = –66 to 0 dB	-	0.2	10	mV
		G_v = 0 to +20 dB	-	2	15	mV
	in any treble and fader position	G_v = –66 to 0 dB	-	-	10	mV
	in any bass position	G_v = –66 to 0 dB	-	-	10	mV
External mute (pin 9)						
V_9	input voltage for MUTE-ON (LOW)	fader is switched into general mute position	0	-	1.5	V
	input voltage for MUTE-OFF (HIGH)	Tables 2 and 5	3	-	V_P	V
	input voltage for MUTE-OFF	pin 9 open-circuit	-	5	-	V
I_9	input current		-	-	±10	μA
I²C-bus, SCL and SDA (pins 11 and 12)						
$V_{11, 12}$	input voltage HIGH-level		3	-	V_P	V
	input voltage LOW-level		0	-	1.5	V
$I_{11, 12}$	input current		-	-	±10	μA
V_{ACK}	output voltage at acknowledge (pin 12)	I_{12} = –3 mA	-	-	0.4	V
Power-on reset, when reset is active the GMU-bit (general mute) is set and the bus receiver is in reset position						
V_P	supply voltage for start of reset	increasing voltage	-	-	2.5	V
	supply voltage for end of reset	increasing voltage	5.2	6.0	6.8	V
	supply voltage for start of reset	decreasing voltage	4.2	5.0	5.8	V

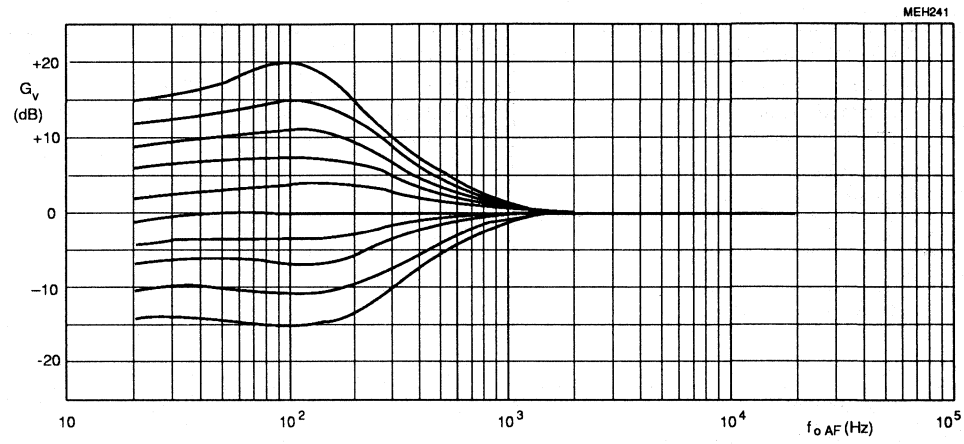


Fig.5 Bass control with enhanced control range (T-filter coupling, Fig.1).

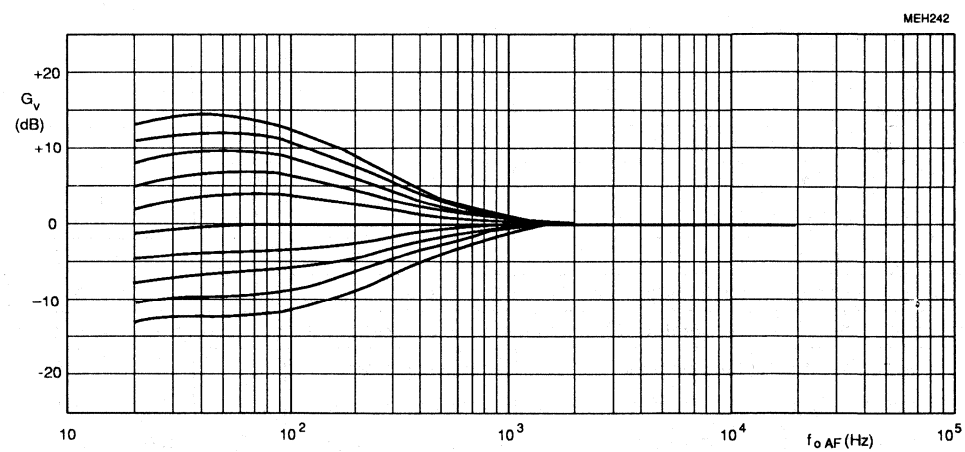


Fig.6 Bass control with normal control range (Fig.1).

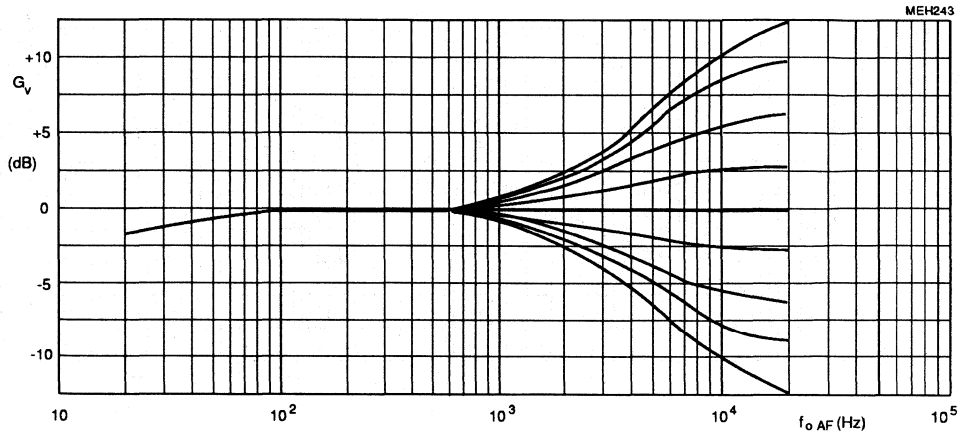


Fig.7 Treble control.

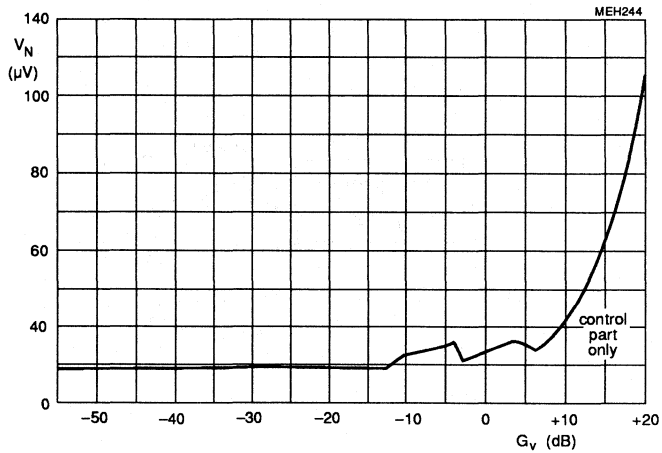


Fig.8 Noise voltage on outputs (CCIR 468-2 weighted, quasi-peak).

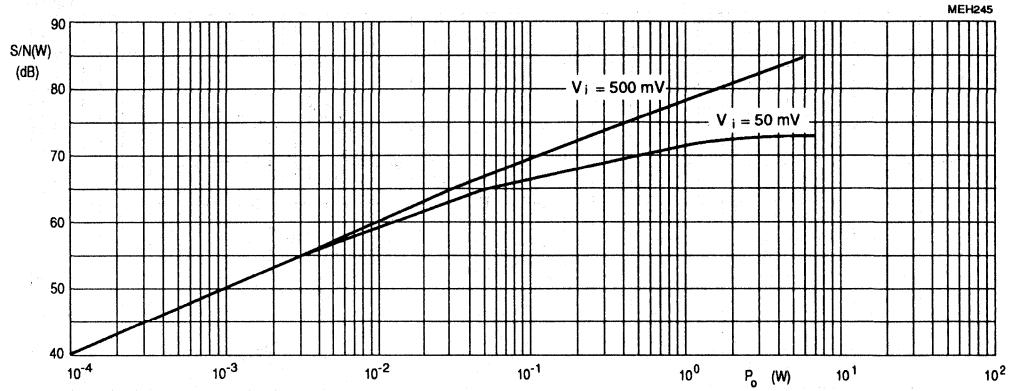


Fig.9 Signal-to-noise ratio (CCIR 468-2 weighted, quasi-peak) for TEA6330T with a 6 W power amplifier (20 dB gain, Fig.10). Measurements without noise contribution of the power amplifier.

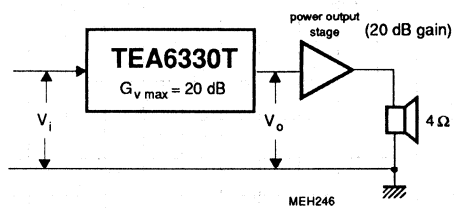


Fig.10 Signal-to-noise ratio measurement (Fig.9) with V_i = 50 mV RMS, V_o = 500 mV RMS for P_{max} = 6 W.

I²C-BUS PROTOCOL

I²C-bus format

S	SLAVE ADDRESS	A	SUBADDRESS	A	DATA	P

S = start condition
SLAVE ADDRESS = **1000 000X**
A = acknowledge, generated by the slave
SUBADDRESS = subaddress byte, Table 1
DATA = data byte, Table 1
P = stop condition

X = read/write control bit
X = 0, order to write (the circuit is slave receiver only)

If more than 1 byte DATA are transmitted, then auto-increment of the subaddress is performed.

Byte organisation

Table 1 I²C-bus transmission

function	subaddress byte								data byte D7	D6	D5	D4	D3	D2	D1	D0
volume left	0	0	0	0	0	0	0	0	0	0	VL5	VL4	VL3	VL2	VL1	VL0
volume right	0	0	0	0	0	0	0	1	0	0	VR5	VR4	VR3	VR2	VR1	VR0
bass	0	0	0	0	0	0	1	0	0	0	0	0	BA3	BA2	BA1	BA0
treble	0	0	0	0	0	0	1	1	0	0	0	0	TR3	TR2	TR1	TR0
fader	0	0	0	0	0	1	0	0	0	0	MFN	FCH	FA3	FA2	FA1	FA0
audio switch	0	0	0	0	0	1	0	1	GMU	EQN	0	0	0	0	0	0

Function of the bits:

VL0 to VL5 volume control of left channel (balance control)
VR0 to VR5 volume control of right channel (balance control)
BA0 to BA3 bass control of both channels
TR0 to TR3 treble control of both channels
FA0 to FA3 fader control front to rear

FCH select fader channels front or rear
MFN mute control of the selected channels front or rear
GMU mute control, general mute
EQN equalizer switchover (0 = equalizer-on)

Table 2(a) Volume setting LEFT

G_v dB	DATA VL5	VL4	VL3	VL2	VL1	VL0
+20	1	1	1	1	1	1
+18	1	1	1	1	1	0
+16	1	1	1	1	0	1
+14	1	1	1	1	0	0
+12	1	1	1	0	1	1
+10	1	1	1	0	1	0
+8	1	1	1	0	0	1
+6	1	1	1	0	0	0
+4	1	1	0	1	1	1
+2	1	1	0	1	1	0
0	1	1	0	1	0	1
–2	1	1	0	1	0	0
–4	1	1	0	0	1	1
–6	1	1	0	0	1	0
–8	1	1	0	0	0	1
–10	1	1	0	0	0	0
–12	1	0	1	1	1	1
–14	1	0	1	1	1	0
–16	1	0	1	1	0	1
–18	1	0	1	1	0	0
–20	1	0	1	0	1	1
–22	1	0	1	0	1	0
–24	1	0	1	0	0	1
–26	1	0	1	0	0	0
–28	1	0	0	1	1	1
–30	1	0	0	1	1	0
–32	1	0	0	1	0	1
–34	1	0	0	1	0	0
–36	1	0	0	0	1	1
–38	1	0	0	0	1	0
–40	1	0	0	0	0	1
–42	1	0	0	0	0	0
–44	0	1	1	1	1	1
–46	0	1	1	1	1	0
–48	0	1	1	1	0	1
–50	0	1	1	1	0	0
–52	0	1	1	0	1	1
–54	0	1	1	0	1	0
–56	0	1	1	0	0	1
–58	0	1	1	0	0	0
–60	0	1	0	1	1	1
–62	0	1	0	1	1	0
–64	0	1	0	1	0	1
–66	0	1	0	1	0	0
mute left	0	1	0	0	1	1
mute left	0	1	0	0	1	0
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mute left	0	0	0	0	0	0

Table 2(b) Volume setting RIGHT

G_v dB	DATA VR5	VR4	VR3	VR2	VR1	VL0
+20	1	1	1	1	1	1
+18	1	1	1	1	1	0
+16	1	1	1	1	0	1
+14	1	1	1	1	0	0
+12	1	1	1	0	1	1
+10	1	1	1	0	1	0
+8	1	1	1	0	0	1
+6	1	1	1	0	0	0
+4	1	1	0	1	1	1
+2	1	1	0	1	1	0
0	1	1	0	1	0	1
–2	1	1	0	1	0	0
–4	1	1	0	0	1	1
–6	1	1	0	0	1	0
–8	1	1	0	0	0	1
–10	1	1	0	0	0	0
–12	1	0	1	1	1	1
–14	1	0	1	1	1	0
–16	1	0	1	1	0	1
–18	1	0	1	1	0	0
–20	1	0	1	0	1	1
–22	1	0	1	0	1	0
–24	1	0	1	0	0	1
–26	1	0	1	0	0	0
–28	1	0	0	1	1	1
–30	1	0	0	1	1	0
–32	1	0	0	1	0	1
–34	1	0	0	1	0	0
–36	1	0	0	0	1	1
–38	1	0	0	0	1	0
–40	1	0	0	0	0	1
–42	1	0	0	0	0	0
–44	0	1	1	1	1	1
–46	0	1	1	1	1	0
–48	0	1	1	1	0	1
–50	0	1	1	1	0	0
–52	0	1	1	0	1	1
–54	0	1	1	0	1	0
–56	0	1	1	0	0	1
–58	0	1	1	0	0	0
–60	0	1	0	1	1	1
–62	0	1	0	1	1	0
–64	0	1	0	1	0	1
–66	0	1	0	1	0	0
mute right	0	1	0	0	1	1
mute right	0	1	0	0	1	0
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mute right	0	0	0	0	0	0

Table 3(a) Bass setting with equalizer passive (EQN = 1)

G_v dB	DATA D3	D2	D1	D0
+15	1	1	1	1
+15	1	1	1	0
+15	1	1	0	1
+15	1	1	0	0
+12	1	0	1	1
+9	1	0	1	0
+6	1	0	0	1
+3	1	0	0	0
0	0	1	1	1
–3	0	1	1	0
–6	0	1	0	1
–9	0	1	0	0
–12	0	0	1	1
–12	0	0	1	0
–12	0	0	0	0

Table 3(b) Bass setting with equalizer active (EQN = 0)

G_v dB	DATA D3	D2	D1	D0
+15	1	1	1	1
+15	1	1	1	0
+15	1	1	0	1
+15	1	1	0	0
+12	1	0	1	1
+9	1	0	1	0
+6	1	0	0	1
+3	1	0	0	0
0	0	1	1	1
–3	0	1	1	0
–6	0	1	0	1
–9	0	1	0	0
–12	0	0	1	1
–12	0	0	1	0
–12	0	0	0	0

Table 4(a) Treble setting with equalizer passive (EQN = 1)

G_v dB	DATA D3	D2	D1	D0
+12	1	1	1	1
+12	1	1	1	0
+12	1	1	0	1
+12	1	1	0	0
+12	1	0	1	1
+9	1	0	1	0
+6	1	0	0	1
+3	1	0	0	0
0	0	1	1	1
–3	0	1	1	0
–6	0	1	0	1
–9	0	1	0	0
–12	0	0	1	1
–12	0	0	1	0
–12	0	0	0	0

Table 4(b) Treble setting with equalizer active (EQN = 0)

G_v dB	DATA D3	D2	D1	D0
0	1	1	1	1
0	1	1	1	0
0	1	1	0	1
0	1	1	0	0
0	1	0	1	1
0	1	0	1	0
0	1	0	0	1
0	1	0	0	0
0	0	1	1	1
0	0	1	1	0
0	0	1	0	1
0	0	1	0	0
0	0	0	1	1
0	0	0	1	0
0	0	0	0	0

Table 5(a) Fader function front

setting front dB	setting rear dB	DATA MFN	FCH	FA3	FA2	FA1	FA0
		fader-off					
0	0	1	1	1	1	1	1
0	0	0	1	1	1	1	1
		fader front					
–2	0	1	1	1	1	1	0
–4	0	1	1	1	1	0	1
–6	0	1	1	1	1	0	0
–8	0	1	1	1	0	1	1
–10	0	1	1	1	0	1	0
–12	0	1	1	1	0	0	1
–14	0	1	1	1	0	0	0
–16	0	1	1	0	1	1	1
–18	0	1	1	0	1	1	0
–20	0	1	1	0	1	0	1
–22	0	1	1	0	1	0	0
–24	0	1	1	0	0	1	1
–26	0	1	1	0	0	1	0
–28	0	1	1	0	0	0	1
–30	0	1	1	0	0	0	0
		mute front					
–84	0	0	1	1	1	1	0
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–84	0	0	1	0	0	0	0

Table 5(b) Fader function rear

setting front dB	setting rear dB	DATA MFN	FCH	FA3	FA2	FA1	FA0
		fader-off					
0	0	1	0	1	1	1	1
0	0	0	0	1	1	1	1
		fader rear					
0	–2	1	0	1	1	1	0
0	–4	1	0	1	1	0	1
0	–6	1	0	1	1	0	0
0	–8	1	0	1	0	1	1
0	–10	1	0	1	0	1	0
0	–12	1	0	1	0	0	1
0	–14	1	0	1	0	0	0
0	–16	1	0	0	1	1	1
0	–18	1	0	0	1	1	0
0	–20	1	0	0	1	0	1
0	–22	1	0	0	1	0	0
0	–24	1	0	0	0	1	1
0	–26	1	0	0	0	1	0
0	–28	1	0	0	0	0	1
0	–30	1	0	0	0	0	0
		mute rear					
0	–84	0	0	1	1	1	0
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	---			---			---
0	–84	0	0	0	0	0	0

Table 6 Mute control

MUTE control	DATA GMU-bit	remarks
active	1	outputs QLF, QLR, QRF and QRR are muted
passive	0	no general mute

Table 7 Equalizer

equalizer control	DATA EQN-bit	remarks
active	0	signal outputs for equalizer are pins 4 and 17, inputs are pins 6 and 15; Tables 3(b) and 4(b)
passive	1	no general mute; Tables 3(a) and 4(a)

5-band stereo equalizer circuit TEA6360

FEATURES

- Monolithic integrated 5-band stereo equalizer circuit
- Five filters for each channel
- Centre frequency, bandwidth and maximum boost/cut defined by external components
- Choise for variable or constant Q-factor via I²C software
- Defeat mode
- All stages are DC-coupled
- I²C-bus control for all functions
- Two different modul addresses programmable

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage (pin 14)	7	8.5	13.2	V
I_P	supply current	-	24.5	-	mA
$V_{1,32}$	input voltage range	-	2.1 to V_{P-1}	-	V
V_o	maximum output signal level (RMS value, pins 13 and 20)	- 1.1		-	V
G_v	total signal gain, all filters linear	–0.5	-	0	dB
B	-1 dB frequency response (linear)	0 to 20	-	-	kHz
T_{amb}	operating ambient temperature	–40	-	85	°C

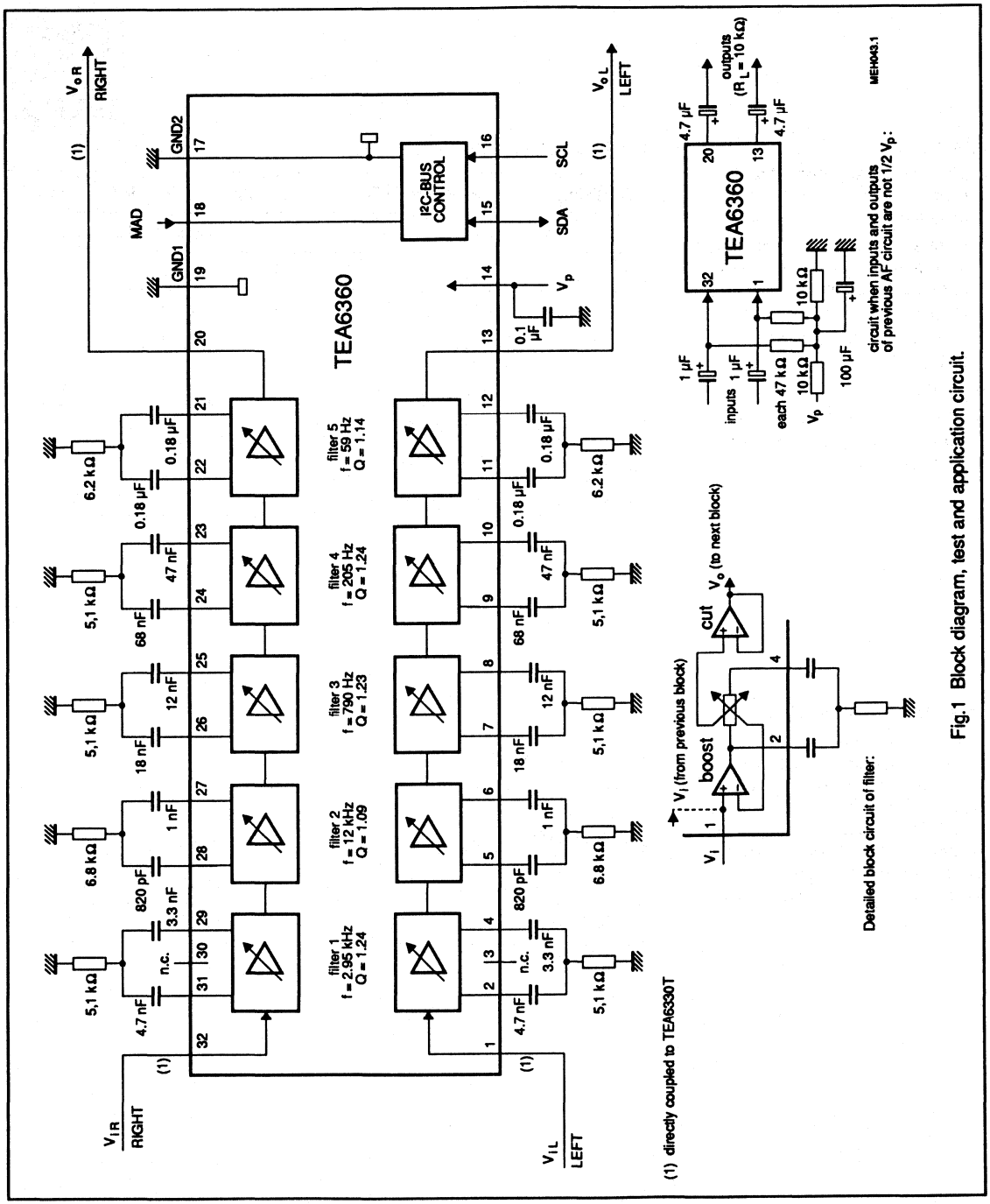
GENERAL DESCRIPTION

The 5-band stereo equalizer is an I²C-bus controlled tone processor for application in car radio sets, TV sets and music centres. It offers the possibility of sound control as well as equalization of sound pressure behaviour of different rooms or loudspeakers, especially in cars.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TEA6360	32	shrink DIL	plastic	SOT232
TEA6360/T	32	mini-pack	plastic	SOT287

5-band stereo equalizer circuit TEA6360



PINNING

SYMBOL	PIN	DESCRIPTION
V_{iL}	1	audio frequency input LEFT
F1LA	2	connection A for filter 1 LEFT (f = 2.95 kHz)
n.c.	3	not connected
F1LB	4	connection B for filter 1 LEFT(f = 2.95 kHz)
F2LA	5	connection A for filter 2 LEFT (f = 12 kHz)
F2LB	6	connection B for filter 2 LEFT (f = 12 kHz)
F3LA	7	connection A for filter 3 LEFT (f = 790 Hz)
F3LB	8	connection B for filter 3 LEFT (f = 790 Hz)
F4LA	9	connection A for filter 4 LEFT (f = 205 Hz)
F4LB	10	connection B for filter 4 LEFT (f = 205 Hz)
F5LA	11	connection A for filter 5 LEFT (f = 59 Hz)
F5LB	12	connection B for filter 5 LEFT (f = 59 Hz)
V_{oL}	13	audio frequency output LEFT
V_P	14	supply voltage (+8.5 V)
SDA	15	I^2C-bus data line
SCL	16	I^2C-bus clock line
GND2	17	ground 2 (I^2C-bus ground)
MAD	18	modul address
GND1	19	ground 1 (analog ground)
V_{oR}	20	audio frequency output RIGHT
F5RB	21	connection B for filter 5 RIGHT (f = 59 Hz)
F5RA	22	connection A for filter 5 RIGHT (f = 59 Hz)
F4RB	23	connection B for filter 4 RIGHT (f = 205 Hz)
F4RA	24	connection A for filter 4 RIGHT (f = 205 Hz)
F3RB	25	connection B for filter 3 RIGHT (f = 790 Hz)
F3RA	26	connection A for filter 3 RIGHT (f = 790 Hz)
F2RB	27	connection B for filter 2 RIGHT (f = 12 kHz)
F2RA	28	connection A for filter 2 RIGHT (f = 12 kHz)
F1RB	29	connection B for filter 1 RIGHT (f = 2.95 kHz)
n.c.	30	not connected
F1RA	31	connection A for filter 1 RIGHT (f = 2.95 kHz)
V_{iR}	32	audio frequency input RIGHT

PIN CONFIGURATION

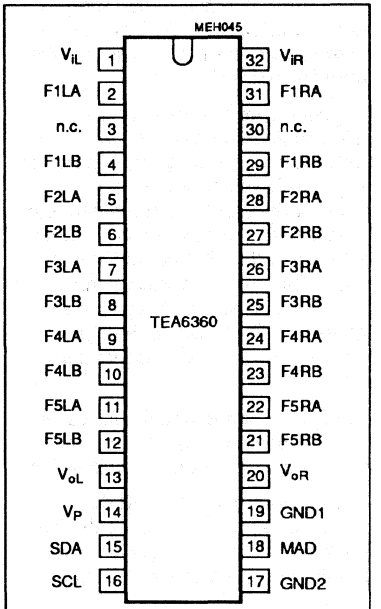


Fig.2 Pin configuration

FUNCTIONAL DESCRIPTION

The TEA6360 is performed with two stereo channels (RIGHT and LEFT), each one consists of five equal filter amplifiers (Fig.1).

The centre frequencies for the different filters as well as the bandwidth and the control ranges for boost and cut depend on the external components. Each filter can have different external components but for one definite pair of filters the centre frequency as well as the control range for boost and cut are the same. That means, they have symmetrical curves for boost and cut.

The control range (maximum value in dB) is divided into five steps and one extra step for the linear position.

At maximum gain of 12 dB the typical step resolution is 2.4 dB. The internal resistor chain of each filter amplifier is optimized for 12 dB maximum gain. Therefore the typical gain factors for 15 dB application are as follows:

step 1 = 2.7 dB
step 2 = 5.5 dB
step 3 = 8.4 dB
step 4 = 11.6 dB
step 5 = 15.0 dB

The control of the different filters is obtained by selecting the appropriate subaddress byte (Tab.1). The position of the filter in the left channel and that in the right channel is always the same (stereo). The position of the boost part and the cut part is independently controllable (Tables 2 and 3).

The quality factor of the filter has its maximum in the maximum position (steps 5), if boost (cut on step 0) or cut (boost on step 0) is used. The quality factor decreases also with the step number (variable quality factor). In this mode the control pattern are according to Table 4.

A different control is necessary to achieve a constant quality factor over the whole control range. For boost with a constant quality factor over the boost range position +5 is selected and boost control is then performed using cut. This control technique is applied to the cut range with position –5 selected and the boost is varied (Table 5).

The cut part has to follow the boost part in each filter for economic reasons. So the signal is first amplified and then attenuated. This has to be taken into account for the internal level diagram in case of constant quality factor. This may result in a mode between constant Q and non-constant Q mode; for example for the position +2 it is not necessary to amplify by step +5 and then attenuate by –3 step. The combination of step +4 and step –2 to reach position +2 is a good result (quasi constant quality factor, Table 6).

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).
Ground pins 19, 28 and 43 connected together.

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_P	supply voltage (pin 14)	0	13.2	V
V_n	voltage on all pins, grounds excluded	0	V_P	V
P_{tot}	total power dissipation	0	500	mW
T_{stg}	storage temperature range	–40	150	°C
T_{amb}	operating ambient temperature range	–40	85	°C
V_{ESD}	electrostatic handling* for all pins		±500	V

* Equivalent to discharging a 200 pF capacitor through a 0 Ω series resistor.

CHARACTERISTICS

V_P = 8.5 V; f_i = 1 kHz (R_S = 600 Ω), R_L = 10 kΩ, T_{amb} = 25 °C and measurements taken in Fig.1, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage.range (pin 14)		7	8.5	13.2	V
I_P	supply current (pin 14)	V_P = 8.5 V	-	25.5	-	mA
		V_P = 12 V	-	26.0	-	mA
Analog part						
R_i	input resistor (pins 1 and 32)		1	-	-	MΩ
$V_{1,32}$	input voltage range at any stage		2.1 to V_P–1	-	-	V
$V_{13,20}$	output voltage range at any stage		1.0 to V_P–1	-	-	V
V_o	output signal level (RMS value, pins 13 and 20)	control range 0 to +5, variable Q-factor or quasi constant Q-factor	1.1	-	-	V
R_o	output resistor (pins 13 and 20)		-	100	-	Ω
R_L	admissable load resistance at outputs (pins 13 and 20)		2	-	-	kΩ
C_L	admissable load capacitance at outputs (pins 13 and 20)		-	-	2.5	nF
G_v	total signal gain ($G = V_o / V_i$)	all filters linear	–0.5	-	0	dB
B	frequency response	all filters linear, roll off frequency for –1 dB				
	minimum value	(DC-coupled)	0	-	-	Hz
	maximum value		20	-	-	kHz
α_{Cr}	crosstalk attenuation between channels	f = 250 to 10000 Hz				
	all filters linear		60	75	-	dB
	all filters maximum boost		55	-	-	dB
	all filters maximum cut		55	-	-	dB
THD	distortion (pins 13 and 20)	f = 20 to 12500 Hz V_P = 8.5 to 12 V				
	$V_{o\ (rms)}$ = 1.1 V	all filters linear	-	0.2	0.5	%
	$V_{o\ (rms)}$ = 0.1 V	all filters linear	-	0.05	0.2	%
	$V_{o\ (rms)}$ = 1.1 V	all filters max. boost	-	0.5	1.0	%
	$V_{o\ (rms)}$ = 0.1 V	all filters max. boost	-	0.1	0.3	%
	$V_{o\ (rms)}$ = 0.1 V	all filters maximum cut	-	0.2	0.5	%
	$V_{o\ (rms)}$ = 1 V	all filters max. boost f = 1 kHz	-	-	0.35	%

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_N	weighted output noise voltage (RMS value)	CCIR 468-3, maximum gain/filter of 12 dB				
	defeat mode		-	8	16	µV
	all filters linear		-	23	46	µV
	all filters maximum boost		-	70	140	µV
	all filters maximum cut		-	23	46	µV
α_{Cr}	crosstalk between bus inputs and signal outputs, 20 log (V_{bus} (p-p) / V_o rms)	all filters linear	-	120	-	dB
RR	ripple rejection at V_{ripple} rms < 200 mV	all filters linear				
	for f = 100 Hz		-	70	-	dB
	for f = 40 to 12500 Hz		-	60	-	dB
Internal filters of analog part						
Q	Q-factor dependent on maximum gain					
	maximum gain 10 dB maximum gain 12 dB maximum gain 15 dB		0.1 0.1 0.1	- - -	1.2 1.4 1.8	
R_{tot}	total resistor of different filter sections		29.6	37.0	44.4	kΩ
ΔR_{tot}	tolerance between any filter section		-	-	±4	%
Internal controls of analog part via I²C-bus						
Step	number of steps for boost or for cut		-	5	-	
	position for linear		-	1	-	
	step resolution	maximum gain 12 dB	-	2.4	-	dB
	step set error		-	0.5	-	dB
ΔV_o	DC offset between any step or neighbouring step or defeat		-	-	±10	mV
I²C-bus control SDA and SCL (pins 15 and 16)						
V_{IH}	input level HIGH		3	-	V_P	V
V_{IL}	input level LOW		0	-	1.5	V
I_I	input current		-	-	±10	µA
V_{ACK}	acknowledge voltage on SDA	I_{15} = 3 mA at LOW	-	-	0.4	V
Module address bit (pin 18)						
V_{IH}	input level HIGH for address 1000 0110		3	-	V_P	V
V_{IL}	input level LOW for address 1000 0100		0	-	1.5	V
I_I	input current		-	-	±10	µA
Power on reset: When reset is active the DEF-bit (defeat) is set and the I²C-bus receiver is in reset position.						
RESET	start of reset	increasing V_P	-	-	2.5	V
		decreasing V_P	4.2	5.0	5.8	V
	end of reset	increasing V_P	5.2	6.0	6.8	V

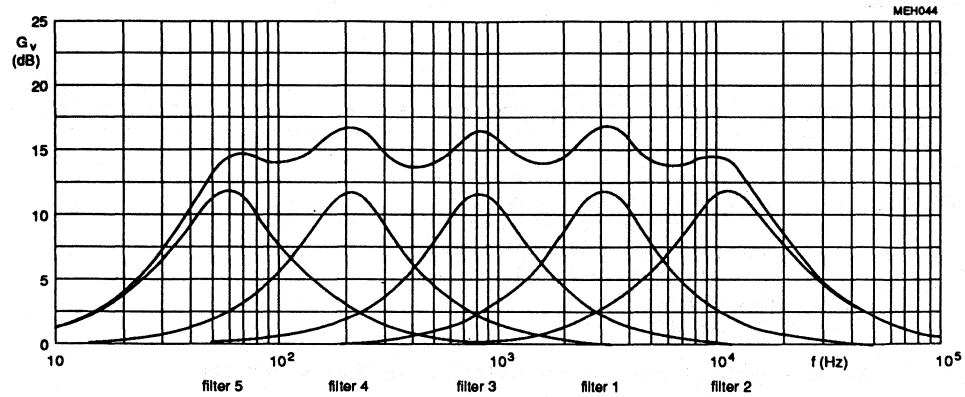


Fig.3 Frequency response for maximum boost of +12 dB according to Fig.1. For maximum cut the curves are symmetrical to negative gain values.

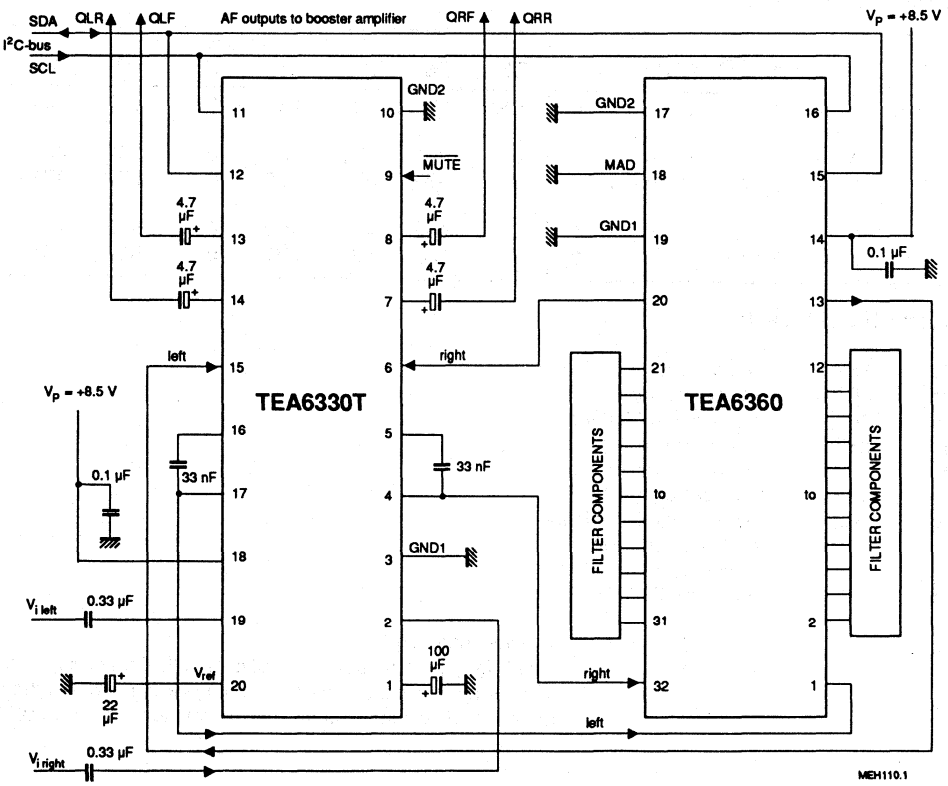


Fig.4 Application for car radio (V_P <8.5 V).

I²C-BUS PROTOCOL

I²C-bus format

S	SLAVE ADDRESS	A	SUBADDRESS	A	DATA	P

S = start condition
SLAVE ADDRESS = **1000 0100** when pin 18 is set LOW
or **1000 0110** when pin 18 is set HIGH or open-circuit
A = acknowledge, generated by the slave
SUBADDRESS = subadress byte, see Table 1
DATA = data byte, see Table 1
P = stop condition

If more than 1 byte DATA are transmitted, then auto-increment of the subaddress is performed.

Byte organisation

Table 1 I²C-bus transmission.

function	subaddress byte								data byte							
									D7	D6	D5	D4	D3	D2	D1	D0
filter 1 /defeat	0	0	0	0	0	0	0	0	DEF	1B2	1B1	1B0	0	1C2	1C1	1C0
filter 2	0	0	0	0	0	0	0	1	0	2B2	2B1	2B0	0	2C2	2C1	2C0
filter 3	0	0	0	0	0	0	1	0	0	3B2	3B1	3B0	0	3C2	3C1	3C0
filter 4	0	0	0	0	0	0	1	1	0	4B2	4B1	4B0	0	4C2	4C1	4C0
filter 5	0	0	0	0	0	1	0	0	0	5B2	5B1	5B0	0	5C2	5C1	5C0

Function of the bits of Table 1:

1B0 to 1B2 boost control for filter 1
1B0 to 1B2 cut control for filter 1
2B0 to 2B2 boost control for filter 2
2B0 to 2B2 cut control for filter 2
3B0 to 3B2 boost control for filter 3
3B0 to 3B2 cut control for filter 3
4B0 to 4B2 boost control for filter 4
4B0 to 4B2 cut control for filter 4
5B0 to 5B2 boost control for filter 5
5B0 to 5B2 cut control for filter 5

DEF
DEF = 0 (defeat bit): All filters operating.
DEF = 1 : Linear frequency response, input is directly connected to the output of the output amplifier. The filter settings are stored but the internal amplification is controlled to 0 dB, independent on bits nB2 to nB0.

Table 2 Boost control for filter n

DATA				
position		nB2	nB1	nB0
step 0	(no boost)	0	0	0
step 1		0	0	1
step 2		0	1	0
step 3		0	1	1
step 4		1	0	0
step 5	(maximum boost)	1	0	1
step 5	(maximum boost)	1	1	0
step 5	(maximum boost)	1	1	1

Table 3 Cut control for filter n

DATA				
position		nB2	nB1	nB0
step 0	(no cut)	0	0	0
step 1		0	0	1
step 2		0	1	0
step 3		0	1	1
step 4		1	0	0
step 5	(maximum cut)	1	0	1
step 5	(maximum cut)	1	1	0
step 5	(maximum cut)	1	1	1

Table 4 Filter control with variable quality factor

position	D7 X	D6 nB2	D5 nB1	D4 nB0	D3 X	D2 nC2	D1 nC1	D0 nC0	comment
+5 (maximum boost)	0	1	0	1	0	0	0	0	(+5) + (−0) = +5
+4	0	1	0	0	0	0	0	0	(+4) + (−0) = +4
+3	0	0	1	1	0	0	0	0	(+3) + (−0) = +3
+2	0	0	1	0	0	0	0	0	(+2) + (−0) = +2
+1	0	0	0	1	0	0	0	0	(+1) + (−0) = +1
0 (linear)	0	0	0	0	0	0	0	0	(+0) + (−0) = 0
−1	0	0	0	0	0	0	0	1	(+0) + (−1) = −1
−2	0	0	0	0	0	0	1	0	(+0) + (−2) = −2
−3	0	0	0	0	0	0	1	1	(+0) + (−3) = −3
−4	0	0	0	0	0	1	0	0	(+0) + (−4) = −4
−5 (maximum cut)	0	0	0	0	0	1	0	1	(+0) + (−5) = −5

Table 5 Filter control with constant quality factor

position	D7 X	D6 nB2	D5 nB1	D4 nB0	D3 X	D2 nC2	D1 nC1	D0 nC0	comment
+5 (maximum boost)	0	1	0	1	0	0	0	0	(+5) + (–0) = +5
+4	0	1	0	1	0	0	0	1	(+5) + (–1) = +4
+3	0	1	0	1	0	0	1	0	(+5) + (–2) = +3
+2	0	1	0	1	0	0	1	1	(+5) + (–3) = +2
+1	0	1	0	1	0	1	0	0	(+5) + (–4) = +1
0 (linear)	0	0	0	0	0	0	0	0	(+0) + (–0) = 0
–1	0	1	0	0	0	1	0	1	(+4) + (–5) = –1
–2	0	0	1	1	0	1	0	1	(+3) + (–5) = –2
–3	0	0	1	0	0	1	0	1	(+2) + (–5) = –3
–4	0	0	0	1	0	1	0	1	(+1) + (–5) = –4
–5 (maximum cut)	0	0	0	0	0	1	0	1	(+0) + (–5) = –5

Table 6 Filter control with quasi-constant quality factor

position	D7 X	D6 nB2	D5 nB1	D4 nB0	D3 X	D2 nC2	D1 nC1	D0 nC0	comment
+5 (maximum boost)	0	1	0	1	0	0	0	0	(+5) + (–0) = +5
+4	0	1	0	1	0	0	0	1	(+5) + (–1) = +4
+3	0	1	0	1	0	0	1	0	(+5) + (–2) = +3
+2	0	1	0	0	0	0	1	0	(+4) + (–2) = +2
+1	0	0	1	1	0	0	1	0	(+3) + (–2) = +1
0 (linear)	0	0	0	0	0	0	0	0	(+0) + (–0) = 0
–1	0	0	1	0	0	0	1	1	(+2) + (–3) = –1
–2	0	0	1	0	0	1	0	0	(+2) + (–4) = –2
–3	0	0	1	0	0	1	0	1	(+2) + (–5) = –3
–4	0	0	0	1	0	1	0	1	(+1) + (–5) = –4
–5 (maximum cut)	0	0	0	0	0	1	0	1	(+0) + (–5) = –5

Front-end and PLL synthesizer for car radios

TEA6810V; TEA6811V

FEATURES

- Synthesizer function which includes a voltage controlled oscillator (VCO), dividers, phase detector, charge-pump and in-lock detector
- FM mixer with AGC
- AM RF amplifier with AGC
- AM mixer.

APPLICATIONS

- Car radios.

GENERAL DESCRIPTION

The TEA6810V; TEA6811V, together with TEA6821V forms an AM/FM receiving concept for electronically tuned car radios.

The TEA6810V; TEA6811V is an FM/AM front-end with one local synthesized oscillator for both AM and FM which is used together with the TEA6821V in a double-conversion concept. It delivers a first FM-IF of 72.2 MHz and, for MW/LW, a first AM-IF of 10.7 MHz. Minimum alignments are required due to wideband RF inputs and the common AM/FM VCO.

High dynamic behaviour and minimum distortion is obtained by a special RF input design combined with AGC. High sensitivity is possible in combination with RF input FETs.

Minimum interference is experienced due a to special synthesizer loop design and ensuring that the I²C-bus is inoperative in the locked-tuned condition.
The reference frequency for the synthesizer and the I²C-bus information is delivered by the TEA6821V.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CCA1}	analog supply voltage (pin 2)		4.75	5.0	5.25	V
V_{CCA2}	analog supply voltage (pin 13)		8.1	8.5	8.9	V
V_{AMant}	AM AGC range	see Fig.3	0.3	–	6.0	V
V_{FMant}	FM AGC range	see Fig.4	10	–	600	mV
f_{AMant}	AM input frequency		0.144	–	22	MHz
f_{FMant}	FM input frequency		60	–	108	MHz
T_{amb}	operating ambient temperature		–40	–	+85	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TEA6810V	VSO40	plastic very small outline package; 40 leads	SOT158-1
TEA6811V	VSO40	plastic very small outline package; 40 leads; face down	SOT158-2

BLOCK DIAGRAM

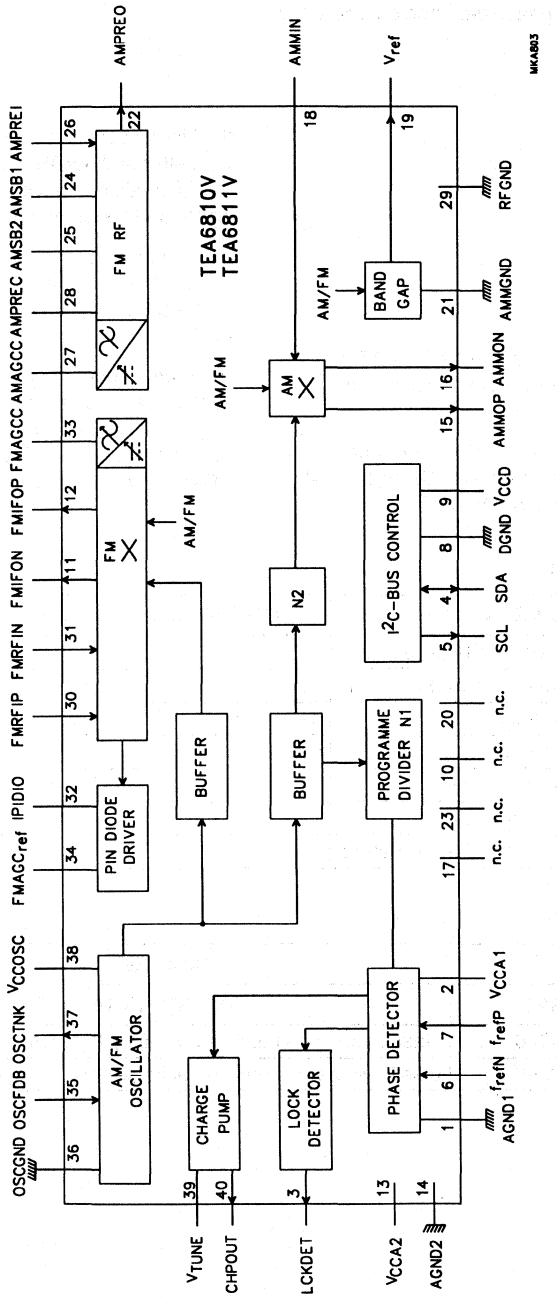


Fig.1 Block diagram.

PINNING

SYMBOL	PIN[1]		DESCRIPTION
	TEA6810	TEA6811	
AGND1	1	1	analog ground 1
V_{CCA1}	2	2	analog supply voltage 1 (+5 V)
LCKDET	3	3	lock detector flag
SDA	4	4	serial data input/output; I^2C-bus
SCL	5	5	serial clock input; I^2C-bus
f_{refN}	6	6	reference frequency input from TEA6821 N-terminal
f_{refP}	7	7	reference frequency input from TEA6821 P-terminal
DGND	8	8	digital ground
V_{CCD}	9	9	digital supply voltage (+5 V)
n.c.	10	10	not connected
FMIFON	11	11	FM mixer negative output (72.2 MHz)
FMIFOP	12	12	FM mixer positive output (72.2 MHz)
V_{CCA2}	13	13	analog supply voltage 2 (+8.5 V)
AGND2	14	14	analog ground 2
AMMOP	15	15	AM mixer positive output (10.7 MHz)
AMMON	16	16	AM mixer negative output (10.7 MHz)
n.c.	17	17	not connected
AMMIN	18	18	AM mixer RF input
V_{ref}	19	19	reference voltage output from AM bandgap
n.c.	20	20	not connected
AMMGND	21	21	AM mixer ground
AMPREO	22	22	AM preamplifier output
n.c.	23	23	not connected
AMSB1	24	24	AM feedback switch SB1
AMSB2	25	25	AM feedback switch SB2
AMPREI	26	26	AM preamplifier input
AMAGCC	27	27	AM AGC capacitor
AMPREC	28	28	AM preamplifier decoupling capacitor
RFGND	29	29	RF ground
FMRFIP	30	30	RF positive input for FM mixer
FMRFIN	31	31	RF negative input for FM mixer
IPIDIO	32	32	pin diode drive
FMAGCC	33	33	FM AGC integrating capacitor
$FMAGC_{ref}$	34	34	FM AGC reference voltage
OSCFDB	35	35	oscillator feedback input
OSCGND	36	36	oscillator ground
OSCTNK	37	37	oscillator tank output

SYMBOL	PIN[1]		DESCRIPTION
	TEA6810	TEA6811	
V_{CCOSC}	38	38	oscillator supply voltage (+8.5 V)
V_{TUNE}	39	39	tuning voltage
CHPOUT	40	40	charge pump output

Note

1. Pins 10, 17, 20 and 23 should be connected to a common ground.

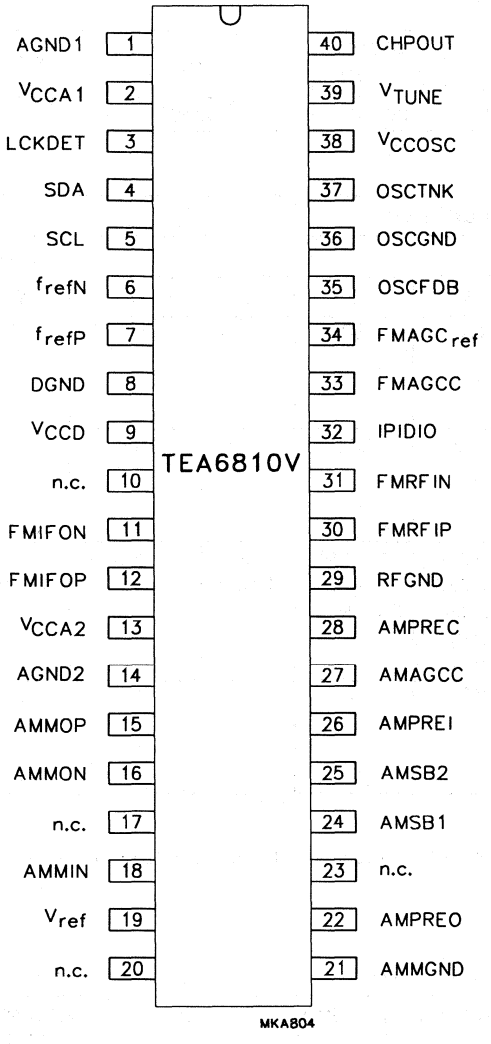


Fig.2 Pin configuration (TEA6810).

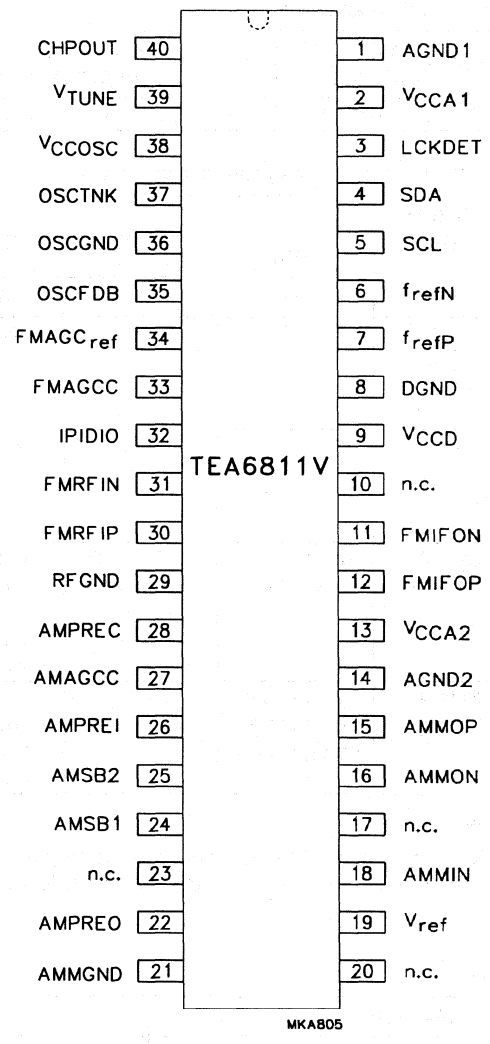


Fig.3 Pin configuration (TEA6811).

I²C-BUS ORGANIZATION

The TEA6810V; TEA6811V is controlled via the I²C-bus which is driven from the TEA6821V. For programming purposes a module address and four data bytes are required. When used partially, the transmission must be ended by a stop condition.

Table 1 Bit organization.

START	MODULE ADDRESS	PROGRAMMABLE DIVIDER DATA					SWITCH CONTROL	TEST			STOP
S	byte 0	A	byte 1	A	byte 2	A	byte 3	A	byte 4	A	P

Table 2 I²C-bus address and received bytes.

BYTES TO BE RECEIVED (4 BYTES)	BUS ADDRESS							
	MSB							LSB
	1	1	0	0	0	1	0	0
Byte 1[1] program divider N1 (Low byte)	S7	S6	S5	S4	S3	S2	S1	S0
Byte 2[1] program divider N1 (High byte)	S15	S14	S13	S12	S11	S10	S9	S8
Byte 3 switching	MSB in-lock counter	LSB in-lock counter	1 = HIGH 0 = LOW current tuning oscillator	1 = HIGH 0 = LOW current charge pump	1 = FM local 0 = FM dx	MSB divider N2	LSB divider N2	1 = FM 0 = AM
Byte 4 testing	1 = 3-state 0 = normal charge pump	1 = f_{div} 0 = LCKDET	1 = test 0 = normal in-lock counter	X[2]	X	X	X	X

Notes

1. N1 divider ratio is (N + 2); where N is the programmed binary number composed of bytes 1 and 2. For the minimum ratio; if N < 2048 then N1 divider ratio is {2048 + (N – 2)}.
2. X = don't care.

Table 3 N2 divider.

N2 DIVIDER	MSB	LSB
3	0	0
5	0	1
10	1	0
15	1	1

Table 4 In-lock.

IN-LOCK	MSB	LSB	AM/FM
8	0	0	FM
16	1	0	AM or FM
32	1	1	AM or FM
48	0	0	AM
64	0	1	AM

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CCA1}	analog supply voltage (pin 2)		−0.3	12	V
V_{CCA2}	analog supply voltage (pin 13)		−0.3	12	V
V_{CCD}	digital supply voltage (pin 9)		−0.3	12	V
V_{CCOSC}	oscillator supply voltage (pin 38)		−0.3	12	V
P_{tot}	maximum power dissipation		–	0.55	W
T_{stg}	storage temperature		−65	+150	°C
V_{es}	electrostatic handling	note 1	−300	+300	V

Note

1. Machine model: equivalent to discharging a 200 pF capacitor through 0 Ω.

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air	90	K/W

DC CHARACTERISTICS

$V_{13} = V_{38} = 8.5$ V; $V_9 = V_2 = 5.0$ V; $T_{amb} = 25$ °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
I_{CCA1}	analog input current (pin 2)	AM mode	7	9	mA
		FM mode	6	8	mA
I_{CCA2}	analog input current (pin 13)	AM mode	17	22	mA
		FM mode	15	18	mA
I_{CCOSC}	oscillator input current (pin 38)	AM mode	4	6	mA
		FM mode	6	8	mA
I_{CCD}	digital input current (pin 9)	AM mode	32	35	mA
		FM mode	27	30	mA
I_{AMMO}	AM mixer output current (pins 15 and 16)	AM mode	8.5	–	mA
		FM mode	0	–	mA
I_{FMIFO}	FM mixer output current (pins 11 and 12)	AM mode	0	–	mA
		FM mode	10	–	mA

AC CHARACTERISTICS

All voltage and current values are RMS values; noise values are unweighted within the bandwidth 0.03 to 20 kHz; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
AM signal channel; (note 1; see Fig.4)						
RF PREAMPLIFIER STAGE						
Z_{21}	transimpedance		40	65	–	kΩ
AGC STAGE; f_{i2} = 1 MHz						
V_{i2}	HF input voltage	AGC start level 1	–	750	–	mV
		AGC start level 2	–	850	–	mV
		AGC stop level 1	–	145	–	mV
		AGC stop level 2	–	170	–	mV
$I_{AGCsink}$	AGC sink current	$V_{18} = V_{19} + 0.5$ V; $V_{27} = V_{19}$	–	1	–	µA
$I_{AGCsource}$	AGC source current	$V_{18} = V_{19} - 0.5$ V; $V_{27} = V_{19}$	–	2	–	mA
MIXER (f_o = 10.7 MHz)						
R_i	input resistance between pins 18 and 21		15[2]	20	–	kΩ
C_i	input capacitance between pins 18 and 21		–	5	–	pF
C_o	output capacitance between pins 15 and 16		–	–	5[2]	pF
G_{mC}	conversion transconductance (I_{15} to I_{16}/V_{18} to V_{19}		2.4	2.75	3.1	mS
ΔG_{mC}	variation in conversion transconductance		–	–0.005	–	mS/K
IP_3	third-order intermodulation		130[2]	137	–	dBµV
CP	–1 dB compression point		114[2]	120	–	dBµV
$V_{n(eq)}$	equivalent input noise voltage		–	9	–	nV/√Hz
OSCILLATOR/N2 DIVIDER						
R_{N2}	internal divider ratio (N2)	set by I²C-bus; see Table 3	–	15	–	
			–	10	–	
			–	5	–	
			–	3	–	
REFERENCE VOLTAGE (PIN 19)						
V_o	output reference voltage		–	2.75	–	V
Z_o	output impedance		–	40	–	Ω
$I_{o(max)}$	maximum output current		–	–	0.1	mA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
FM signal channel (note 3; see Fig.5)						
MIXER						
R_i	input resistance between pins 30 and 31		1.65[2]	2	–	kΩ
C_i	input capacitance between pins 30 and 31		3.4[2]	4	4.5[2]	pF
R_o	output resistance between pins 11 and 12		10	–	–	kΩ
C_o	output capacitance between pins 11 and 12		6.5[2]	8	9[2]	pF
G_m	transconductance	I_{11} to I_{12}/V_{30} to $V_{31} < V_{AGC1}$	5.5	6.3	6.9	mS
		I_{11} to I_{12}/V_{30} to $V_{31} < V_{AGC2}$	–	4.7	–	mS
		I_{11} to I_{12}/V_{30} to $V_{31} < V_{AGC3}$	–	2.3	–	mS
		I_{11} to I_{12}/V_{30} to $V_{31} > V_{AGC3}$	–	1.0	–	mS
$\Delta G_m T$	variation in transconductance with temperature	$<V_{AGC1}$	–	–0.015	–	mS/K
F	noise figure (both sidebands)	f_i = 72.2 MHz; PLL tuned	–	7[2]	–	dB
IP_3	third-order intermodulation		135[2]	139	–	dBμV
CP	–1 dB compression point		120[2]	127	–	dBμV
α_{IF1}	1st IF rejection		25[2]	30	–	dB
$V_{AGC(S)}$	AGC start voltage between pins 30 and 31	start level 1	4.8	6.2	7.8	mV
		start level 2	–	15	–	mV
		start level 3	–	39	–	mV
$V_{AGC(H)}$	AGC hysteresis voltage	hysteresis level 1	–	1	–	mV
		hysteresis level 2	–	2	–	mV
		hysteresis level 3	–	3	–	mV
R_{33}	FM AGC output resistance		–	5	–	kΩ
I_{pin}	pin diode current	V_{32} = 1.4 V	4	–	–	mA
V_{pin}	start level pin diode voltage between pins 30 and 31	I_o = 1 mA	–	57	–	mV
OSCILLATOR						
f_{osc}	oscillator frequency		116.8	–	207	MHz
$\Delta f_{osc}/\Delta T$	oscillator temperature dependence		–	–90	–	10^{-6}/K

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
SYNTHESIZER (SEE FIG.6)							
Reference frequency input (pins 6 and 7)							
$V_{ref(p-p)}$	reference frequency input voltage (V_6 to V_7) (peak-to-peak value)			–	0.4	–	V
t_{trans}	reference frequency transition time			–	–	50	ns
f_{ref}	input reference frequency for:	tuning step (kHz)	N2				
	FM	50	–	–	50	–	kHz
	AM standard SW1	5	10	–	50	–	kHz
	AM fullband MW (USA)	10	5	–	50	–	kHz
	FM	25	–	–	25	–	kHz
	AM fullband SW1	5	5	–	25	–	kHz
	AM standard MW/LW	1	15	–	15	–	kHz
	AM fullband MW/LW	3	5	–	15	–	kHz
	AM fullband SW2	5	3	–	15	–	kHz
	FM	10	–	–	10	–	kHz
	AM standard SW1	1	10	–	10	–	kHz
	AM fullband MW/LW	1	5	–	5	–	kHz
	AM fullband SW1	1	5	–	5	–	kHz
	AM fullband SW2	1	3	–	5	–	kHz
Phase detector/charge pump							
I_{OL}	LOW level output charge pump current	V_{40} = 4 V		120	175	215	µA
I_{OH}	HIGH level output charge pump current	V_{40} = 4 V		0.85	1	1.2	mA
V_{OL}	LOW level tuning voltage at charge pump LOW	$I_O = 0.5I_{charge}$; V_{13} = 8.5 V		0.2	–	8.25	V
V_{OH}	HIGH level tuning voltage at charge pump HIGH	$I_O = 0.5I_{charge}$; V_{13} = 8.5 V		0.4	–	8.0	V
I_{oz}	3-state output current	V_{40} = 4 V		–5	–	+5	nA
$\Delta f_{r(p-p)}$	residual FM frequency (peak-to-peak value)	B = 300 Hz to 20 kHz; $I_{charge} = I_{OL}$; f_i = 100 MHz		–	9	16	Hz
t_{lock}	lock time	FM = 88 to 108 MHz		–	2	–	ms
		FM = 108 to 88 MHz		–	2	–	ms
		AM = 510 to 1710 kHz		–	2	–	ms
		AM = 1710 to 510 kHz		–	2	–	ms

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
Programmable divider							
N_{min}	minimum programmable ratio			–	2050	–	
N_{max}	maximum programmable ratio			–	65537	–	
DR	divider ratio for:	tuning step (kHz)	N2				
	FM	50	–	2050	–	3604	
	FM	25	–	6388	–	7208	
	FM	10	–	15970	–	18020	
	FM	5	–	31940	–	36040	
	AM standard MW/LW	1	15	10844	–	12420	
	AM standard SW1	5	10	3320	–	4140	
	AM standard SW1	1	10	16600	–	20700	
	AM fullband MW/LW	3	5	10448	–	10973	
	AM fullband MW/LW	1	5	31344	–	32920	
	AM fullband SW1	5	5	6700	–	8240	
	AM fullband SW1	1	5	33500	–	41200	
	AM fullband SW2	5	3	8240	–	10640	
	AM fullband SW2	1	3	41200	–	53200	
	AM fullband MW (USA)	10	5	3172	–	3292	
In-lock detector (reset by any start condition on I^2C-bus)							
V_{OH}	in-lock HIGH level output voltage (pin 3)			4.0	–	5.0	V
V_{OL}	in-lock LOW level output voltage (pin 3)			0	–	0.4	V
t_d	in-lock delay	counter length = N		–	$N \times 1/f_{ref}$	–	ms

Notes

1. f_{i1} = 1053 kHz; f_{mod} = 400 Hz; m = 0.3; $V_{i1} = V_{i2}$ = 1 mV; N2 divider switched to divide by 15.
2. Not measured 100% in production.
3. V_{i1} = 1 mV; f_{i1} = 98 MHz; f_{mod} = 1 kHz; $\Delta f = \pm 22.5$ kHz.

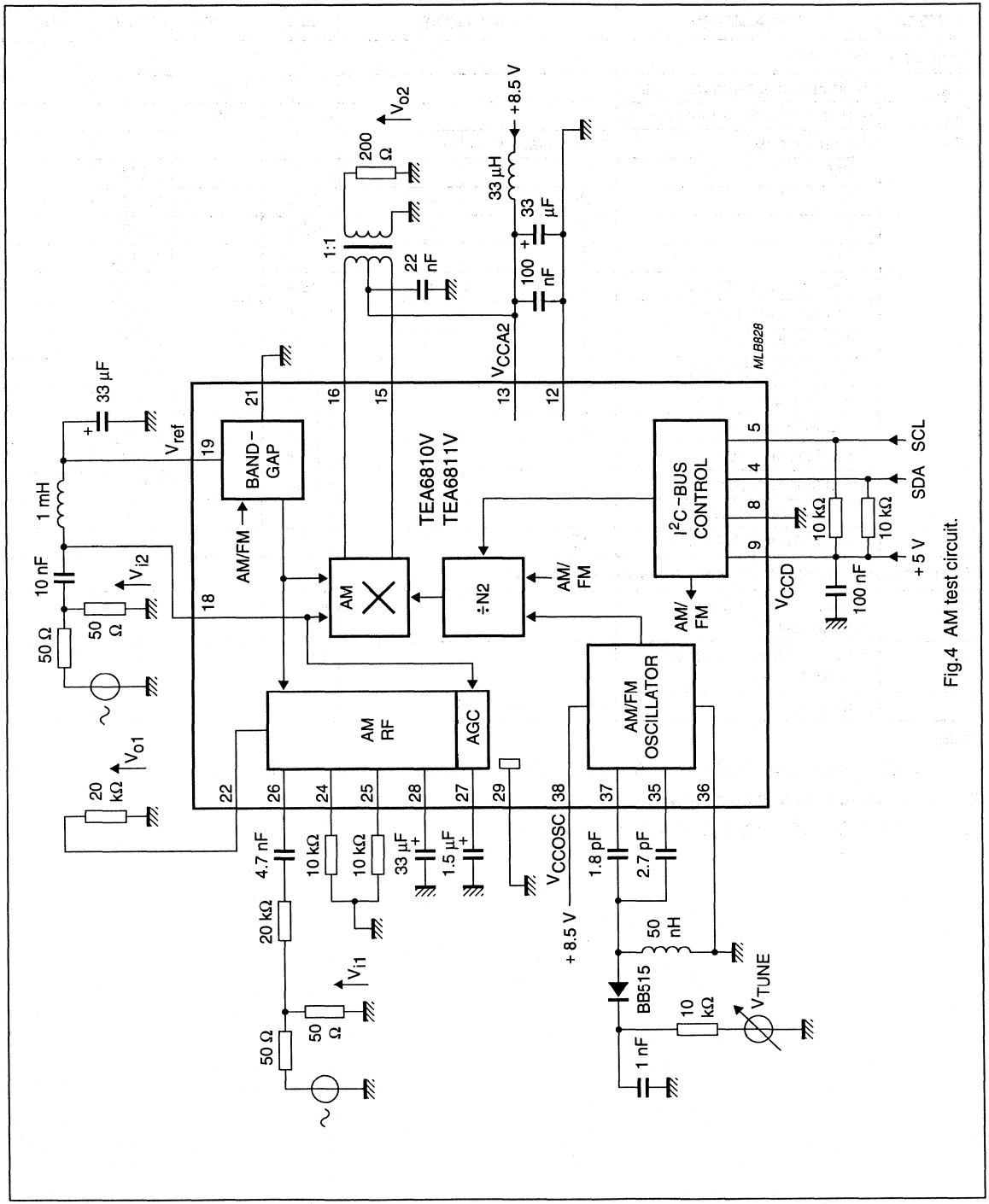


Fig.4 AM test circuit.

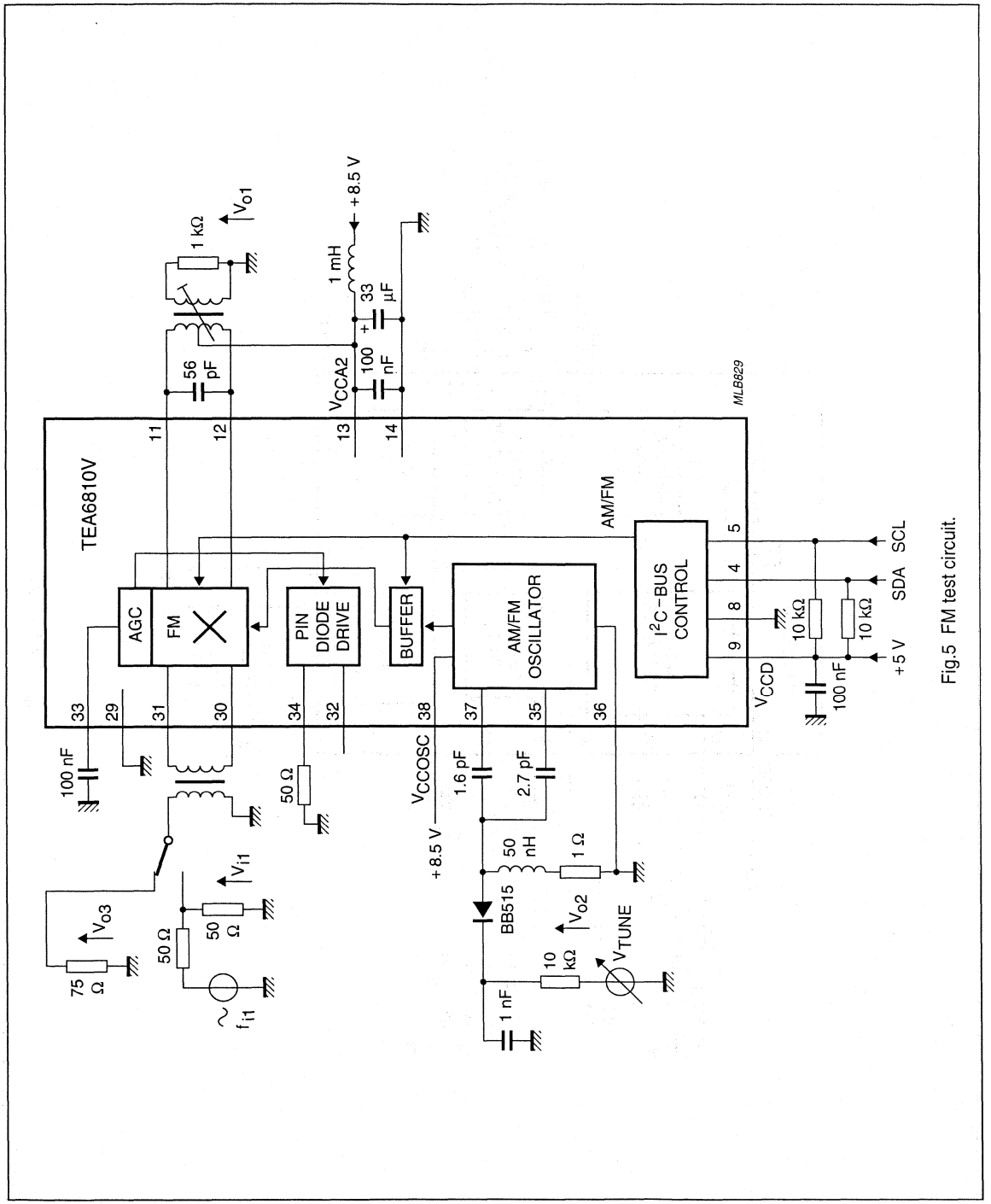


Fig.5 FM test circuit.

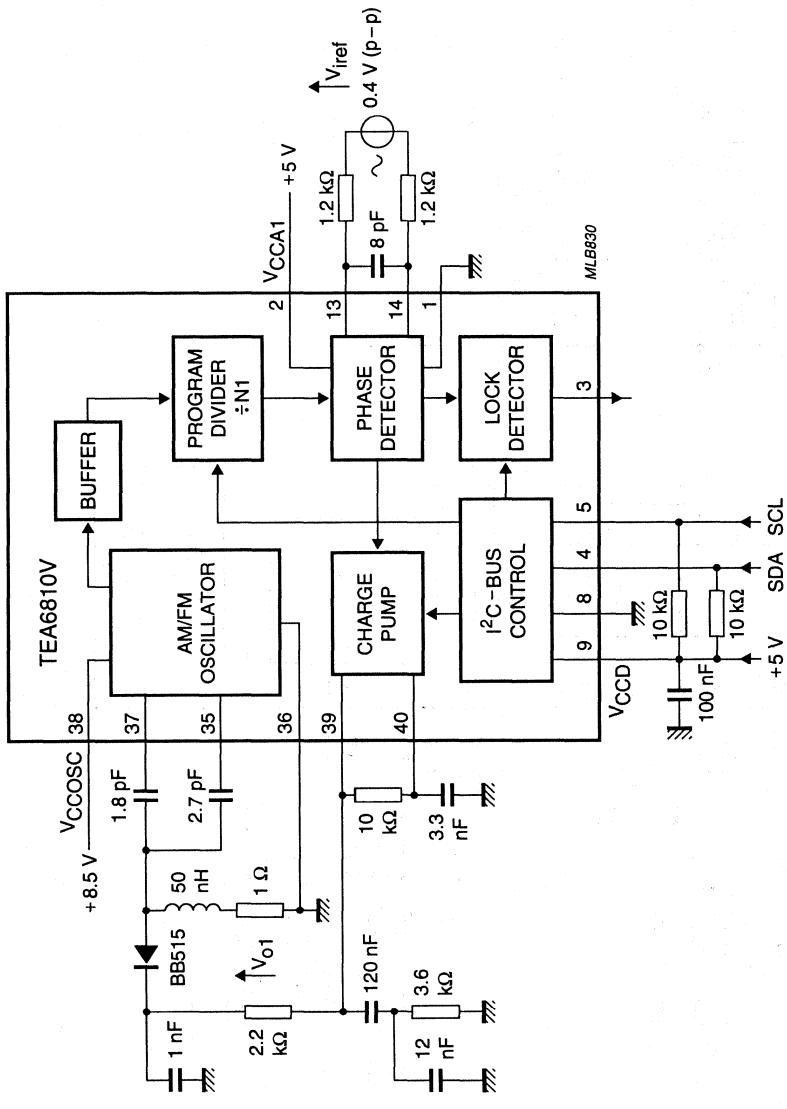


Fig.6 Synthesizer test circuit.

INTERNAL PIN CONFIGURATION

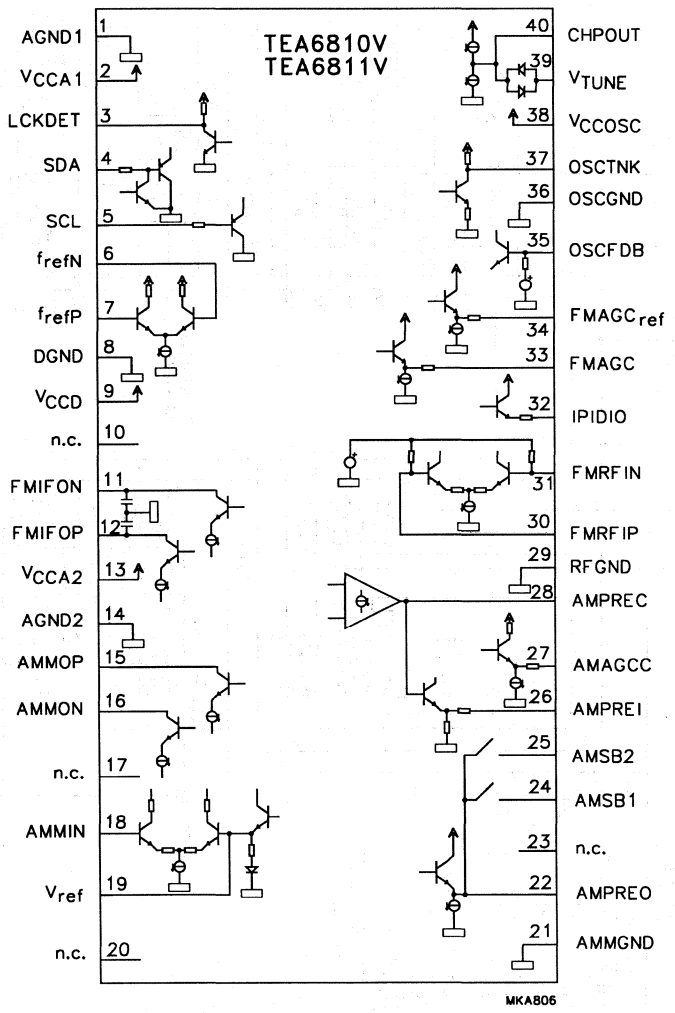


Fig.7 Internal pin configuration.

APPLICATION INFORMATION

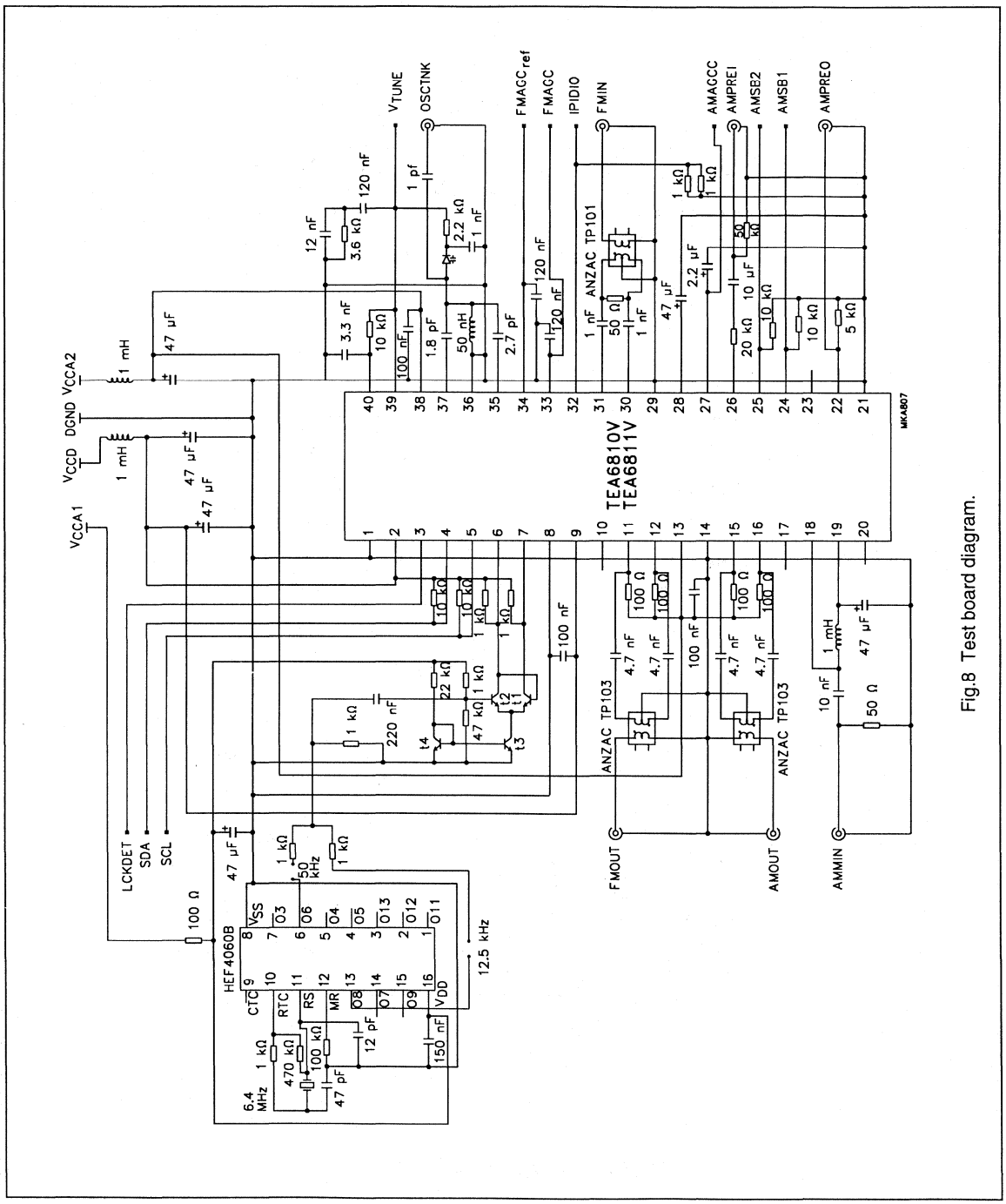


Fig.8 Test board diagram.

ICE car radio

TEA6821T

FEATURES

- FM mixer for conversion from FM IF_1 = 72.2 MHz to FM IF_2 = 10.7 MHz
- AM mixer for conversion from AM IF_1 = 10.7 MHz to AM IF_2 = 450 kHz
- FM IF gain stage
- Crystal oscillator providing mixer frequencies and references for IF count and stereo decoder
- FM quadrature demodulator with automatic centre frequency adjust and THD compensation
- Level and multipath and noise detectors
- Soft mute
- Stereo noise cancelling and variable de-emphasis
- PLL stereo decoder
- Noise blanker
- AM IF amplifier and demodulator
- I^2C-bus transceiver
- IF count for AM and FM
- Reference frequency generation for PLL synthesizer
- Reduced external components
- SW applicable.

GENERAL DESCRIPTION

The TEA6821T together with the TEA6810T / TEA6811T forms an AM/FM electronic tuned car radio in a double conversion receiver concept for European, American and Japanese frequency range.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{s1}	supply voltage 1 (pins 56 and 28)	note 1	7	8.5	10	V
V_{s1}	operating range		8.1	8.5	8.9	V
I_{s1}	supply current 1 FM		–	28	–	mA
I_{s1}	supply current 1 AM		–	24	–	mA
V_{s2}	supply voltage 2 (pin 5)	note 1	4.5	5.0	5.5	V
V_{s2}	operating range		4.75	5.0	5.25	V
I_{s2}	supply current 2 FM		–	31	–	mA
I_{s2}	supply current 2 AM		–	28	–	mA
S+N/N	signal-to-noise AM	m = 0.3	–	57	–	dB
THD	distortion AM		–	1	2	%
S+N/N	signal-to-noise FM	Δf = 22.5 kHz at pins 43 and 47	66	72	–	dB
THD	distortion FM	Δf = 75 kHz	–	0.1	0.35	%
α	channel separation (adjusted)		40	–	–	dB
T_{amb}	operating ambient temperature		–40	–	+85	°C

Note to the quick reference data

1. IC is functional, specifed parameters may deviate from limits which are valid for operating range.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TEA6821T	56	mini-pack	plastic	SOT190

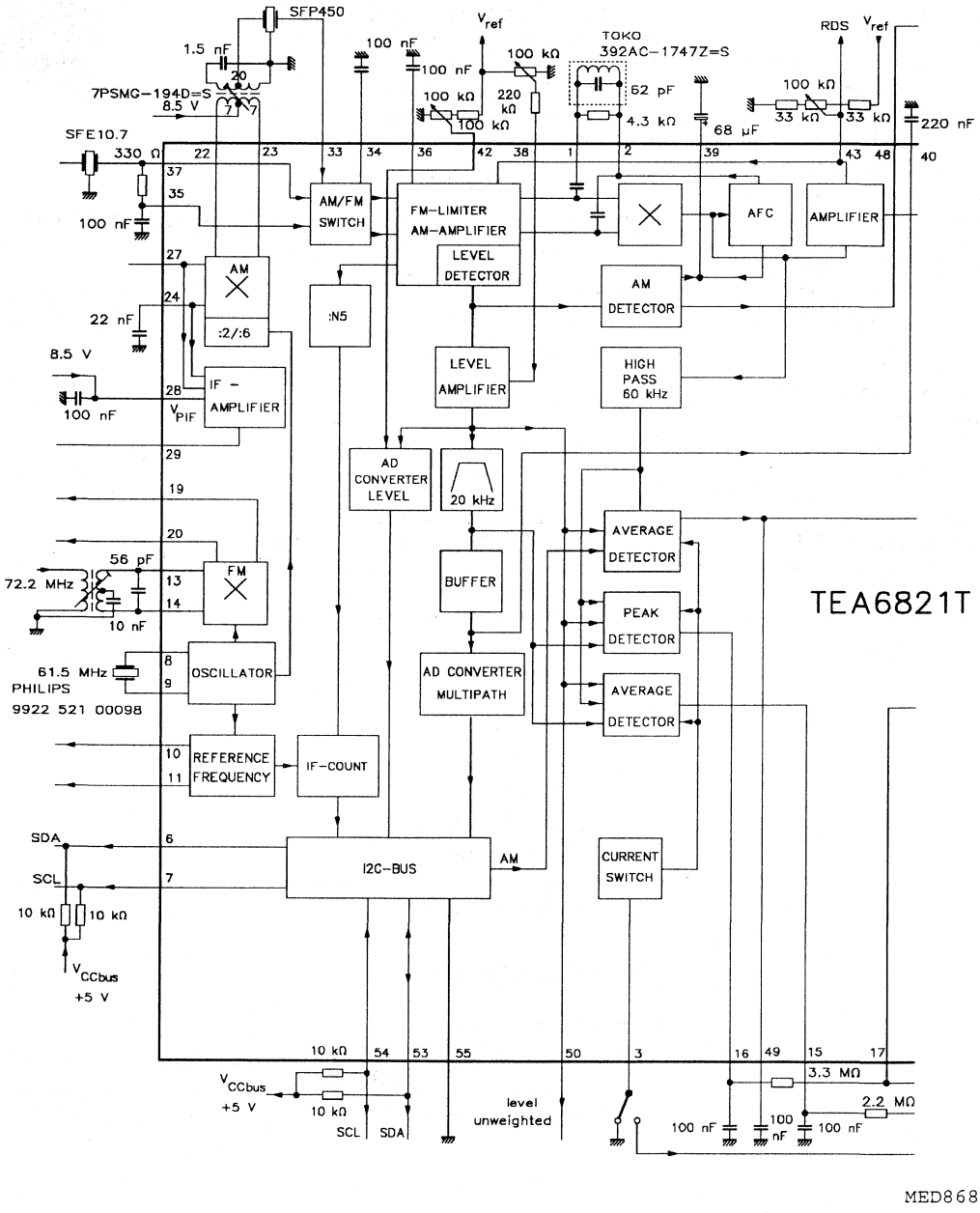


Fig.1 Block diagram (continued in Fig.2).

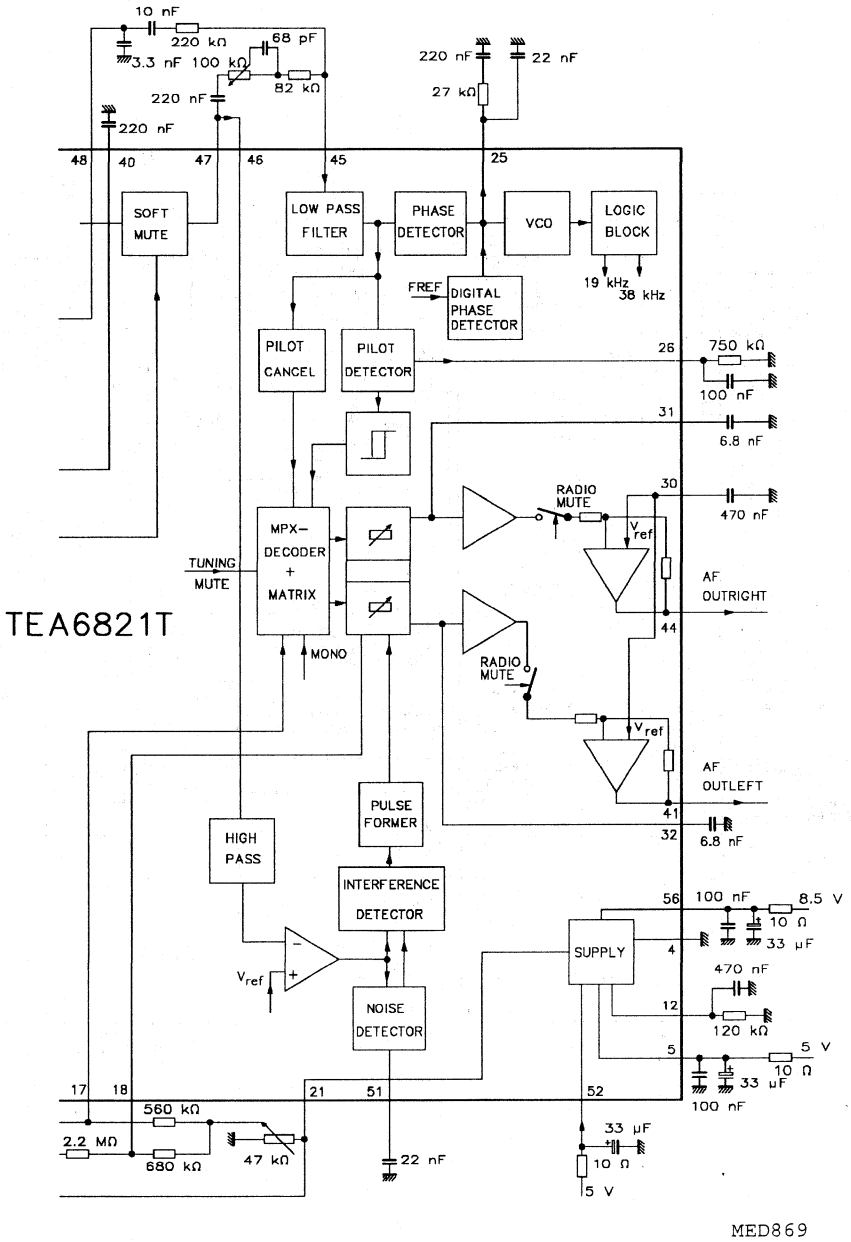


Fig.2 Block diagram (continued from Fig.1).

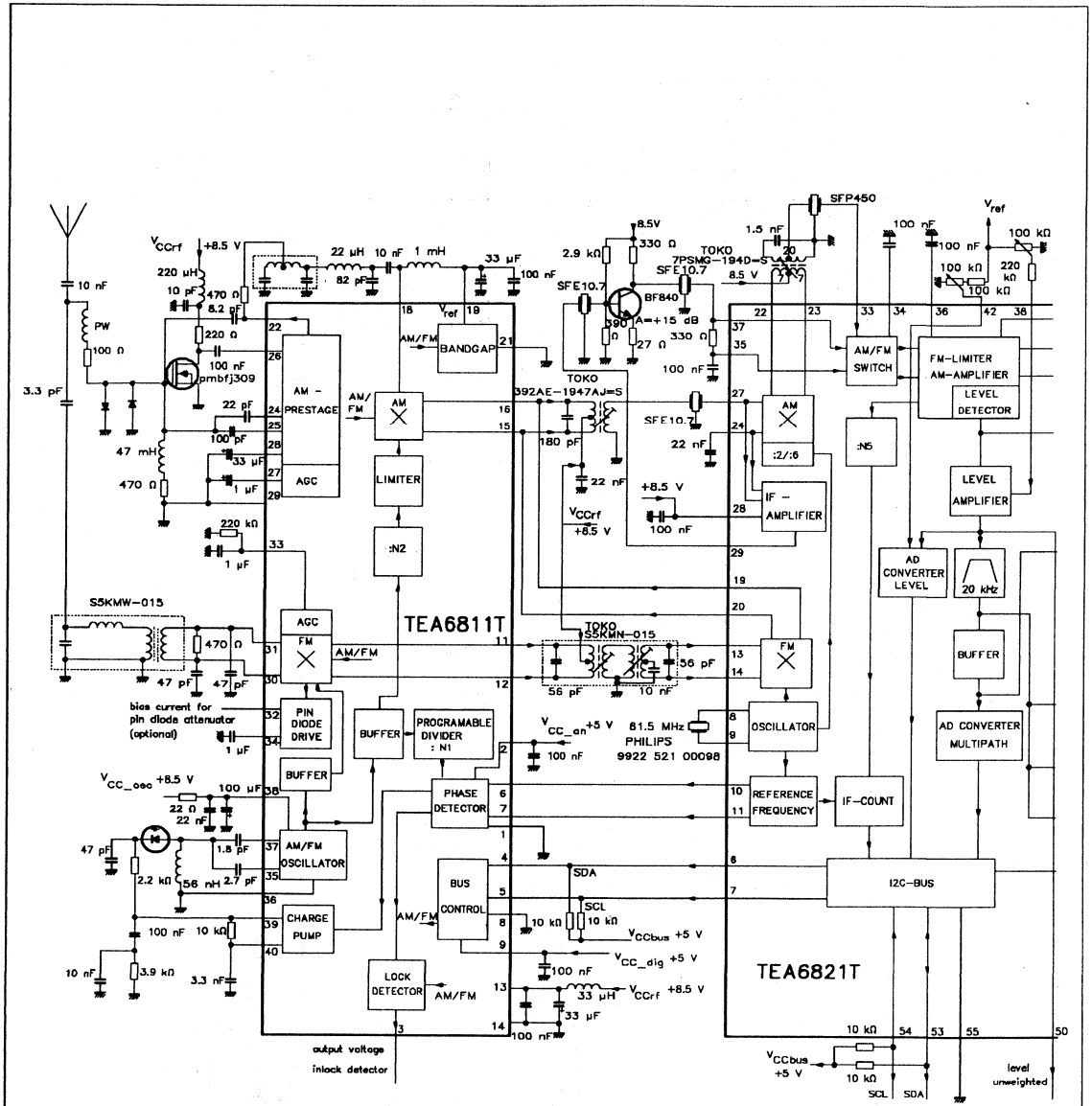


Fig.3 ICE91 application diagram (continued in Fig.4).

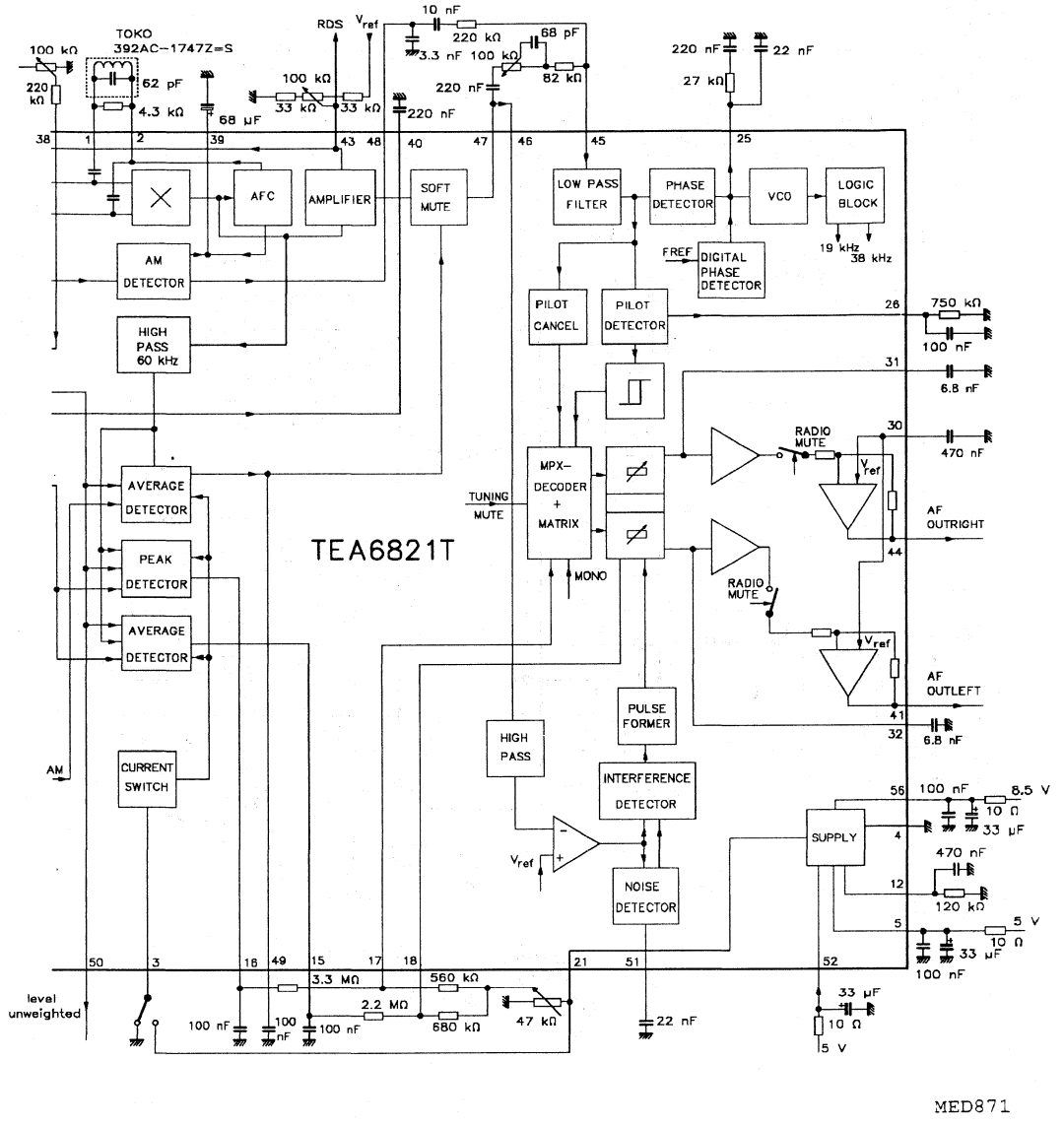


Fig.4 ICE91 application diagram (continued from Fig.3).

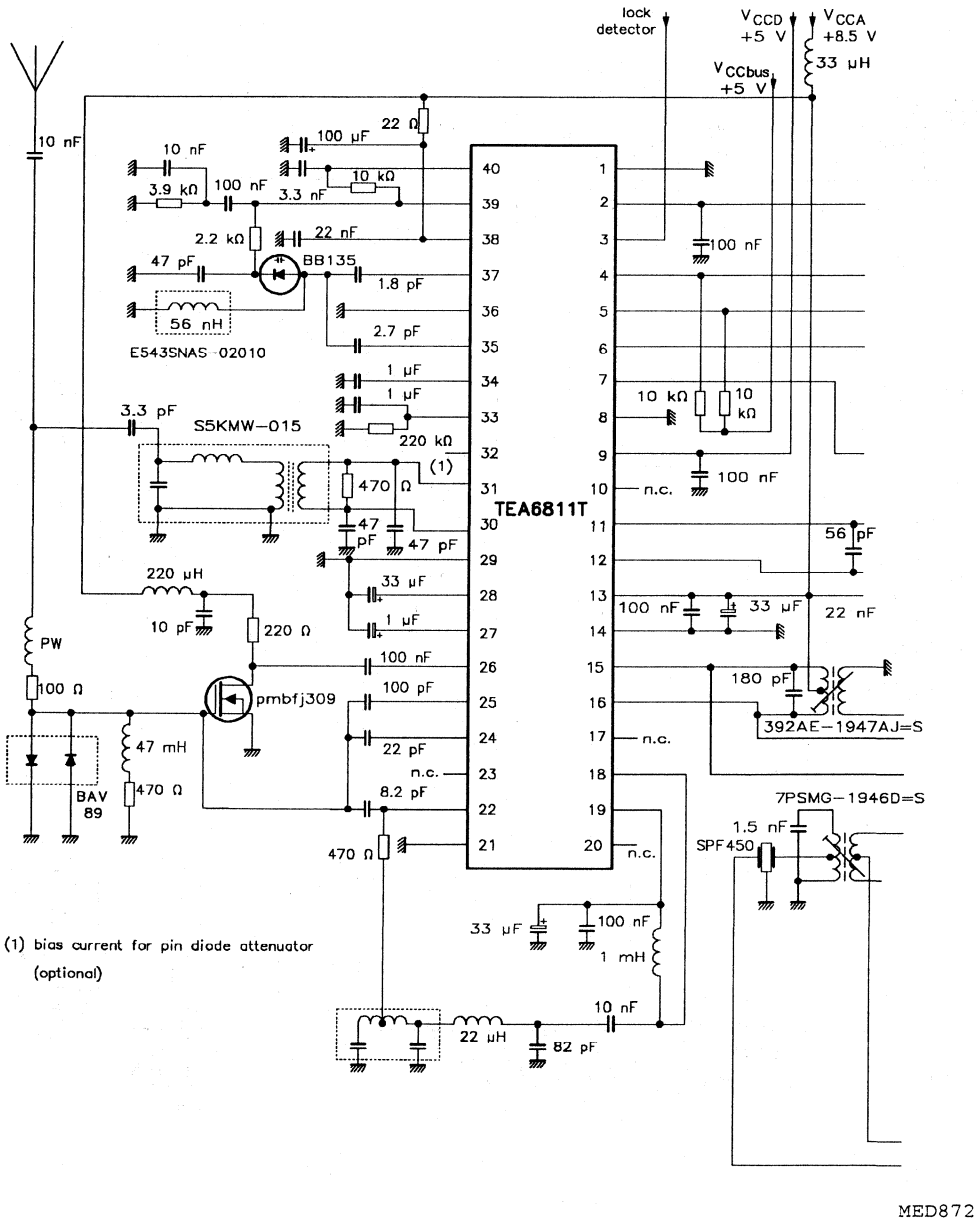


Fig.5 AM/FM car radio receiver with TEA6811T and TEA6821T (continued in Fig.6).

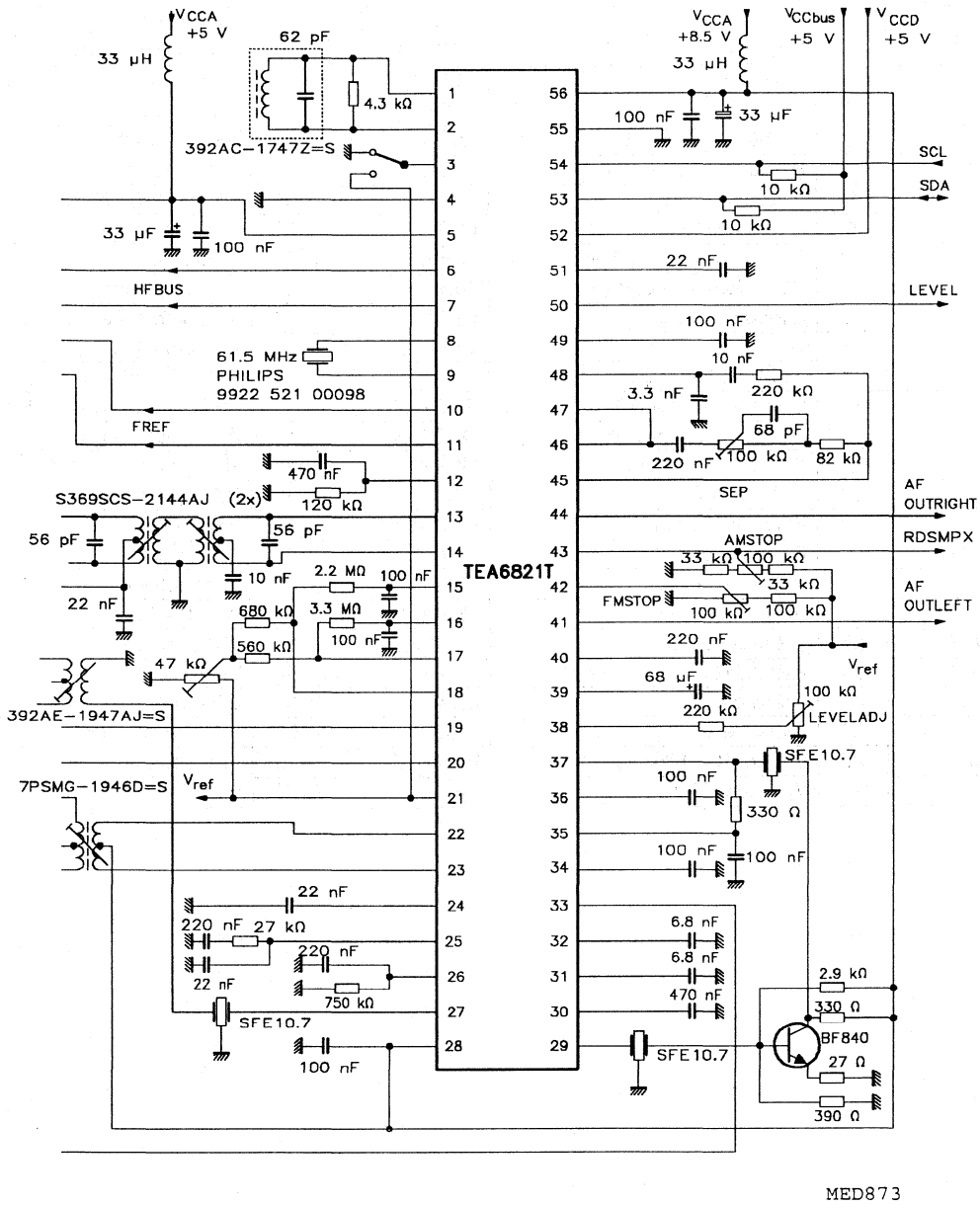


Fig.6 AM/FM car radio receiver with TEA6811T and TEA6821T (continued from Fig.5).

PINNING

SYMBOL	PIN	DESCRIPTION
QDET1	1	demodulator tank
QDET2	2	demodulator tank
TSWITCH	3	time switch
GND	4	analog ground
V_{P5}	5	5 V supply voltage
HFBUS1	6	HF bus, pull-up to 5 V
HFBUS2	7	HF bus, pull-up to 5 V
XTAL1	8	crystal oscillator
XTAL2	9	crystal oscillator
F_{REFP}	10	PLL reference frequency
F_{REFN}	11	PLL reference frequency
I_{REF}	12	reference current
FMIF1IN1	13	70 MHz FM-IF input
FMIF1IN2	14	70 MHz FM-IF input
TSDR	15	time constant for SDR
TSDS	16	time constant for SDS
V_{SDS}	17	SDS control voltage
V_{SDR}	18	SDR control voltage
FMIF2OUT1	19	FM mixer output
FMIF2OUT2	20	FM mixer output
V_{REF}	21	reference voltage
AMIF2OUT1	22	AM mixer output
AMIF2OUT2	23	AM mixer output
FMAMDEC	24	FM/AM 10.7 MHz decoupling
PHASEDET	25	phase detector
PILDET	26	pilot detector
FMAM10.7	27	FM/AM 10.7 MHz input
V_{PIF}	28	V_P IF amplifier

SYMBOL	PIN	DESCRIPTION
FMIFAMPOUT	29	FM-IF amplifier output
AFGND	30	AF ground
DEEMPHR	31	de-emphasis capacitor right
DEEMPHL	32	de-emphasis capacitor left
AMIF2IN1	33	AM IF2 input 1
AMIF2IN2	34	AM IF2 input 2
FMIN2	35	FM limiter input
DCFEED	36	DC feed FM limiter
FMIN1	37	FM limiter input
LEVELADJ	38	level adjust
C_{AFC}	39	AFC capacitor
MPBUF	40	multipath buffer time constant
OUTLEFT	41	AF output left
FMSTOP	42	FMSTOP adjust
RDS/AMSTOP	43	MPX for RDS/AMSTOP adjust
OUTRIGHT	44	AF output right
MPXIN	45	stereo decoder MPX input
IAC_{IN}	46	IAC input
MPXOUT	47	FM demodulator MPX output
AMAFOUT	48	AM demodulator AF output
V_{MUTAML}	49	mute voltage / AM level
LEVELUNWEIG	50	level unweighted
$I_{ACCONTR}$	51	IAC control voltage
V_{PDIG}	52	V_P digital
SDA	53	SDA, pull-up to 5 V
SCL	54	SCL, pull-up to 5 V
BUSGND	55	bus ground
$V_{P8.5}$	56	V_P 8.5 V

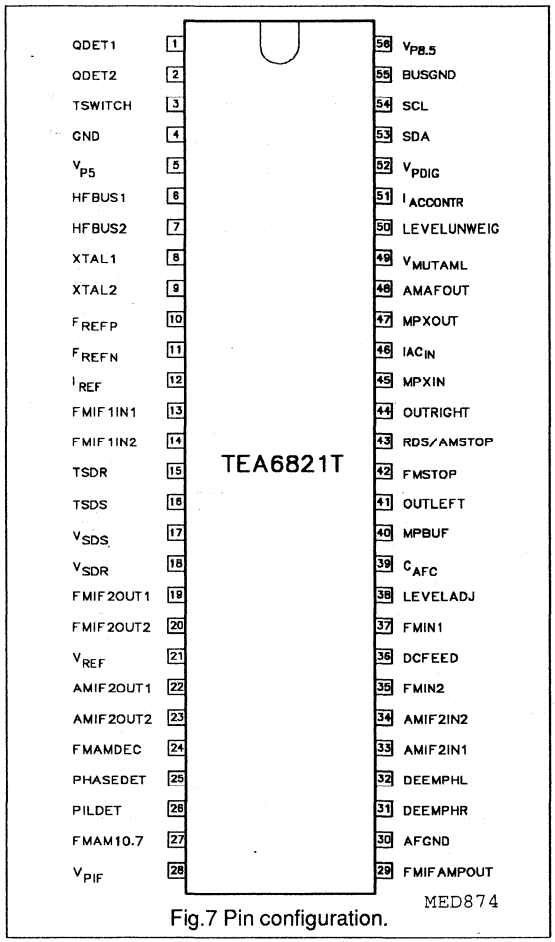


Fig.7 Pin configuration.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{s1}	supply voltage 1 (pins 56 and 28)	−0.3	+12	V
V_{s2}	supply voltage 2 (pin 5)	−0.3	+6.5	V
V_{s3}	supply voltage 3 (pin 52)	−0.3	+6.5	V
T_{stg}	storage temperature	−55	+150	°C
T_{amb}	operating ambient temperature	−40	+85	°C
V_{ESD}	electrostatic handling (note 1)			
	for pins 8 and 9	−	±100	V
	for other pins	−	±300	V

Note to the limiting values

1. Charge device model class B: discharging a 200 pF capacitor through a 0 Ω series resistor.

CHARACTERISTICS

$V_{56-4} = V_{28-4} = 8.5$ V, $V_{5-4} = V_{52-55} = 5$ V, $T_{amb} = +25$ °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Current consumption						
I_{s1}	supply current 1	FM	24	30	36	mA
I_{56}	supply current 1 at pin 56		16	20	24	mA
I_{28}	supply current 1 at pin 28		2.4	3.0	3.6	mA
$I_{19} + I_{20}$	supply current 1 at pins 19 and 20		4.8	6.0	7.2	mA
I_{s1}	supply current 1	AM	18	24	30	mA
I_{56}	supply current 1 at pin 56		9.5	12	15	mA
$I_{22} + I_{23}$	supply current 1 at pins 22 and 23		8	10	12.5	mA
I_{s2}	supply current 2 at pin 5	FM	18	21	25	mA
		AM	14	17	21	mA
I_{s3}	supply current 3 at pin 52		8	10	12	mA
FM IF path						
FM mixer						
R_{13-14}	input resistance		5	7	–	kΩ
C_{13-4}, C_{14-4}	input capacitance		–	3	4.5	pF
R_{opt}	optimum generator resistance		–	1.2	–	kΩ
R_{19-20}	output resistance		15	20	–	kΩ
C_{19-4}, C_{20-4}	output capacitance		–	5	7	pF
$I_{19IF2}/V_{13-14IF1}$	conversion gain		1.65	1.9	2.2	mS
I_{19}, I_{20}	mixer bias current		2.4	3.0	3.6	mA
	mixer leakage current	in AM position	–	–	2	µA
V_{19-20}	maximum output voltage (peak-to-peak value)		12.0	14.0	–	V
IP3	third order intermodulation		114	124	–	dBµV

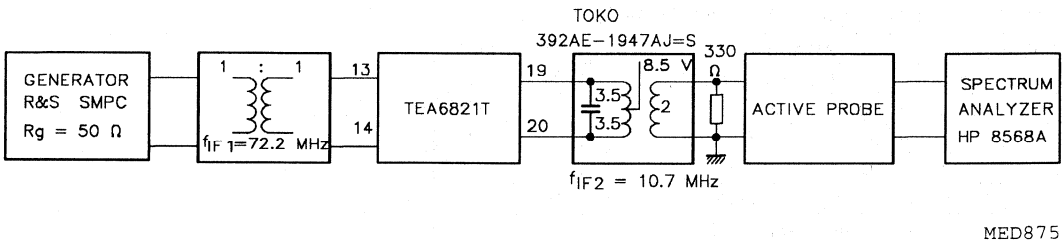


Fig.8 Test circuit FM mixer.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Oscillator						
f_{osc}	oscillator frequency		–	61.5	–	MHz
	oscillator spread		–	–	250	Hz
$\Delta f_{osc}/\Delta T$	temperature dependence of oscillator frequency	crystal type PHILIPS 9922 521 00098	–	30	–	ppm/K
R_1	crystal motional resistance		–	–	70	Ω
C_0	crystal shunt capacitance		–	–	5	pF
FM IF2 amplifier						
V_{29-4}/V_{27-24}	amplifier gain	loaded with 330 Ω; see Fig.9	8	10	12	dB
V_{27-24}	maximum input voltage for 1 dB compression point (RMS value)		80	110	–	mV
V_{29-4}	maximum output voltage (RMS value)		220	270	–	mV
R_{27-24}	input resistance		300	330	360	Ω
C_{27-4}, C_{24-4}	input capacitance		–	–	5	pF
R_{29-4}	output resistance		300	330	360	Ω
C_{29-4}	output capacitance		–	–	5	pF

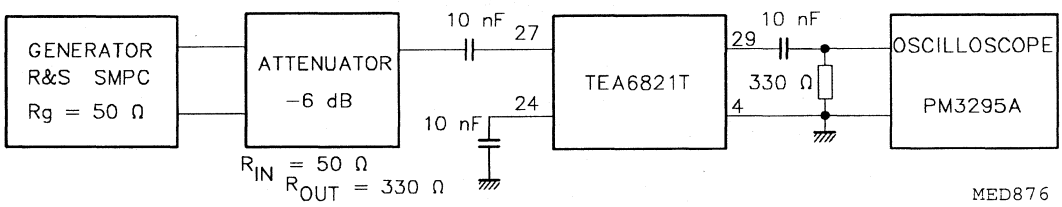


Fig.9 Test circuit IF amplifier.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
FM IF2 limiter						
V_{1-2}/V_{37-35}	limiter gain	see Fig.10	–	74	–	dB
C_{37-4}	input capacitance		–	–	5	pF
R_{1-2}	output resistance		–	–	1.0	kΩ
C_{1-2}	output capacitance		10	15	20	pF
V_{1-2}	limiter output voltage (peak-to-peak value)		500	700	–	mV

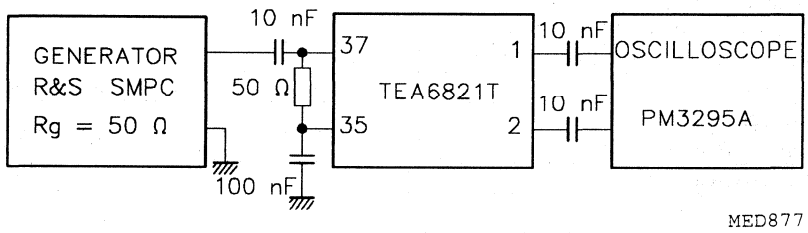


Fig.10 Test circuit limiter gain.

f_{mod} = 1 kHz; deviation = 22.5 kHz; R_g = 50 Ω; V_{37-35} = 10 mV; with de-emphasis = 50 μS; coil quality = 15 unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
FM demodulator						
V_{47-4}	MPX output (RMS value)		160	200	240	mV
R_{47out}	output resistance		–	–	500	Ω
B	AF bandwidth		200	–	–	kHz
V_{43-4}	MPX output for RDS (RMS value)		160	200	240	mV
R_{43out}	output resistance		–	–	500	Ω
B	AF bandwidth		200	–	–	kHz
V_{37-35}	start of limiting (RMS value)	α_{AF} = –3 dB	–	40	60	μV
V_{37-35}	intput voltage for signal-plus-noise-to-noise ratio (RMS value)	see Fig.11 for pin 47 (MPXOUT) and Fig.12 for pin 43 (RDS/AMSTOP)				
		S+N/N = 26 dB	–	40	55	μV
		S+N/N = 46 dB	–	100	140	μV
S+N/N	signal-plus-noise-to-noise ratio		66	72	–	dB
V_{43FM}/V_{43AM}	suppression	Δf = 22.5 kHz; f_{modAM} = 1 kHz; m_{AM} = 30%; V_{37-35} = 3 mV to 300 mV	55	60	–	dB
V_{47FM}/V_{47AM}	suppression	V_{37-35} = 1 mV to 300 mV	55	60	–	dB
THD	total harmonic distortion	detuning ≤ 50 kHz; Δf = 75 kHz; f_{mod} = 1 kHz without de-emphasis L_{demod} = typical value				
		pin 43 V_{37-35} = 300 μV to 800 mV	–	0.1	0.35	%
		pin 47 V_{37-35} = 1 mV to 800 mV	–	0.1	0.35	%
$\Delta V_{43AFCdisabled}/\Delta V_{43AFCactive}$	demodulator frequency control (AFC) efficiency at 100 kHz detune from exact tuning		30	34	–	dB
ΔV_{43}	residual DC-offset	ΔL_{demod} = typical value;				
		10 μV < V_{37-35} < 80 μV	–	100	1000	mV
		80 μV < V_{37-35} < 800 mV	–	10	30	mV

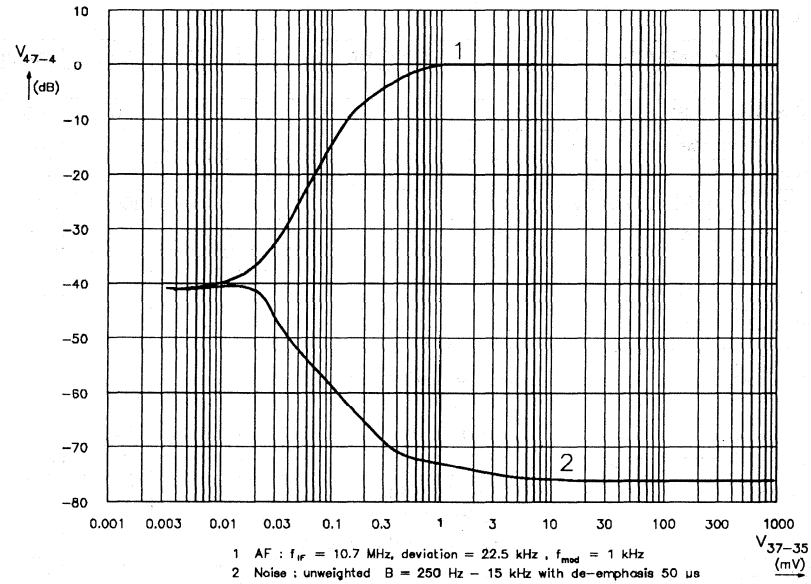


Fig.11 Signal and noise of muted MPX voltage.

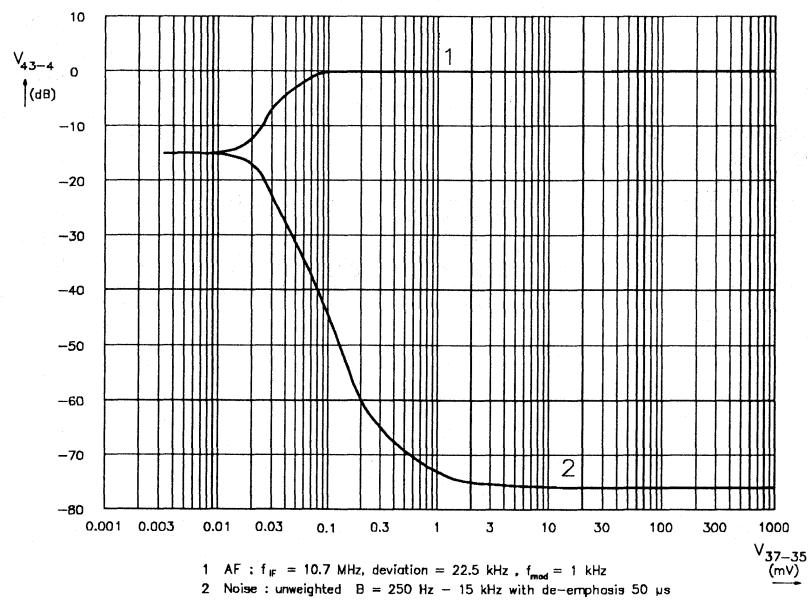


Fig.12 Signal and noise of unmuted MPX voltage.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Unweighted level voltage						
BW_{50}	bandwidth		500	–	–	kHz
R_{out50}	output resistance		–	–	100	Ω
V_{50-4}	level unweighted voltage	see Fig.13; V_{38} = 2.52 V;				
		$V_{37-35} \leq 2.5$ μV	1.8	2.4	3.2	V
		V_{37-35} = 1.0 mV	2.7	3.4	4.7	V
V/20 dB	slope of level unweighted voltage $\Delta V_{50-4}/\Delta V_{37-35}$	$V_{37-35} \leq 100$ μV (RMS) < 300 mV	0.75	0.845	0.95	V
$\Delta V_{50-4}/VK$	temperature dependence	V_{37-35} = 1 mV	–	4.0	–	mV/VK

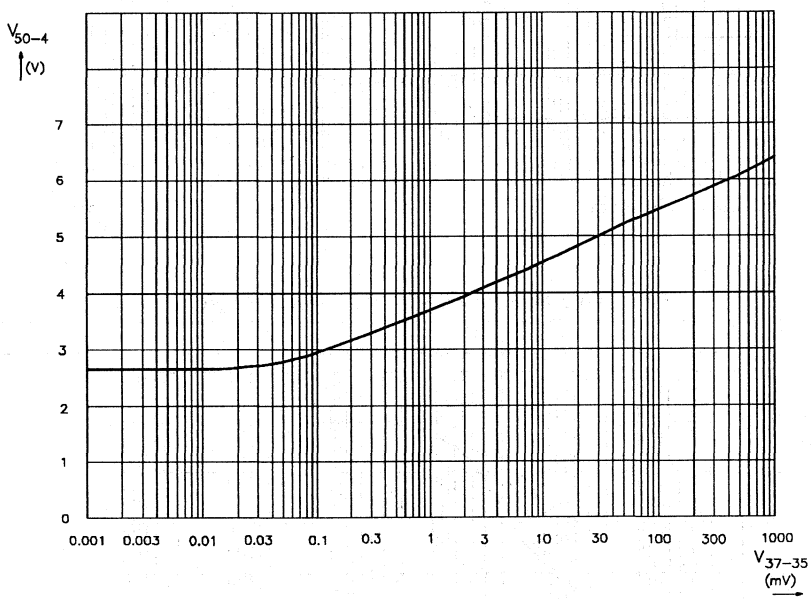


Fig.13 Level unweighted voltage (typical curve).

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Adjust of level unweighted voltage and V_{mutaml}; typical adjusting range see Figs 14 and 17						
ΔV_{50}	adjusting range	V_{37-35} = 1 mV (RMS)	–	±2	–	V
$\Delta V_{50-4}/\Delta V_{38-4}$	adjusting gain		–	–0.9	–	–
R_{38}	input resistance		–	80	–	kΩ
V_{38-4}	internal bias voltage		–	2.6	–	V
Muting dependence on adjust of level unweighted voltage; typical curve see Fig.15						
$\alpha = V_{43}/V_{47}$	start of mute	V_{49}/V_{21} = 0.6	–	3	–	–
$\Delta\alpha/\Delta V_{49}$	mute slope	α = –6 dB	–	25	–	dB/V

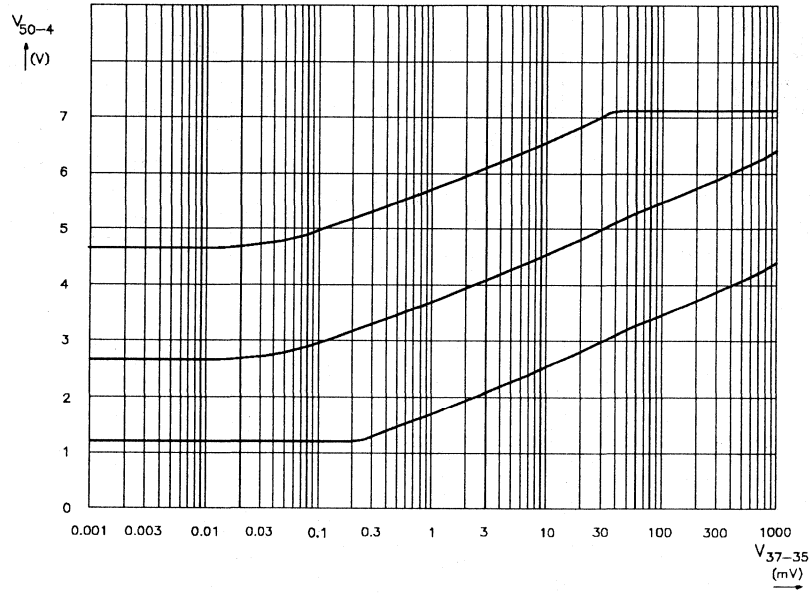


Fig.14 Adjustment range level unweighted voltage.

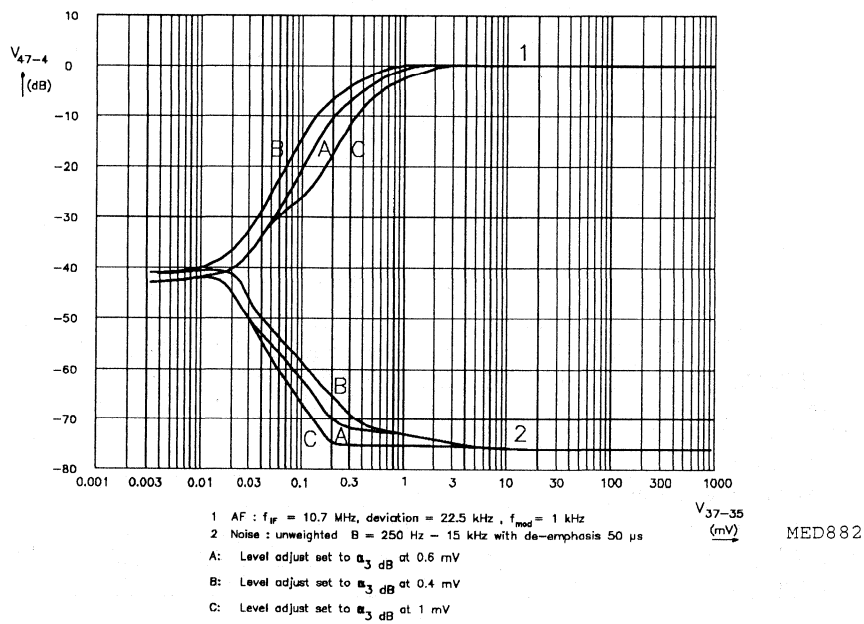


Fig.15 Muting dependence on adjust of level unweighted voltage (typical curve).

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Soft mute, time constant control, mono/stereo blend and high-cut control						
Time constant control (see application diagram Fig.3): Slow or fast attack and decay time constants for soft mute, mono/stereo and high-cut control can be chosen connecting pin 3 to GND or pin 21.						
Mute voltage: The static mute voltage follows the level unweighted voltage as function of FM IF_2 voltage and level adjust voltage V_{38-4}. It additionally depends on multipath level, noise (adjacent channel interferences) and the position of Tswitch. Typical curve for mute voltage dependence on V_{37-35} see Fig.16.						

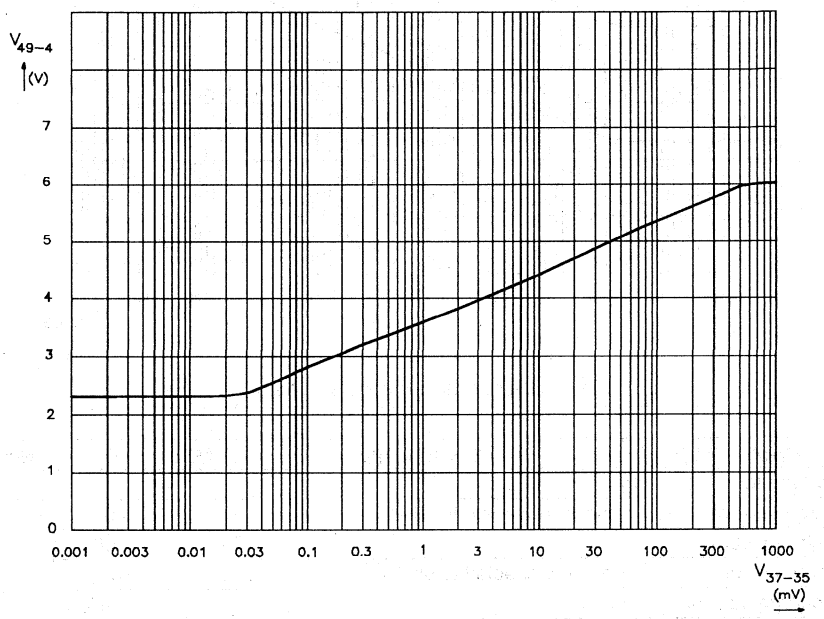


Fig.16 Typical mute voltage as function of FM IF_2 voltage.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{49-4}	mute voltage	V_{38} = 2.52 V;				
		$V_{37-35} \leq 2.5$ μV	1.8	2.2	3.2	V
		V_{37-35} = 1.0 mV	2.7	3.3	4.7	V
V/20 dB	slope of mute voltage $\Delta V_{49-4}/\Delta V_{37-35}$	$V_{37-35} \leq 100$ μV (RMS) < 300 mV	0.75	0.845	0.95	V
$\Delta V_{49-4}/VK$	temperature dependence	V_{37-35} = 1 mV	–	4.0	–	mV/VK

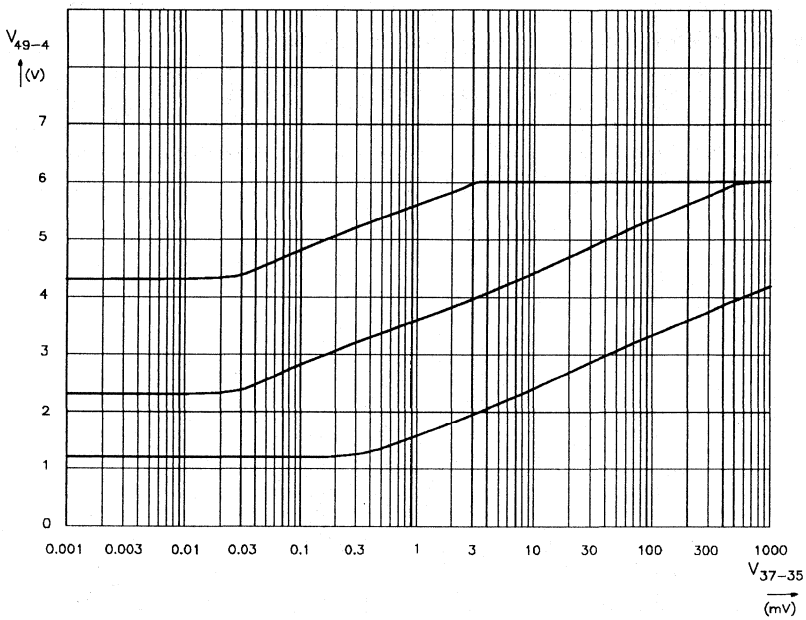


Fig.17 Adjustment range mute voltage.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Attack and decay time for mute voltage						
I_{49}	charge current	pin 3 connected to GND	–	3.0	–	μA
	discharge current		–	−3.6	–	μA
	charge current	pin 3 connected to pin 21	–	130	–	μA
	discharge current		–	−160	–	μA
Δf	muting activated by 60 kHz FM interference	pin 3 connected to GND; V_{37-35} = 3 mV; V_{49} < 2 V; f_{mod} = 60 kHz	–	30	–	kHz
Time constant for mono/stereo blend voltage. The mono/stereo blend voltage is generated as a function of FM IF_2 voltage, multipath level, noise and position of Tswitch.						
I_{16}	charge current	V_{37-35} = 3 mV; pin 3 connected to GND	–	0.5	–	μA
	discharge current		–	−18	–	μA
	charge current	V_{37-35} = 3 mV; pin 3 connected to pin 21	–	26	–	μA
	discharge current		–	−800	–	μA
m	mono/stereo blend activated by 20 kHz AM interference	V_{16} < 2 V; V_{37-35} = 3 mV; R_{L16} > 50 MΩ; f_{mod} = 20 kHz; pin 3 connected to GND	–	45	–	%
		pin 3 connected to pin 21	–	40	–	%
Δf	mono/stereo blend activated by 60 kHz FM interference	V_{16} < 3 V; V_{37-35} = 3 mV; R_{L16} > 50 MΩ; f_{mod} = 60 kHz; pin 3 connected to GND	–	30	–	kHz
		pin 3 connected to pin 21	–	22	–	kHz

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Time constant for high-cut control voltage (SDR). The high-cut control voltage is generated as a function of FM IF_2 voltage, multipath level, noise and position of Tswitch						
I_{15}	charge current	V_{37-35} = 3 mV; pin 3 connected to GND	–	0.4	–	µA
	discharge current		–	–0.44	–	µA
	charge current	V_{37-35} = 3 mV; pin 3 connected to pin 21	–	41	–	µA
	discharge current		–	–44	–	µA
m	high-cut control activated by 20 kHz AM interference	V_{15} < 2 V; V_{37-35} = 3 mV; R_{L15} > 50 MΩ; f_{mod} = 20 kHz; pin 3 connected to GND	–	40	–	%
		pin 3 connected to pin 21	–	35	–	%
Δf	high-cut control activated by 60 kHz FM interference	V_{15} < 2 V; V_{37-35} = 3 mV; R_{L15} > 50 MΩ; f_{mod} = 60 kHz; pin 3 connected to GND	–	25	–	kHz
		pin 3 connected to pin 21	–	20	–	kHz
Multipath detector						
f_{MP}	multipath detector band-pass centre frequency		–	20	–	kHz
B_{MP}	band-pass bandwidth		7.0	–	–	kHz
Reference voltage						
V_{21-4}	output voltage	I_{21} = –1 mA	4.5	5.1	5.7	V
ΔV_{21-4}	temperature dependence		–	3.3	–	mV/VK
I_{21}	output current		–	–	1	mA

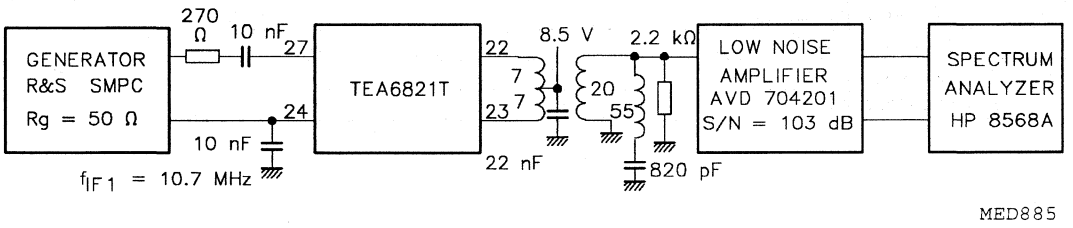


Fig.18 Test circuit AM mixer.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
AM IF path						
AM mixer (see Fig.18)		f_{IF1} = 10.7 MHz; f_{IF2} = 450 kHz				
R_{27-24}	input resistance		300	330	360	Ω
C_{27-24}	input capacitance		–	5	8	pF
R_{22-23}	output resistance		10.0	20.0	–	kΩ
C_{22-23}	output capacitance		–	5	10	pF
$I_{22IF2}/V_{27-24IF1}$	conversion gain		2.2	2.7	3.4	mS
I_{22}, I_{23}	mixer bias current		4.0	5.0	6.0	mA
	mixer leakage current	in FM position	–	–	2	μA
V_{22-23}	maximum output voltage (peak-to-peak value)		12	15	–	V
IP3	third order intermodulation		–	137	–	dBμV
AM oscillator						
The AM oscillator signal is generated by division of the 61.5 MHz crystal oscillator. Two divider ratios programmable via I^2C-bus: division by 6 (AM IF_1 = 10.7 MHz), division by 2 (AM IF_1 = 30 MHz)						
AM detector		f_{AMIF2} = 450 kHz; f_{mod} = 400 Hz; m = 30%				
V_{48-4}	AF output level (RMS value)	R_{L48} > 500 kΩ; 300 μV ≤ V_{33-34} ≤ 300 mV	190	240	290	mV
V_{33-34}	sensitivity (RMS value)	S+N/N = 26 dB	–	150	250	μV
		S+N/N = 46 dB	–	500	700	μV
S+N/N	signal-plus-noise-to-noise ratio		54	57	–	dB
THD	total harmonic distortion	m = 0.8; 1 mV ≤ V_{24-23} ≤ 300 mV	–	1.0	3.0	%
V_{33-34}	AM IF_2 minimum input (RMS value)	THD ≤ 5%; m = 0.8	–	–	500	μV
	AM IF_2 maximum input (RMS value)		800	–	–	mV
R_{33-34}	IF_2 input resistance		1.8	2.0	2.2	kΩ
C_{24-23}	IF_2 input capacitance		–	10	15	pF
R_{48out}	output resistance		27	33	39	kΩ
C_{48out}	output capacitance		–	–	10	pF
typical AM level curve see Fig.19						

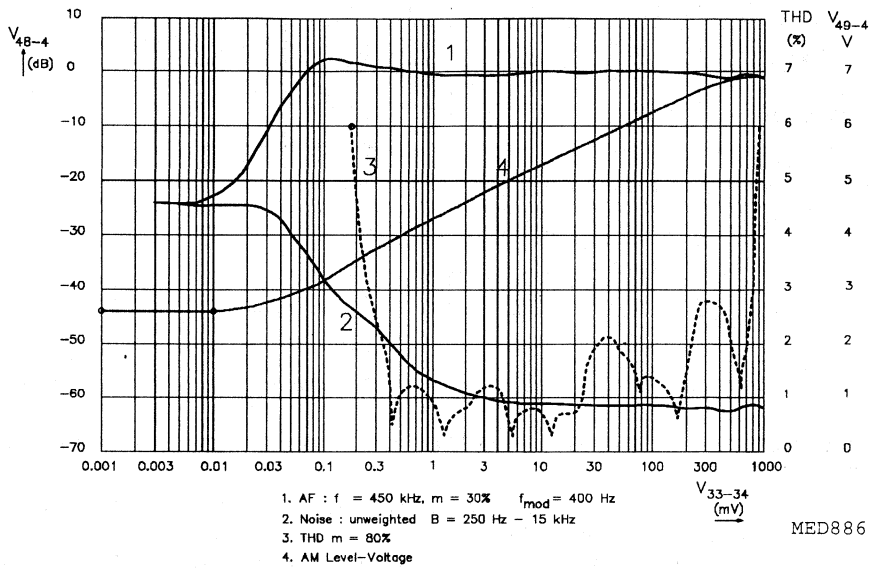


Fig.19 Signal, noise and distortion of AM AF output voltage and AM level voltage (typical curve).

Stereo decoder

FEATURES

- adjustment-free PLL-VCO
- pilot depending mono/stereo switching
- analog control of mono/stereo blend
- adjacent channel noise suppression (114 kHz)
- pilot canceller
- analog control of de-emphasis
- integrated low-pass filters for 190 kHz adjacent channel interferences and signal delay for interference absorption circuit

FUNCTIONAL DESCRIPTION

By changing the value of the input resistor at pin 12 the MPX input can be adapted to the level of the FM demodulator output (see Fig.20).

A 3rd order low-pass filter f_g = 90 kHz at the MPX input provides extra 190 kHz ACI suppression.

For AM the VCO is switched off.

Interference gate at MPX demodulator outputs.

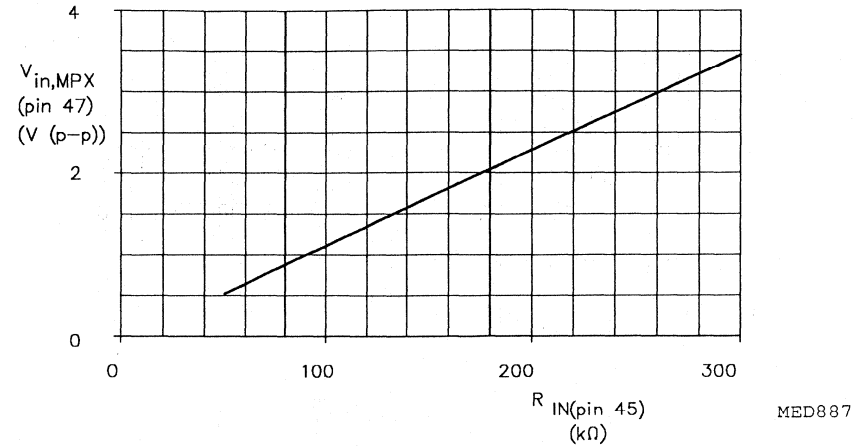


Fig.20 Adaption of MPX input to FM-demodulator output level by variation of the input resistor.

Input signal (Δf = 75 kHz) V_{MPX} (p-p) = 1.7 V; modulation frequency f_{mod} = 1 kHz; de-emphasis time constant τ = 50 µs; nominal input resistor (pin 45) R_i = 168 kΩ.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	MPX input overdrive margin	THD = 1%	4	–	–	dB
V_{44-4}, V_{41-4}	AF output voltage (RMS value)		800	900	1000	mV
V_{44-4}/V_{41-4}	difference of output voltage		–	–	±1	dB
R_{o44}, R_{o41}	output resistor		–	–	130	Ω
R_{lmin}	minimum load resistor		12	–	–	kΩ
I_{44}, I_{41}	maximum output current		150	–	–	µA
V_{44-4}, V_{41-4}	DC output voltage		3.3	3.8	4.3	V
α	channel separation (adjusted; a typical roll-off at f_{MPX} = 38 kHz of 1 dB is internally compensated)		40	–	–	dB
THD	total harmonic distortion		–	0.1	0.3	%
S+N/N	signal-plus-noise-to-noise ratio	f = 20 Hz to 20 kHz	74	80	–	dB
Carrier and harmonic suppression at the output (note to the stereo decoder)						
α_{19}	pilot signal	f = 19 kHz	–	50	–	dB
α_{38}	subcarrier	f = 38 kHz	–	50	–	dB
α_{57}		f = 57 kHz	–	46	–	dB
α_{76}		f = 76 kHz	–	60	–	dB
α_2	intermodulation	f_{mod} = 10 kHz; f_{spur} = 1 kHz	–	60	–	dB
α_3		f_{mod} = 13 kHz; f_{spur} = 1 kHz	–	58	–	dB
α_{57}	traffic radio (ARI)	f = 57 kHz	–	70	–	dB
α_{67}	subsidiary communications authorization	f = 67 kHz	70	–	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
α_{114}	adjacent channel frequency	f = 114 kHz	–	80	–	dB
α_{190}		f = 190 kHz	–	70	–	dB
α_{rr}	ripple rejection at output	f_r = 100 Hz; V_r = 100 mV_{eff}	–	30	–	dB
Mono/stereo control						
V_{ipil}	pilot threshold voltage	stereo on	–	24	30	mV
		mono on	8	20	–	mV
ΔV_{ipil}	switch hysteresis V_{ion}/V_{ioff}		–	2	–	dB
The stereo decoder can be set to mono via the I^2C-bus						
Pilot presence indication via I^2C-bus						
External mono/stereo control						
$V_{17} - 0.75V_{21}$	control voltage channel separation	see Fig.21				
		α = 6 dB	–	–80	–	mV
		α = 16 dB	–	–40	–	mV

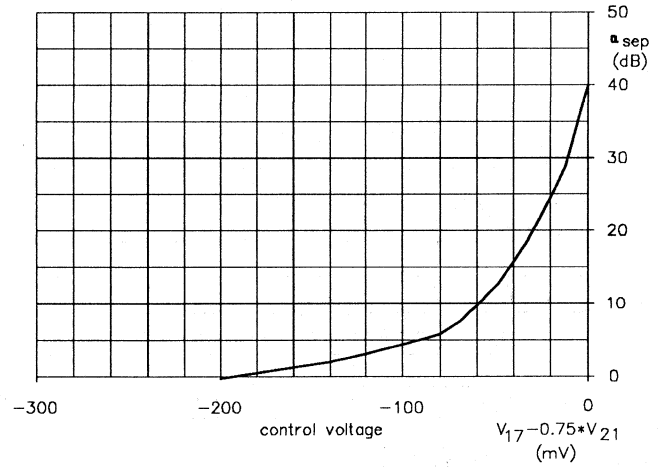


Fig.21 Channel separation as function of control voltage.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Muting functions (mute via I^2C-bus)						
α_{mute}	tuned mute		60	–	–	dB
ΔV_{44}, ΔV_{41}	DC offset voltage		–50	–	+50	mV
α_{mute}	radio mute (in combination with tuned mute)		80	–	–	dB
ΔV_{44}, ΔV_{41}	DC offset voltage		–300	–	+300	mV
High-cut control (see Fig.22)						
τ_{deemph}	control range of de-emphasis		50	–	80	µs
$V_{18} - 0.75V_{21}$	control voltage	τ_{deemph} = 50 µs	0	–	–	mV
		τ_{deemph} = 80 µs	–	–300	–	mV
The nominal de-emphasis value can be changed to 75 µs with C_{31}, C_{32} = 10 nF						

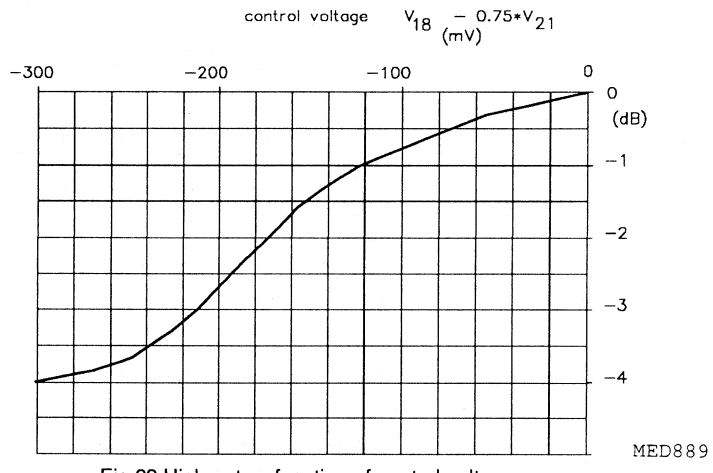


Fig.22 High-cut as function of control voltage.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Voltage controlled oscillator						
The VCO is adjusted by means of a digital auxiliary PLL						
f_{osc}	oscillator frequency range		450	456	462	kHz

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Noise blanker						
Interference detection at pin 50 level unweighted or MPXOUT (pin 47)						
T_{sup}	interference suppression time		–	40	50	µs
f_c	high-pass input filter for interference pulse, 2nd order	3 dB frequency	150	200	250	kHz
IAC control						
I_{51}	charge current (into 4 V)		5.0	10	18	µA
	discharge current (from 8.5 V)		–0.5	–1.0	–1.8	mA
V_{pulse}	trigger sensitivity	τ_{pulse} = 10 µs	–	–	20	mV
ΔV_{DC} (pin 51)	trigger threshold measured with	V_{noise} (pin 46) = 10 mV	–	200	–	mV
V_{tr} (pin 46)	f_{int} = 250 kHz	V_{DC} (pin 51) = 7.7 V	–	10	–	mV
ΔV_{DC} (pin 51)		V_{noise} (pin 46) = 100 mV	–	2.3	–	V
V_{tr} (pin 46)		V_{DC} (pin 51) = 6.7 V	–	100	–	V
I_{os}	gate input offset current at pins 31 and 32 during suppression pulse duration		–	20	50	nA

I²C-BUS SPECIFICATION AND I²C-BUS CONTROLLED FUNCTIONS

I²C-bus specification

The standard I²C-bus specification is expanded by the following definitions.
Structure of the I²C-bus logic: slave transceiver with auto increment and expansion to switch a direct transfer of all transmissions to an output for the radio front end IC (TEA6810T respectively TEA6811T).
Subaddresses are not used.

Data transfer to the TEA6821T
Data sequence:
address byte 1 byte 2
The data transfer has to be only in this order. The transfer direction of the data bytes is defined by the LSB of the address.
The data becomes valid at the output of the internal latches with the acknowledge of each byte. A stop condition after any byte can shorten transmission times.
When writing to the transceiver by using the stop condition before completion of the whole transfer:

- The remaining bytes will contain the old information
- If the transfer of a byte was not completed, this byte is lost and the previous information is available

Data transfer to an output of the front end IC
A data bit in the transceiver of the TEA6821T enables or disables a direct transfer of all transmissions to an interface stage for the front end IC.
For a transmission to the front end IC the address and the data format of the front end IC has to be used.
Hint: The pull-up resistors for the front end interface (pins 6 and 7) should not be connected to the 5 V supply voltage of the front end IC, otherwise a bus pull-down (pin 53) can occur during switching off the front end supply when the interface stage is enabled.
Data transfer to the IF IC (TEA6821T) is independent of the state of interface stage for the front end IC.

bus address of the TEA6821T	1100 001X
subaddress	not used
hardware (pin) programmable address bits	not available
default settings by power-on reset	radio mute and 40 ms IF count time is enabled, all other bits are random

Data to be received by the IC

data byte 1:

- bit 0: switch for mono: bit 0 = 1; stereo: bit 0 = 0
- bit 1: LSB reference frequency for synthesizer
- bit 2: reference frequency for synthesizer
- bit 3: MSB reference frequency for synthesizer
- bit 4: tuning mute, bit 4 = 1: off; bit 4 = 0: on
- bit 5: SDS/SDR hold, bit 5 = 1: off; bit 5 = 0: on
- bit 6: radio mute, bit 6 = 1: off; bit 6 = 0: on
- bit 7: I^2C-bus to front end, bit 7 = 1: enabled; bit 7 = 0: disabled

reference frequency setting in byte 1:

bit 3	bit 2	bit 1	
0	0	0	3 kHz
0	0	1	5 kHz
0	1	0	10 kHz
0	1	1	15 kHz
1	0	0	25 kHz
1	0	1	50 kHz
1	1	0	not defined
1	1	1	not defined

data byte 2:

- bit 0: AM/FM, bit 0 = 0: AM; bit 0 = 1: FM
- bit 1: divider for AM mixer, bit 1 = 0: division by 2; bit 1 = 1: division by 6
- bit 2: measure time IF count, bit 2 = 0: 40 ms; bit 2 = 1: 4 ms
- bit 3: SDR off, bit 3 = 0: SDR off; bit 3 = 1: SDR on
- bit 4: not used
- bit 5: not used
- bit 6: not used
- bit 7: not used

Data to be transmitted by the IC

data byte 1:

- bit 0: LSB level information
- bit 1: level information
- bit 2: MSB level information
- bit 3: LSB multipath information
- bit 4: multipath information
- bit 5: MSB multipath information
- bit 6: bit 6 = 1: stereo pilot presence
- bit 7: not used

The A/D conversion for multipath and level will be done while a transmission of any address to the I^2C-bus.

data byte 2:

bit 0:	LSB of the IF-counter
bit 1:	IF-counter
bit 2:	IF-counter
bit 3:	IF-counter
bit 4:	IF-counter
bit 5:	IF-counter
bit 6:	IF-counter
bit 7:	MSB of the IF-counter

Reference frequency generation
Division ratios
All specified frequencies are valid for a crystal oscillator frequency of 61.5 MHz.

DIVISION RATIO	REFERENCE FREQUENCY (kHz)
20500	3
12300	5
6150	10
4100	15
2460	25
1230	50

Output signal of reference frequency divider

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
C_{10-4}, C_{11-4}	output capacitance	–	–	4	pF
R_{10-52}, R_{11-52}	output resistance	800	1000	1200	Ω
V_{10-11}	differential output voltage (peak-to-peak value)	0.3	0.4	0.5	V
V_{10-4}, V_{11-4}	single-ended output voltage (peak-to-peak value)	0.15	0.2	0.3	V

IF-counter

SYMBOL	PARAMETER	MIN.	UNIT
V_{33-34}	IF-counter sensitivity for AM, m = 0	200	μV
V_{37-35}	IF-counter sensitivity for FM	200	μV

Counting windows	AM:	4 ms, (40 ms)
	FM:	40 ms, 4 ms
Counting resolution	AM:	250 Hz, (25 Hz)
	FM:	5 kHz, 50 kHz
IF-prescaler	AM:	division by 1
	FM:	division by 200

The IF-count windows are valid for a crystal oscillator frequency of 61.5 MHz.

The FM/AM switching is done by bit 0 of byte 2 of the received data of the IC.
The IF-counter operates continuously.
The IF-counter and window-counter will be resetted when the I^2C-bus logic detects the address of the IC. This disables changes in the latches for the IF-count, while reading this value. If the transmission to the front end IC will be disabled after the synthesizer loop of the TEA6811T front end IC has locked for a new frequency, the IF-count will be available after the set measuring time.
The IF-counter starts at 0. The IF-counter output are the **8 least significant bits** of the counting result.

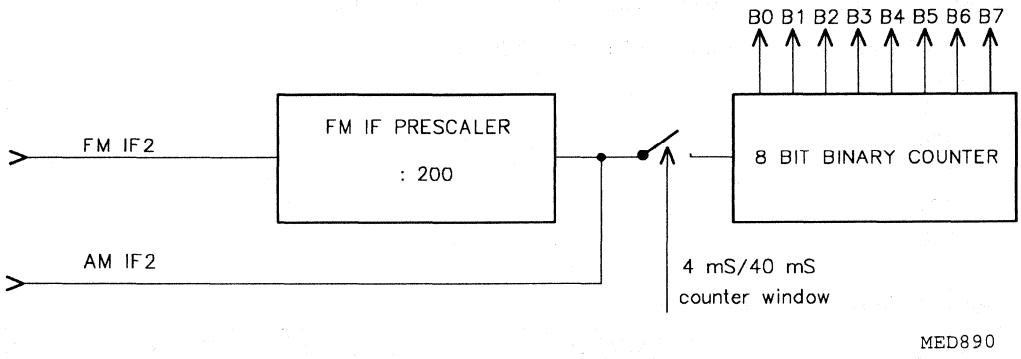
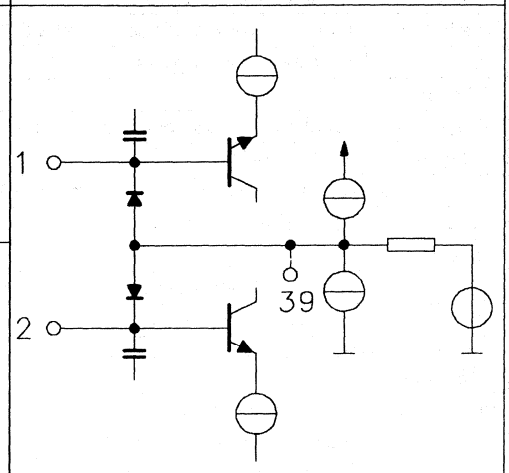
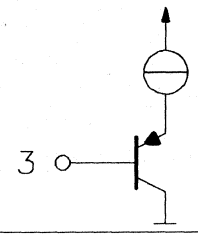
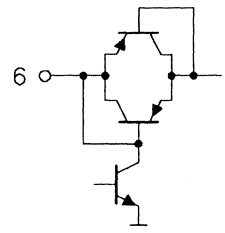
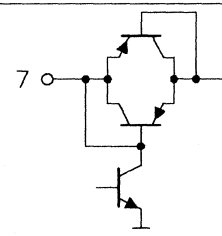


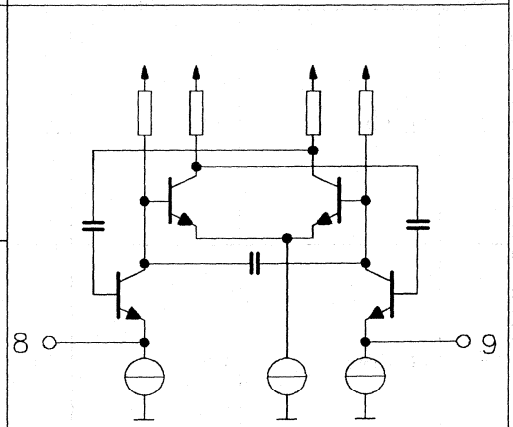
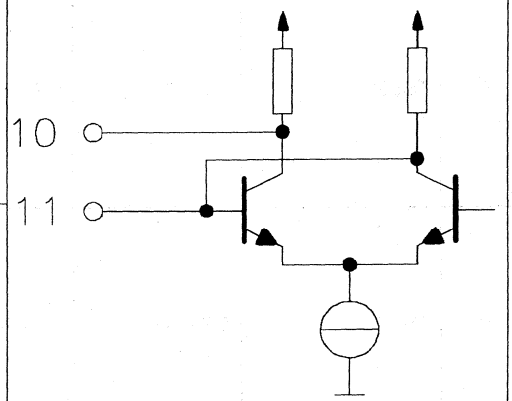
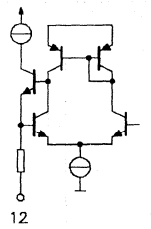
Fig.23 IF-counter structure.

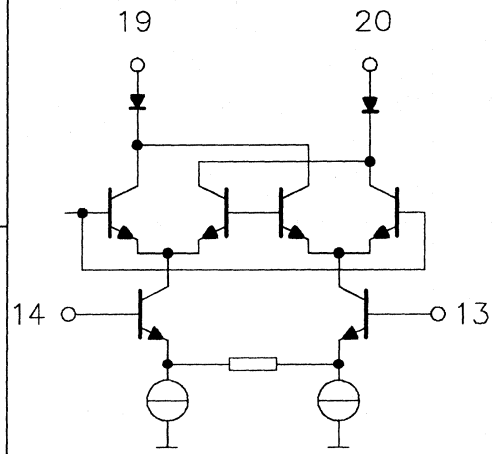
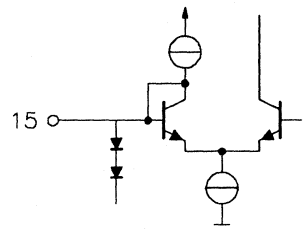
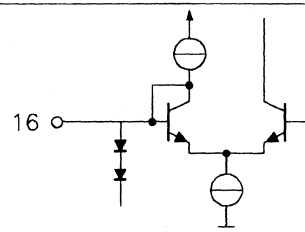
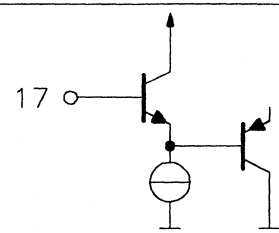
A/D converters for level and multipath voltage

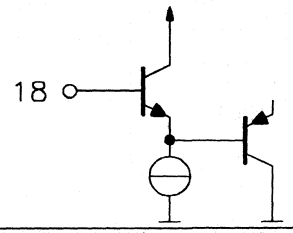
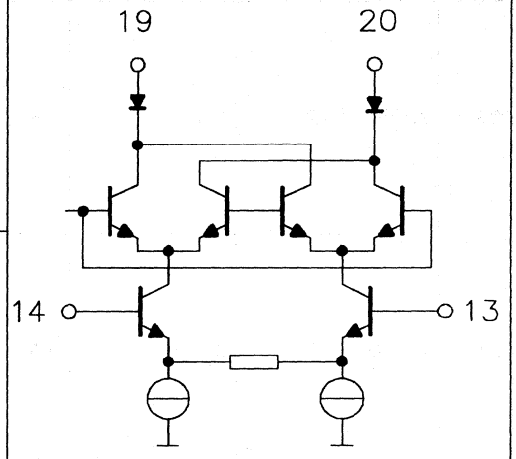
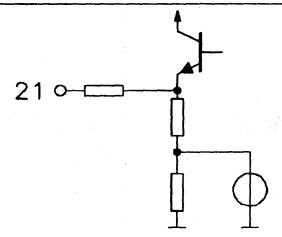
SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
A/D converter for FM level information					
The FM level information V_{50-3} is A/D converted with 3 bit					
ΔV_{50-4}	AD conversion step size	–	6	–	dB/step
FM stop					
ΔV_{stop}	variation of stop level as function of V_{42-4}	–	30	–	dB/V
A/D converter for AM level information					
The AM level information V_{49-4} is A/D converted with 3 bit					
ΔV_{49-4}	AD conversion step size	–	6	–	dB/step
AM stop					
ΔV_{stop}	variation of stop level as function of V_{43-4}	–	30	–	dB/V
A/D converter for multipath information					
The multipath information V_{40-4} is A/D converted with 3 bit covering an IF_2 amplitude modulation range $0.15 \leq m \leq 0.9$; f_{mod} = 20 kHz					
m	multipath conversion step 0	–	–	–	%
	multipath conversion step 1	–	15	–	%
	multipath conversion step 2	–	30	–	%
	multipath conversion step 3	–	40	–	%
	multipath conversion step 4	–	50	–	%
	multipath conversion step 5	–	58	–	%
	multipath conversion step 6	–	66	–	%
	multipath conversion step 7	–	74	–	%

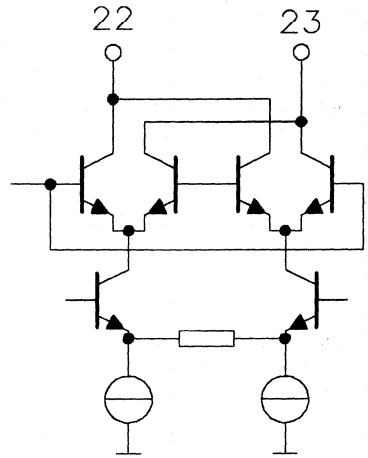
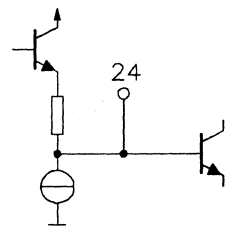
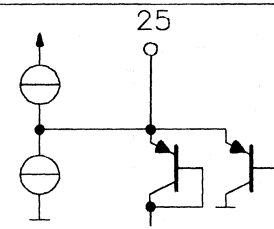
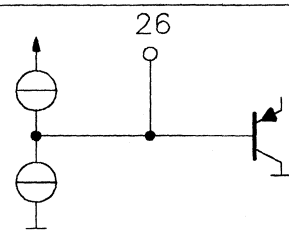
Table 1 Equivalent pin circuits and pin voltages.

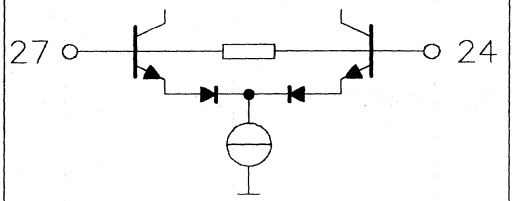
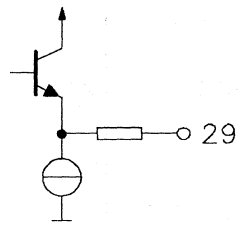
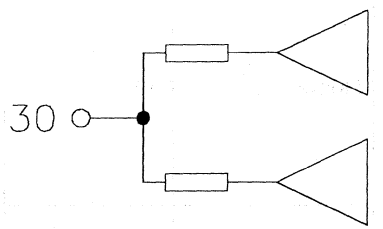
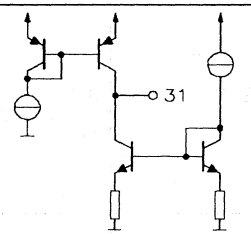
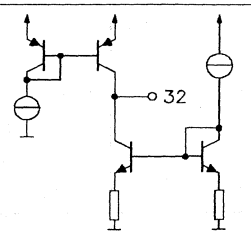
PIN NO.	PIN NAME	DC VOLTAGE (V)		INTERNAL CIRCUIT
		AM	FM	
1	QDET1	4.0	4.0	
2	QDET2	4.0	4.0	
3	TSWITCH	open	0 / V_{21}	
4	GND			
5	V_{P5}	5.0	5.0	
6	HFBUS1	5.0	5.0	
7	HFBUS2	5.0	5.0	

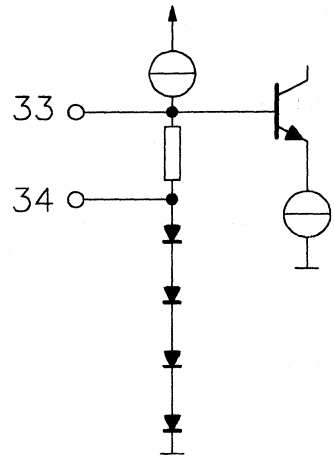
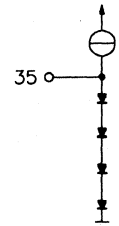
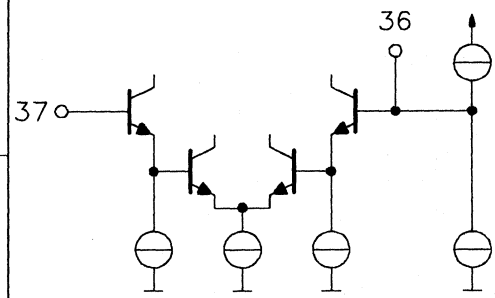
PIN NO.	PIN NAME	DC VOLTAGE (V)		INTERNAL CIRCUIT
		AM	FM	
8	XTAL1	4.1	4.1	
9	XTAL2	4.1	4.1	
10	F_{REFP}	4.9	4.9	
11	F_{REFN}	4.9	4.9	
12	I_{REF}	4.3	4.3	

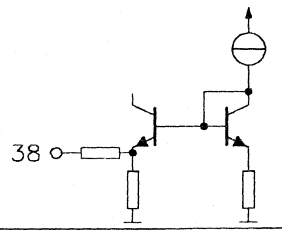
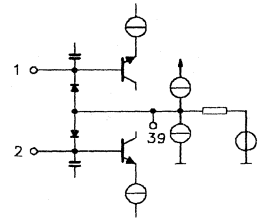
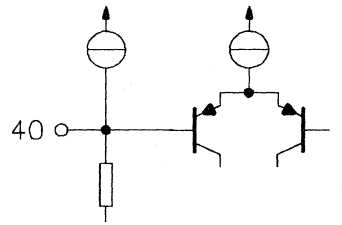
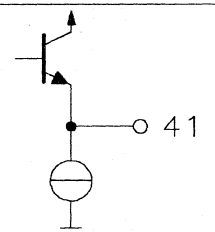
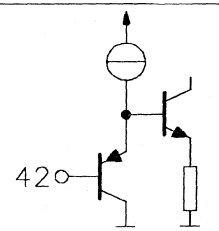
PIN NO.	PIN NAME	DC VOLTAGE (V)		INTERNAL CIRCUIT
		AM	FM	
13	FMIFIN1	2.3	2.3	
14	FMIFIN2	2.3	2.3	
15	TSDR	0.7 – 5.5	0.7 – 5.5	
16	TSDS	0.7 – 5.5	0.7 – 5.5	
17	V_{SDS}	3.0 – 5.5	3.0 – 5.5	

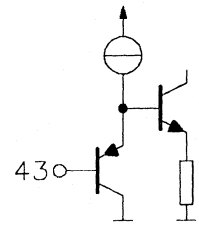
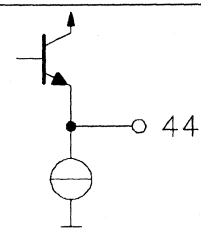
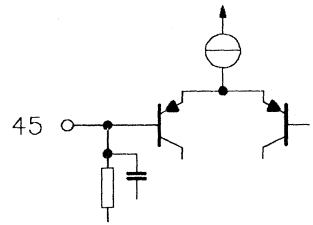
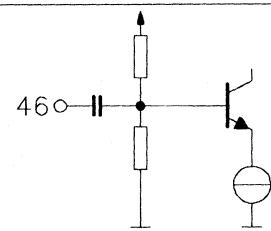
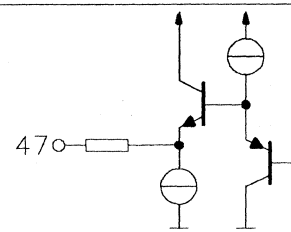
PIN NO.	PIN NAME	DC VOLTAGE (V)		INTERNAL CIRCUIT
		AM	FM	
18	V_{SDR}	3.0 – 5.5	3.0 – 5.5	
19	FMIF2OUT1	8.5	8.5	
20	FMIF2OUT2	8.5	8.5	
21	V_{REF}	5.1	5.1	

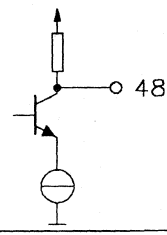
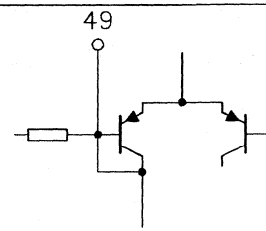
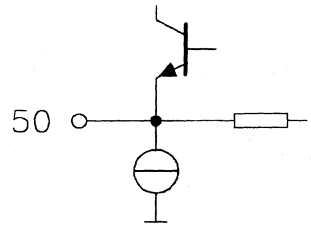
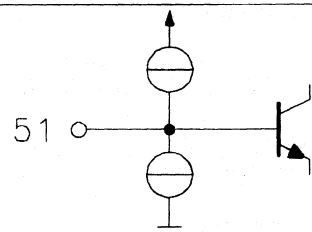
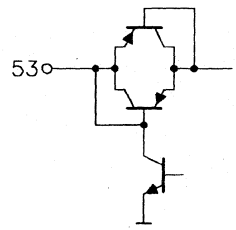
PIN NO.	PIN NAME	DC VOLTAGE (V)		INTERNAL CIRCUIT
		AM	FM	
22	AMIF2OUT1	8.5	8.5	
23	AMIF2OUT2	8.5	8.5	
24	FMAMDEC	3.0	3.0	
25	PHASEDET	3.0 – 7.0	3.0 – 7.0	
26	PILDET	0.7	0.7 – 7.0	

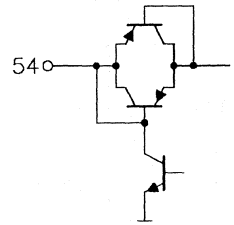
PIN NO.	PIN NAME	DC VOLTAGE (V)		INTERNAL CIRCUIT
		AM	FM	
27	FMAM10.7	3.0	3.0	
28	V_{PIF}	8.5	8.5	
29	FMIFAMPOUT	6.0	6.0	
30	AFGND	3.6	3.6	
31	DEEMPHR	2.3	2.3	
32	DEEMPHL	2.3	2.3	

PIN NO.	PIN NAME	DC VOLTAGE (V)		INTERNAL CIRCUIT
		AM	FM	
33	AMIF2IN1	2.7	0.7	
34	AMIF2IN2	2.7	0.7	
35	FMIN2	0.7	2.7	
36	DCFEED	2.7	2.7	
37	FMIN1	0.7	2.7	

PIN NO.	PIN NAME	DC VOLTAGE (V)		INTERNAL CIRCUIT
		AM	FM	
38	LEVELADJ	2.6	2.6	
39	C_{AFC}	1.0 – 2.2	1.0 – 7.0	
40	MPBUF	0.7 – 6.0	0.7 – 6.0	
41	OUTLEFT	3.6	3.6	
42	FMSTOP	0 – 5.2	0 – 5.2	

PIN NO.	PIN NAME	DC VOLTAGE (V)		INTERNAL CIRCUIT
		AM	FM	
43	RDS/AMSTOP	0 – 5.2	3.0	
44	OUTRIGHT	3.6	3.6	
45	MPXIN	2.8	2.8	
46	IAC_{IN}	0	0	
47	MPXOUT	0	3.0	

PIN NO.	PIN NAME	DC VOLTAGE (V)		INTERNAL CIRCUIT
		AM	FM	
48	AMAFOUT	3.7	4.8	
49	V_{MUTAML}	1.0 – 5.5	1.0 – 5.5	
50	LEVELUNWEIG	1.0 – 7.0	1.0 – 7.0	
51	$I_{ACCONTR}$	0	6.0	
52	V_{PDIG}	5.0	5.0	
53	SDA	5.0	5.0	

PIN NO.	PIN NAME	DC VOLTAGE (V)		INTERNAL CIRCUIT
		AM	FM	
54	SCL	5.0	5.0	
55	BUSGND	0	0	
56	$V_{P8.5}$	8.5	8.5	

Notes to the stereo decoder characteristic

$$\alpha_2 = \frac{V_o \text{ (signal) (at 1 kHz)}}{V_o \text{ (spurious) (at 1 kHz)}}; f_s = (2 \times 10 \text{ kHz}) - 19 \text{ kHz}$$

$$\alpha_3 = \frac{V_o \text{ (signal) (at 1 kHz)}}{V_o \text{ (spurious) (at 1 kHz)}}; f_s = (3 \times 13 \text{ kHz}) - 38 \text{ kHz}$$

$$\alpha_{57} \text{ (ARI)} = \frac{V_o \text{ (signal) (at 1 kHz)}}{V_o \text{ (spurious) (at 1 kHz} \pm 23 \text{ Hz)}}$$

$$\alpha_{67} = \frac{V_o \text{ (signal) (at 1 kHz)}}{V_o \text{ (spurious) (at 9 kHz)}}; f_s = (2 \times 38 \text{ kHz}) - 67 \text{ kHz}$$

$$\alpha_{114} = \frac{V_o \text{ (signal) (at 1 kHz)}}{V_o \text{ (spurious) (at 4 kHz)}}; f_s = 110 \text{ kHz} - (3 \times 38 \text{ kHz})$$

$$\alpha_{190} = \frac{V_o \text{ (signal) (at 1 kHz)}}{V_o \text{ (spurious) (at 4 kHz)}}; f_s = 186 \text{ kHz} - (5 \times 38 \text{ kHz})$$

IF filter / amplifier / demodulator for FM radio receivers TEA6850

FEATURES

- Improved dynamic selectivity and sensitivity because of tunable IF filter
- Fully integrated, frequency matched FM demodulator
- High linearity
- Unweighted level detector output
- Soft mute
- MPX output for RDS and diversity
- Internal source selector.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage (pin 7)	7	8.5	10	V
I_P	supply current (pin 7)	14	17.5	21	mA
DS200	dynamic selectivity for 200 kHz distance (EMF = 700 μV; filter bandwidth = 50 kHz)	22	27	–	dB
S/N	signal-to-noise ratio (Δf = ±22.5 kHz; f_m = 1 kHz)	61	67	–	dB
THD	total harmonic distortion (Δf = ±75 kHz; f_m = 1 kHz)	–	0.3	0.5	%
V_O	AF output signal at pin 4 (RMS value)	180	200	220	mV
T_{amb}	operating ambient temperature	–40	–	+85	°C

GENERAL DESCRIPTION

The TEA6850 is a monolithic bipolar integrated circuit for IF filtering, FM demodulation and level detection. Using IF filters tuned by the demodulated signal, dynamic selectivity and sensitivity are improved.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TEA6850H	44	QFP	plastic	SOT307

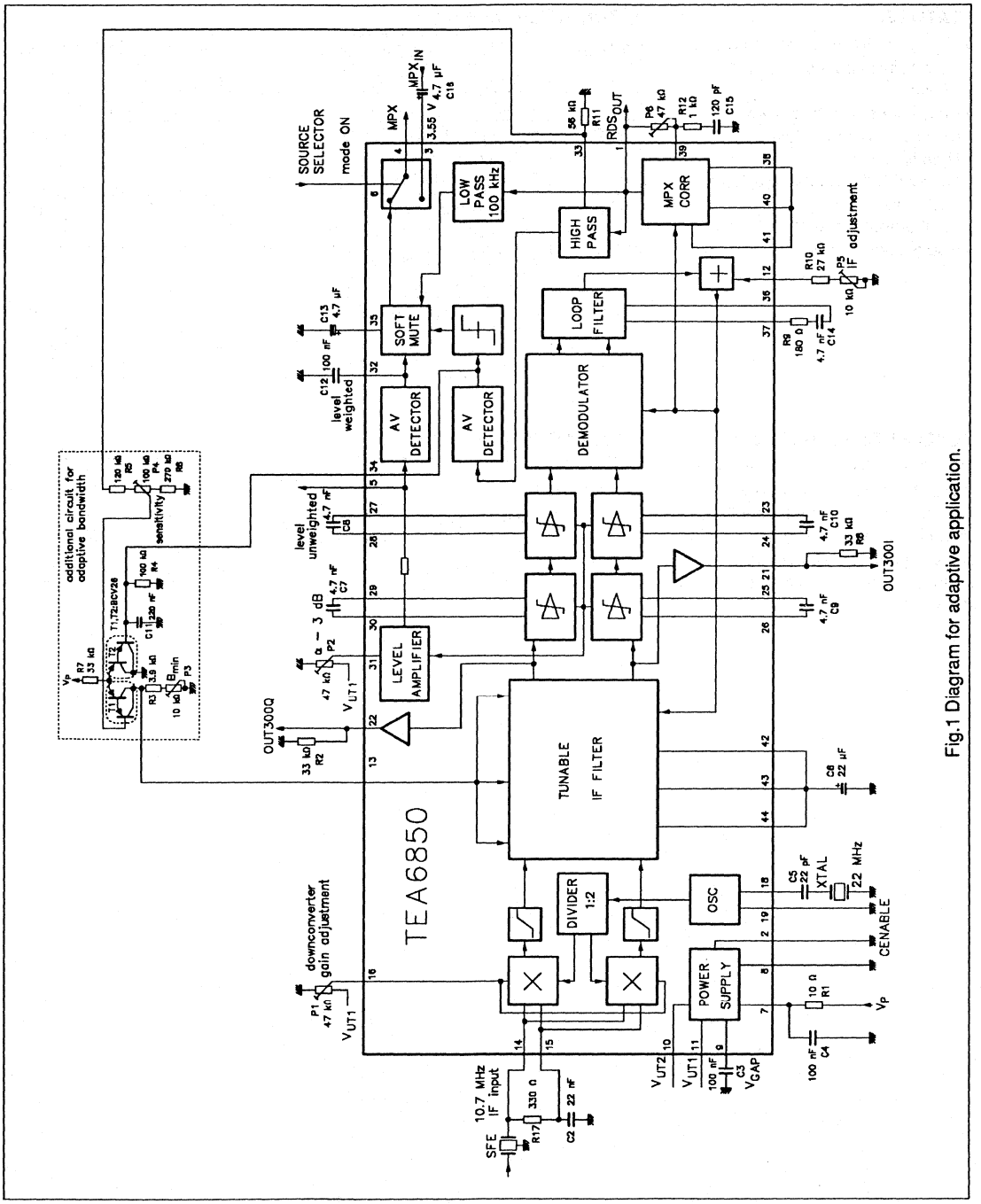


Fig.1 Diagram for adaptive application.

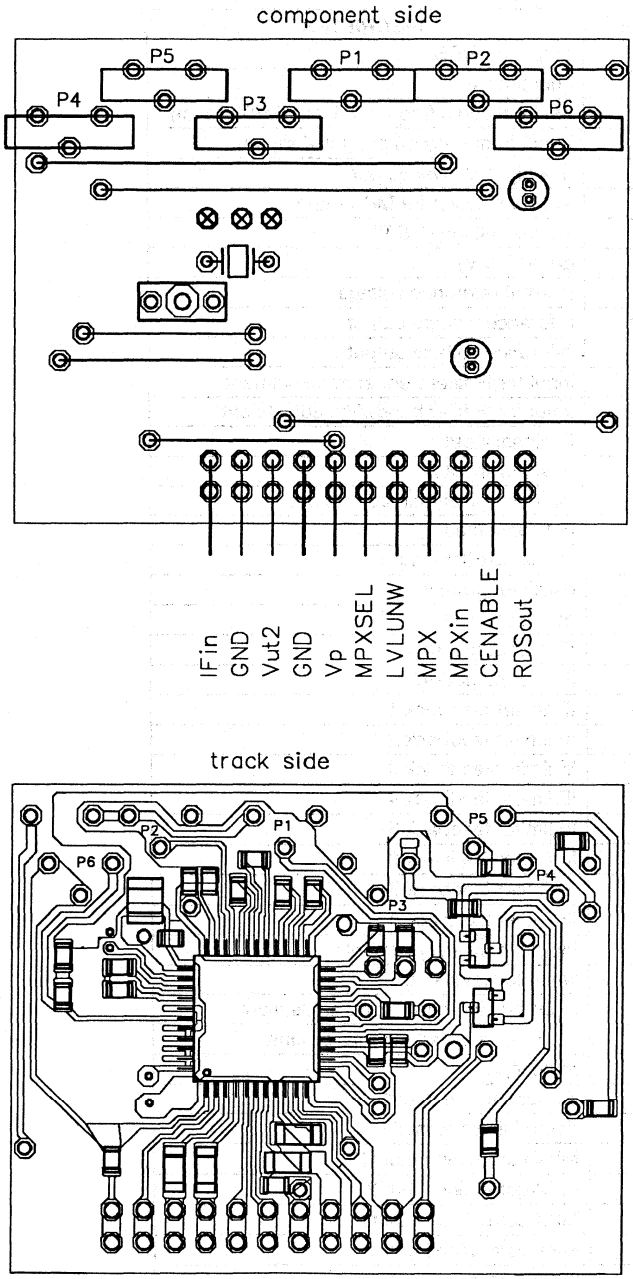


Fig.2 TEA6850H (adaptive version), printed-circuit board.

PINNING

SYMBOL	PIN	DESCRIPTION
RDS_{OUT}	1	output for RDS
CENABLE	2	chip enable
MPX_{IN}	3	external audio frequency input (MPX signal)
MPX	4	audio frequency output (MPX signal)
LVLUNW	5	unweighted level output
MPXSEL	6	source selector for MPX signal
V_P	7	supply voltage (8.5 V)
GND	8	ground (0 V)
V_{GAP}	9	internal reference voltage
V_{UT2}	10	reference voltage output
V_{UT1}	11	reference voltage output
IFADJ	12	input for IF filter frequency adjustment
BWADJ	13	input for IF filter bandwidth adjustment
IF_{IN}	14	IF signal input 1
IF_{INI}	15	IF signal input 2
GAINADJ	16	input for mixer gain adjustment
n.c.	17	not connected
CRYSTAL	18	crystal oscillator input
GND	19	oscillator ground
n.c.	20	not connected
OUT300I	21	IF filter output (0°)
OUT300Q	22	IF filter output (90°)
CLIM1I	23	IF limiter feedback 1
CLIM2I	24	IF limiter feedback 2
CLIM3I	25	IF limiter feedback 3
CLIM4I	26	IF limiter feedback 4
CLIM1Q	27	IF limiter feedback 5
CLIM2Q	28	IF limiter feedback 6
CLIM3Q	29	IF limiter feedback 7
CLIM4Q	30	IF limiter feedback 8
LVLADJ	31	input for level adjustment
LVLWEI	32	weighted level output
IHP60	33	input for high-pass –3 dB adjustment
CHPMUTE	34	output of rectified high-pass signal
CMUTE	35	mute input
DEMOLOOP1	36	demodulator output 1
DEMOLOOP2	37	demodulator output 2
COP2	38	MPX correction output 2
CON2	39	MPX correction input 2
COO1	40	MPX correction output 1
CON1	41	MPX correction input 1
IFLOOP1	42	IF loop filter output 1
IFLOOP2	43	IF loop filter output 2
IFLOOP3	44	IF loop filter output 3

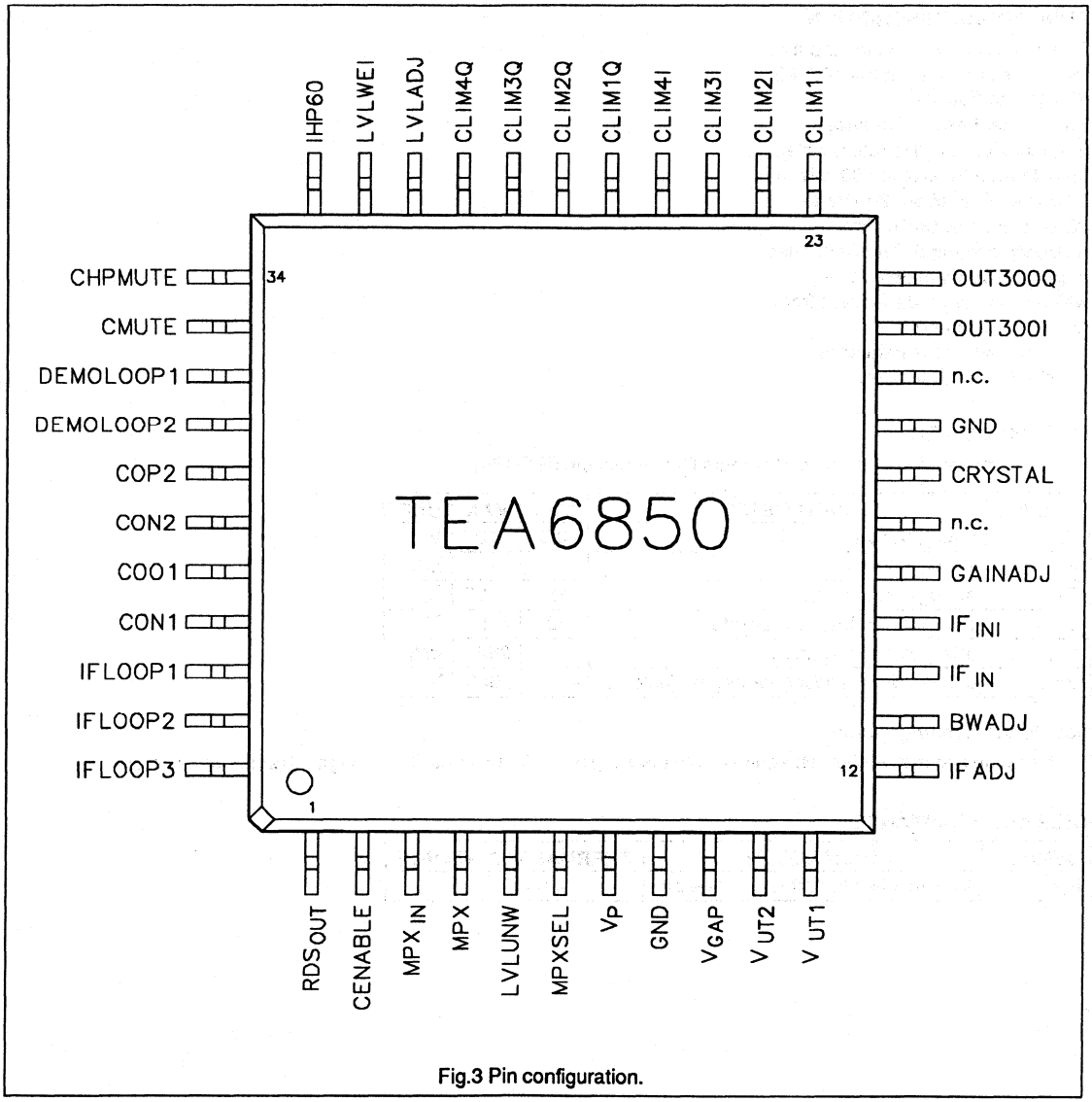


Fig.3 Pin configuration.

FUNCTIONAL DESCRIPTION

The first mixer stage at the input of the circuit is for mixing the 10.7 MHz IF signal to 300 kHz.
The IF filter has a resonance frequency of 300 kHz (adjustable), tunable from 50 kHz to 500 kHz, and a bandwidth of about 20 kHz to 80 kHz tunable. Static filter response see Fig.5. The limiter has a gain of approximately 90 dB, which is virtually independent from temperature change.
The demodulator is frequency matched with the IF filter.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_P	supply voltage	−0.3	+12	V
I_P	supply current	–	21	mA
T_{stg}	storage temperature	−55	+125	°C
T_{amb}	operating ambient temperature	−40	+85	°C
P_{tot}	total power dissipation	–	252	mW
V_{ESD}	electrostatic handling for all pins (note 1)	–	±300	V

Note to the Limiting Values

1. Charge device model class B: equivalent to discharging a 200 pF capacitor through a 0 Ω series resistor.

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient in free air	65 K/W

DC CHARACTERISTICS

V_P = 8.5 V; T_{amb} = +25 °C; all voltages referenced to ground unless otherwise specified.

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage	7	8.5	10	V
I_P	supply current (TEA6850 enable)	14	17.5	21	mA
I_P	supply current (TEA6850 disable)	320	400	480	µA
V_1	voltage at pin 1	2.1	2.4	2.7	V
V_2	voltage at pin 2	tbn	tbn	tbn	V
V_3	voltage at pin 3	3.3	3.55	3.8	V
V_4	voltage at pin 4	3.3	3.55	3.8	V
V_5	voltage at pin 5	tbn	tbn	tbn	V
V_6	voltage at pin 6	2.1	2.3	2.5	V
V_{12}	voltage at pin 12	0.98	1.08	1.18	V
V_{13}	voltage at pin 13	tbn	tbn	tbn	V
V_{14}	voltage at pin 14	1.8	2	2.2	V
V_{15}	voltage at pin 15	1.8	2	2.2	V
V_{16}	voltage at pin 16	tbn	tbn	tbn	V
V_{18}	voltage at pin 18	3.0	3.3	3.6	V
V_{21}	voltage at pin 21	3.2	3.5	3.8	V
V_{22}	voltage at pin 22	3.2	3.5	3.8	V
V_{23}	voltage at pin 23	3.9	4.2	4.5	V
V_{24}	voltage at pin 24	3.9	4.2	4.5	V
V_{25}	voltage at pin 25	3.9	4.2	4.5	V
V_{26}	voltage at pin 26	3.9	4.2	4.5	V
V_{27}	voltage at pin 27	3.9	4.2	4.5	V
V_{28}	voltage at pin 28	3.9	4.2	4.5	V
V_{29}	voltage at pin 29	3.9	4.2	4.5	V
V_{30}	voltage at pin 30	3.9	4.2	4.5	V
V_{31}	voltage at pin 31	tbn	tbn	tbn	V
V_{32}	voltage at pin 32	tbn	tbn	tbn	V
V_{33}	voltage at pin 33	4.1	4.4	4.7	V
V_{34}	voltage at pin 34	2.7	2.9	3.3	V
V_{35}	voltage at pin 35	2.1	2.4	2.7	V
V_{36}	voltage at pin 36	4.2	4.4	4.6	V
V_{37}	voltage at pin 37	4.2	4.4	4.6	V
V_{38}	voltage at pin 38	2.1	2.4	2.7	V
V_{39}	voltage at pin 39	2.1	2.4	2.7	V
V_{40}	voltage at pin 40	2.1	2.4	2.7	V
V_{41}	voltage at pin 41	2.1	2.4	2.7	V
V_{42}	voltage at pin 42	1.6	1.75	1.9	V
V_{43}	voltage at pin 43	1.6	1.75	1.9	V
V_{44}	voltage at pin 44	1.6	1.75	1.9	V

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
Reference voltage source					
V_9	voltage at pin 9	2.4	2.55	2.7	V
V_{10}	voltage at pin 10	2.95	3.25	3.55	V
V_{11}	voltage at pin 11	0.98	1.08	1.2	V
TK	temperature coefficient of V_{10} and V_{11}	–	3.3	–	10^{-3}/K

AC CHARACTERISTICS

V_P = 8.5 V; T_{amb} = +25 °C; f = 10.7 MHz with f_m = 1 kHz, ±22.5 kHz deviaton (Δf = ±22.5 kHz); EMF = 30 mV RMS; 50 µs de-emphasis; filter bandwidth = 50 kHz overall; –6 dB gain from EMF to IF filter output (pins 21 and 22); in noise frequency band for S/N measurements 300 Hz to 15 kHz; S/N stereo measurement with ideal decoder; measurements taken in Fig.4 unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
DS100	dynamic selectivity for 100 kHz distance	EMF = 700 µV	13	16	–	dB
		EMF = 14 mV	10	12	–	dB
DS200	dynamic selectivity for 200 kHz distance	EMF = 700 µV	22	27	–	dB
		EMF = 14 mV	18	22	–	dB
S/N	signal-to-noise ratio	mono	61	67	–	dB
		stereo	54	57	–	dB
EMF	IF signal	S/N = 26 dB; V_5 = 5 V	–	20	45	µV
		S/N = 46 dB; V_5 = 5 V	–	130	370	µV
EMF	input voltage for start of limiting (RMS value)	–3 dB at MPX output; V_5 = 5 V	–	10	20	µV
THD	total harmonic distortion	Δf = 75 kHz	–	0.3	0.5	%
		Δf = 100 kHz	–	0.5	1	%
		f_m = 8 kHz; Δf = 75 kHz	–	3	5	%
D_{57}	attenuation of third harmonic measured at pin 4	f_m = 19 kHz; Δf = 6.75 kHz; measured at 57 kHz compared to 57 kHz Δf = 2 kHz	14	20	–	dB
EMF	admissible maximum input voltage (RMS value)		300	–	–	mV
$A_{14\text{-}21,22}$	gain to IF filter output (adjustable)		–	–6	–	dB
ΔA_{DC}	downconverter adjustable range		–10	–	+6	dB
V_O	MPX output voltage (RMS value)		180	200	220	mV
ΔV_O	MPX output voltage ripple	1 kHz < f_{mod} < 15 kHz	–	–	±2	dB
		23 kHz < f_{mod} < 53 kHz	–	–	±2	dB
RR	power supply ripple rejection	f = 200 Hz to 20 kHz; V_{rmax} = 100 mV (on V_P); ripple at MPX output	38	–	–	dB
α_{AM}	AM suppression	f_{mod} = 400 Hz; modulation = 30%	–	50	–	dB
		500 µV < EMF < 100 mV	40	44	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
RDS output (pin 1)						
Z_O	output impedance		–	–	1	kΩ
R_L	load resistance		15	–	–	kΩ
C_L	load capacitance		–	–	50	pF
V_1	RDS signal output voltage	f_{mod} = 57 kHz; Δf = 2 kHz; $R_L = \infty$; C_L = 0	4	6	–	mV
t_{switch}	switch on time		–	–	500	ms
10.7 MHz input (pins 14 and 15)						
R_i	input resistance		3.5	5	6.5	kΩ
C_i	input capacitance		–	–	5	pF
V_{14}	residual oscillator signal	$f_{osc}/2$ = 11 MHz; R_G = 300 Ω	–	–	30	μV
Crystal						
f_0	standard frequency		–	22	–	MHz
$\Delta f_0/f_0$	frequency tolerance		–100	–	+100	ppm
C_0	shunt capacitance		–	–	7	pF
R_s	equivalent series resistance		–	–	120	Ω
$\Delta T_0/T_0$	temperature drift	–40 °C < T < +85 °C	–50	–	+50	ppm
Oscillator (measured at pin 18)						
V_{18}	22 MHz output level		13	20	40	mV
OUT300Q, I output (pins 21 and 22; R_{OUT300} = 33 kΩ; see Fig.4)						
$V_{21,22}$	output voltage	EMF = 75 mV	7	12	14	mV
$\lvert V_{21}\rvert - \lvert V_{22}\rvert$	I, Q output level difference		–	–	1.5	mV
TC	temperature coefficient of output voltage		–	3.3	–	10^{-3}/K
Z_O	output impedance		–	1.26	–	kΩ
Tunable filter (–40 °C < T < +85 °C; filter response see Fig.5)						
ΔF_0	frequency temperature shift		–10	0	+10	kHz
ΔB	bandwidth temperature shift		–5	0	+3	kHz
B_{max}	maximum adjustable bandwidth	V_{13} = 0 V	70	80	–	kHz
B_{min}	minimum adjustable bandwidth		–	20	–	kHz
Level amplifier (pin 5; typical curve and adjusting range see Fig.7)						
Z_O	output impedance		8	10	12	kΩ
TC	temperature coefficient of output voltage		–	3.3	–	10^{-3}/K
V_5	output voltage	α = –3 dB for EMF = 200 μV; EMF = 100 μV	2.1	2.35	2.6	V
		EMF = 1 mV	2.95	3.3	3.65	V
S	slope of output voltage	100 μV < EMF < 10 mV	–	950	–	mV/20 dB
V_5	level shift adjustment range	EMF = 0	±0.5	±1.0	±1.5	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Soft mute (typical curves see Fig.8)						
level dependence						
EMF	start of mute (α = –3 dB) for IF input (RMS value)		–	200	–	µV
EMF	–3 dB adjustment range for IF input		100	–	300	µV
S_M	mute slope at –15 dB		29	32	35	dB/Dec
V_{MPX}/V_{MPX0}	muting depth	EMF < 5 µV; α = –3 dB for EMF = 200 µV	–35	–32	–29	dB
I_{32}	charge current	V_5 = 4.5 V; V_{32} = 3.9 V	10	13	17	µA
	discharge current	V_5 = 4.5 V; V_{32} = 5.1 V	20	26	34	µA
τ_{mute}	time constant from unmuted to muted		0.75	1	1.3	ms
τ_{unmute}	time constant from muted to unmuted		1.5	2	2.6	ms
high-pass dependence (see Fig.9)						
V_{MPX}/V_{MPX0}	muting depth		–12	–10	–8	dB
V_1	voltage at pin 1 (RMS value)	f = 60 kHz; V_{MPX}/V_{MPX0} = –3 dB	165	185	205	mV
I_{34}	charge current	V_{34} = 0 V	140	200	260	µA
	discharge current	V_{34} = 5 V	0.7	1	3	µA
ΔV_4	residual DC offset at MPX output	EMF < 80 µV	–	–	60	mV
		80 µV < EMF < 2 mV	–	–	60	mV
MPX output (pin 4)						
R_O	output resistance		–	–	100	Ω
R_L	load resistance	$V_4 \leq 1$ V	3	–	–	kΩ
C_L	load capacitance		–	–	50	pF
V_4	clipping DC voltage		1.5	–	7	V
V_4	residual signal of 300 kHz and higher harmonics (RMS value)		–	–	10	mV
CENABLE (pin 2)						
V_2	voltage range	chip enable	–0.3	+0.6	+1.1	V
		chip disable	1.9	2.4	5.5	V
R_I	input resistance		100	–	–	kΩ
Source selector isolation (f < 12.5 kHz; mode TEA6850 signal: V_6 > 1.9 V or pin not connected; mode external signal: V_6 < 1.1 V)						
V_{MPX}/V_{MPXIN}	isolation of external signal	mode TEA6850 signal; Δf = 0; V_{MPXIN} = 200 mV; f = 12.5 kHz	–70	–80	–	dB
V_{MPX}/V_{MPX0}	isolation of TEA6850 signal	mode external signal; Δf = 22.5 kHz; R_g (pin 3) < 10 kΩ; f_{mod} = 12.5 kHz	–70	–80	–	dB
R_I	input resistance at pin 6	V_6 > 1.9 V	1	–	–	MΩ
		V_6 < 1.1 V	3	–	–	kΩ
	input resistance at pin 3		23	30	37	kΩ
I_6	input current	$V_{sselect}$ < 1.1 V	–	–	20	µA

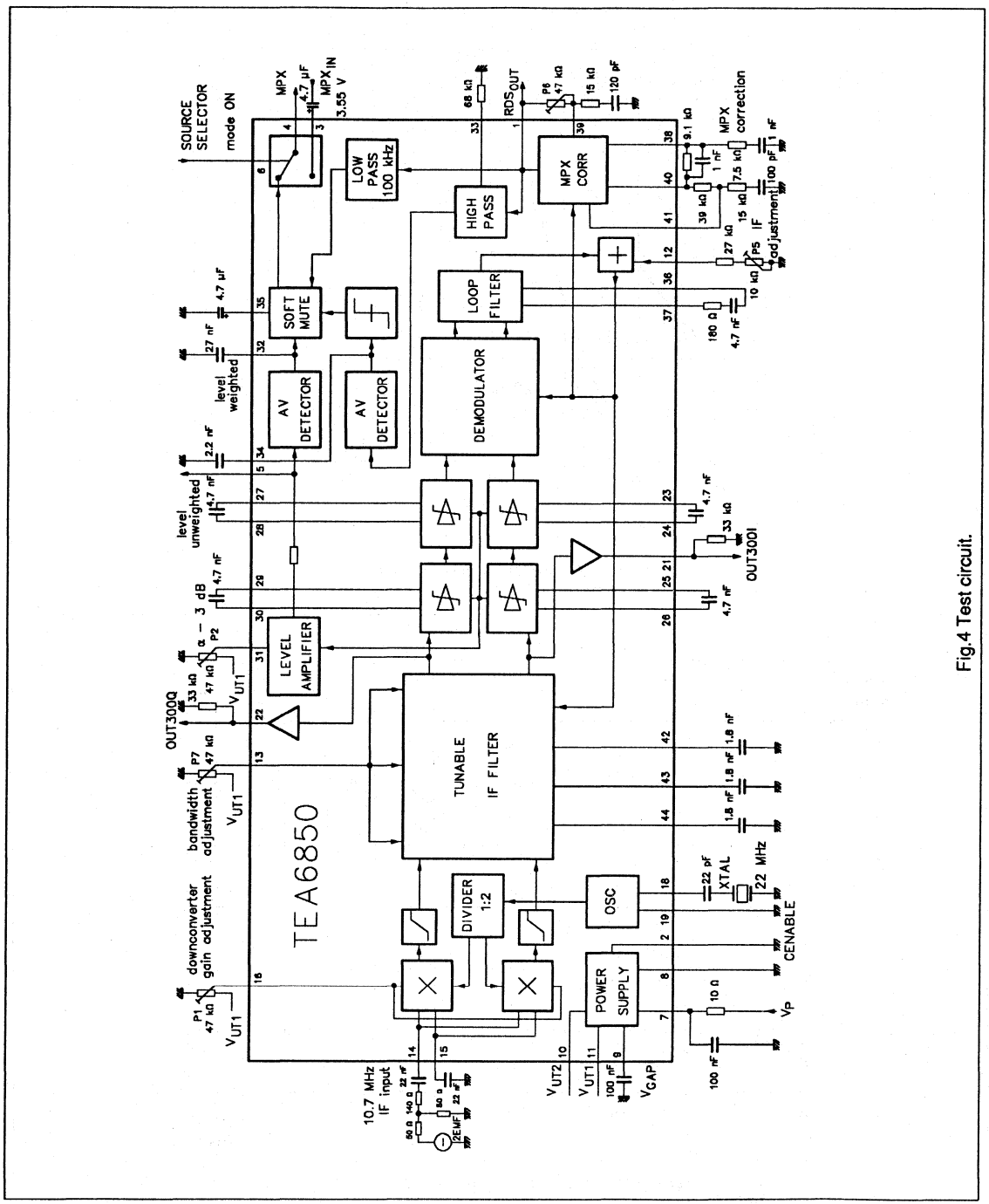


Fig.4 Test circuit.

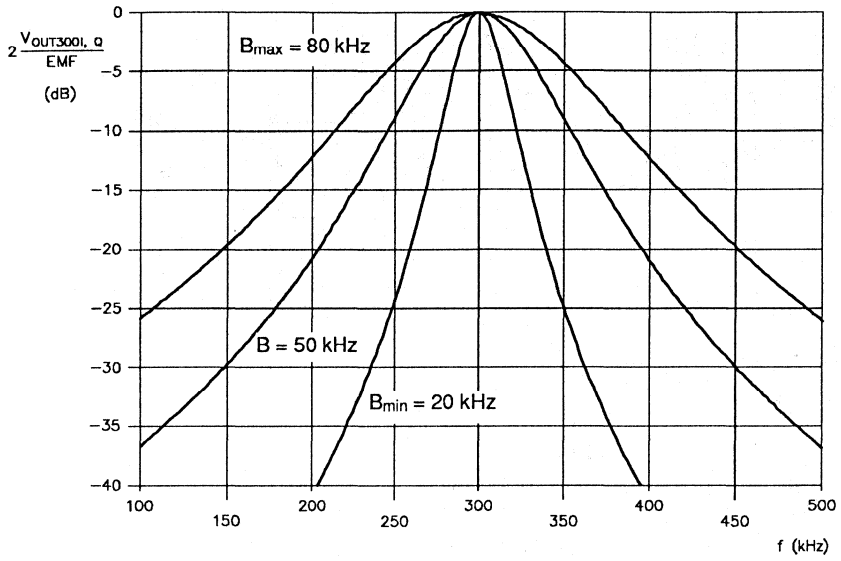


Fig.5 IF filter frequency response.

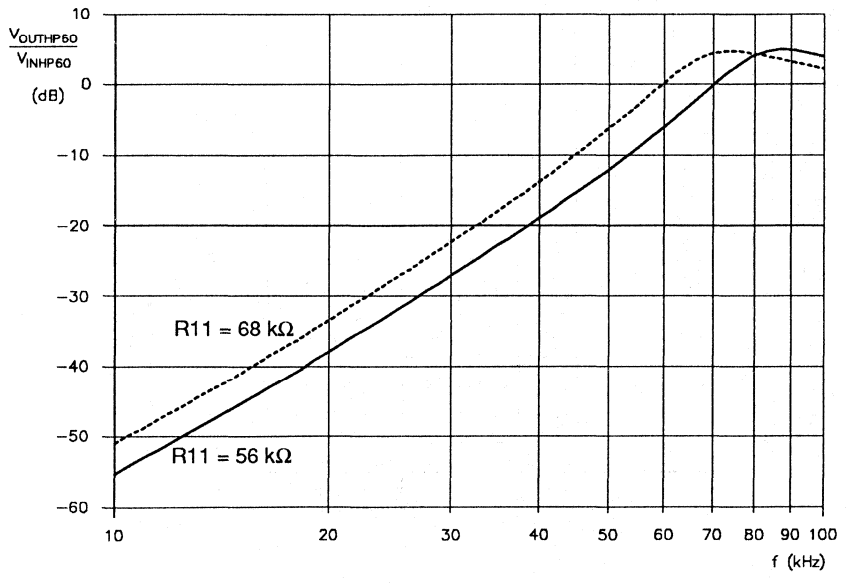


Fig.6 High-pass frequency response (see Fig.1).

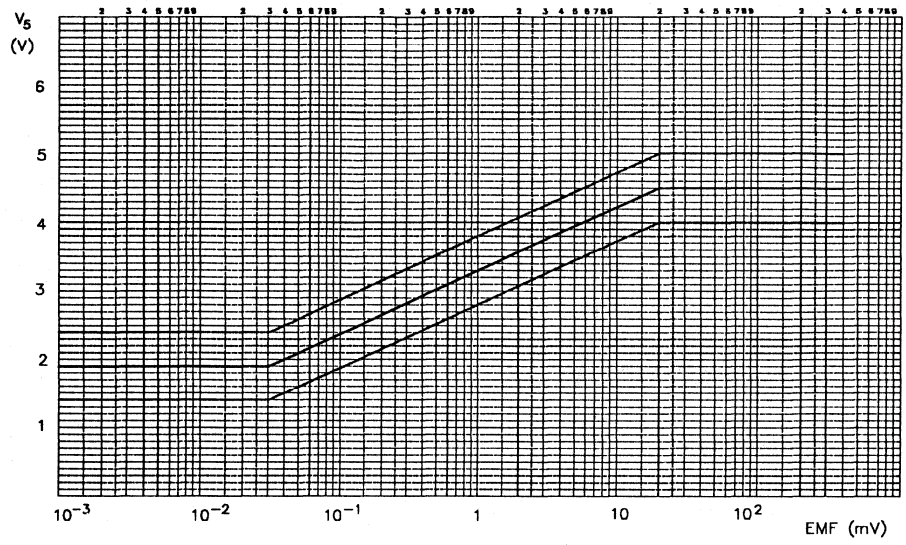


Fig.7 LEVELAMP output voltage.

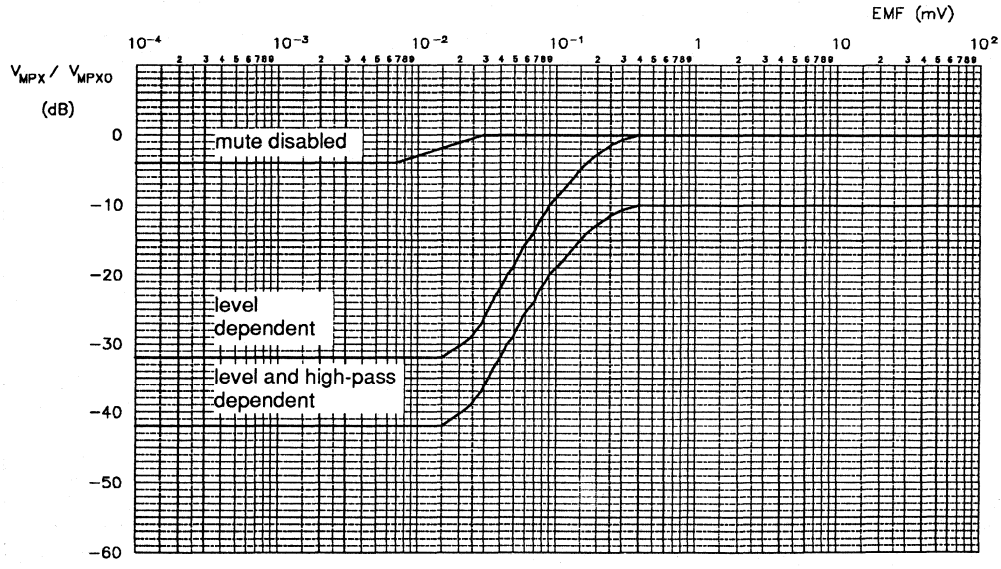


Fig.8 Soft mute curve.

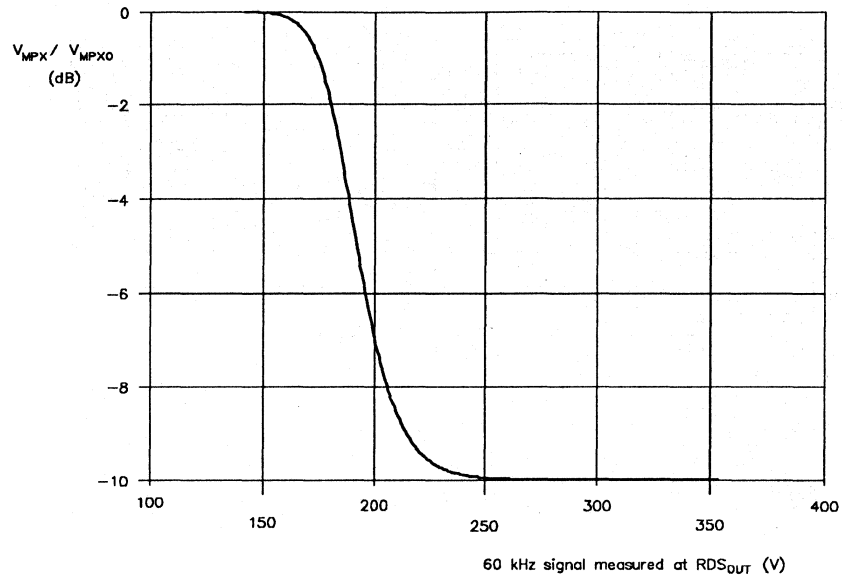


Fig.9 High-pass mute curve.

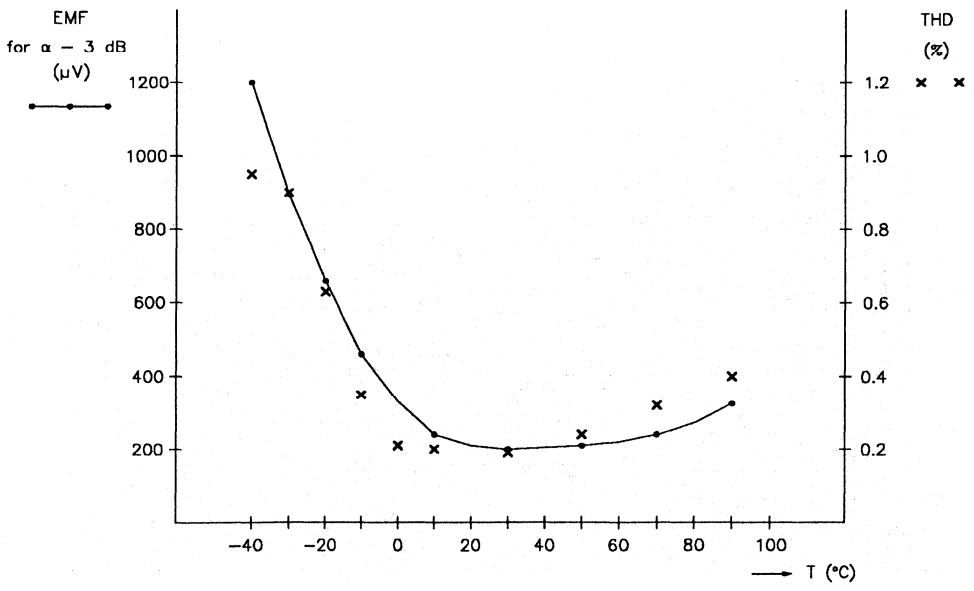


Fig.10 Temperature dependence of α − 3 dB and THD.

APPENDIX

Alignment procedure for the test circuit (see Fig.4)

1. Connect a spectrum analyser to pin 21 or pin 22. Set centre frequency to 300 kHz and frequency span from 200 kHz to 400 kHz.
2. Set frequency of RF-generator to 10.7 MHz, EMF-level to 4 mV RMS, modulation frequency to 1 kHz and frequency deviation to 75 kHz.
3. Turn poti P7 in the mid position. Align centre frequency of the tunable IF-filter with poti P5. The alignment is correct, if the spectrum measured at pin 21 is symetric.
4. Set frequency deviation of RF-generator to zero (EMF = 4 mV RMS). Align the downconverter gain with poti P1. The alignment is correct, if the level at pin 21 is 2 mV RMS.
5. Short pin 36 and pin 37. Set frequency of RF-generator to 10.6 MHz respectively 10.8 MHz (EMF = 4 mV RMS, $\Delta f = 0$). Align bandwidth of the tunable IF-filter with poti P7. The alignment is correct, if the level measured at 200 kHz respectively 400 kHz is 21 dB below the maximum. Remove the short.
6. Set frequency of the RF-generator to 10.7 MHz, EMF-level to 20 mV RMS, modulation frequency to 1 kHz and frequency deviation to 22.5 kHz. Measure level of the 1 kHz signal at pin 4. Set the EMF-level to 200 μV. Align start of mute ($\alpha - 3$ dB) with poti P2.
7. Set EMF-level back to 20 mV RMS and vary the modulation frequency. Align MPX output voltage ripple (see ΔV_O in the AC CHARACTERISTICS) with poti P6.

RADIO TUNING PLL FREQUENCY SYNTHESIZER

GENERAL DESCRIPTION

The TSA6057/6057T is a bipolar single chip frequency synthesizer manufactured in SUBILO-N technology (components laterally separated by oxide). It performs all the tuning functions of a PLL radio tuning system. The IC is designed for application in all types of radio receivers.

Features

- On-chip AM and FM prescalers with high input sensitivity
- On-chip high performance one input (two output) tuning voltage amplifier for the AM and FM loop filters
- On-chip 2-level current amplifier (charge pump) to adjust the loop gain
- Only one reference oscillator (4 MHz) for both AM and FM
- High speed tuning due to a powerful digital memory phase detector
- 40 kHz output reference frequency for co-operation with the FM/IF system and microcomputer-based tuning interface IC (TEA6100)
- Oscillator frequency ranges of: 512 kHz to 30 MHz and 30 MHz to 150 MHz
- Three selectable reference frequencies of 1 kHz, 10 kHz or 25 kHz for both tuning ranges
- Serial 2-wire I^2C-bus interface to a microcomputer and one programmable address input
- Software controlled bandswitch output

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage						
pin 3		$V_{CC1} = V_{3-4}$	4.5	5.0	5.5	V
pin 16		$V_{CC2} = V_{16-4}$	V_{CC1}	8.5	12	V
Supply current	no outputs loaded					
pin 3		I_3	12	20	28	mA
pin 16		I_{16}	0.7	1.0	1.3	mA
Max. input frequency on AM_I		f_{iAM}	30	–	–	MHz
Min. input frequency on AM_I		f_{iAM}	–	–	0.512	MHz
Max. input frequency on FM_I		f_{iFM}	150	–	–	MHz
Min. input frequency on FM_I		f_{iFM}	–	–	30	MHz
Input voltage on AM_I (RMS value)	$V_{iFM} = 0$ V	$V_{iAM(rms)}$	30	–	500	mV
Input voltage on FM_I (RMS value)	$V_{iAM} = 0$ V	$V_{iFM(rms)}$	20	–	300	mV
Total power dissipation		P_{tot}	–	0.14	–	W
Operating ambient temperature range		T_{amb}	–30	–	+ 85	°C

PACKAGE OUTLINES

TSA6057: 16-lead DIL; plastic (SOT38).
TSA6057T: 16-lead minipack; plastic (SO16L; SOT162A).

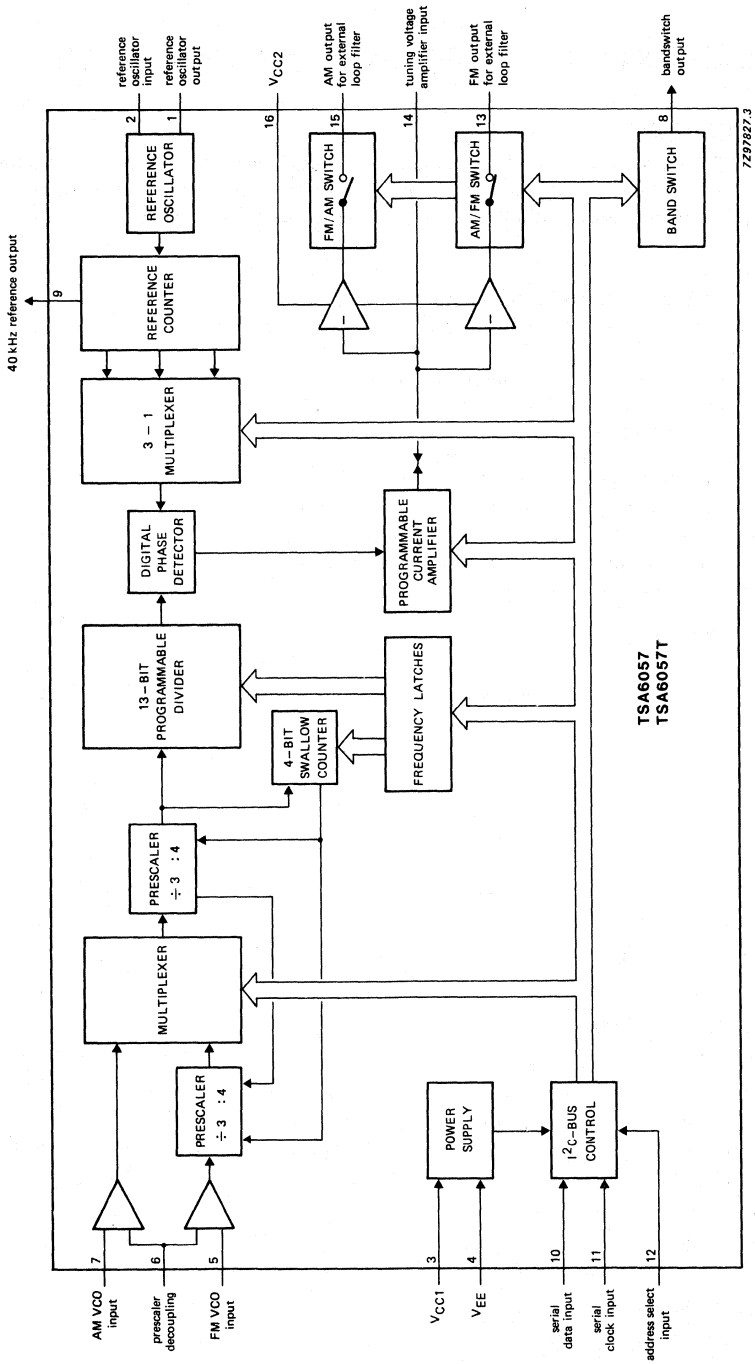


Fig.1 Block diagram.

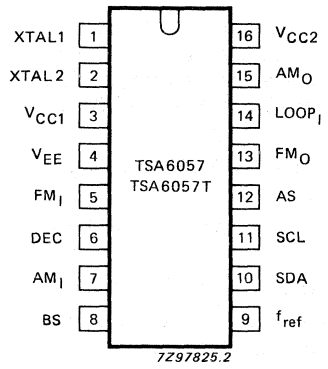


Fig.2 Pinning diagram.

PINNING

1	XTAL1	reference oscillator output
2	XTAL2	reference oscillator input
3	V_{CC1}	positive supply voltage
4	V_{EE}	ground
5	FM_I	FM VCO input
6	DEC	prescaler decoupling
7	AM_I	AM VCO input
8	BS	bandswitch output
9	f_{ref}	40 kHz reference output
10	SDA	serial data input (I²C-bus)
11	SCL	serial clock input (I²C-bus)
12	AS	address select input (I²C-bus)
13	FM_O	FM output for external loop filter
14	$LOOP_I$	tuning voltage amplifier input
15	AM_O	AM output for external loop filter
16	V_{CC2}	positive supply voltage

FUNCTIONAL DESCRIPTION

The TSA6057/6057T contains the following parts and facilities:

- Separate input amplifiers for the AM and FM VCO-signals.
- A prescaler with the divisors 3:4 on AM and 15:16 on FM, a multiplexer to select AM or FM and a 4-bit programmable swallow counter.
- A 13-bit programmable counter.
- A digital memory phase detector.
- A reference frequency channel comprised of a 4 MHz crystal oscillator followed by a reference counter. The reference frequency can be 1 kHz, 10 kHz or 25 kHz and is applied to the digital memory phase detector. The reference counter also outputs a 40 kHz reference frequency to pin 9 for co-operation with the FM/IF system and microcomputer-based tuning interface IC (TEA6100).
- A programmable current amplifier (charge pump) which consists of a 5 μA and a 450 μA current source. This allows adjustment of loop gain, thus providing high current-high speed tuning and low current-stable tuning.
- A one input – two output tuning voltage amplifier. One output is connected to the external AM loop filter and the other output to the external FM loop filter. Under software control, the AM output is switched to a high impedance state by the FM/AM switch in the FM position and the FM output is switched to a high impedance state by the AM/FM switch in the AM position. The outputs can deliver a tuning voltage of up to 10.5 V.
- An I²C-bus interface with data latches and control logic. The I²C-bus is intended for communication between microcontrollers and different ICs or modules. Detailed information on the I²C-bus specification is available on request.
- A software-controlled bandswitch output.

FUNCTIONAL DESCRIPTION (continued)

Controls

The TSA6057/6057T is controlled via the 2-wire I^2C-bus. For programming there is one module address, a logic 0 R/W bit, a subaddress byte and four data bytes. The subaddress determines which one of the four data bytes is transmitted first. The module address contains a programmable address bit (D1) which with address select input AS (pin 12) makes it possible to operate two TSA6057s in one system.

The auto increment facility of the I^2C-bus allows programming of the TSA6057/6057T within one transmission (address + subaddress + 4 data bytes).

- The TSA6057/6057T can also be partially programmed. Transmission must then be ended by a stop condition.

The bit organization of the 4 data bytes is shown in Fig.3 and are described in sections (a) to (f).

(a) The bits S0 to S16 (DB0: D7-D1; DB1: D7-D0; DB2: D1-D0) together with bit FM/AM (DB2: D5) are used to set the divisor of the input frequency at inputs AM_I (pin 7) or FM_I (pin 5). If the system is in lock the following is valid:

FM/$\overline{AM}$	input frequency (f_i)	input
0	$(S0 \times 2^0 + S1 \times 2^1 \ldots\ldots + S13 \times 2^{13} + S14 \times 2^{14}) \times f_{ref}$	AM_I
1	$(S0 \times 2^0 + S1 \times 2^1 \ldots\ldots + S15 \times 2^{15} + S16 \times 2^{16}) \times f_{ref}$	FM_I

Where

The minimum dividing ratio for AM mode is $2^6 = 64$
The minimum dividing ratio for FM mode is $2^8 = 256$

(b) The bit CP is used to control the charge pump current (DB0: D0).

CP	current
0	low
1	high

(c) The bits REF1 and REF2 are used to set the reference frequency applied to the phase detector (DB2: D7-D6).

REF1	REF2	frequency (kHz)
0	0	1
0	1	10
1	0	25
1	1	none

(d) The bit $\overline{FM}$/AM OPAMP controls the switch AM/FM; FM/AM in the tuning voltage amplifier output circuitry (DB2: D4).

$\overline{FM}$/AM OPAMP	switch FM/AM	switch AM/FM
1	closed	open
0	open	closed

(e) The bit BS controls the open collector bandswitch output (DB2: D2).

BS	bandswitch output
1	sink current
0	floating

(f) The data byte DB3 must be set to 0 . . . . . 0. It is also used for test purposes.

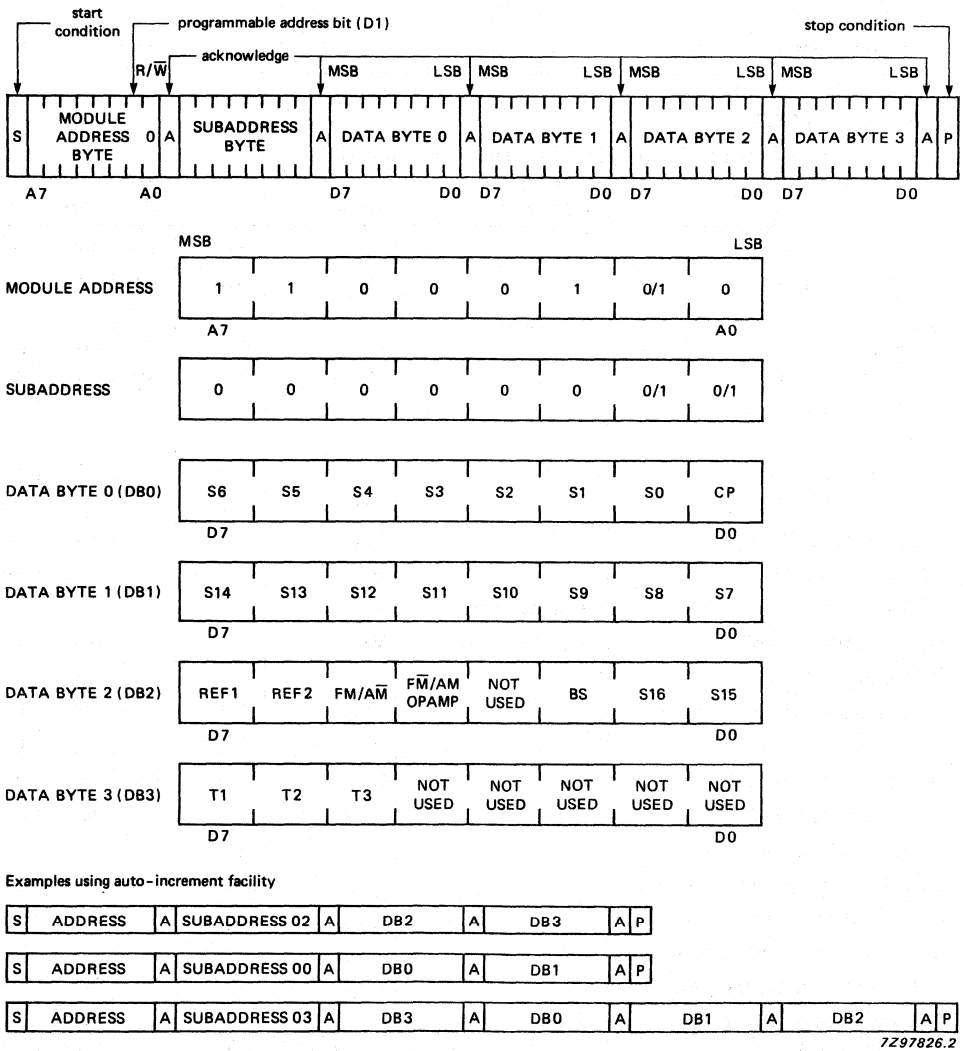


Fig.3 Bit organization.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage (pin 3)	$V_{CC1} = V_{3-4}$	−0.3	5.5	V
Supply voltage (pin 16)	$V_{CC2} = V_{16-4}$	V_{CC1}	12.5	V
Total power dissipation	P_{tot}	−	0.85	W
Operating ambient temperature	T_{amb}	−30	+ 85	°C
Storage temperature range	T_{stg}	−65	+ 150	°C

CHARACTERISTICS

V_{CC1} = 5 V; V_{CC2} = 8.5 V; T_{amb} = 25 °C; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage (pin 3)		V_{CC1}	4.5	5.0	5.5	V
Supply voltage (pin 16)		V_{CC2}	V_{CC1}	8.5	12	V
Supply current	no outputs loaded					
pin 3		I_{CC1}	12	20	28	mA
pin 16		I_{CC2}	0.7	1.0	1.3	mA
I²C-bus inputs (SDA; SCL)						
Input voltage HIGH		V_{IH}	3.0	−	5.0	V
Input voltage LOW		V_{IL}	−0.3	−	1.5	V
Input current HIGH		I_{IH}	−	−	10	μA
Input current LOW		I_{IL}	−	−	10	μA
SDA output	open collector					
Output voltage LOW	I_{OL} = 3.0 mA	V_{OL}	−	−	0.4	V
AS input						
Input voltage HIGH		V_{IH}	3.0	−	5.0	V
Input voltage LOW		V_{IL}	−0.3	−	1.0	V
Input current HIGH		I_{IH}	−	−	10	μA
Input current LOW		I_{IL}	−	−	10	μA
RF input (AM; FM)						
Max. input frequency on AM_I		f_{iAM}	30	−	−	MHz
Min. input frequency on AM_I		f_{iAM}	−	−	0.512	MHz
Max. input frequency on FM_I		f_{iFM}	150	−	−	MHz
Min. input frequency on FM_I		f_{iFM}	−	−	30	MHz
Input voltage on AM_I (RMS value)	V_{iFM} = 0 V measured in Fig.4	$V_{iAM(rms)}$	30	−	500	mV
Input impedance AM_I						
resistance		R_{AM}	−	5.9	−	kΩ
capacitance		C_{AM}	−	2	−	pF

parameter	conditions	symbol	min.	typ.	max.	unit
RF input (continued)						
Input voltage on FM_I (RMS value)	V_{iAM} = 0 V measured in Fig.4	$V_{iFM(rms)}$	20	–	300	mV
Input impedance FM_I						
resistance		R_{FM}	–	3.6	–	kΩ
capacitance		C_{FM}	–	2	–	pF
Oscillator (XTAL1; XTAL2)						
Crystal resonance resistance (4 MHz)	see Fig.5	R_{XTAL}	–	–	150	Ω
Programmable charge pump						
Output current to loop filter						
bit CP = logic 0		I_{chp}	3	5	7	μA
bit CP = logic 1		I_{chp}	400	500	600	μA
Ripple rejection	f_{ripple} = 100 Hz					
20 log $\Delta V_{CC1}/\Delta V_O$		RR	40	50	–	dB
20 log $\Delta V_{CC2}/\Delta V_O$		RR	40	50	–	dB
Bandswitch output (pin 8)						
Output voltage HIGH		V_{OH}	–	–	12	V
Output voltage LOW	I_{OL} = 3 mA	V_{OL}	–	–	0.8	V
Output leakage current	V_{OH} = 12 V	I_{LO}	–	–	10	μA
Reference frequency output (pin 9)						
Output frequency	4 MHz crystal	f_{ref}	–	40	–	kHz
Output voltage HIGH	I_{source} = 5 μA	V_{OH}	1.2	1.4	1.7	V
Output voltage LOW		V_{OL}	–	0.1	0.2	V
Tuning voltage amplifier outputs						
AM output (pin 15)						
max. output voltage	I_{source} = 0.5 mA	$V_{O(max)}$	V_{CC2} −1.5	–	–	V
min. output voltage	I_{sink} = 1 mA	$V_{O(min)}$	–	–	0.8	V
max. output source current		I_{source}	0.5	–	–	mA
max. output sink current		I_{sink}	1.0	–	–	mA
FM output (pin 13)						
max. output voltage	I_{source} = 0.5 mA	$V_{O(max)}$	V_{CC2} −1.5	–	–	V
min. output voltage	I_{sink} = 1 mA	$V_{O(min)}$	–	–	0.8	V
max. output source current		I_{source}	0.5	–	–	mA
max. output sink current		I_{sink}	1.0	–	–	mA
Impedance of switched off output		$Z_{O(off)}$	5	–	–	MΩ
Input bias current (absolute value)		I_{bias}	–	1	5	nA

SENSITIVITY MEASUREMENT

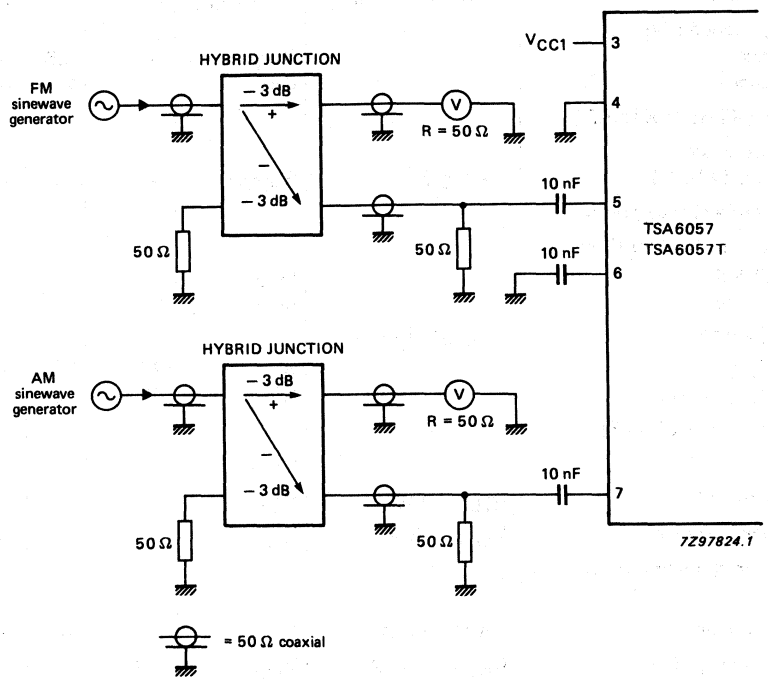


Fig.4 Prescaler input sensitivity.

APPLICATION INFORMATION

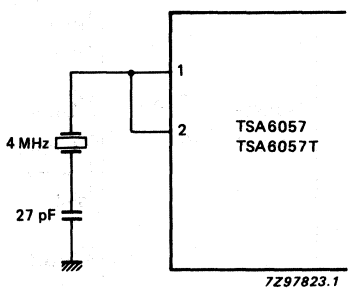


Fig.5 Crystal connection (4 MHz).

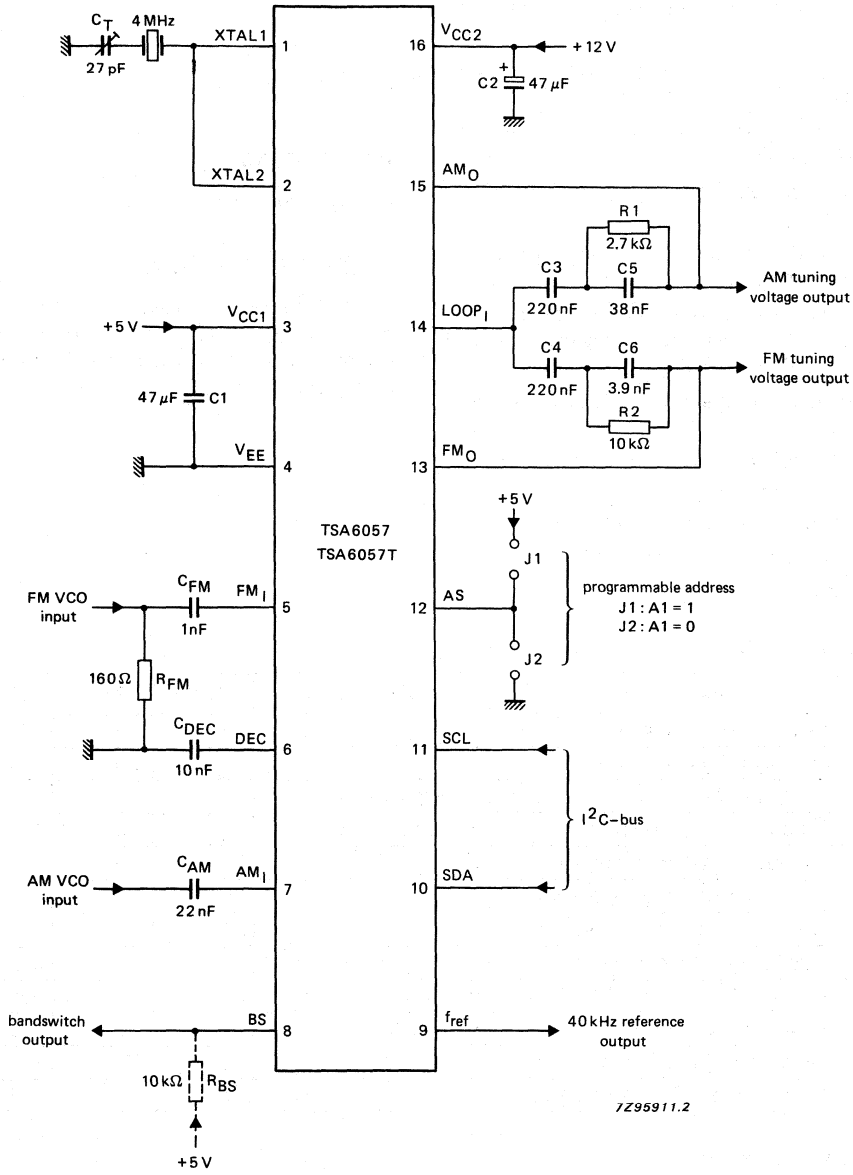


Fig.6 Application diagram

Fast radio tuning PLL frequency synthesizer

TSA6060

FEATURES

- On-chip AM and FM prescalers with high input sensitivity
- On-chip high-performance one-input-two-output, tuning voltage amplifier for the AM and FM loop filters
- On-chip two-level current amplifier (charge pump) for loop gain adjustment
- One reference oscillator (4 or 8 MHz) for both AM and FM
- High-speed tuning provided by a powerful digital memory phase detector
- 40 kHz output reference frequency for communication between the FM/IF system and microcontroller-based tuning interface IC (TEA6100)
- Oscillator frequency range of 500 kHz to 30 MHz and 30 MHz to 200 MHz
- Four selectable reference frequencies: 1, 10, 25 or 50 kHz, for both tuning ranges
- I²C-bus interface to a microcontroller
- Software controlled band switch output
- In-lock detector output.

APPLICATIONS

- All types of radio receivers.

GENERAL DESCRIPTION

The TSA6060 is a single-chip frequency synthesizer manufactured in SUBILO-N technology (components laterally separated by oxide). The device performs all the tuning functions of a PLL radio tuning system.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC1}	supply voltage (pin 3)		4.5	5.0	5.5	V
V_{CC2}	supply voltage (pin 16)		V_{CC1}	8.5	12.0	V
I_{CC1}	supply current (pin 3)	no outputs loaded	–	15	–	mA
I_{CC2}	supply current (pin 16)	no outputs loaded	0.7	1.0	1.5	mA
f_{iAMmax}	maximum AM input frequency		30	–	–	MHz
f_{iAMmin}	minimum AM input frequency		–	–	500	kHz
f_{iFMmax}	maximum FM input frequency		200	–	–	MHz
f_{iFMmin}	minimum FM input frequency		–	–	30	MHz
$V_{iAM(rms)}$	AM input voltage (RMS value)	V_{iFM} = 0 V; f_i < 15 MHz	30	–	500	mV
$V_{iFM(rms)}$	FM input voltage (RMS value)	V_{iAM} = 0 V	20	–	300	mV
P_{tot}	total power dissipation		–	100	–	mW
T_{amb}	operating ambient temperature		–40	–	+85	°C

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TSA6060	16	DIL16	plastic	SOT38
TSA6060T	16	SO16	plastic	SOT162A

BLOCK DIAGRAM

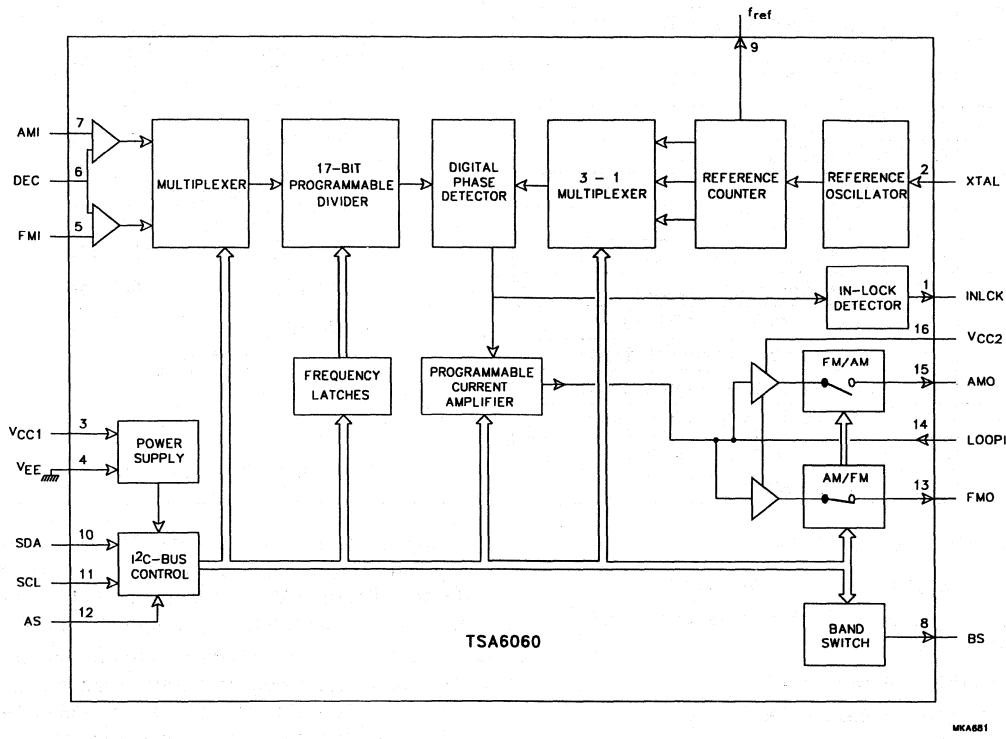


Fig.1 Block diagram.

Fast radio tuning PLL frequency synthesizer

TSA6060

PINNING

SYMBOL	PIN	DESCRIPTION
INCLK	1	in-lock detector output
XTAL	2	crystal reference oscillator input
V_{CC1}	3	supply voltage (+5 V)
V_{EE}	4	ground
FM_I	5	FM VCO input
DEC	6	prescaler decoupling
AM_I	7	AM VCO input
BS	8	band switch output
f_{ref}	9	40 kHz reference output
SDA	10	serial data input (I^2C-bus)
SCL	11	serial clock input (I^2C-bus)
AS	12	address select input (I^2C-bus)
FM_O	13	FM output for external loop filter
$LOOP_I$	14	tuning voltage amplifier input
AM_O	15	AM output for external loop filter
V_{CC2}	16	supply voltage (+12 V)

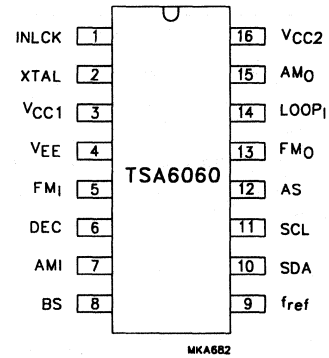


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The TSA6060 contains the following parts:

- Separate input amplifiers for the AM and FM VCO signals.
- A 17-bit programmable counter.
- A digital memory phase detector.
- A reference frequency channel which contains a 4 MHz or 8 MHz cyrstal oscillator which is followed by a reference counter. The reference frequency can be either 1, 5, 10 or 50 kHz and is applied to the digital memory phase detector. The reference counter can also output a 40 kHz reference frequency to pin 9 for communication between the FM/IF system and the microcontroller-based tuning interface IC (TEA6100).
- A programmable current amplifier (charge pump) which consists of a 25 mA and a 500 mA current source. This allows adjustment of the loop gain thereby providing high-current high-speed tuning and low-current stable tuning.
- A one-input-two-output tuning voltage amplifier. One output is connected to the external AM loop filter and the other output to the external FM loop filter. Under software control, the AM output is switched to a low impedance to ground by the FM/AM switch in the FM position. The FM output is switched to a low impedance to ground by the AM/FM switch in the AM position. The outputs can deliver a tuning voltage of up to 10.5 V.
- An I^2C-bus interface with data latches and control logic. The I^2C-bus is intended for communication between microcontrollers and different ICs or modules. Detailed information concerning the I^2C-bus specification is available on request.
- A software controlled band switch output.

Controls

The TSA6060 is controlled via the 2-wire I^2C-bus. For programming there is one module address, a logic 0 ($R/\overline{W}$ bit) and four data bytes. The module address contains an address select bit (AS) which enables two TSA6060s to be operated in one system.

The auto-increment facility of the I^2C-bus allows programming of the TSA6060 within one transmission (address + 4 data bytes).

The TSA6060 can also be partially programmed. Transmission must then be ended by a stop condition.

The bit organization of the 4 data bytes is shown in Fig.3. Further information is given in Tables 2, 3, 4 and 5.

The bits S0 to S16 (DB0: D7 to D1; DB1: D7 to D0; DB2: D1 to D0) together with bit FM/AM (DB2: D5) are used to set the divider of the input frequency at inputs AM_I (pin 7) or FM_I (pin 5). If the system is in-lock the following is valid, as shown in Table 1.

Table 1 System-in-lock (note 1).

FM/$\overline{AM}$	INPUT FREQUENCY (f_I)	INPUT
0	$(S2 \times 2^0 + S3 \times 2^1 ..... + S15 \times 2^{13} + S16 \times 2^{14}) \times f_{ref}$	AM
1	$(S0 \times 2^0 + S1 \times 2^1 ..... + S15 \times 2^{15} + S16 \times 2^{16}) \times f_{ref}$	FM

Note

1. The minimum dividing ratio for the AM mode is $2^6 = 64$ and for the FM mode is $2^8 = 256$.

Table 2 Bit CP is used to control the charge pump current (DB0: D0).

CP	CURRENT
0	LOW
1	HIGH

Table 3 Bits REF1 and REF2 are used to set the reference frequency applied to the phase detector (DB2: D7 to D6).

REF1	REF2	REFERENCE FREQUENCY (kHZ)
0	0	1
0	1	10
1	0	25
1	1	50

Table 4 Bit $\overline{FM}$/AM OPAMP controls the switch AM/FM, FM/AM in the tuning voltage amplifier circuits (DB2: D4).

$\overline{FM}$/AM OPERATIONAL AMPLIFIER	SWITCH	
	FM/AM	AM/FM
1	closed	open
0	open	closed

Table 5 Bit BS controls the open-collector band switch output (DB2: D2).

BS	BAND SWITCH OUTPUT
1	sink current
0	floating

The bit 8/4 MHz controls a divide-by-1/divide-by-2 divider cell in the reference oscillator section. This allows the use of a 4 MHz or 8 MHz crystal.

Table 6 Test mode.

T3	T2	T1	FUNCTION
0	X	0	normal
1	0	1	CP source
0	1	1	CP sink
1	1	1	CP 3-state
0	0	1	CP sink + source
1	1	X	BS = main divider output
1	0	X	BS = reference divider output

The data byte DB3 must be set to 0.....0. It is also used for test purposes (see Fig.3).

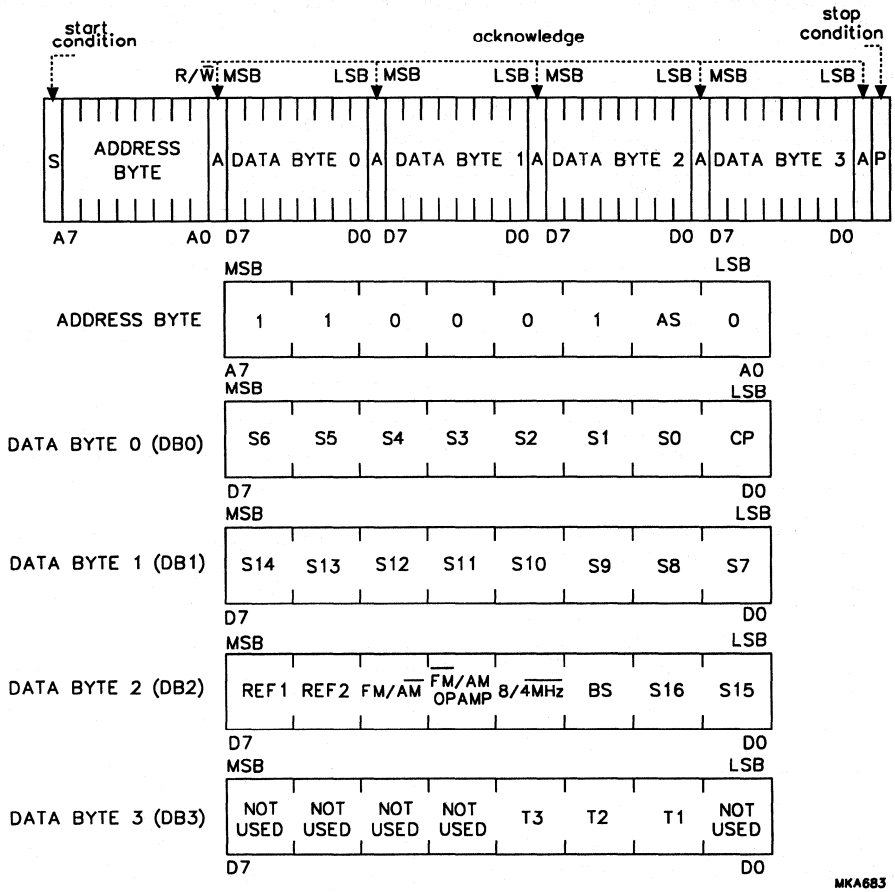


Fig.3 Bit organization.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC !34).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{CC1}	supply voltage (pin 3)	−0.3	+5.5	V
V_{CC2}	supply voltage (pin 16)	V_{CC1}	12.5	V
P_{tot}	total power dissipation	–	850	mW
T_{amb}	operating ambient temperature	−40	+85	°C
T_{stg}	storage temperature	−65	+150	°C
V_{es}	electrostatic handling	−200	+200	V

HANDLING

Classification: machine model; C = 200 pF; R = 0 Ω; V = ±200 V.

CHARACTERISTICS

V_{CC1} = 5 V; V_{CC2} = 8.5 V; T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{CC1}	supply voltage (pin 3)		4.5	5.0	5.5	V
V_{CC2}	supply voltage (pin 16)		V_{CC1}	8.5	12.0	V
I_{CC1}	supply current (pin 3)	no outputs loaded	–	15	–	mA
I_{CC2}	supply current (pin 16)	no outputs loaded	0.7	1.0	1.5	mA
I²C-bus inputs: SDA, SCL (pins 10 and 11)						
V_{IH}	HIGH level input voltage		3.0	–	5.0	V
V_{IL}	LOW level input voltage		−0.3	–	1.5	V
I_{IH}	HIGH level input current		–	–	10	μA
I_{IH}	LOW level input current		–	–	10	μA
SDA output (pin 10)						
V_{OL}	LOW level output voltage	open collector; I_{OL} = 3 mA	–	–	0.4	V
INCLK output (pin 1); see Fig.6; INCLK = HIGH						
V_{OH}	HIGH level output voltage	I_{OH} = −10 μA	V_{CC} − 1	–	V_{CC}	V
V_{OL}	LOW level output voltage	I_{OL} = 1 mA	0	–	0.4	V
RF inputs: AM_I, FM_I (pins 5 and 7)						
f_{iAMmax}	maximum AM input frequency		30	–	–	MHz
f_{iAMmin}	minimum AM input frequency		–	–	500	kHz
f_{iFMmax}	maximum FM input frequency		200	–	–	MHz
f_{iFMmin}	minimum FM input frequency		–	–	30	MHz

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{iAM(rms)}$	AM input voltage (RMS value)	f_i < 15 MHz; measured in Fig.4	30	–	500	mV
		15 MHz < f_i < 30 MHz; measured in Fig.4	40	–	500	mV
R_{iAM}	AM input resistance		–	5.9	–	kΩ
C_{iAM}	AM input capacitance		–	2	–	pF
$V_{iFM(rms)}$	FM input voltage (RMS value)	V_{iAM} = 0 V	20	–	300	mV
R_{iFM}	FM input resistance		–	3.6	–	kΩ
C_{iFM}	FM input capacitance		–	2	–	pF
Oscillator (pin 2)						
R_{xtal}	crystal resonance resistance (4 or 8 MHz)	see Fig.5	–	–	150	Ω
Programmable charge pump						
I_{chp}	output current to loop filter	bit CP = logic 0	20	25	30	µA
		bit CP = logic 1	400	500	600	µA
Ripple rejection						
$SVRR_1$	supply voltage ripple rejection; 20 log $\Delta V_{CC1}/\Delta V_{tune}$	f_{ripple} = 100 Hz	40	50	–	dB
$SVRR_2$	supply voltage ripple rejection; 20 log $\Delta V_{CC2}/\Delta V_{tune}$	f_{ripple} = 100 Hz	40	50	–	dB
Band switch output: BS (pin 8)						
$V_{o(max)}$	maximum output voltage	programmed HIGH	–	–	12	V
V_{OL}	LOW level output voltage	I_{OL} = 3 mA	–	–	0.8	V
$\|I_{OL}\|$	output leakage current	V_{OH} = 12 V	–	–	10	µA
Reference frequency output: f_{ref} (pin 9)						
f_{ref}	reference output frequency		–	40	–	kHz
V_{OH}	HIGH level output voltage	I_{source} = 5 µA	1.2	1.4	1.7	V
V_{OL}	LOW level output voltage	I_{source} = 5 µA	–	0.1	0.2	V
Tuning voltage amplifiers						
AM OUTPUT (PIN 15)						
ΔV_{OH}	HIGH level output voltage swing	I_O = –0.6 mA	V_{CC2} – 0.9	–	–	V
ΔV_{OL}	LOW level output voltage swing	I_O = 0.6 mA	–	–	0.8	V
FM OUTPUT (PIN 13)						
ΔV_{OH}	HIGH level output voltage swing	I_O = –0.6 mA	V_{CC2} – 0.9	–	–	V
ΔV_{OL}	LOW level output voltage swing	I_O = 0.6 mA	–	–	0.8	V
$Z_{o(off)}$	impedance of switched-off output to ground		–	500	–	Ω
$\|I_{bias}\|$	input bias current		–	1	5	nA

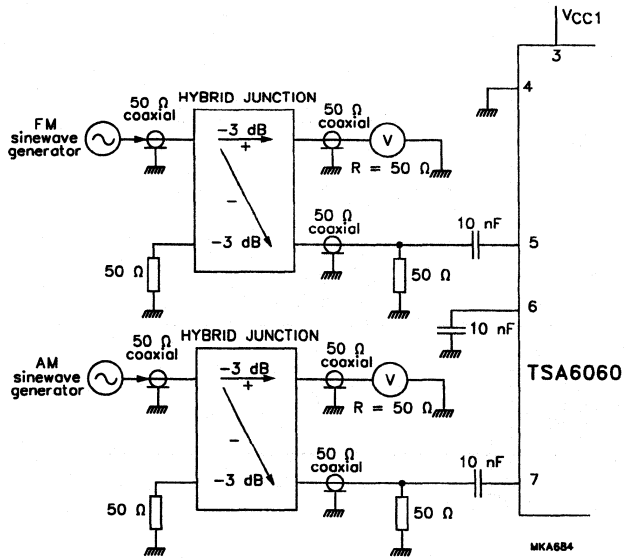


Fig.4 Prescaler input sensitivity.

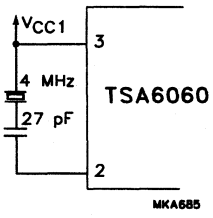


Fig.5 Crystal connection.

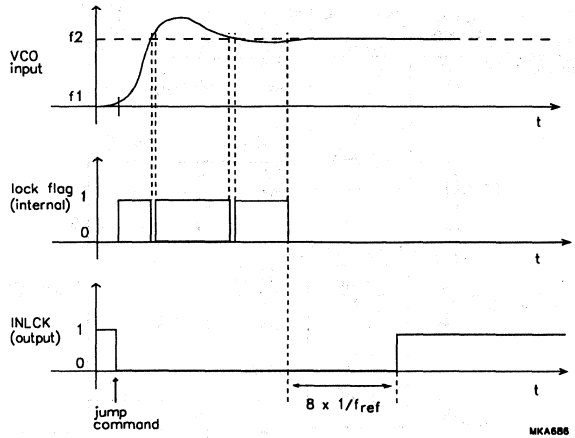


Fig.6 Timing diagram.

APPLICATION INFORMATION

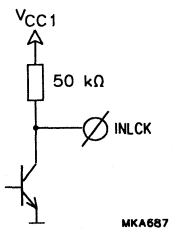
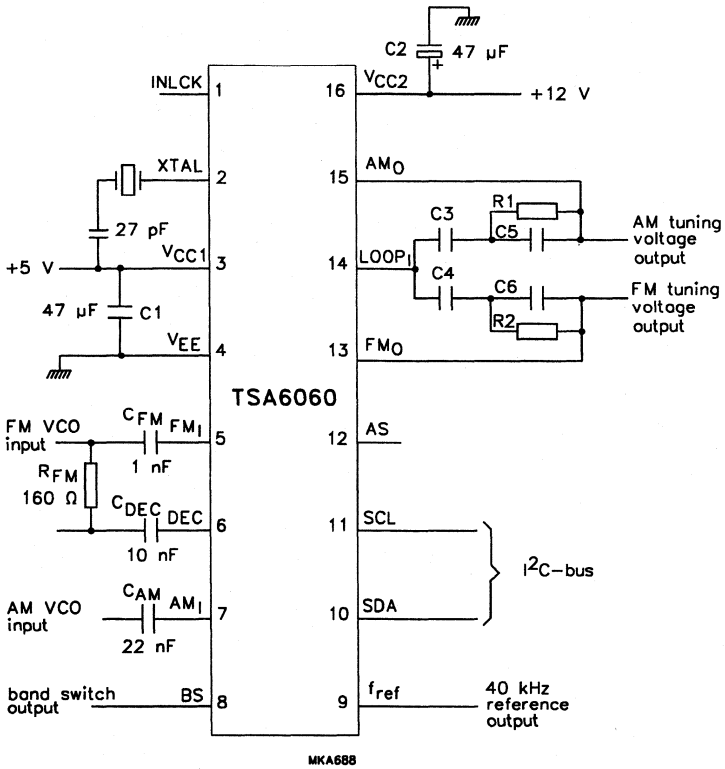


Fig.7 Equivalent output circuit.



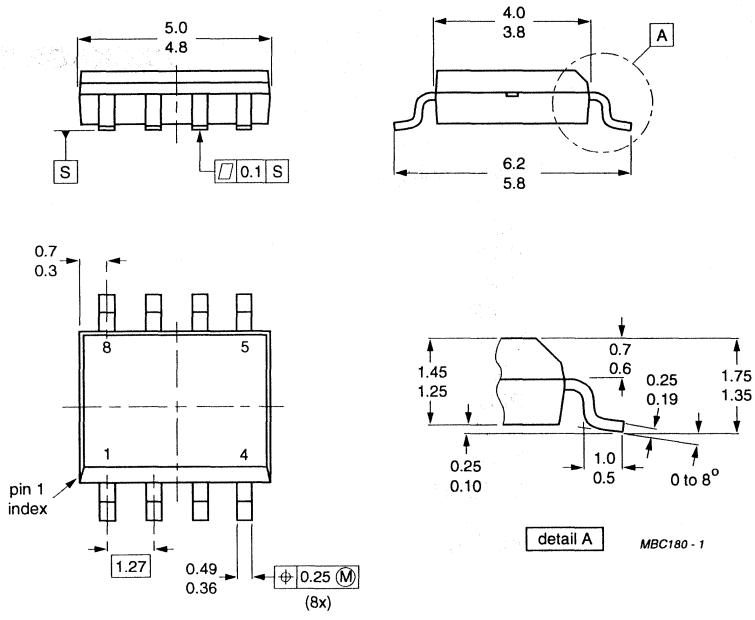
For FM: VCO = 5 MHz/V; R2 = 8.2 kΩ, C4 = 68 nF, C6 = 4.7 nF.
For AM: VCO = 0.75 MHz/V; R1 = 47 kΩ, C3 = 440 nF, C5 = 0.47 nF.

Fig.8 Application example; loop filter dependent on VCO and tuning speed.

PACKAGE INFORMATION

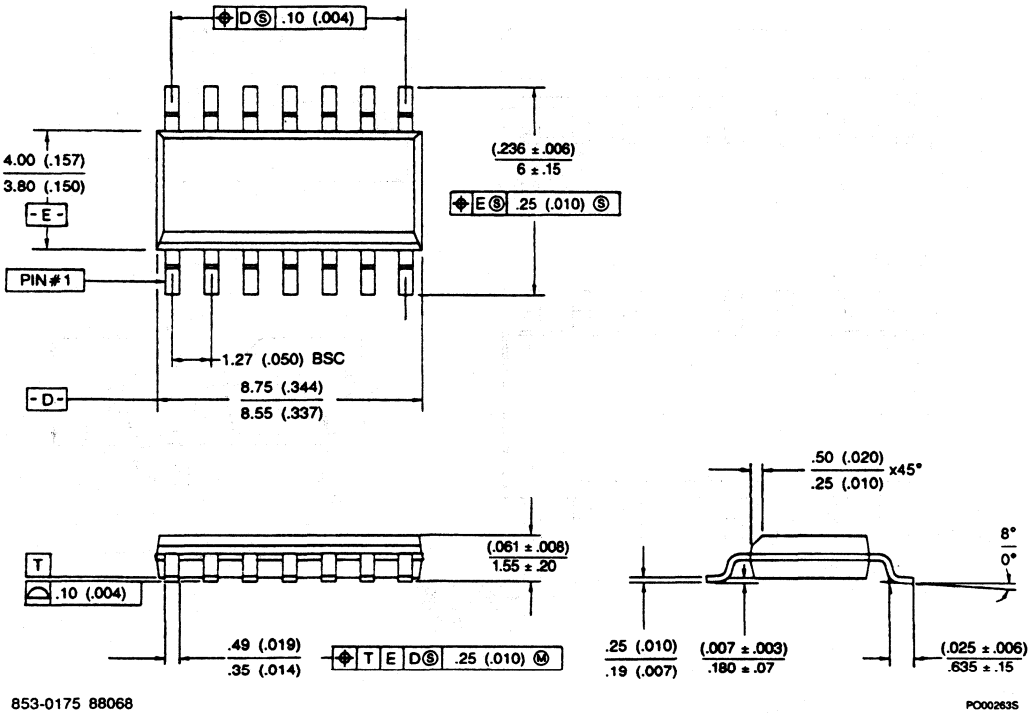
PACKAGE OUTLINES

SO



Dimensions in mm.

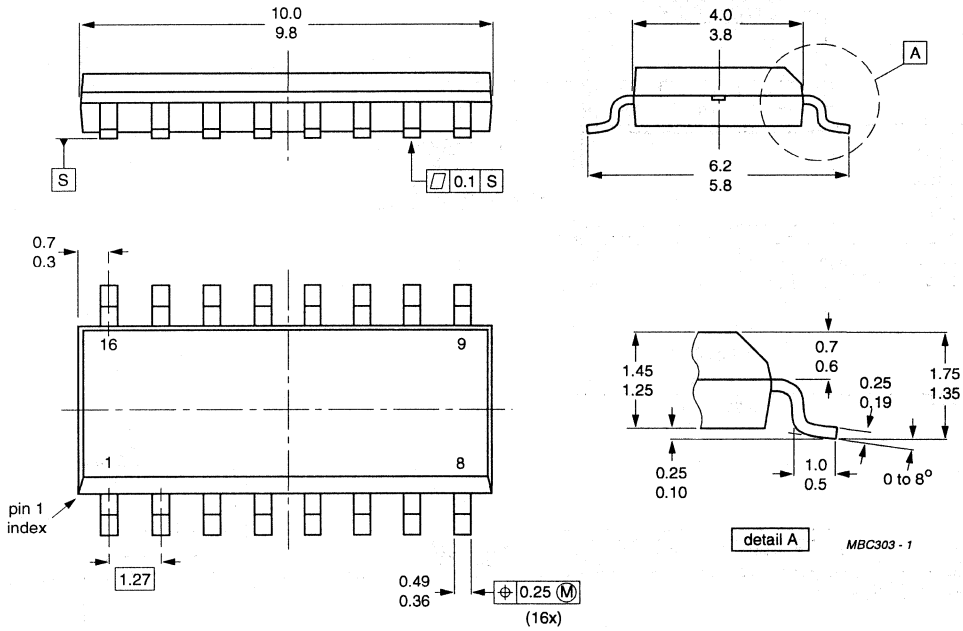
Fig.1 8-lead mini-pack; plastic (SO8; SOT96A).
Plastic small outline package; 8 leads; body width 3.9 mm; SO8; SOT96-1.



NOTES:

1. Package dimensions conform to JEDEC specification MS-012-AB for standard small outline (SO) package, 14 leads, 3.75mm (.150") body width (issue A, June 1985).
2. Controlling dimensions are in mm. Inch dimensions in parentheses.
3. Dimensions and tolerancing per ANSI Y14.5M- 1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .15mm (.006") on any side.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #14 when viewed from top.
6. Signetics ordering code for a product packaged in a plastic small outline (SO) package is the suffix D after the product number.

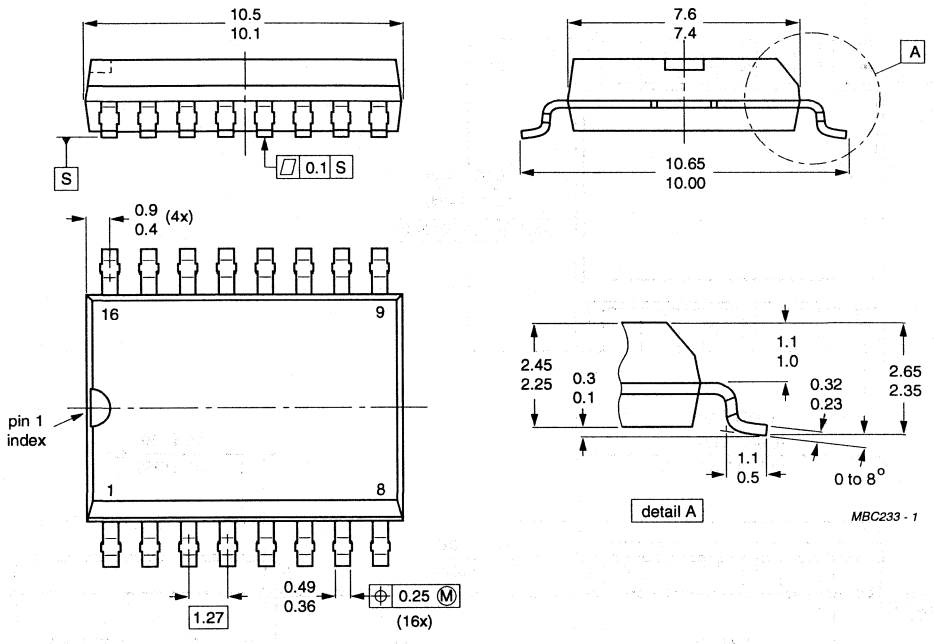
Fig.2 14-lead mini-pack; plastic; SO14 (D package).



Dimensions in mm.

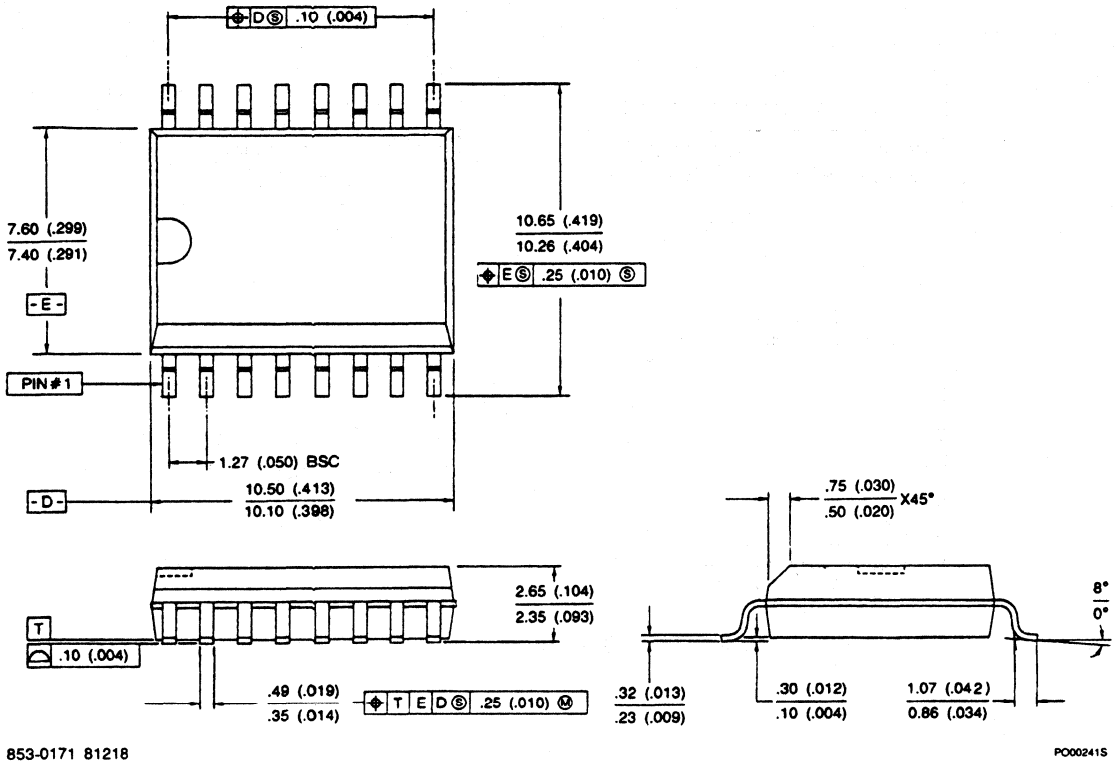
Fig.3 16-lead mini-pack; plastic (SO16; SOT109A).
Plastic small outline package; 16 leads; body width 3.9 mm; SO16; SOT109-1.

Package information



Dimensions in mm.

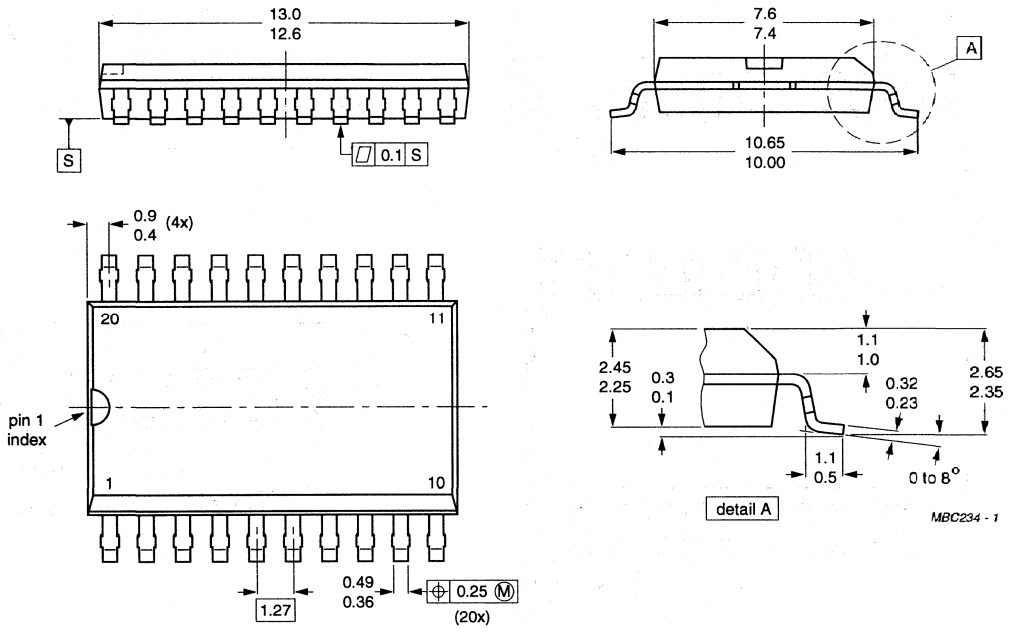
Fig.4 16-lead mini-pack; plastic (SO16L; SOT162A).
Plastic small outline package; 16 leads; body width 7.5 mm; SO16; SOT162-1.



NOTES:

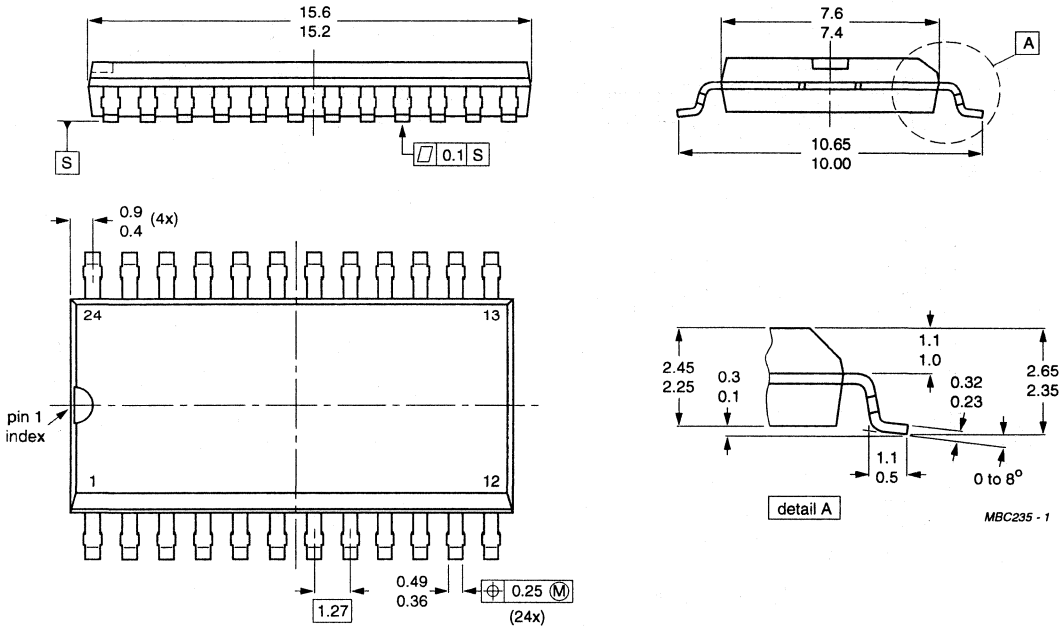
1. Package dimensions conform to JEDEC specification MS-013-AA for standard small outline (SO) package, 16 leads, 7.50mm (.300") body width (issue A, June 1985).
2. Controlling dimensions are in mm. Inch dimensions in parentheses.
3. Dimensions and tolerancing per ANSI Y14.5M- 1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .15mm (.006") on any side.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #16 when viewed from top.
6. Signetics ordering code for a product packaged in a plastic small outline (SO) package is the suffix D after the product number.

Fig.5 16-lead mini-pack; plastic; SO16L (D package).



Dimensions in mm.

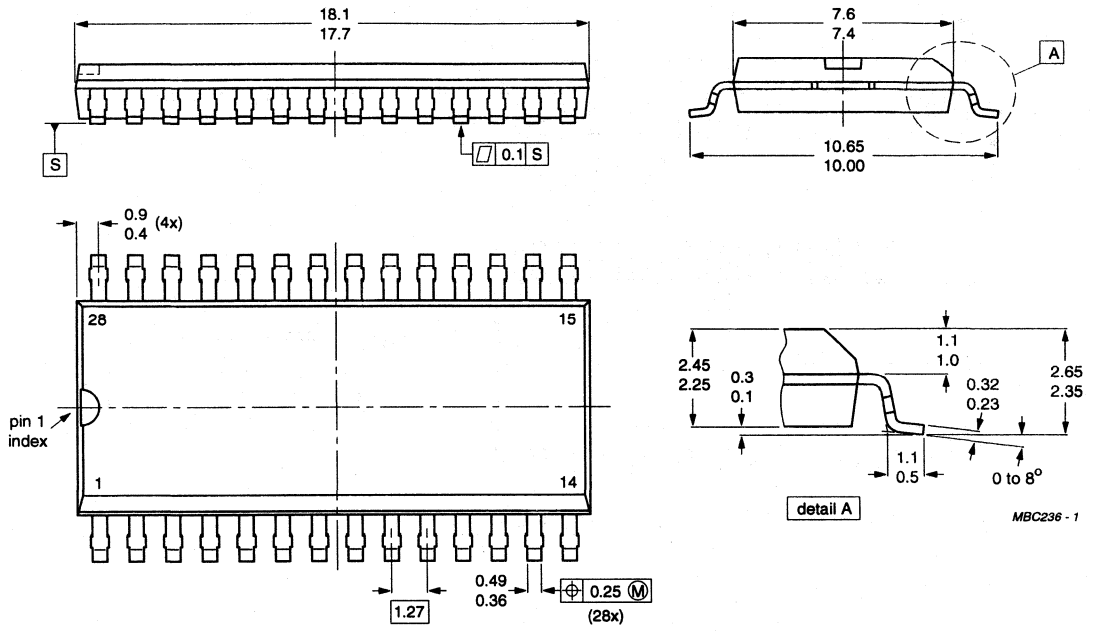
Fig.6 20-lead mini-pack; plastic (SO20; SOT163A).
Plastic small outline package; 20 leads; body width 7.5 mm; SO20; SOT163-1.



Dimensions in mm.

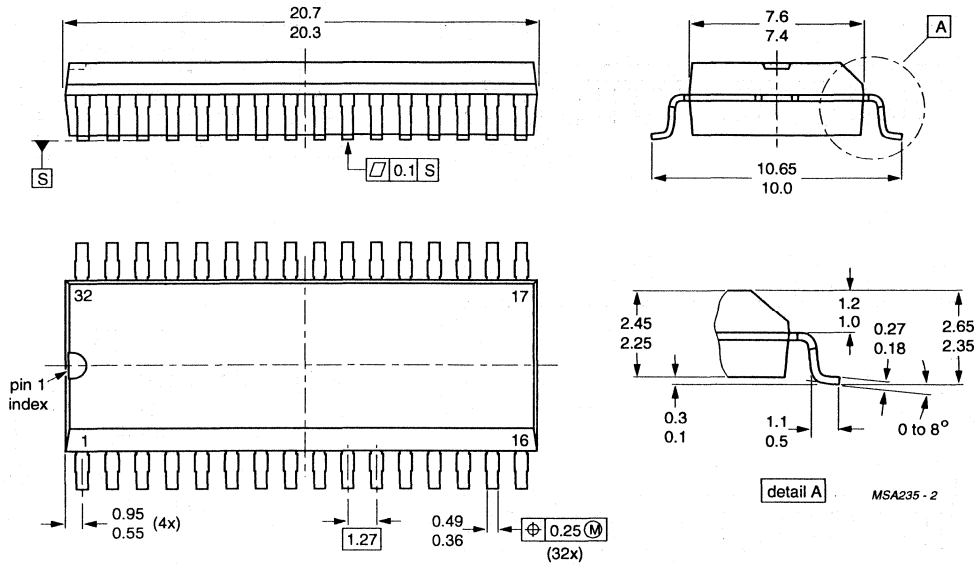
Fig.7 24-lead mini-pack; plastic (SO24; SOT137A).
Plastic small outline package; 24 leads; body width 7.5 mm; SO24; SOT137-1.

Package information



Dimensions in mm.

Fig.8 28-lead mini-pack; plastic (SO28; SOT136A).
Plastic small outline package; 28 leads; body width 7.5 mm; SO28; SOT136-1.



Dimensions in mm.

Fig.9 32-lead mini-pack; plastic (SO32; SOT287).
Plastic small outline package; 32 leads; body width 7.5 mm; SO32; SOT287-1.

vso

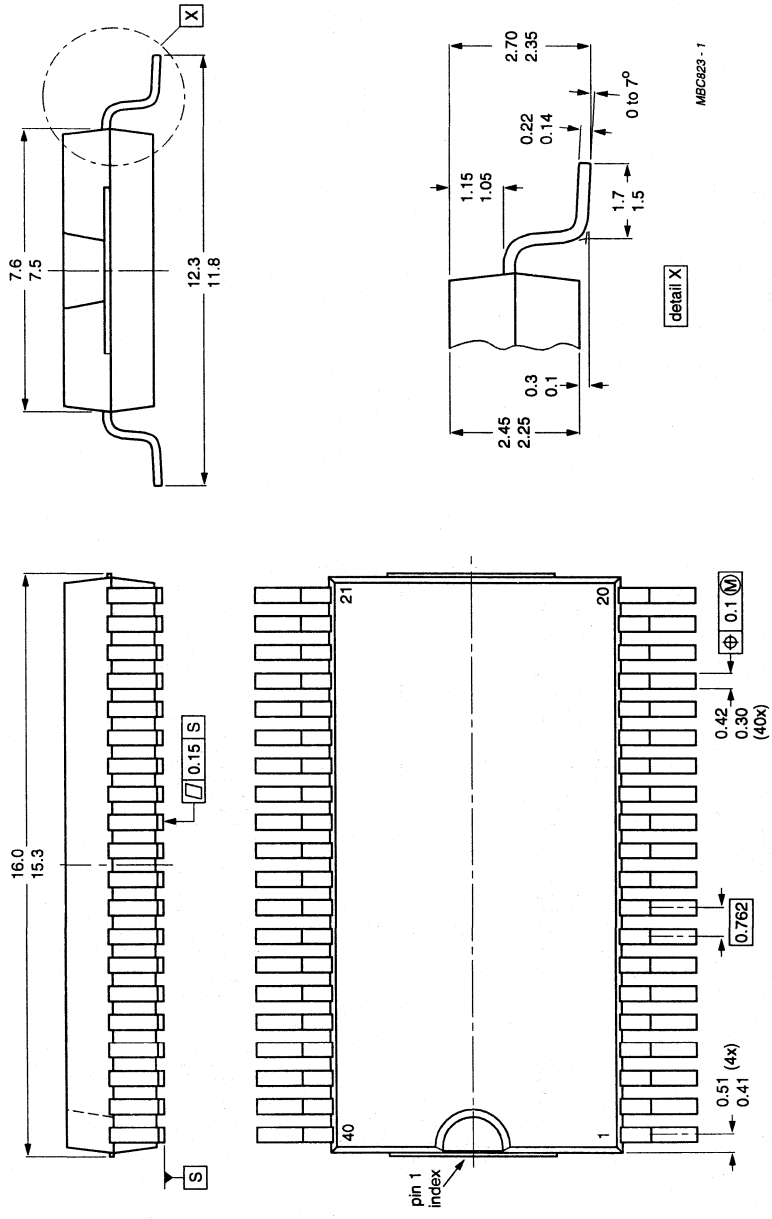
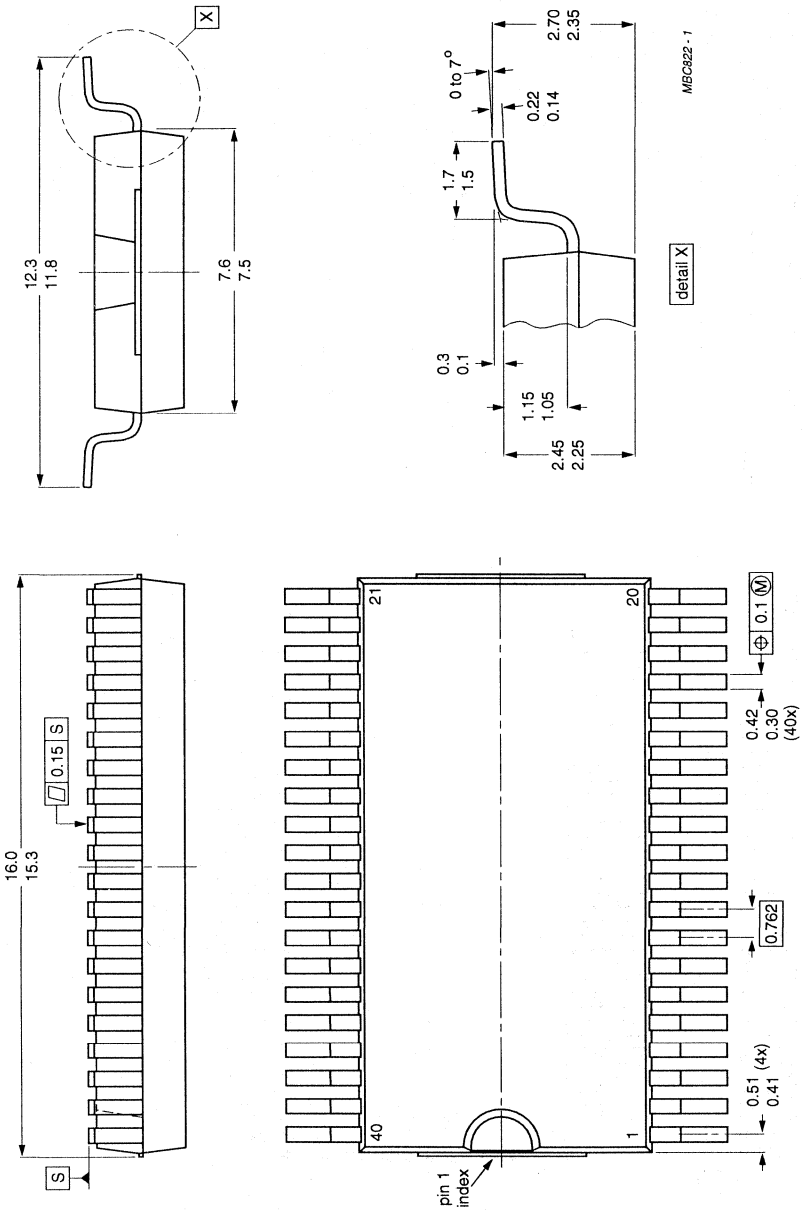


Fig.10 Plastic very small outline package; 40 leads; VSO40; SOT158-1.

Dimensions in mm.



Dimensions in mm.

Fig.11 Plastic very small outline package; 40 leads; face down; VSO40; SOT158-2.

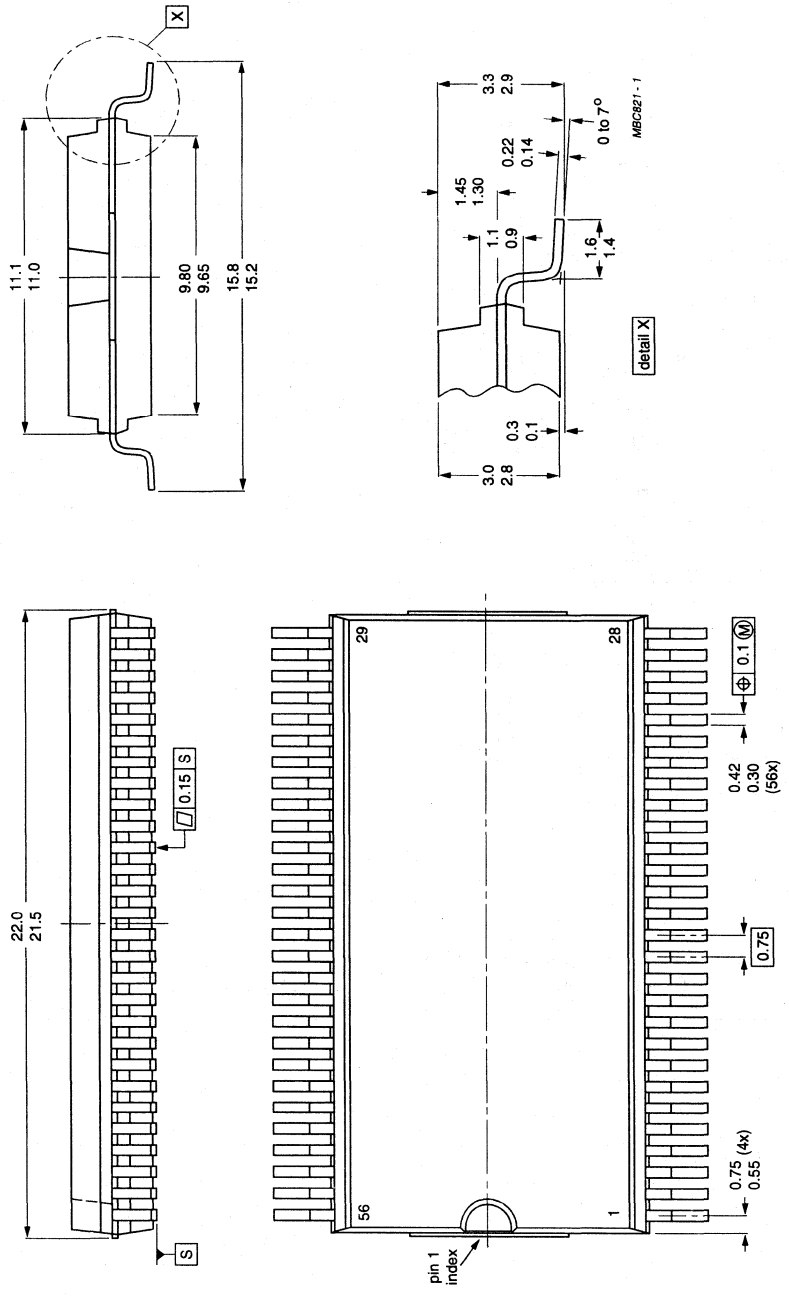
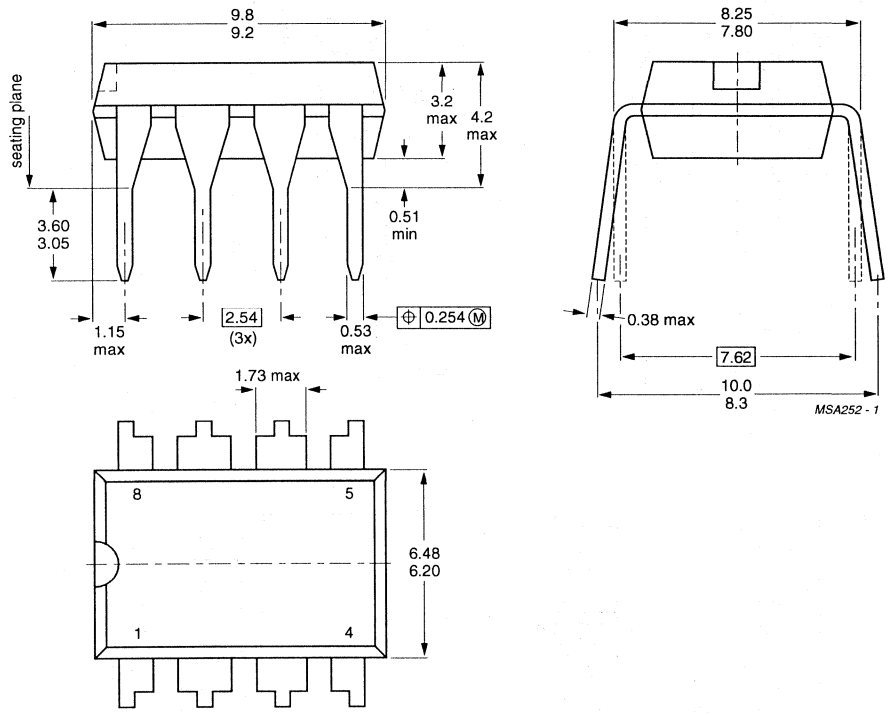


Fig.12 Plastic very small outline package; 56 leads; VSO56; SOT190-1.

Dimensions in mm.

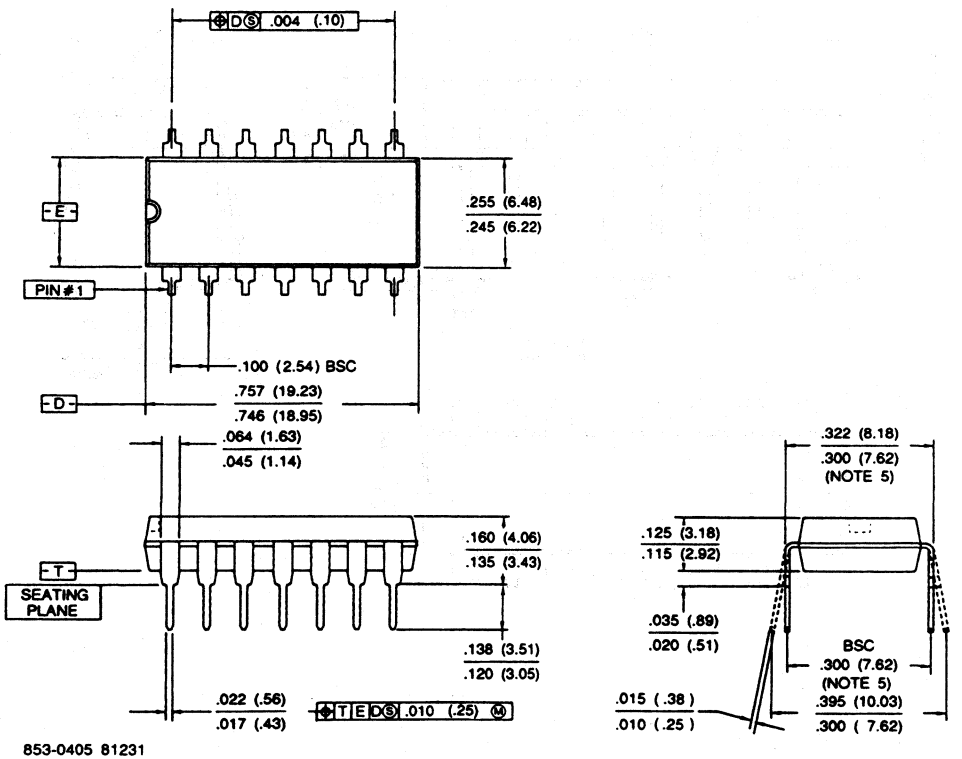
Package information

DIP



Dimensions in mm.

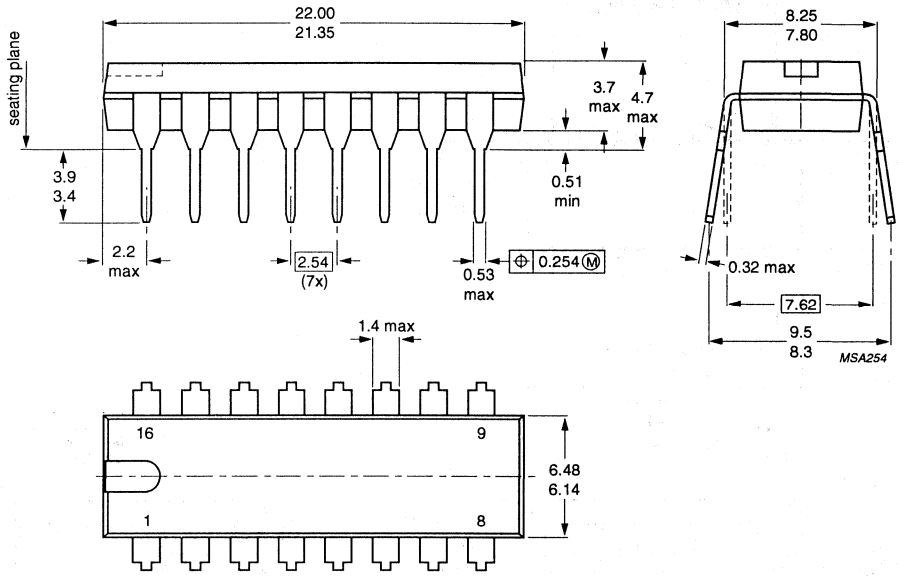
Fig.13 8-lead DIL; plastic (SOT97).
Plastic dual in-line package; 8 leads (300 mil); DIP8; SOT97-1.



NOTES:

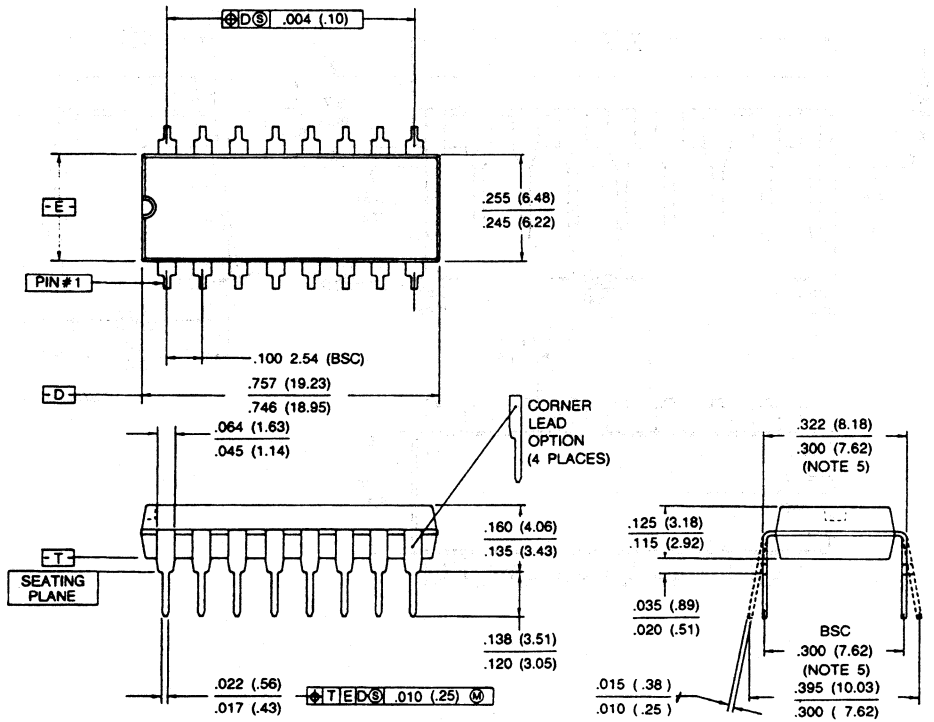
1. Controlling dimension: inches. Metric are shown in parentheses.
2. Package dimensions conform to JEDEC specification MS-001-AC for standard dual in-line (DIP) package .300 inch row spacing (PLASTIC) 14 leads (issue B. 7/85)
3. Dimensions and tolerancing per ANSI Y14. 5M-1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010 inch (.25mm) on any side.
5. These dimensions measured with the leads constrained to be perpendicular to plane T.
6. Pin numbers start with pin #1 and continue counterclockwise to pin #14 when viewed from the top.

Fig.14 14-lead DIP; plastic (N package).



Dimensions in mm.

Fig.15 16-lead DIL; plastic (SOT38).
Plastic dual in-line package; 16 leads (300 mil); long body; DIP16; SOT38-1.



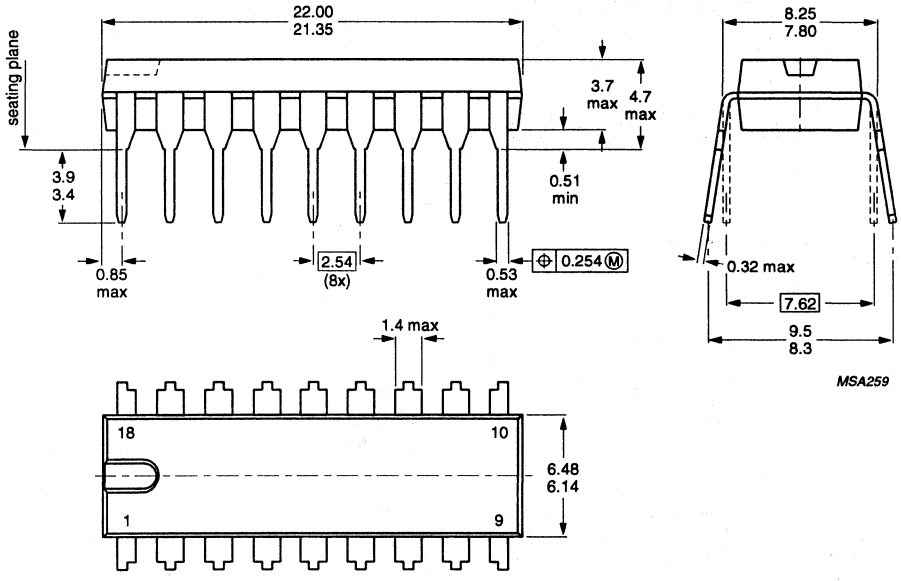
853-0406 81232

NOTES:

1. Controlling dimension: inches. Metric are shown in parentheses.
2. Package dimensions conform to JEDEC specification MS-001-AA for standard dual in-line (DIP) package .300 inch row spacing (PLASTIC) 16 leads (issue B. 7/85)
3. Dimensions and tolerancing per ANSI Y14. 5M-1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010 inch (.25mm) on any side.
5. These dimensions measured with the leads constrained to be perpendicular to plane T.
6. Pin numbers start with pin #1 and continue counterclockwise to pin #16 when viewed from the top.

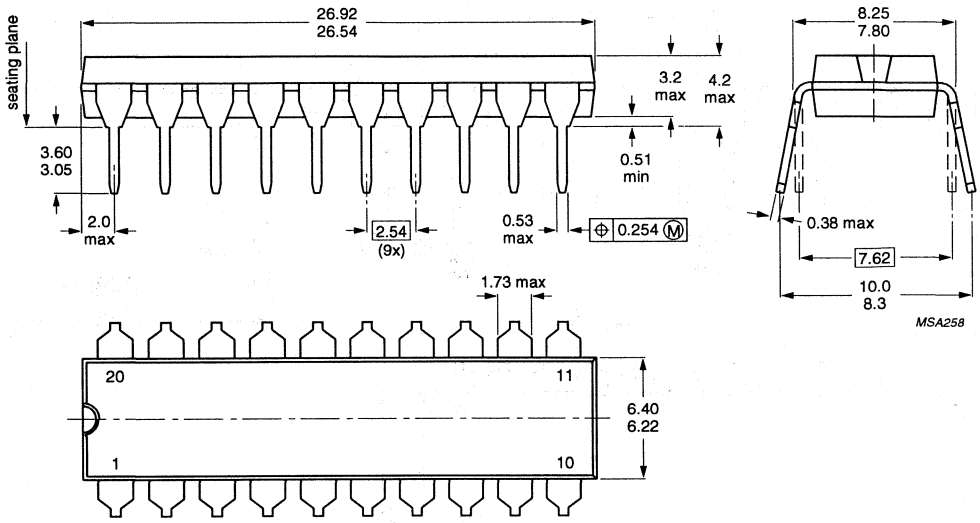
Fig.16 16-lead DIP; plastic (N package).

Package information



Dimensions in mm.

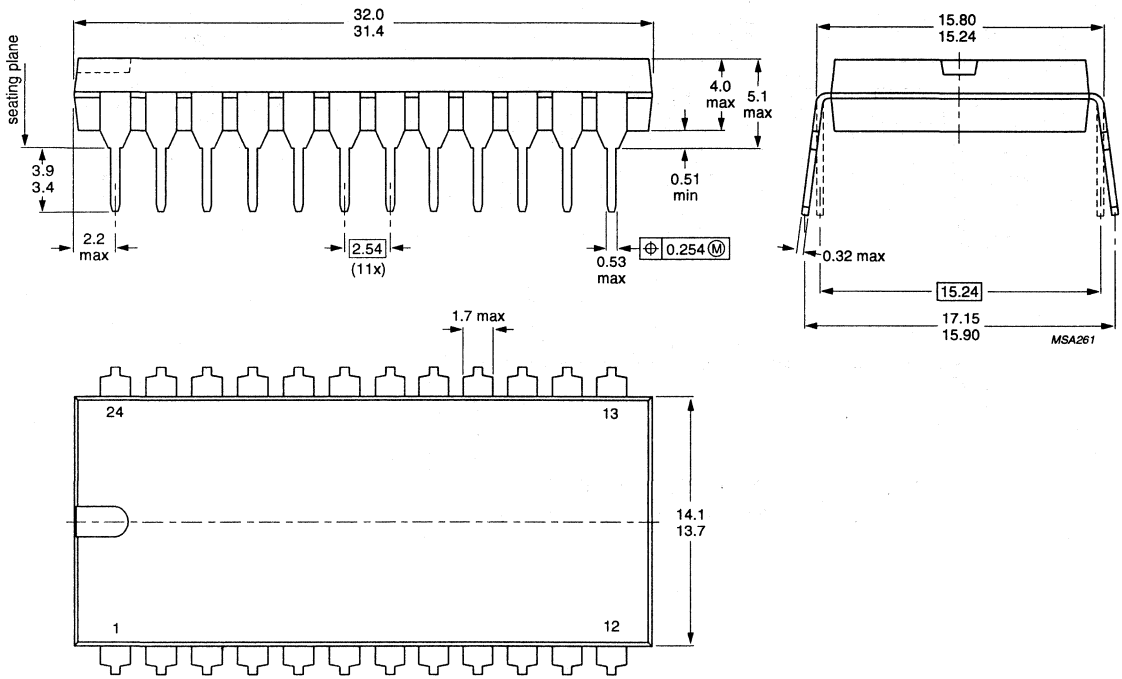
Fig.17 18-lead DIL; plastic (SOT102).
Plastic dual in-line package; 18 leads (300 mil); DIP18; SOT102-1.



Dimensions in mm.

Fig.18 20-lead DIL; plastic (SOT146).
Plastic dual in-line package; 20 leads (300 mil); DIP20; SOT146-1.

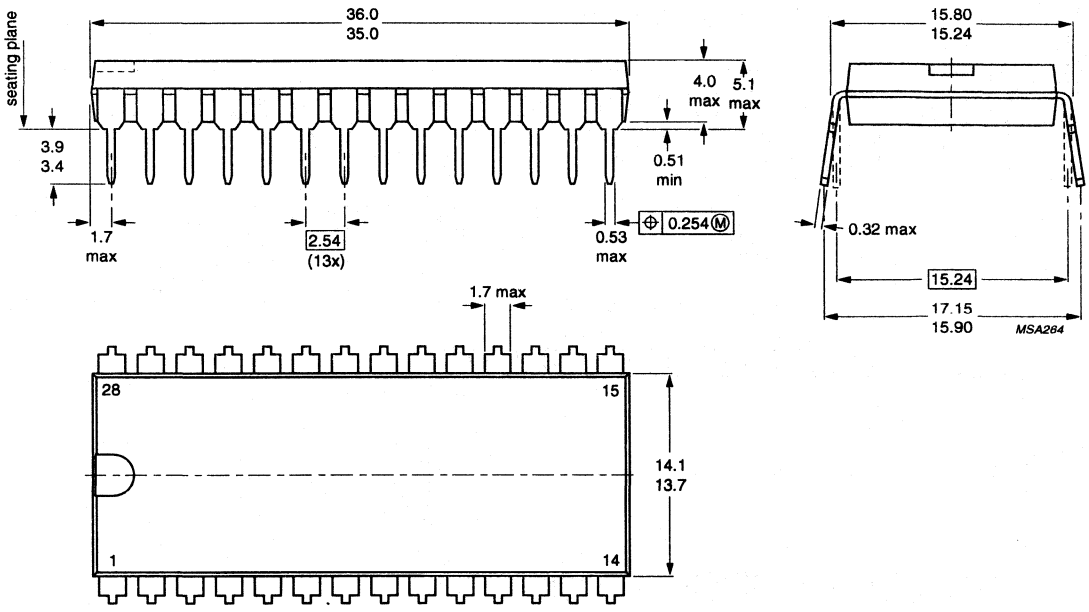
Package information



Dimensions in mm.

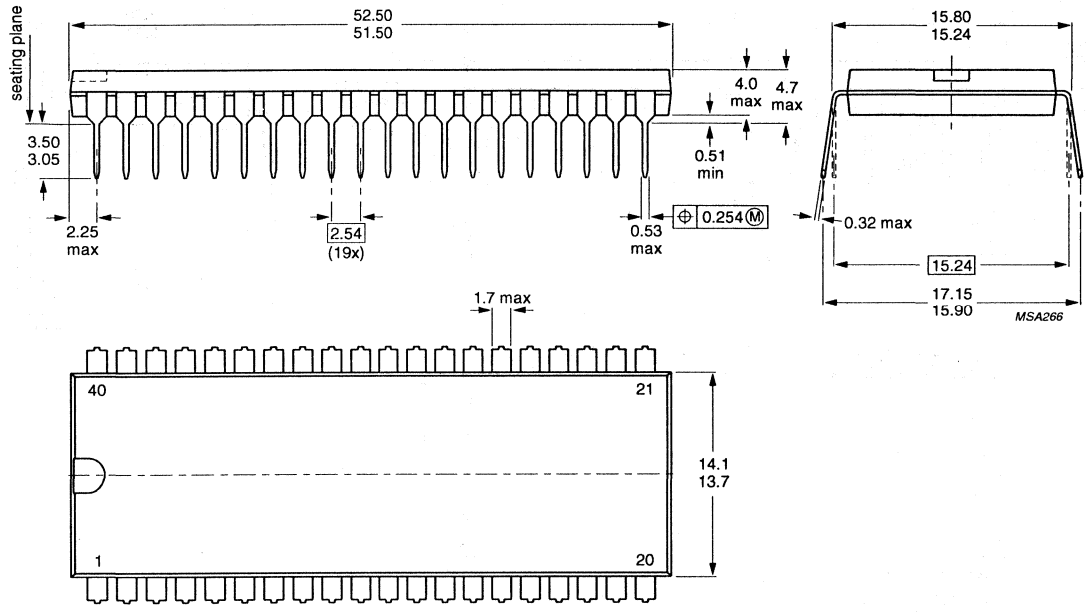
Fig.19 24-lead DIL; plastic (SOT101A).
Plastic dual in-line package; 24 leads (600 mil); DIP24; SOT101-1.

Package information



Dimensions in mm.

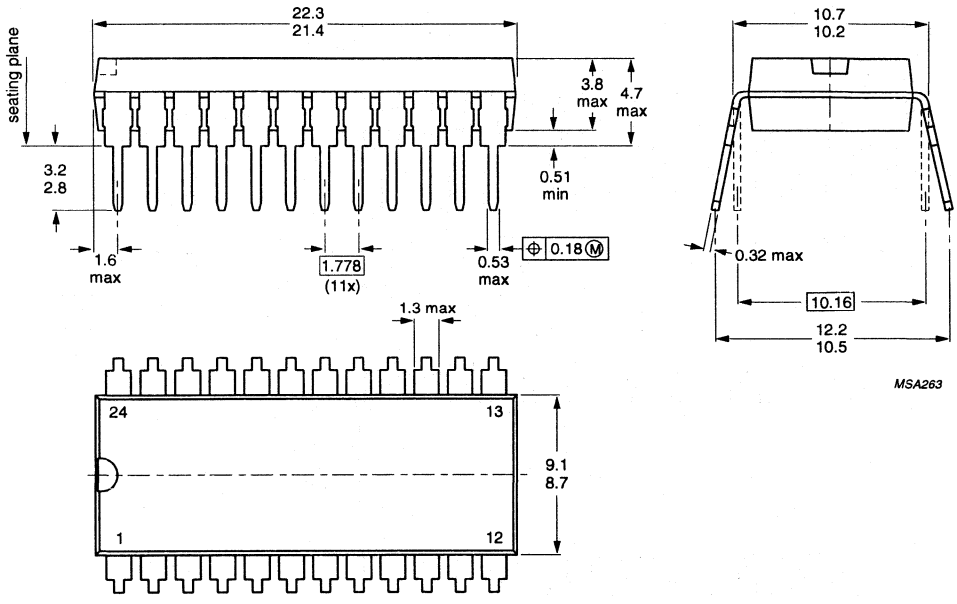
Fig.20 28-lead DIL; plastic (SOT117).
Plastic dual in-line package; 28 leads (600 mil); DIP28; SOT117-1.



Dimensions in mm.

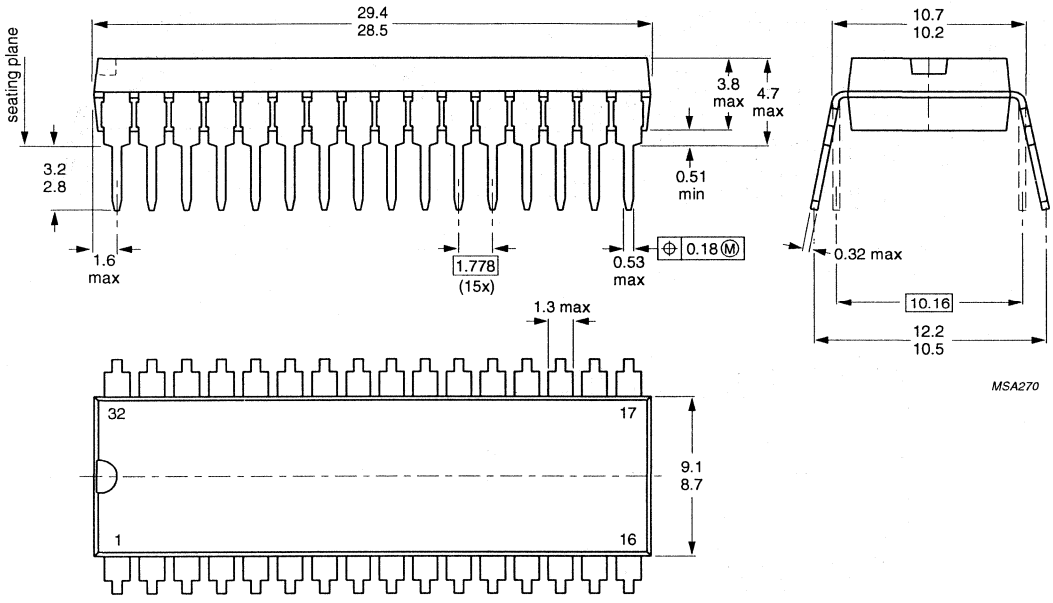
Fig.21 40-lead DIL; plastic (SOT129).
Plastic dual in-line package; 40 leads (600 mil); DIP40; SOT129-1.

SDIP



Dimensions in mm.

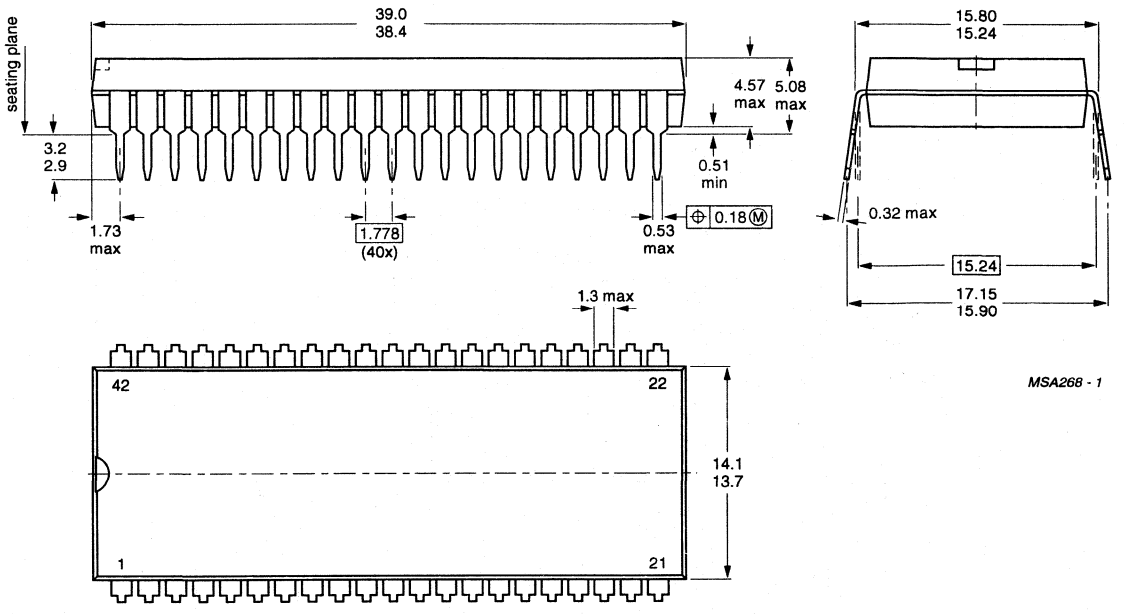
Fig.22 24-lead shrink DIL; plastic (SOT234).
Plastic shrink dual in-line package; 24 leads (400 mil); SDIP24; SOT234-1.



Dimensions in mm.

Fig.23 32-lead shrink DIL; plastic (SOT232).
Plastic shrink dual in-line package; 32 leads (400 mil); SDIP32; SOT232-1.

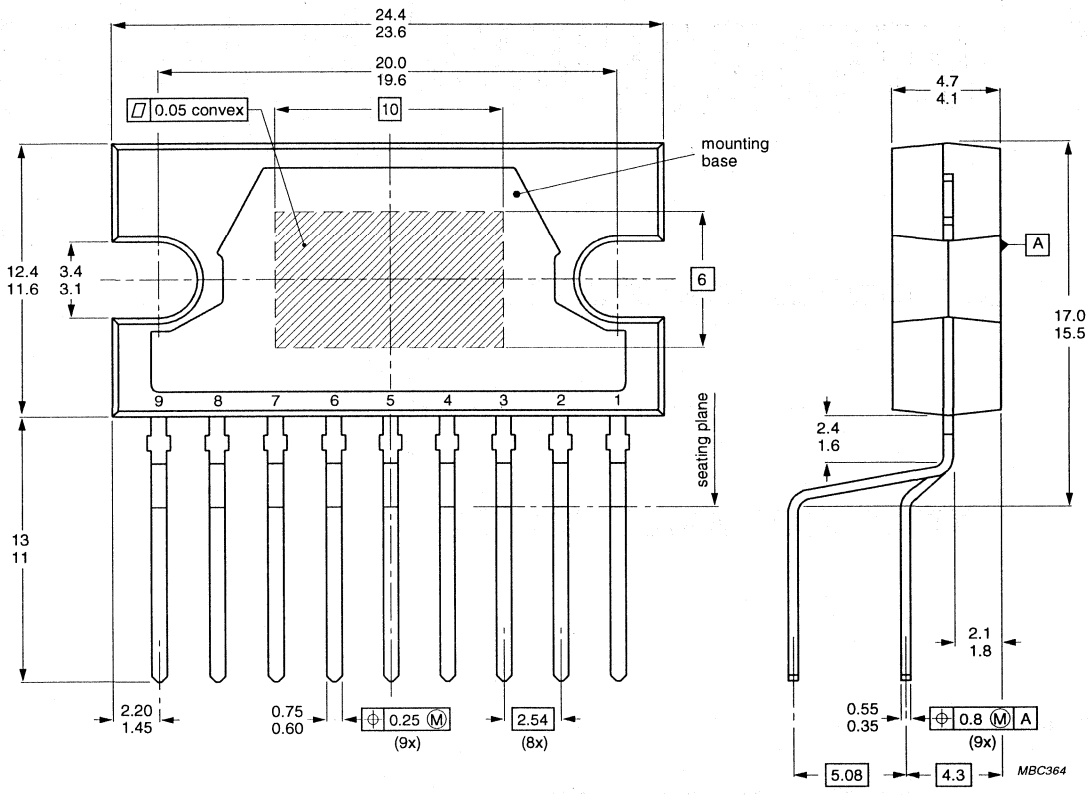
Package information



Dimensions in mm.

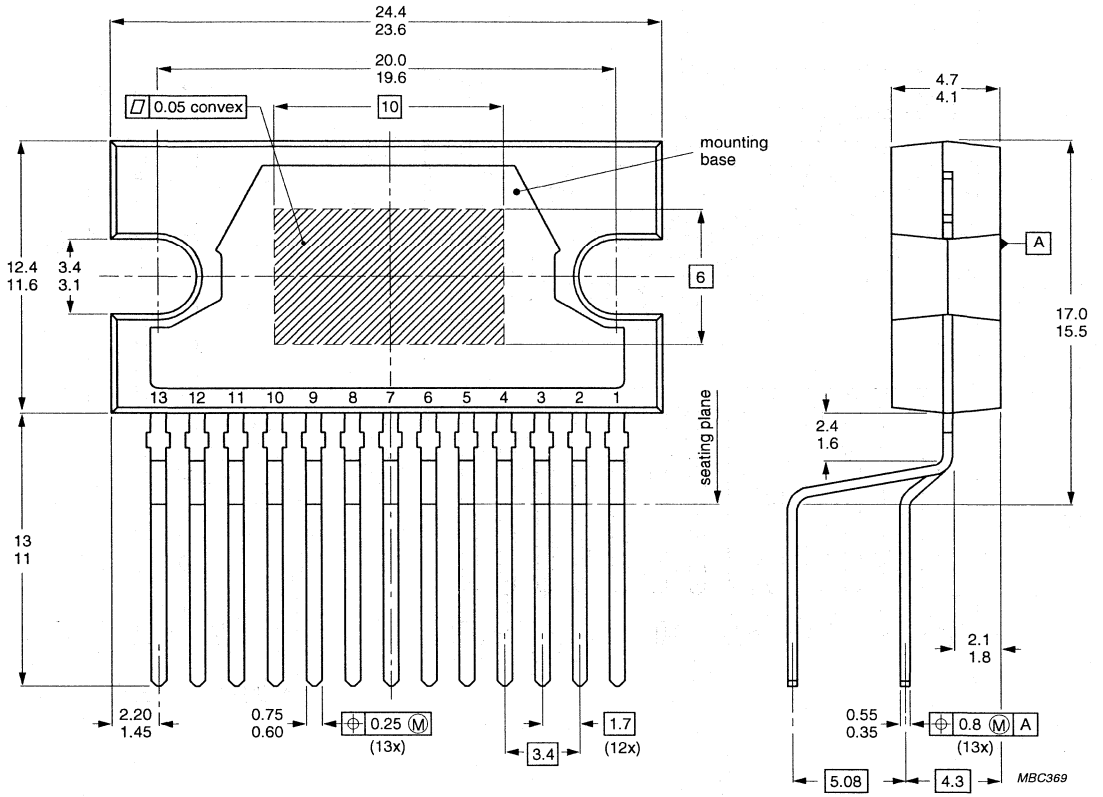
Fig.24 42-lead shrink DIL; plastic (SOT270).
Plastic shrink dual in-line package; 42 leads (600 mil); SDIP42; SOT270-1.

DBS



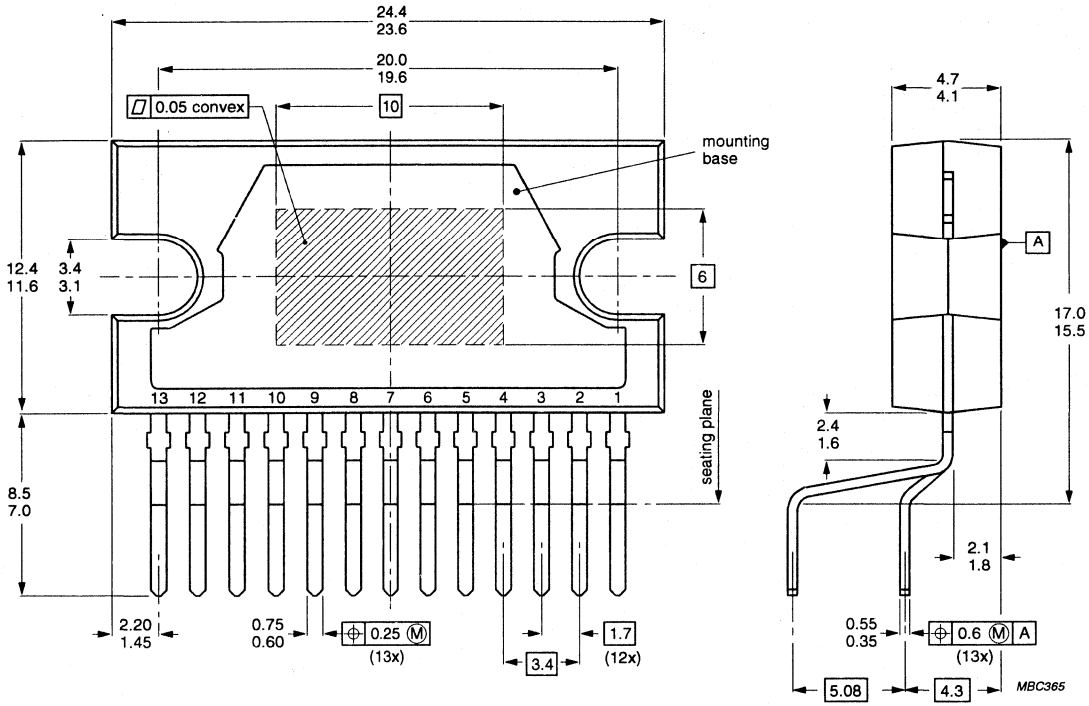
Dimensions in mm.

Fig.25 9-lead SIL-bent-to-DIL; plastic; power (SOT157).
Plastic DIL-bent-SIL power package; 9 leads (lead length 12 mm); DBS9P; SOT157-2.



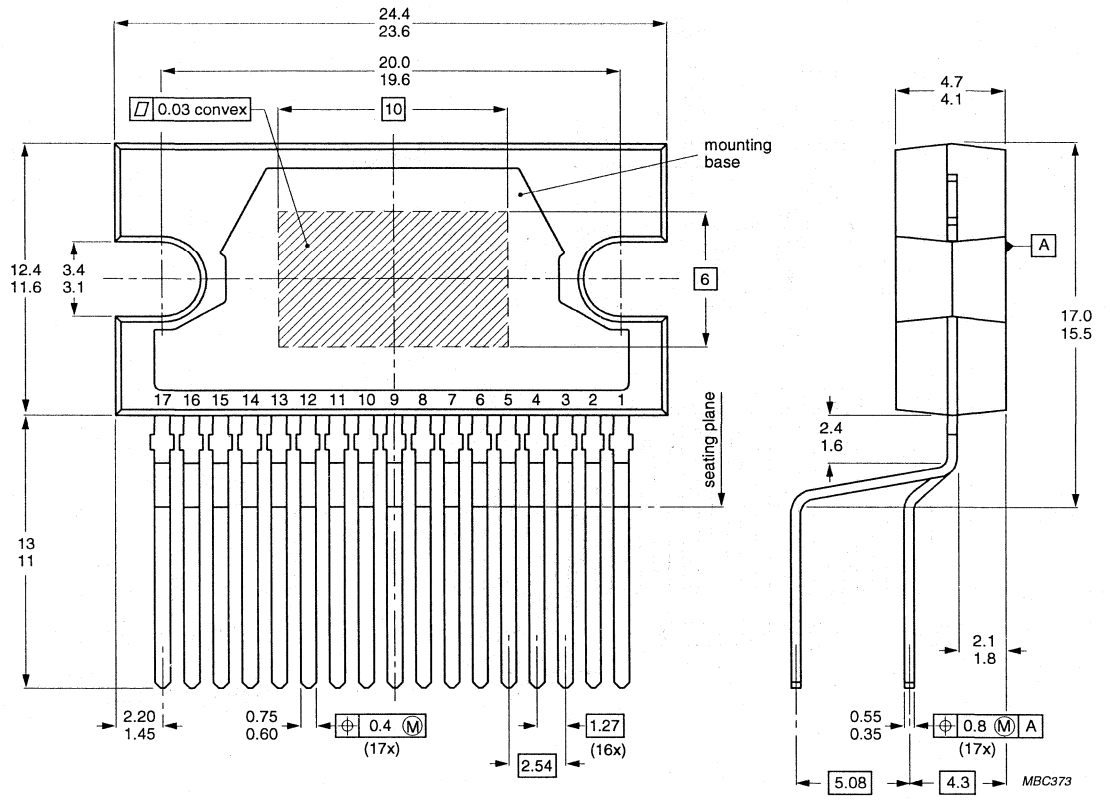
Dimensions in mm.

Fig.26 13-lead SIL-bent-to-DIL; plastic; power (SOT141).
Plastic DIL-bent-SIL power package; 13 leads (lead length 12 mm); DBS13P; SOT141-6.



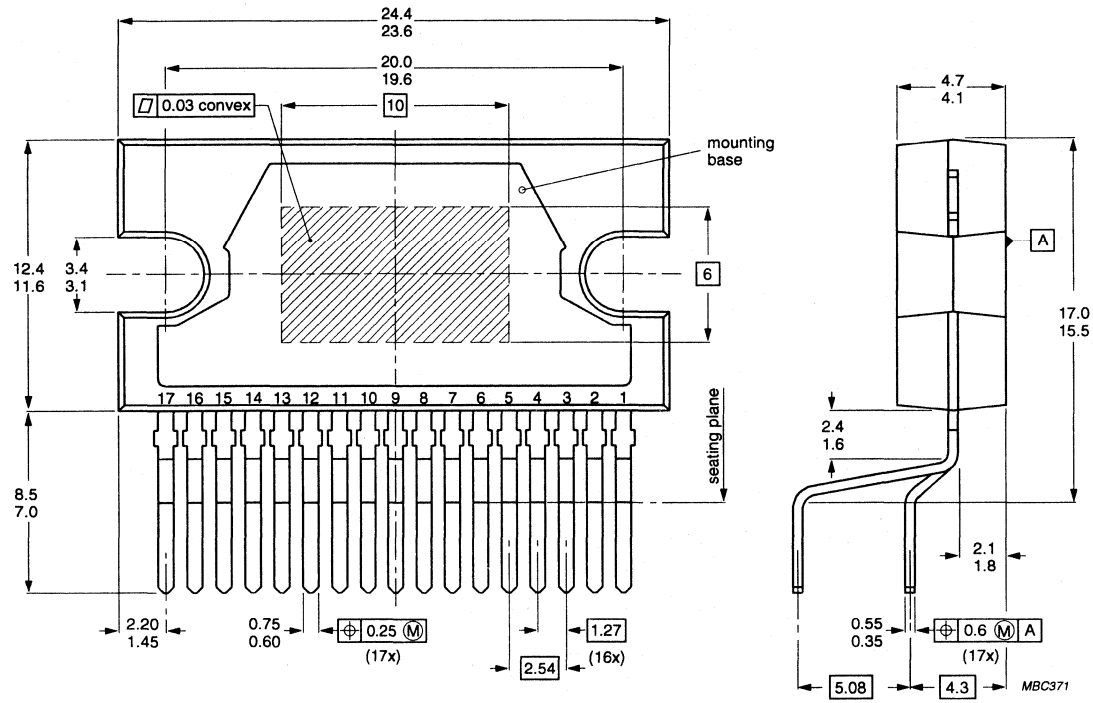
Dimensions in mm.

Fig.27 13-lead SIL-bent-to-DIL; plastic; power (SOT141).
Plastic DIL-bent-SIL power package; 13 leads (lead length 7.7 mm); DBS13P; SOT141-8.



Dimensions in mm.

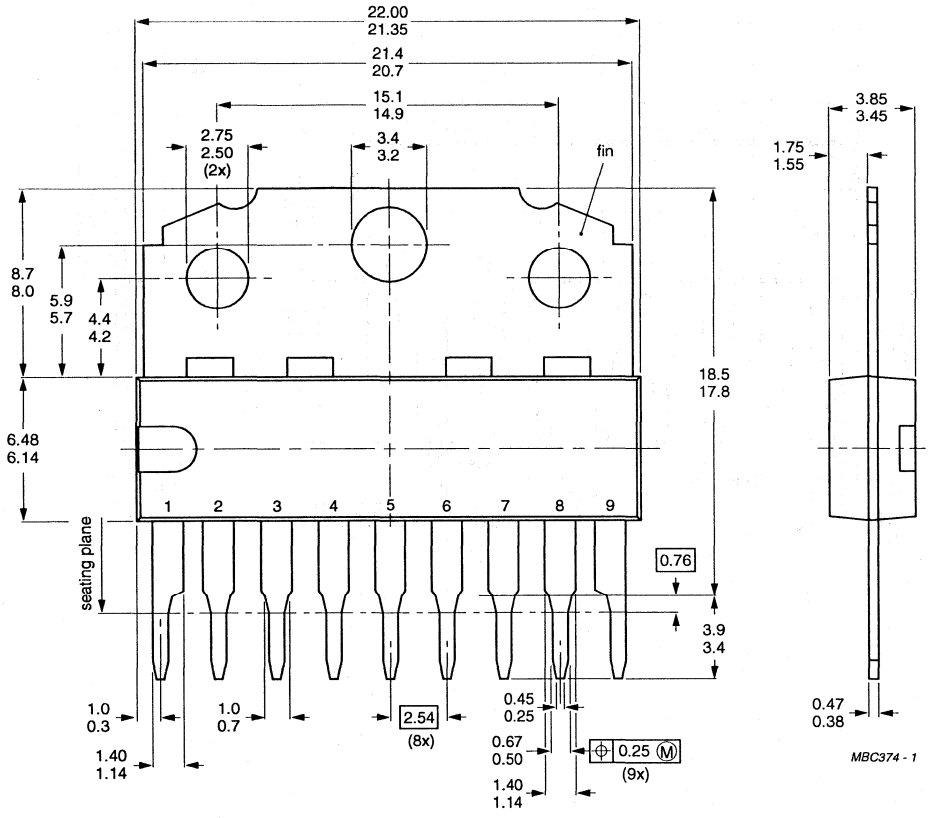
Fig.28 17-lead SIL-bent-to-DIL; plastic; power (SOT243).
Plastic DIL-bent-SIL power package; 17 leads (lead length 12 mm); DBS17P; SOT243-1.



Dimensions in mm.

Fig.29 17-lead SIL-bent-to-DIL; plastic; power (SOT243).
Plastic DIL-bent-SIL power package; 17 leads (lead length 7.7 mm); DBS17P; SOT243-3.

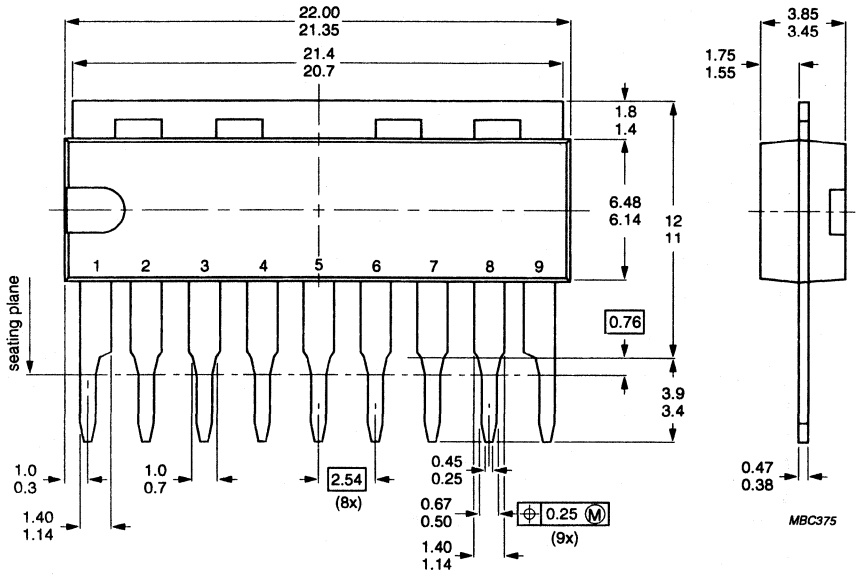
SIL



Dimensions in mm.

Fig.30 9-lead SIL; plastic (SOT110).
Plastic single in-line medium power package with fin; 9 leads; SIL9MPF; SOT110-1.

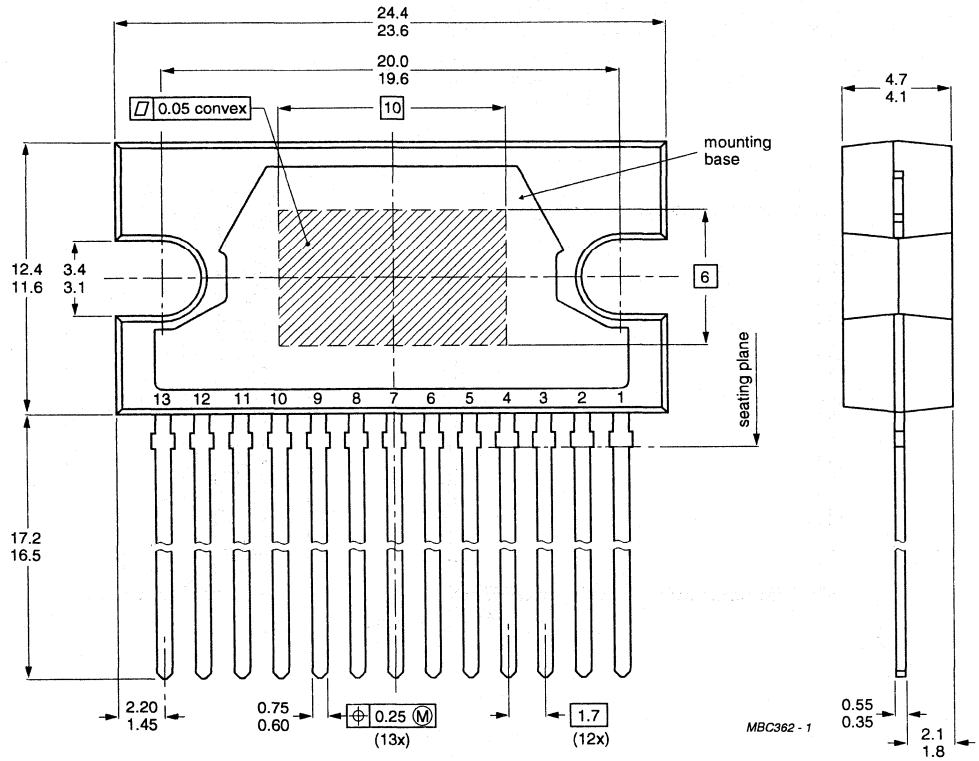
Package information



Dimensions in mm.

Fig.31 9-lead SIL; plastic, medium power (SOT142).
Plastic single in-line medium power package; 9 leads; SIL9MP; SOT142 -1.

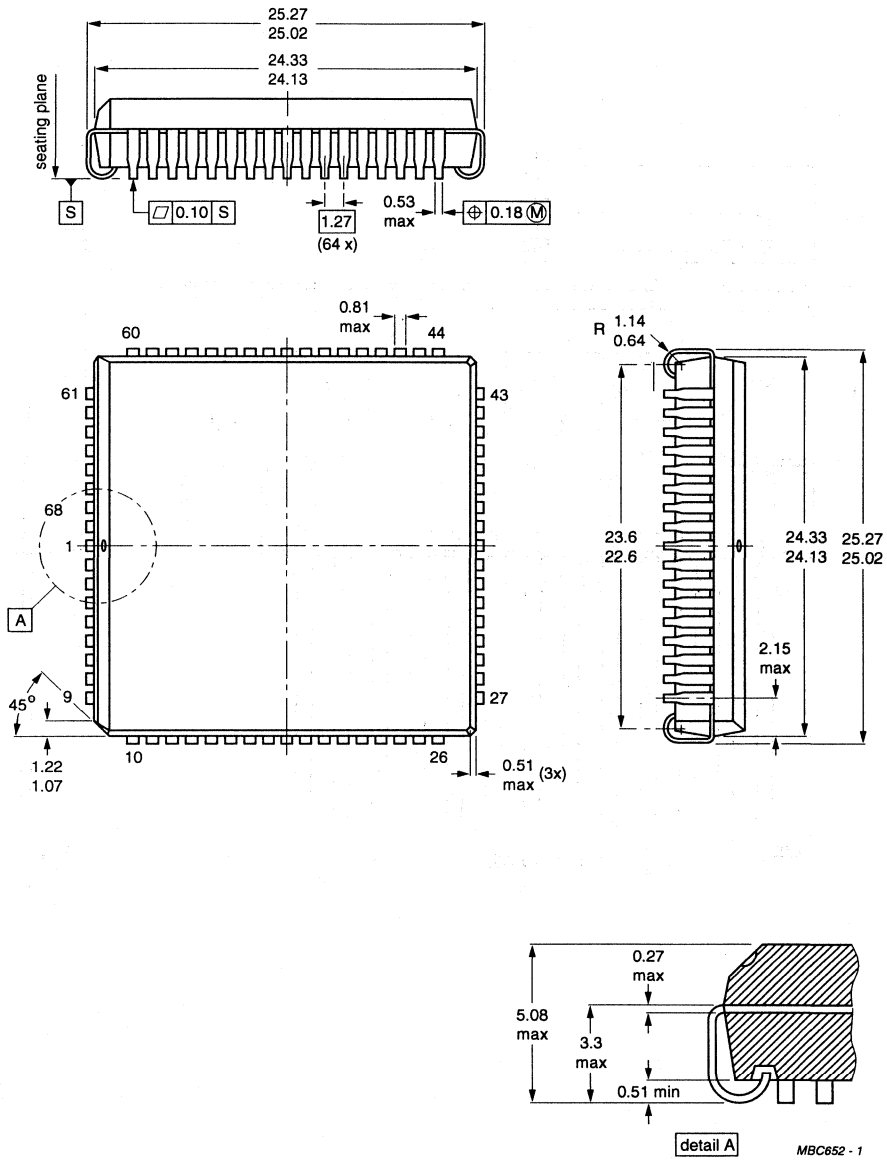
Package information



Dimensions in mm.

Fig.32 9-lead SIL; plastic power (SOT131).
Plastic single in-line power package; 9 leads; SIL9P; SOT131-2.

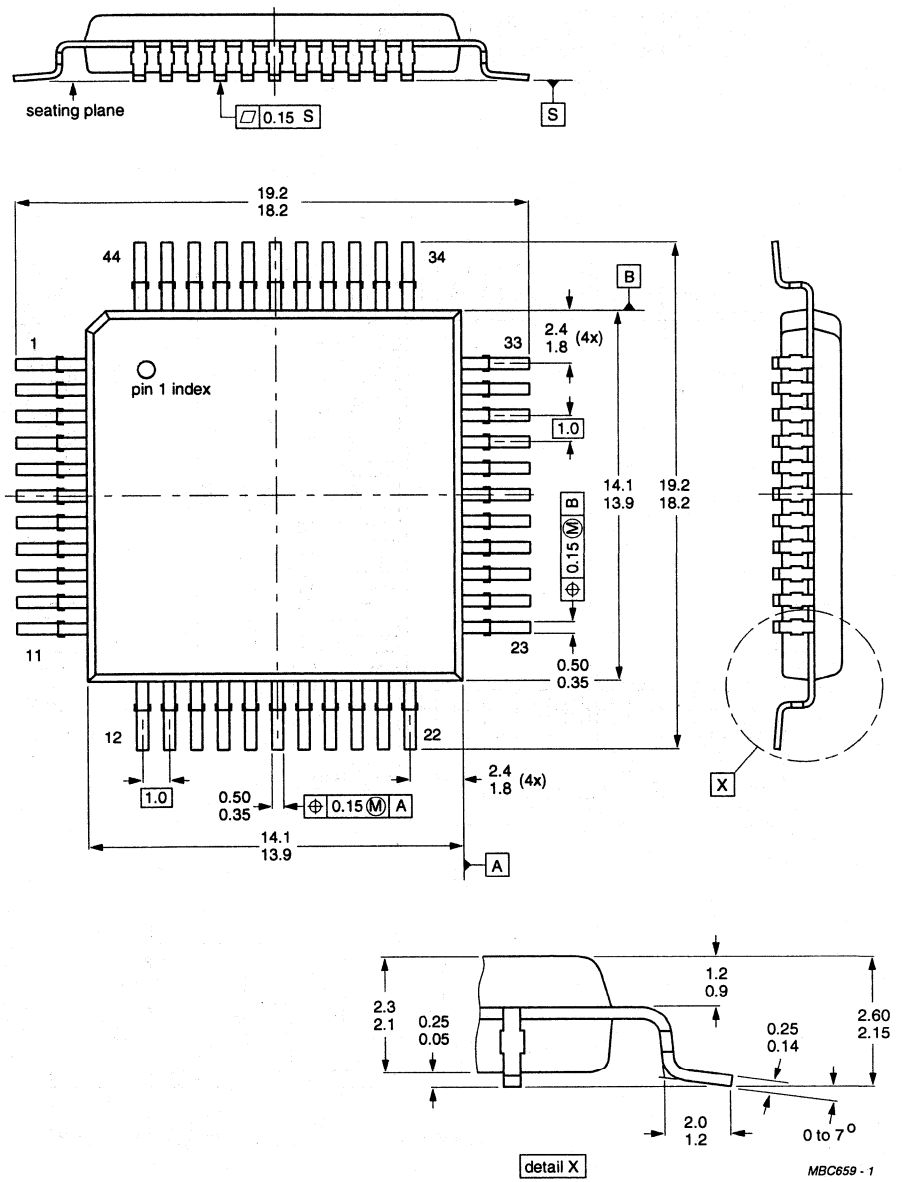
PLCC



Dimensions in mm.

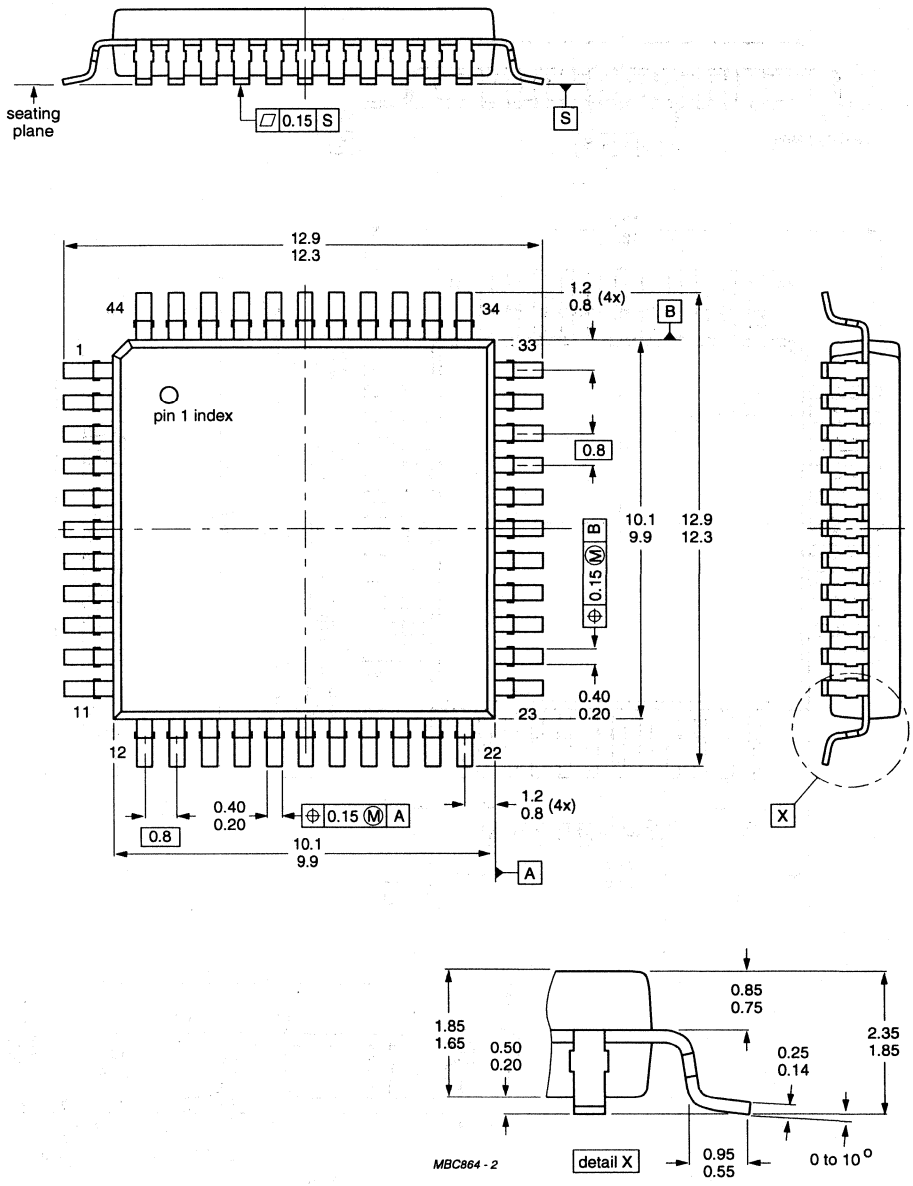
Fig.33 68-lead plastic leaded chip carrier (SOT188).
Plastic leaded chip carrier; 68 leads; PLCC68; SOT188-2.

QFP



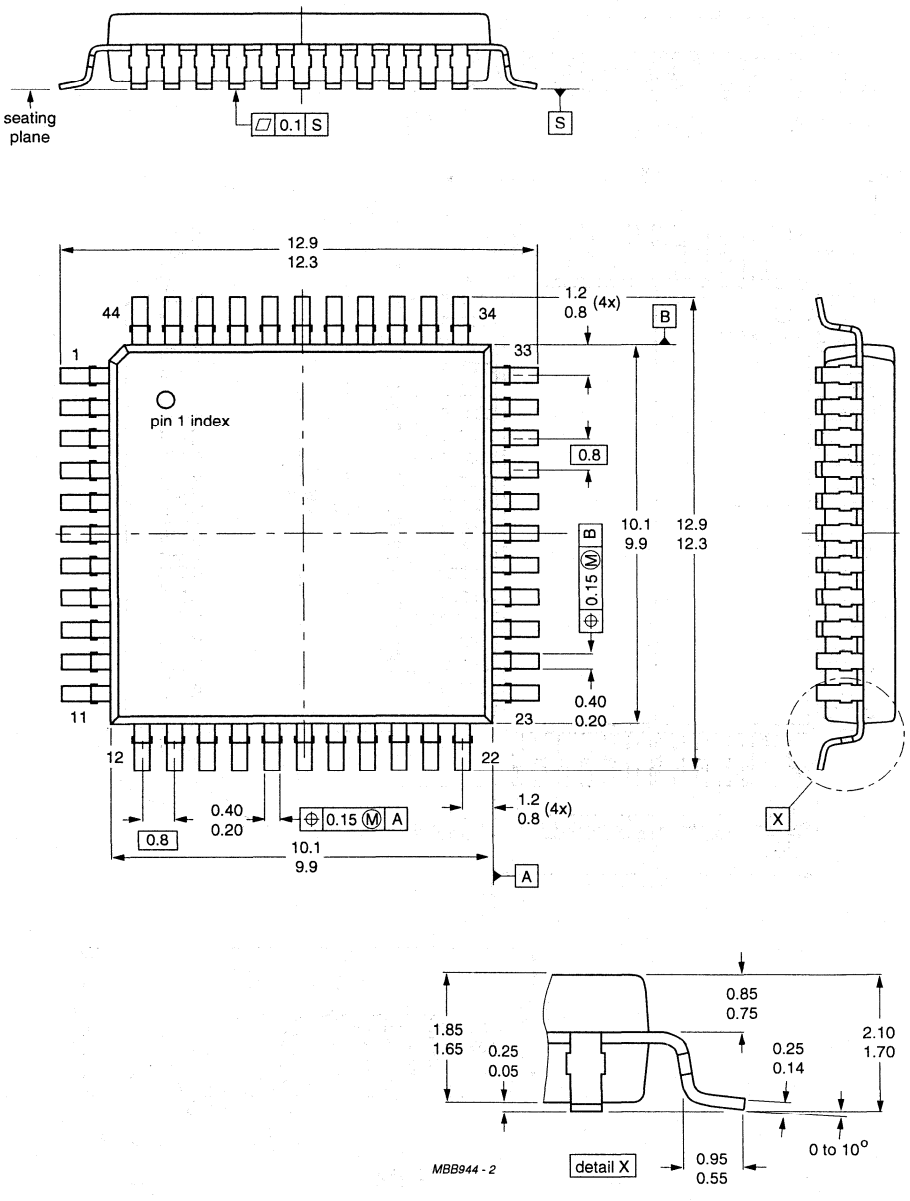
Dimensions in mm.

Fig.34 44-pin plastic quad flat pack (SOT205A).
Plastic quad flat package; 44 leads (lead length 2.35 mm); body 14 x 14 x 2.2 mm; QFP44; SOT205-1.



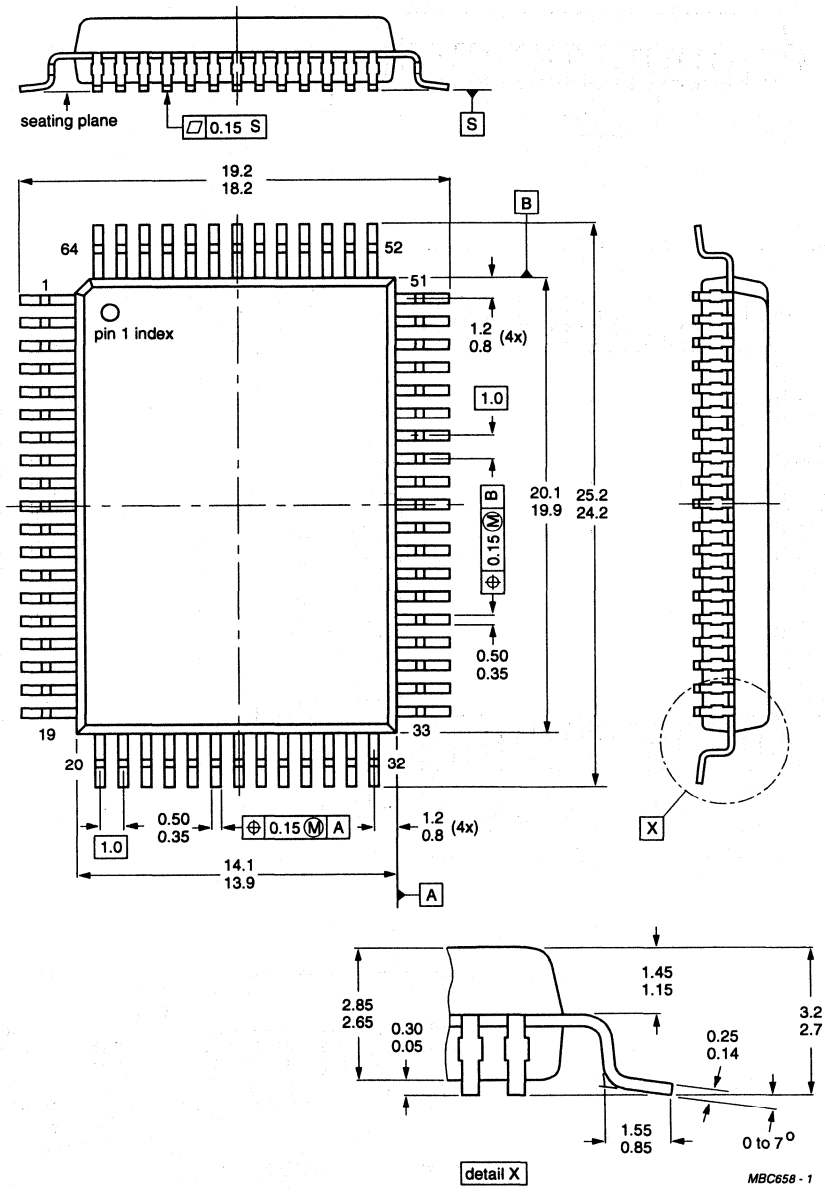
Dimensions in mm.

Fig.35 44-pin plastic quad flat pack (SOT307).
Plastic quad flat package; 44 leads (lead length 1.3 mm); body 10 x 10 x 1.75 mm; high stand-off height; QFP44; SOT307-1.



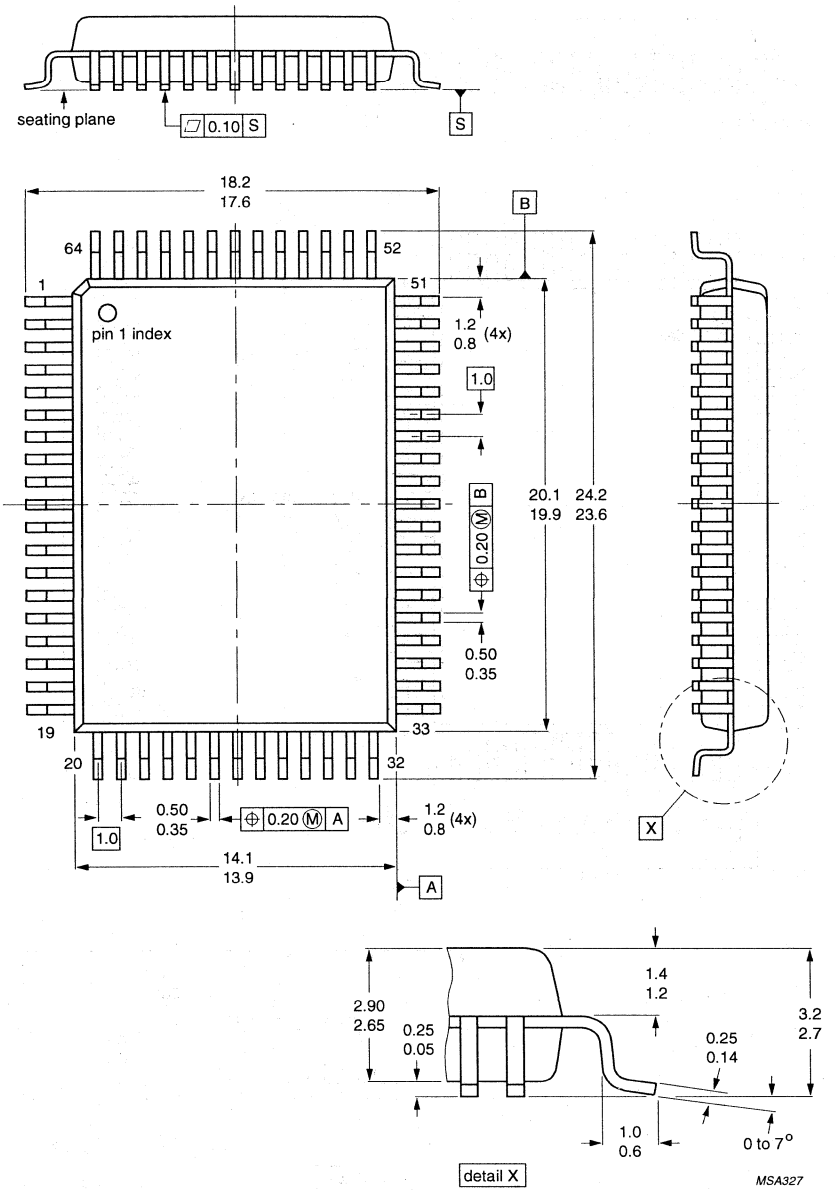
Dimensions in mm.

Fig.36 44-pin plastic quad flat pack (SOT307).
Plastic quad flat package; 44 leads (lead length 1.3 mm); body 10 x 10 x 1.75 mm; QFP44; SOT307-2.



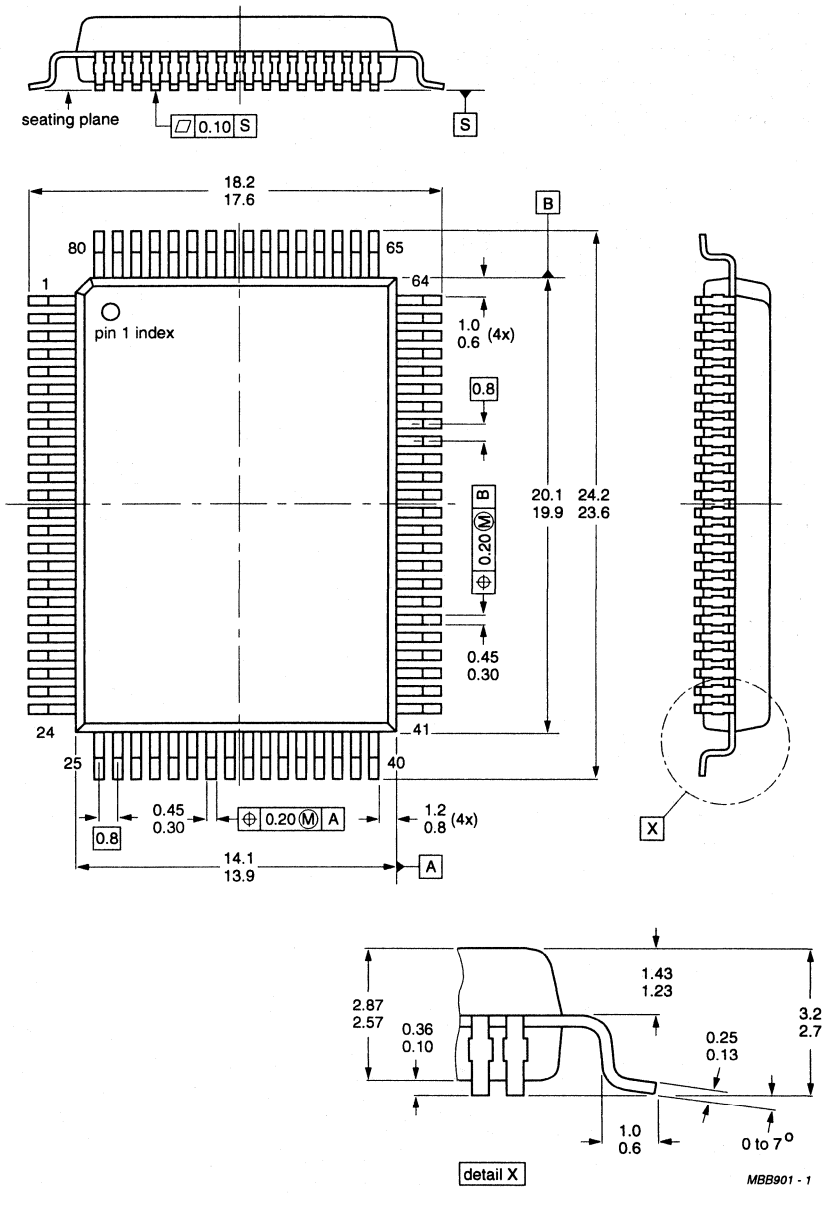
Dimensions in mm.

Fig.37 64-pin plastic quad flat pack (SOT208A).
Plastic quad flat package; 64 leads (lead length 2.35 mm); body 14 x 20 x 2.75 mm; QFP64; SOT208-1.



Dimensions in mm.

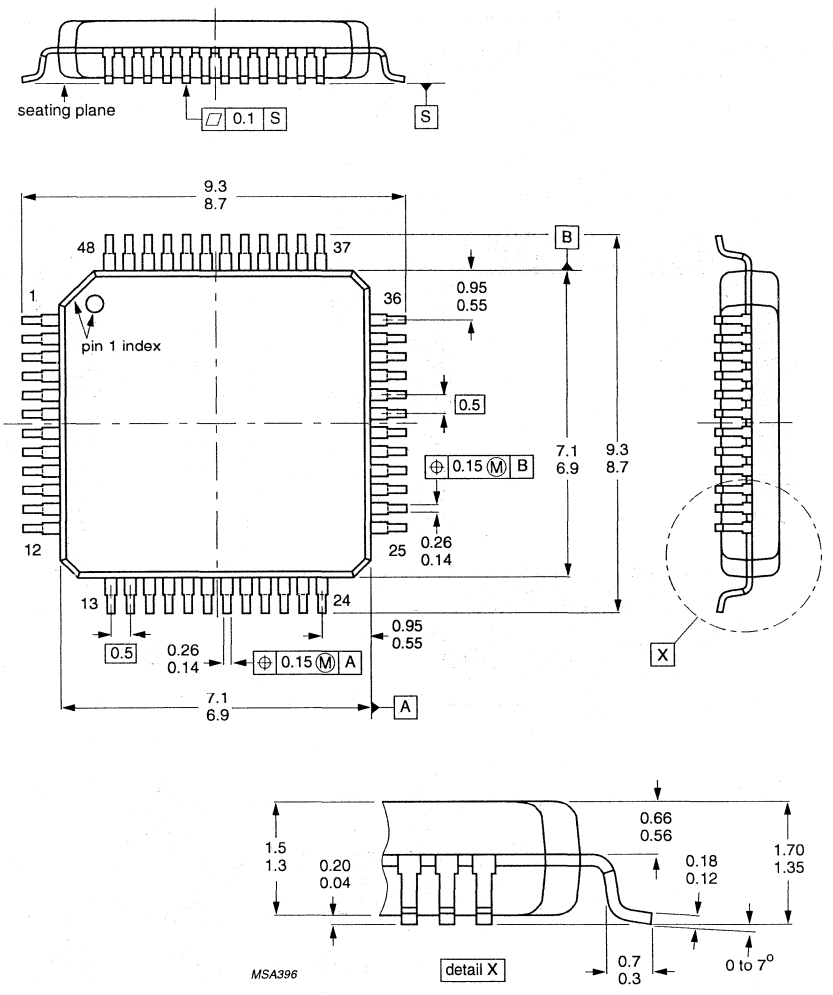
Fig.38 Plastic quad flat package; 64 leads (lead length 1.95 mm); body 14 x 20 x 2.8 mm; QFP64; SOT319-2.



Dimensions in mm.

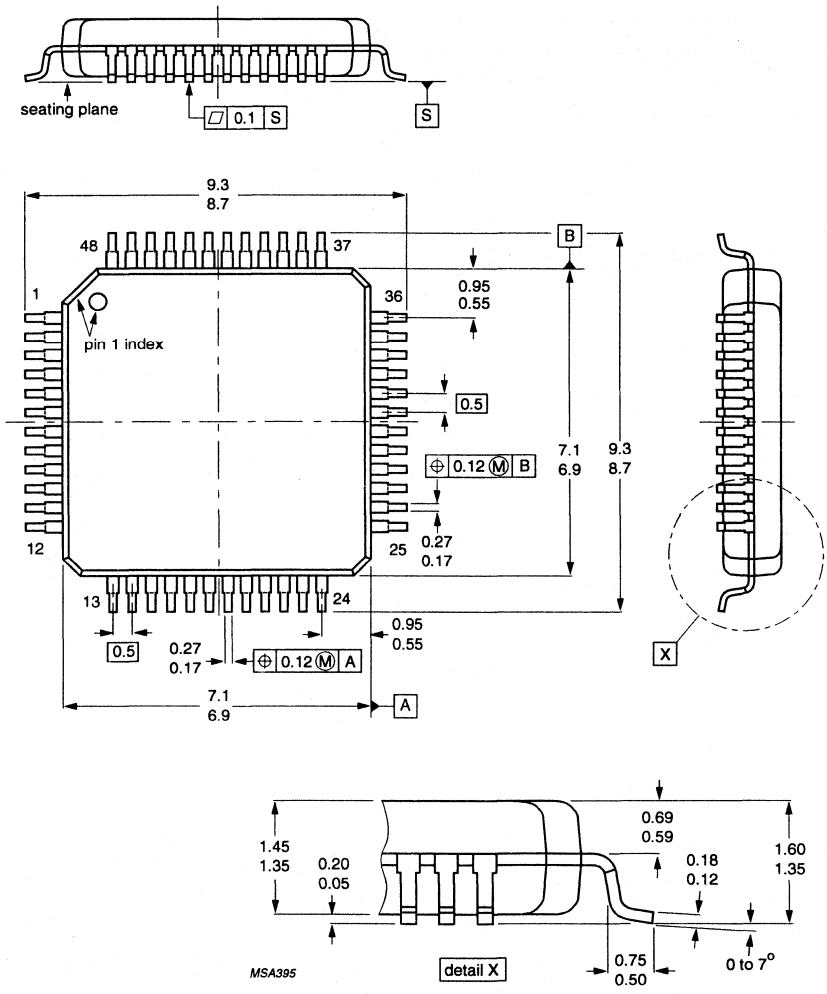
Fig.39 Plastic quad flat package; 80 leads (lead length 1.95 mm); body 14 x 20 x 2.8 mm; QFP80; SOT318-2.

TQFP



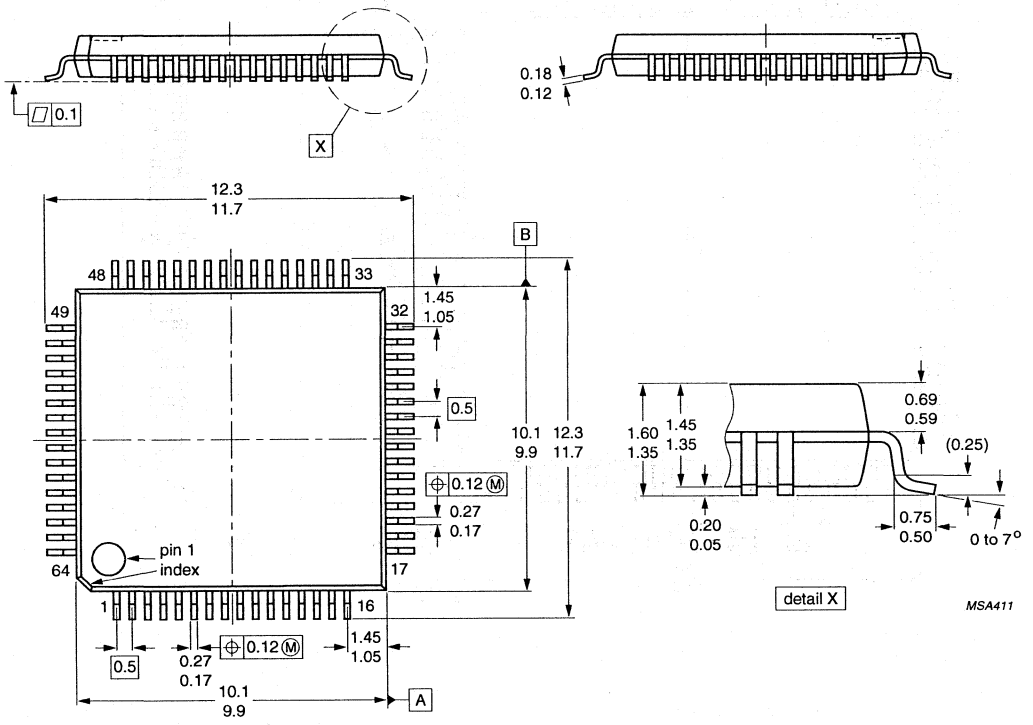
Dimensions in mm.

Fig.40 Plastic thin quad flat package; 48 leads; body 7 x 7 x 1.4 mm; TQFP48; SOT313-1.



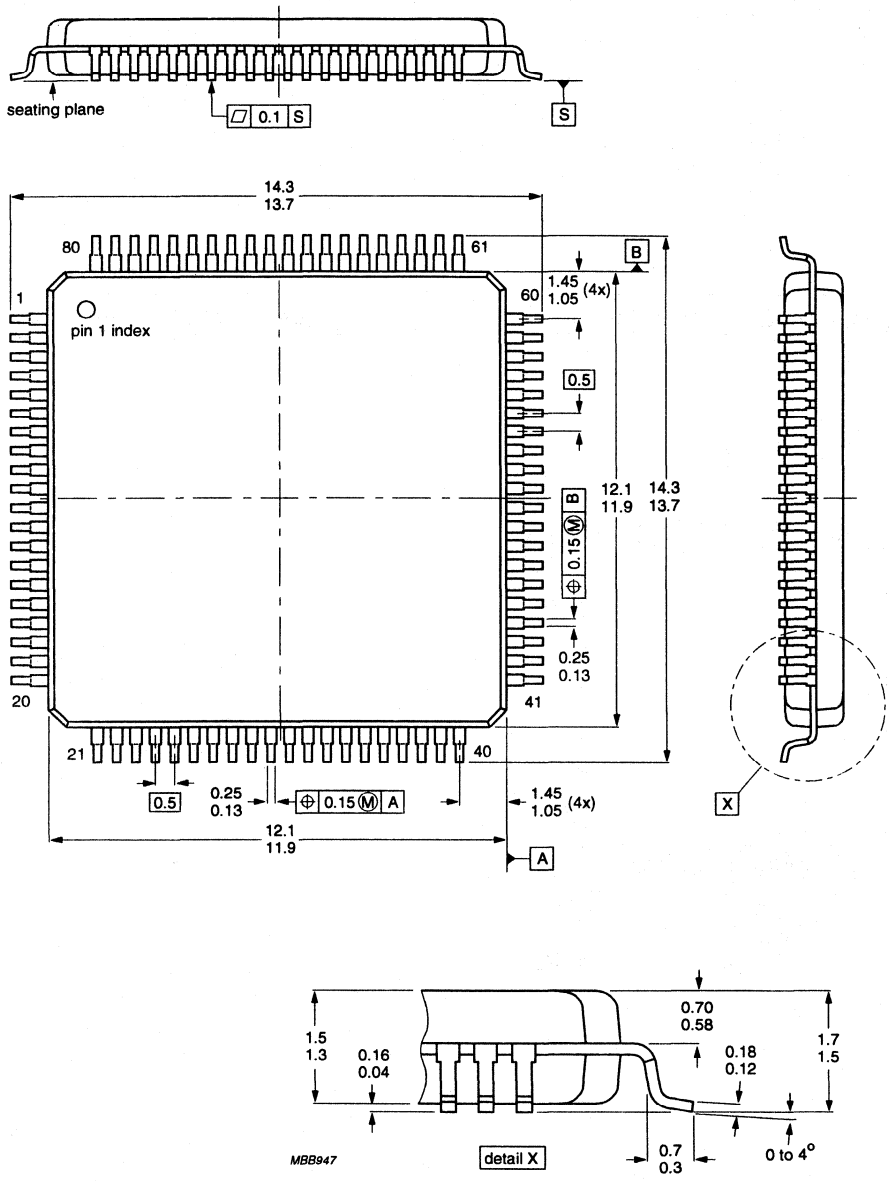
Dimensions in mm.

Fig.41 Plastic thin quad flat package; 48 leads; body 7 x 7 x 1.4 mm; TQFP48; SOT313-2.



Dimensions in mm.

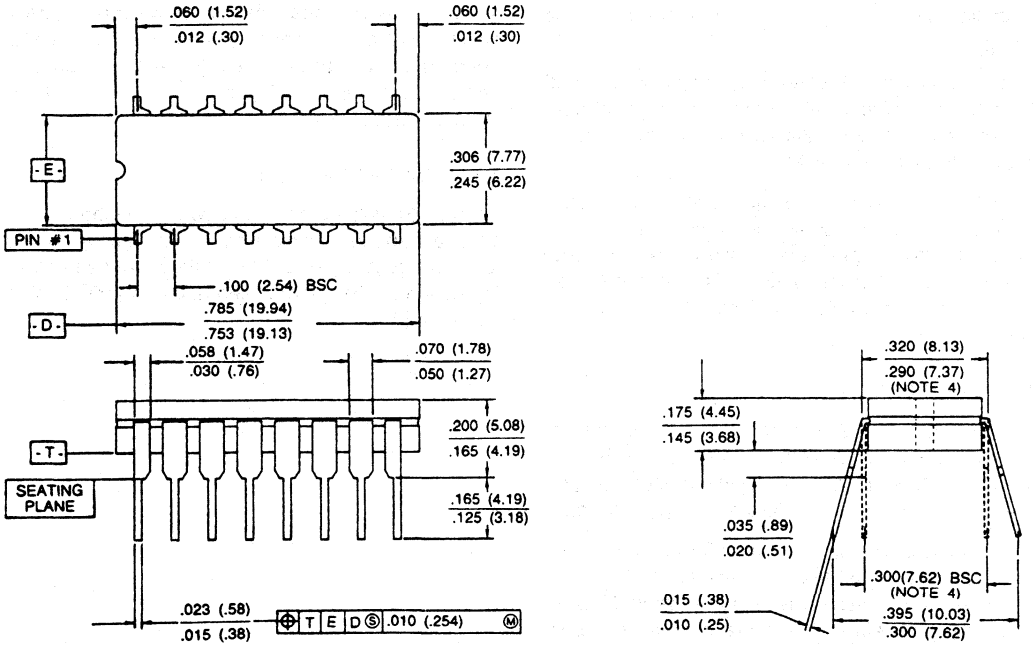
Fig.42 Plastic thin quad flat package; 64 leads; body 10 x 10 x 1.4 mm; TQFP64; SOT314-2.



Dimensions in mm.

Fig.43 Plastic thin quad flat package; 80 leads; body 12 x 12 x 1.4 mm; TQFP80; SOT315-1.

CERDIP



853-0582 81594

NOTES:
1. Controlling dimension: inches. Millimeters are shown in parentheses.
2. Dimensions and tolerancing per ANSI Y14.5M - 1982.
3. "T", "D", and "E" are reference datums on the body and include allowance for glass overrun and meniscus on the seal line, and lid to base mismatch.
4. These dimensions measured with the leads constrained to be perpendicular to plane T.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #16 when viewed from the top.

Fig.44 16-lead CERDIP; ceramic (F package).

SOLDERING

Plastic leaded chip carriers; plastic quad flat packs and plastic small outline packages

BY WAVE

During placement and before soldering, the component must be fixed with a droplet of adhesive. After curing the adhesive, the component can be soldered. The adhesive can be applied by screen printing, pin transfer or syringe dispensing.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder bath is 10 s, if allowed to cool to less than 150 °C within 6 s. Typical dwell time is 4 s at 250 °C.

A modified wave soldering technique is recommended using two solder waves (dual-wave), in which a turbulent wave with high upward pressure is followed by a smooth laminar wave. Using a mildly-activated flux eliminates the need for removal of corrosive residues in most applications.

BY SOLDER PASTE REFLOW

Reflow soldering requires the solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the substrate by screen printing, stencilling or pressure-syringe dispensing before device placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt, infrared, and vapour-phase reflow. Dwell times vary between 50 and 300 s according to method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 min at 45 °C.

REPAIRING SOLDERED JOINTS (BY HAND-HELD SOLDERING IRON OR PULSE-HEATED SOLDER TOOL)

Fix the component by first soldering two, diagonally opposite, end pins. Apply the heating tool to the flat part of the pin only. Contact time must be limited to 10 s at up to 300 °C. When using proper tools, all other pins can be soldered in one operation within 2 to 5 s at between 270 and 320 °C. (Pulse-heated soldering is not recommended for SO packages.)

For pulse-heated solder tool (resistance) soldering of VSO packages, solder is applied to the substrate by dipping or by an extra thick tin/lead plating before package placement.

Plastic dual in-line packages

BY DIP OR WAVE

The maximum permissible temperature of the solder is 260 °C; this temperature must not be in contact with the joint for more than 5 s. The total contact time of successive solder waves must not exceed 5 s.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

REPAIRING SOLDERED JOINTS

Apply a low voltage soldering iron below the seating plane (or not more than 2 mm above it). If its temperature is below 300 °C, it must not be in contact for more than 10 s; if between 300 and 400 °C, for not more than 5 s.

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Data handbook system

DATA HANDBOOK SYSTEM

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